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# DC-Link Ripple Reduction for Parallel Inverter Systems by a Novel Formulation Using Multiple Space Vector-Based Interleaving Schemes

**Akbar Ali Khan [1,2,*], Nauman Ahmad Zaffar [2] and Muhammad Jahangir Ikram [2]**

[1] Institute of Electrical, Electronics and Computer Engineering, University of the Punjab, Lahore 54590, Pakistan
[2] School of Science and Engineering, Lahore University of Management Sciences, Lahore 54792, Pakistan; nauman.zaffar@lums.edu.pk (N.A.Z.); jikram@lums.edu.pk (M.J.I.)
* Correspondence: akbar.khan@lums.edu.pk

**Abstract:** This paper proposes an analytical formulation-based minimization of DC link current ripples for interleaved parallel inverter systems. Parallel inverter systems find applications in multiple fields. The interleaved superposition of the DC link currents in these systems can potentially be adjusted to mitigate the overall harmonics consequently reducing the DC link capacitor size. To this end, a widely used approach in the literature is the Fourier analysis based on interleaving focusing on dominant harmonic mitigation. However, it leaves room for a generic analytical mechanism to provide time shifts leading to an optimal reduction in DC-link ripples. The goal of this work is to target this optimal reduction by utilizing an analytical mechanism. The paper presents an alternate way of DC-link formulation in terms of the piece-wise sinusoids of inverter output currents for space vector modulation-based systems. The formulation is then used to numerically optimize the interleaved shifts for minimum ripples. Moreover, in addition to the traditional concept of fixed time interleaving, a contemporary concept of sequence-based interleaving is utilized, which is anticipated to have more flexibility in the implementation and additional switching synchronism with PWM rectifiers for back–back converters. Therefore, the sequence interleaving has also been utilized in conjunction with the proposed ripple reduction methodology. Further, an underexplored area of using the combined impact of sequence and time interleaving has also been applied in this work. These interleaving methods are shown to provide significantly improved DC-link ripple mitigation, as compared to existing methods, using numerical assessment followed by simulations and experimental evaluation.

**Keywords:** parallel inverter systems; space vector pulse width modulation; interleaving; DC-link current ripple reduction; DC-link capacitor; pulse width modulated inverters; harmonic distortion



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## 1. Introduction

Parallel-inverter systems have been very popular among the recent power electronic systems due to various advantages in terms of switch ratings, filter sizing and cost [1]. They have many associated applications such as parallel inverter systems driving common load via galvanic isolation/integrated inductor for enhanced power ratings [2,3], segmented motor drives/integrated modular motor drives [4,5], multi-drive systems in paper mills, oil extraction, gas mining, electric vehicle traction [6], and renewable generations [7]. Driving multiple inverters from a common DC link provides several degrees of freedom including the selection of modulation technique(s), phase shift adjustments, cascaded scheduling, etc. These flexible control handles can potentially bring multiple dimensions of improvements such as power quality improvement, reduction in size and cost of switches, better networking of the system, etc. [8–10].

A major challenge in enhancing the performance of inverters is the ripple content in the DC-link current. These ripples are produced by the chopping effect of inverter switches,

causing the DC-link current to fluctuate around the required average current, consequently requiring a large DC-link capacitor [11]. These capacitors, typically of electrolytic type, not only contribute significantly to the size, weight, and cost of the converter but also have reduced reliability due to the absorption of large current ripples [12]. The main contributor to the DC-link capacitor failure is the heating stress produced by these current ripples [13]. In addition, voltage ripples on the capacitor vary directly with current ripple as well [14]. So, improvement in the DC-link current quality, thereby reducing the capacitor size is a critical requirement in any inverter-based power electronic system.

The concept of interleaving in a parallel inverter system offers, without any additional/alternate hardware and complexity requirement, a very useful approach to address DC-link current ripple. Interleaving involves the application of time- or phase-shifted modulating carriers in a multi-inverter system as shown in Figure 1. The shift(s) in carrier angle or switching arrangement, can be adjusted to mutually nullify the impact of harmonics among individual inverters [15]. Several works assess the impact of interleaving on DC-link current for various type of carrier/space vector modulation schemes and applications [16–26]. Different researchers [16–20] have proposed standard shifts of 25% and 50% of switching time in space vector pulse width modulation (SVPWM) and sinusoidal pulse width modulation (SPWM), respectively. Among these, refs. [18,19] proposed the idea of dominant harmonic suppression at DC link using these standard shifts based on Fourier analysis, mainly for electric vehicle drive applications. Similarly, refs. [22,23] also provide the idea of the standard shift of $n$ equal divisions of switching time for a generic phase shift in $n$ parallel converters. All these works resort to the computation of the DC-link current in terms of its harmonic constituents and use interleaved carriers for mutual cancellation of dominant harmonic(s) by utilizing a few standard shifts in the carrier for different load conditions. However, such Fourier-based approaches for minimizing dominant harmonics offer only limited ripple reduction in the DC link. Likewise, authors in [24] considered DC-link ripple minimization for a specific case of dual-inverter-based systems considering a three-level space vector equivalent of dual two-level space vectors. They obtain the most suitable space vector from the three-level space vectors, indirectly incorporating interleaving among individual inverters. The available options for shifts among three-level space vectors remain limited. In theory, the overall ripple reduction may not be obtained by the suppression of the dominant harmonic but rather by an optimal combination of all the constituent harmonics. Consequently, the optimal values of time shifts may not necessarily be amongst the limited standard values and can be variable for different load dynamics in various applications. In this regard, refs. [25,26] have recently presented the idea of obtaining the optimal interleaving time shift for SPWM-based single-phase multi-drive systems, based on double integral Fourier series current form, using a surface plotting method. This useful idea can be extended to three-phase parallel inverter systems. Furthermore, a more systematic and practical approach to obtain the optimal solution is required in this regard.

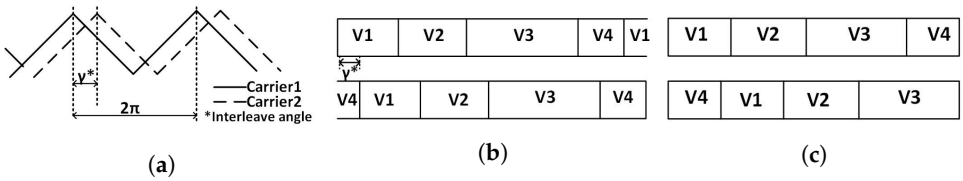



**Figure 1.** Idea of interleaving (**a**). In carrier-based PWM schemes (**b**). As time shift in space vector-based modulations (**c**). As sequence rearrangements in space vector-based modulations.

Another common aspect in the previous works is the usage of constant shifts in the switching carriers for interleaving. However, time-varying shifts in the carrier, if employed and managed properly, can provide more flexibility and improvement. For space vector-based modulations one useful idea is to synchronize time-varying shifts with the sequence arrangement. Not only can this potentially result in the reduction in the DC-link current ripple, which can be compared with those of constant time shifts, but

also offer an added benefit of feasible implementation in back–back converter systems with additional synchronization of series-connected rectifiers [27]. Authors in [27,28] have presented the idea of rearranged sequences for multi-inverter systems, as shown in Figure 1c, but they do not discuss their impact on the DC-link current ripple reduction. Similarly, the idea of applying a rearranged sequence of space vectors for different load or modulation regions has been proposed in [16]. However, its feasibility for a generic range of power factors and phase differences has not been investigated. Lastly, with the available concepts of sequence-based and fixed time-based interleaving, their combined implementation provides an additional avenue for further improvement of current quality which remains an underexplored area in the literature.

As a first contribution in this paper, a novel way of DC-link ripple minimization is presented. We resort to expressing DC-link current explicitly in terms of the switched combination of the inverter output currents. The formulations considers space vector-based modulations since it provides a straightforward DC-link current relationship with the load currents via voltage space vectors. As a result, the DC-link current expression becomes a piece-wise sinusoidal time-varying function. This formulation is generic in nature in which any switching combination of space vector-based PWM can be included in a straightforward manner and can be analysed individually or comparatively. The formulation is used to analyse the current ripple and its behaviour under different load conditions in a typical non-interleaved system. Subsequently, for a parallel two-inverter system, the mechanism of incorporating interleaving time shift in the formulation and employing numerical technique(s) to minimize the DC-link ripple content is demonstrated. The whole formulation has been discussed for conventional symmetric (SVPWM) but can be extendable for any of its variant or modified space vector modulations.

As a second contribution, in addition to constant time shift interleaving, a sequence rearrangement-based variable time interleaving mechanism is presented. We take the idea of sequence bit shifting and minimize the DC-link current ripples based on optimal bits shifted for a given sequence. With discrete shifting possibilities of sequence bits, the optimum interleaving solution is not expected to change greatly with load changes and hence is supposed to be computationally less complex compared to time shift-based interleaving.

Furthermore, a concept of combined sequence and time interleaving is presented, as a third contribution in this paper, by introducing a constant time offset in a rearranged sequence to explore for further minimization in the DC-link current ripple.

The proposed piece-wise formulation is used for comparative evaluation of all these interleaving mechanisms, for a wide variety of load conditions, which reveal the relative extent of improvement, associated computational complexity, and variation pattern of interleaving values for each interleaving method. Furthermore, the results corresponding to standard shifts proposed in the literature are also included in the performance comparison which validates the improvements offered by our proposed interleaving strategies.

The remaining paper is organised as follows: Section 2.1 presents a brief review of the established space vector pulse width modulation (SVPWM). In Section 2.2, we present the analytical piece-wise formulation of the DC-link current, analyse current ripples followed by the impact of interleaving on the current ripples using the proposed formulation and its mechanisms. Section 3 presents the numerical method for the solution of the formulation followed by the numerical results. Section 4 gives simulation and experimental results. Finally, Section 5 presents our concluding remarks.

## 2. Theory

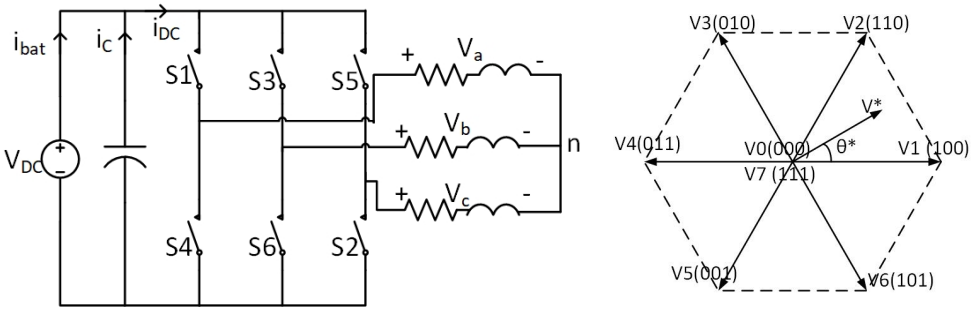
### *2.1. Conventional SVPWM Scheme for Voltage Source Inverter*

A generic three-leg two-level hex-bridge inverter is shown in Figure 2a. Space vector formulation takes the idea of transforming the output voltages $Va$, $Vb$, and $Vc$ to a complex

two-quadrant frame of reference, commonly called the stationary d-q frame, in terms of a complex phasor, say $V\angle\theta$ or $\overrightarrow{V}$ as

$$\overrightarrow{V} = \frac{2}{3}(V_a e^{j0} + V_b e^{\frac{j2\pi}{3}} + V_c e^{\frac{j4\pi}{3}}) \quad (1)$$

In Figure 2a, the complimentary switching of the three legs can produce eight possible output voltage combinations. Corresponding space vectors are shown in Figure 2b, which comprises of six active vectors $V_1$–$V_6$ uniformly distributed in stationary d-q space, and two zero vectors $V_0$ and $V_7$. The angular regions between any two active vectors are named as sectors, with sector 1 between $V_1$ and $V_2$ and so on. Any required three-phase output voltage transformed to this stationary d-q frame can be represented as $V^*\angle\theta^*$ and would exist in the specific sector as per the value of $\theta^*$. For most applications of inverters, the required output voltages are 3-phase balanced sinusoids. For following discussion, these sinusoids are considered as $V_m cos(\omega t)$, $V_m cos(\omega t - 2\pi/3)$ and $V_m cos(\omega t + 2\pi/3)$.




(**a**) (**b**)

**Figure 2.** Three-phase two-level inverter (**a**). Original representation (**b**). Corresponding space vector formulation in stationary d-q frame.

In the conventional SVPWM, any required voltage phasor $V^*\angle\theta^*$ is achieved as a switched combination of active vectors enclosing the corresponding sector as well as zero vector(s) [29]. So, the output voltage $\overrightarrow{V^*}$ for any sector 'i' can be expressed as

$$\overrightarrow{V^*} = \frac{t_i}{T_s}V_i + \frac{t_{i+1}}{T_s}V_{i+1} + \frac{t_z}{T_s}V_z \quad (t_i + t_{i+1} + t_z = T_s) \quad (2)$$

where $V_i$, and $V_{i+1}$ are active vectors for sector '$i$', $V_z$ represents the zero vector and $T_s$ is the switching time period. $t_i, t_{i+1}$, and $t_z$ are the switching times of the corresponding vectors and can be calculated by applying the volt–sec balance in Equation (2) as

$$t_i = \sqrt{3}\frac{V^*}{V_{DC}} * T_s * \sin(\frac{\pi}{3} - \theta_1) \quad (3)$$

$$t_{i+1} = \sqrt{3}\frac{V^*}{V_{DC}} * T_s * \sin\theta_1 \quad (4)$$

$$t_z = T_s - t_i - t_{i+1} \quad (5)$$

where $\theta_1 = mod(\theta^*, \pi/3)$ (*mod* stands for remainder). For balanced sinusoids described above, $V^* = V_m$ according to Equation (1). So the term $\sqrt{3}V^*$ represents the peak value of the output line voltage, that can vary within $[0, V_{DC}]$. So, the quantity $\sqrt{3}\frac{V^*}{V_{DC}}$ can be taken as the modulation index m $\epsilon[0, 1]$ of PWM.

From the implementation perspective, the redundancy in the zero vectors can be utilized in a way to (1) minimize switching transitions, and (2) avoid simultaneous switching among inverter legs. One way is to switch both zero vectors symmetrically around active vectors, for equal times as illustrated in Table 1 as a possible switching sequence.

**Table 1.** Switching details for the SVPWM scheme.

| **Sector No.** | **1** | **2** | **3** | **4** | **5** | **6** |
|---|---|---|---|---|---|---|
| Angle Range | $(0, \pi/3)$ | $(\pi/3, 2\pi/3)$ | $(2\pi/3, \pi)$ | $(\pi, 4\pi/3)$ | $(4\pi/3, 5\pi/3)$ | $(5\pi/3, 2\pi)$ |
| Required Vectors | V1,V2,V0,V7 | V2,V3,V0,V7 | V3,V4,V0,V7 | V4,V5,V0,V7 | V5,V6,V0,V7 | V6,V1,V0,V7 |
| Possible Sequence | 012721 | 723032 | 034743 | 745054 | 056765 | 761016 |
| Order of time segments $t_i, t_{i+1}$, and $t_z$ for given sequence: $\frac{t_z}{2}, \frac{t_i}{2}, \frac{t_{i+1}}{2}, \frac{t_z}{2}, \frac{t_{i+1}}{2}, \frac{t_i}{2}$ | | | | | | |

### *2.2. Formulation of Analytical Expression for Inverter's DC-Link Currents*

To understand the nature of DC-link current ripples and its link with output current, an analytical form of DC-link current is theoretically formulated in this work for SVPWM. This formulation is built on the idea of the DC-link current being a switched reflection of the output currents, as each inverter leg feeding to each individual phase works as a two-state switch between the positive and negative terminals of DC link [30]. Thus, for three-phase inverters with output currents '$I_a$', '$I_b$' and '$I_c$', the expression of the DC-link current '$i_{DC}$' becomes [31]:

$$i_{DC} = S_a I_a + S_b I_b + S_c I_c \tag{6}$$

For illustration, considering the switching state of vector $V_1$ (1,0,0) in Figure 2a. In this state, phase A is connected to the positive end of the DC link while phases B and C are connected to the negative end. So, $I_a$ leaves the positive DC-link rail dividing in $-I_b - I_c$ (according to Kirchoff's Law). Hence, the current demand from the DC side would simply be $I_a$ when $V_1$ is switched. The same can be found from Equation (6) with $(S_a, S_b, S_c)$ = (1,0,0). If balanced sinusoidal voltage requirements are considered, the typical commercial/industrial load, being inductive in nature, would work as an inherent filter for switching harmonics in current; hence, current can be modelled as fundamental frequency sinusoids. For the balanced sinusoidal voltages described in previous section, these currents would be $I_m cos(\omega t - \alpha)$, $I_m cos(\omega t - \alpha - 2\pi/3)$ and $I_m cos(\omega t - \alpha + 2\pi/3)$, $\alpha$ being the load power factor (pf) angle. In this case, $i_{DC}$ relations with output sinusoids can be established for other voltage vectors/switching sequences as given in Table 2.

Extending this idea for SVPWM, as two or more switching combinations are applied in one switching cycle $T_s$ of any given space vector modulation, $i_{\mathrm{DC}}$ can be represented as a piece-wise function of output sinusoids in terms of switching times. Considering the conventional SVPWM presented in Table 1, active voltages $V_i$ and $V_{i+1}$ are switching for any sector $i$. Currents corresponding to these vectors (from Table 2) are

$$i_{\mathrm{DC}} = I_m cos(\omega t - \alpha - (i-2)\frac{\pi}{3}) \quad for \quad V_i \tag{7}$$

$$i_{\mathrm{DC}} = I_m cos(\omega t - \alpha - (i-1)\frac{\pi}{3}) \quad for \quad V_{i+1} \tag{8}$$

Angular range for sector $i$ is $((i-1)\frac{\pi}{3}, i\frac{\pi}{3})$. The angular range is shifted to a range of $(0, \frac{\pi}{3})$ by substituting $t_a$ for $t$ such that $\omega t = \omega t_a + (i-1)\frac{\pi}{3}$. $i_{\mathrm{DC}}$ for the above two vectors then becomes:

$$i_{\mathrm{DC}} = I_m cos(\omega t_a - \alpha - \frac{\pi}{3}) \quad for \quad V_i \tag{9}$$

$$i_{\mathrm{DC}} = I_m cos(\omega t_a - \alpha) \quad for \quad V_{i+1} \tag{10}$$

These two current expressions are now independent of sector $i$ which means that the behaviour of $i_{\mathrm{DC}}$ is similar for each sector or $i_{\mathrm{DC}}$ is periodical with the $\pi/6$ angular period. Thus, manipulations for one sector can be extended to the entire $2\pi$ region. For the sequence of voltage vectors presented in Table 1, this piece-wise expression for $i_{\mathrm{DC}}$ can be more comprehensively presented as

$$i_{DC} = 0[u(t^*) - u(t^* - t_i)] + I_m cos(\omega t_a - \alpha - \frac{\pi}{3})[u(t^* - t_i) - u(t^* - t_{ii})] + I_m cos(\omega t_a - \alpha)[u(t^* - t_{ii}) - u(t^* - t_{iii})] + 0[u(t^* - t_{iii}) - u(t^* - t_{iv})] + I_m cos(\omega t_a - \alpha)[u(t^* - t_{iv}) - u(t^* - t_v)] + I_m cos(\omega t_a - \alpha - \frac{\pi}{3})[u(t^* - t_v) - u(t^* - T_s)] \quad (11)$$

or

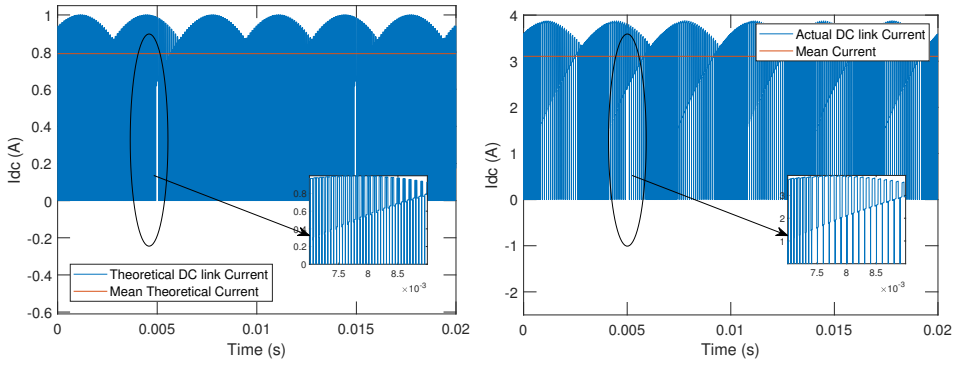
$$i_{DC} = I_m cos(\omega t_a - \alpha - \frac{\pi}{3})[u(t^* - t_i) - u(t^* - t_{ii}) + u(t^* - t_v) - u(t^* - T_s)] + I_m cos(\omega t_a - \alpha)[u(t^* - t_{ii}) - u(t^* - t_{iii}) + u(t^* - t_{iv}) - u(t^* - t_v)] \quad (12)$$

where $u(t)$ represents the step function and $t^* = mod(t, T_s)$, showing the periodic repetition of sinusoids for every switching time. Furthermore, $t_i = \frac{t_z}{2}$, $t_{ii} = \frac{t_z + t_1}{2}$, $t_{iii} = \frac{t_z + t_1 + t_2}{2}$, $t_{iv} = \frac{2t_z + t_1 + t_2}{2}$, $t_v = \frac{2t_z + 2t_2 + t_1}{2}$ and $T_s = t_z + t_1 + t_2$=switching time period, for the sequence presented in Table 1.

**Table 2.** DC input current in terms of output phase currents.

| Space Vector | Input Current '$I_{DC}$' |
|---|---|
| $V_1(1,0,0)$ | $I_a = I_m cos(\omega t - \alpha)$ |
| $V_2(1,1,0)$ | $-I_c = I_m cos(\omega t - \alpha - \pi/3)$ |
| $V_3(0,1,0)$ | $I_b = I_m cos(\omega t - \alpha - 2\pi/3)$ |
| $V_4(0,1,1)$ | $-I_a = I_m cos(\omega t - \alpha - \pi)$ |
| $V_5(0,0,1)$ | $I_c = I_m cos(\omega t - \alpha - 4\pi/3)$ |
| $V_6(1,0,1)$ | $-I_b = I_m cos(\omega t - \alpha - 5\pi/3)$ |
| $V_0(0,0,0), V_7(1,1,1)$ | 0 |

To validate this formulation, a theoretically synthesized DC-link current using the expression developed in Equation (12) as well as its counterpart using actual simulations is presented in Figure 3 for a pf angle of 20° and in Figure 4 for a pf angle of 45° for $m = 1$. To observe at a more granular level the magnified version is also presented alongside in the respective figures. It can be seen that, besides the difference of resolution in the theoretical and simulated variants of current in the figure, these variants are similar at respective loads that verifies the proposed formulation. It can also be seen that current is actually a piece-wise function, following two sinusoidal envelopes along with constant zero segments. Hence, the proposed formulation sufficiently describes $i_{DC}$ mathematically and will be used in the following sections to discuss the nature of DC-link ripples, implications of interleaving shifts and consequently to develop a numerical method to minimize these ripples.

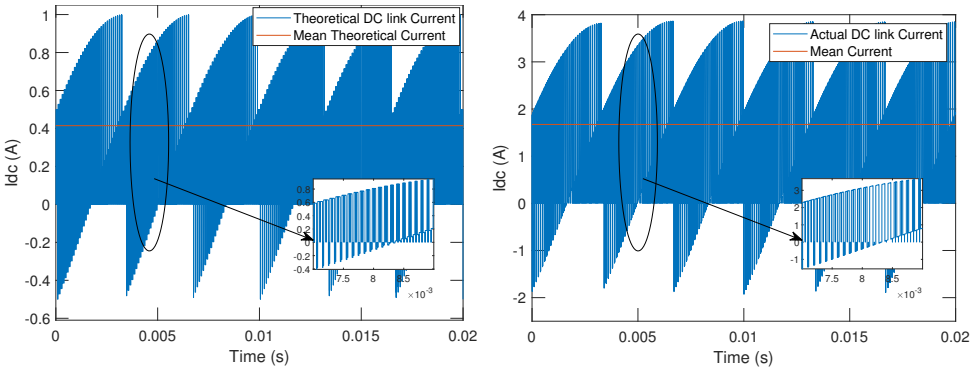



(**a**) (**b**)

**Figure 3.** DC−link current for load pf angle = 20°. (**a**) Theoretically synthesized (using piece-wise formulation). (**b**) Its simulated counterpart.

### *2.3. Analytical Assessment of DC-Link Current Ripple*

The piece-wise formulation of DC-link current described above can be used to explain its high ripple content. As can be deduced from Equations (9) and (10), for a complete angular range of any one sector, i.e., $\omega t_a = [0, \pi/3]$, active components of $i_{\mathrm{DC}}$ vary between $cos(\alpha)$ to $cos(\pi/3 - \alpha)$ and $cos(\alpha + \pi/3)$ to $cos(\alpha)$, respectively, while the third component remains at zero. Note that currents in our analysis are normalized by $I_m$. The average current computed using power balance between the DC side and three-phase output turns out to be $\sqrt{3}/2mcos(\alpha)$. This current is also represented in Figures 3 and 4. The variation of the DC-link current around this average value is balanced by the reactive power provided by the DC-link capacitor which is the main contributor to its size.




(**a**) (**b**)

**Figure 4.** DC−link current for load pf angle = 45°. (**a**) Theoretically synthesized (using piece-wise formulation). (**b**) Its simulated counterpart.

For larger values of $m$, the average current would be quite close to $\cos(\alpha)$. The term $\cos(\alpha)$ at one end is expected to give a low content of ripples. At the other end of $\cos(\pi/3 - \alpha)$ or $\cos(\pi/3 + \alpha)$, the value of ripple starts increasing. This situation worsens for higher values of $\alpha$ as cosines tend to have a higher rate of change at angles around $\pi/2$. On the other hand, for lower values of $m$, the average current is significantly lesser while current envelopes remains same, with a higher portion of zero vector switching. Hence, the ripple content for lower $m$ values is anticipated to be higher. The actual amount of ripples at different values of power factors and angular regions do not have straightforward trends due to the involvement of the varying switching time duration as well as varying respective current components. However, the variations of DC current as discussed here, gives significant insight into the content of ripples and its cause.

### *2.4. Quantification of DC-Link Current Ripple*

As discussed in Section 2.3, the actual DC-link current, comprised of multiple sinusoids truncated periodically due to vector switching, contains significant ripples around the mean. The battery or rectifier system provides the mean current for the active power requirement whereas the DC-link capacitor supplies the ripple content of $i_{\mathrm{DC}}$. The root-mean-square (rms) of this ripple content of DC is given by:

$$i_{\mathrm{c,rms}} = \sqrt{\frac{1}{T}\int_T (i_{\mathrm{DC}} - i_{\mathrm{bat}})^2\, dt} \tag{13}$$

The mean current supplied by the battery/rectifier system $i_{\mathrm{bat}}$ is $\sqrt{3}/2\ mI_m cos\alpha$ as discussed earlier. Furthermore, $i_{DC}$ is periodic with $\pi/3$ angular period. Incorporating these values in Equation (13) for $i_{\mathrm{c,rms}}$ gives

$$i_{\text{c,rms}} = \sqrt{\frac{3}{\pi}\int_0^{\pi/3}(i_{DC} - \frac{\sqrt{3}}{2}mI_m cos\alpha)^2\, d\omega t} \tag{14}$$

where the expression for $i_{\text{DC}}$ is presented in Equation (12). For numerically analysing $i_{\text{c,rms}}$, the integral in Equation (14) is utilized in numerical form in this paper, i.e., $i_{DC}$ is the samples at the small interval of $\omega t$ (say '$\Delta\omega t$') to calculate the switching vectors and timings. This sampled $i_{DC}$ at any given $\Delta\omega t$ is synthesized by further resolving it in '$K$' samples to incorporate switching segments, and taking its mean. The overall expression, normalized by $I_m$ turns out to be

$$i_{\text{c,rms-norm}} = \sqrt{\frac{1}{I_m}(\frac{3\Delta\omega t}{\pi}\sum_{\frac{\pi}{3\Delta\omega t}}(\frac{1}{K}\sum_{K}(\frac{(t_k i_k)}{T_s} - \frac{\sqrt{3}}{2}mI_m cos\alpha)^2))} \tag{15}$$

$i_{\text{c,rms-norm}}$ is the key objective function to be minimized, for our analysis of parallel inverter systems.

In previous works, the metrics used for DC-link ripple analysis include RMS capacitor current [32], current THD [33] and DC-link current ripple factor $K_{\text{DC}}$ [34]. Generic expressions for THD and $K_{\text{DC}}$ can be given as

$$\text{THD} = \frac{\sqrt{\sum I_{\text{harm}}^2}}{I_{\text{fund}}} = \frac{\sqrt{\sum(i_{\text{DC}}^2 - I_{\text{fund}}^2)}}{I_{\text{fund}}} \tag{16}$$

$$K_{\text{DC}} = \frac{\sum I_{\text{harm}}^2}{I_{\text{fund}}^2} = \frac{\sum(i_{\text{DC}}^2 - I_{\text{fund}}^2)}{I_{\text{fund}}^2} \tag{17}$$

It can be seen that these two quality parameters are not only alternate forms of each other, but also similar to the normalized RMS capacitor current in our case by noting that the average current is the fundamental current for DC. Only the normalization term in THD and $K_{\text{DC}}$ is different from our case.

### *2.5. Interleaved Modulation Schemes for Dual-Inverter System*

The sinusoidal output current, in a typical inductive load force the DC-link current to follow the sinusoidal envelope chopped at the switching frequency and is periodic with $\pi/3$ period. This pattern with an arbitrary phase and switching time is valid for every inverter in a multi-inverter system. Therefore, control handles on the phase, switching time, and switching sequence for individual inverters relative to the others can be explored to minimize the overall ripple in the DC-link current. Different current components of individual inverters can compensate each other and can thus improve current quality.

We analyse this for an identically loaded two-inverter system (dual-inverter) fed from a common DC bus. A typical parallel-connected dual-inverter system is shown in Figure 5. Where three-phase one-load and three-phase two-load can be separate loads such as in a multi-drive system, multi-phase/segmented motors or a high-rating common load connected through suitable isolation/filter. As depicted in Figure 1b,c, introduction of interleaving shift in any space vector switching sequence can make different voltage vectors of the two inverters combine with each other, while in the absence of that shift, each vector of one inverter would combine to the same vector of other inverters. Impact of this cross combination of voltage vectors in contrast to similar vector combinations is depicted in Table 3. The table presents sinusoidal current ranges for all possible voltage vector combinations of $i_{DC1}$ and $i_{DC2}$, considering sector 1 of SVPWM given in Table 2.

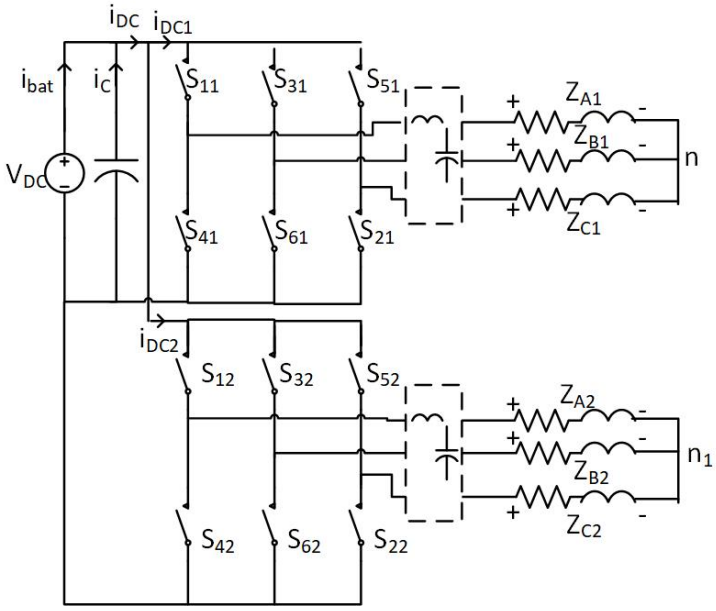



**Figure 5.** Typical three-phase parallel-connected dual-inverter system.

**Table 3.** Combination of different voltage vectors in SVPWM (sector 1) and their (normalized) DC current sinusoids.

| S.V 1 | S.V 2 | $i_{DC1}$ | $i_{DC2}$ | Combined $i_{DC}$ | Current Range for [0, $\pi$/3] |
|---|---|---|---|---|---|
| $V_1$ | $V_1$ | $cos(\omega t-\alpha)$ | $cos(\omega t-\alpha)$ | $2cos(\omega t-\alpha)$ | $2cos(\alpha)-2cos(\pi/3-\alpha)$ |
| $V_1$ | $V_2$ | $cos(\omega t-\alpha)$ | $cos(\omega t-\alpha-\pi/3)$ | $\sqrt{3}cos(\omega t-\alpha-\pi/6)$ | $\sqrt{3}cos(\pi/6+\alpha)-\sqrt{3}cos(\pi/6-\alpha)$ |
| $V_1$ | $V_0/V_7$ | $cos(\omega t-\alpha)$ | 0 | $cos(\omega t-\alpha)$ | $cos(\alpha)-cos(\pi/3-\alpha)$ |
| $V_2$ | $V_2$ | $cos(\omega t-\alpha-\pi/3)$ | $cos(\omega t-\alpha-\pi/3)$ | $2cos(\omega t-\alpha-\pi/6)$ | $2cos(\pi/3+\alpha)-2cos(\alpha)$ |
| $V_2$ | $V_0/V_7$ | $cos(\omega t-\alpha-\pi/3)$ | 0 | $cos(\omega t-\alpha-\pi/3)$ | $cos(\pi/3+\alpha)$–$cos(\alpha)$ |

Table 3 shows that combination of the same active vector for two inverters, i.e., $(V_1, V_1)$ or $(V_2, V_2)$, has a significantly higher current variation range compared to that of two different active vectors. Furthermore, the combination of an active vector with a zero vector halves the ripple variation range which can be closer to the mean current for certain values of the modulation index $m$. Despite this surface view on the current ranges, the actual impact of these vector combination on current ripples depends on their switching time and the extent of overlap which, in turn, depends on the switching sequence implied in the individual inverter, load pf and modulation index. For this purpose, $i_{c,rms-norm}$ can be utilized to gauge the ripple content whose discrete form, in Equation (15), would be modified for the dual-inverter case as

$$i_{\text{c,rms-norm}} = \frac{1}{I_{m1}+I_{m2}}\left(\frac{3\Delta\omega t}{\pi}\sum_{\frac{\pi}{3\Delta\omega t}}\left(\frac{1}{K}\sum_{K}\left(\frac{(t_{k1}i_{k1}+t_{k2}i_{k2})}{T_s}-\frac{\sqrt{3}}{2}m_1I_{m1}cos\alpha_1+\frac{\sqrt{3}}{2}m_2I_{m2}cos\alpha_2\right)^2\right)\right)^{\frac{1}{2}} \quad (18)$$

where $t_{k2}i_{k2}$ represents the discrete form of $i_{DC2}$ that will be applied with some form of interleaving. In continuous time, $i_{DC2}$ would appear as:

$$\begin{aligned} i_{DC} = {} & I_m cos(\omega t_a-\alpha-\frac{\pi}{3})[u(t^*-t_i')-u(t^*-t_{ii}')+u(t^*-t_v')-u(t^*-T_s')]+I_m cos(\omega t_a-\alpha)[u(t^*-t_{ii}') \\ & -u(t^*-t_{iii}')+u(t^*-t_{iv}')-u(t^*-t_v')] \end{aligned} \quad (19)$$

In reference to Equation (12), $t_x' = t_x + t_d$ for all $t_i - t_v$ as well as $T_s$. i.e., a time delay '$t_d$' is added in each switching segment for a second inverter. Based on Equation (18), $i_{c,rms-norm}$ for the vector combinations listed in Table 3 is shown in Figure 6, for different values of the power factor and mod index $m$. In the figure, in addition to the depiction of a higher ripple content for similar vectors than those of cross combinations, it also appears that superiority of different cross combinations at various load scenarios are different.

Hence, the interleaving shift in one inverter has to be adjusted with respect to the other so that, for a given load scenario, the overall utilization of cross combinations can produce a minimized ripple content.

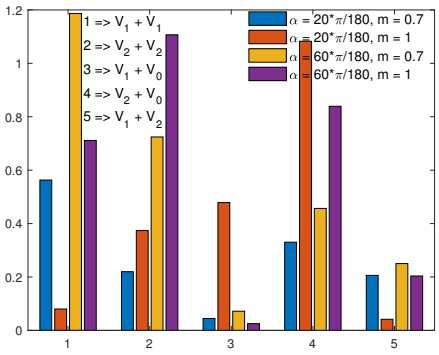



**Figure 6.** Capacitor RMS current depiction for space vector mutual combinations.

### *2.6. Alternative Forms of Interleaving for SVPWM*

General use of interleaving is realized by providing a time shift $t_d \epsilon [0, T_s]$ in the carrier wave, i.e., in the switching cycle of one inverter with respect to the other. It is important to note here that $t_d$ is too small to make any impact on the sine or cosine of $\omega t_a$, the magnitude of the piece-wise current at any given instant, and the corresponding switching time of any voltage vector remains practically unaffected by $t_d$ in above expression.

As SVPWM works on feeding a specific sequence of various voltage vectors to the inverter, each vector for a specified time, another possible way of interleaving in SVPWM is the sequence rearrangement. i.e., one or more bits of one inverter's sequence is shifted with respect to the other. As an example, if the $V_0, V_1, V_2, V_7, V_2, V_1$ sequence is given to one inverter during sector 1 (Table 1) the other inverter(s) can be fed with $V_1, V_2, V_7, V_2, V_1, V_0$ or $V_2, V_7, V_2, V_1, V_0, V_1$ and so on. The cyclic repetition of these switching sequences ensures that the overall symmetry of switching in the sequence-shifted version remains intact. The only difference is when one or more bits lag or lead in one inverter's switching sequence with respect to the other. This rearrangement can also be viewed in terms of time shift, yet the shifts comprise of some combination of vector switching times $t_z, t_1$ and $t_2$. Thus, the time shift here is not static and changes with $\omega t_a$ during one hexagonal period as $t_z, t_1$ and $t_2$ are functions of $\omega t_a$. Moreover, for any given switching sequence of SVPWM, there are discrete possibilities of rearrangements owing to the limited permutations of the actual sequence. As shown in Table 1, the switching sequence consists of six bits; hence, six possible sequence shifts can be applied.

For the sake of discussion, incorporation of time shift $t_d$ in one inverter switching time is named as time interleaving, while rearranging a sequence of one inverter is termed sequence interleaving. Furthermore, in this work, time interleaving will also be combined with sequence rearrangement, i.e., a time shift in the switching period of a rearranged sequence can be applied on one inverter to obtain further improvement in the DC-link current. This combined interleaving will be termed sequence+time interleaving from here onwards.

## 3. Methodology

With the possible interleaving scenarios discussed in Section 2.6, the upfront challenge is to find a suitable value of $t_d$ for minimized $i_{c,rms}$ in Equation (18). For the case of sequence interleaving, there are limited permutations possible as discussed, and hence for any given load characteristics, numerically finding the optimal sequence shift among discrete possibilities is relatively simple. However, for time interleaving or sequence+time interleaving $t_d \epsilon [0, T_s]$ is continuous and its most suitable value needs to be computed. For this purpose, incorporation of $i_{DC1}$ and $i_{DC2}$ from Equations (12) and (19) into Equation (18)

results in a multiple indefinite combination of sinusoids, due to the currently unknown $t_d$, with a sinusoidally varying time step function. Thus, the expression of this $i_{c,rms}$ comes out to be an intractable function ruling out a closed form analytical solution. Hence, a numerical method is devised in this work to search for the suitable interleaving shift for reduced ripple contents.

### *3.1. Numerical Search Algorithm*

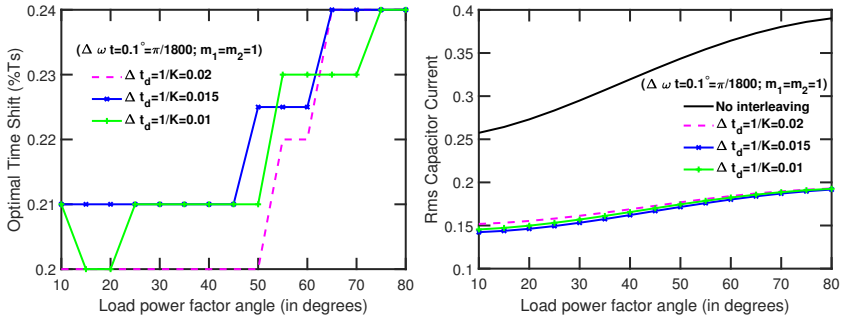
Devising an efficient numerical/heuristic method is not the main target of this work, rather the mathematical quantization of benefits is where our focus lies. As there is a single parameter of optimization $t_d$ with a well-defined and limited range $[0, T_s]$, solving the problem offline could result in high accuracy if the exhaustive search is utilized to find $t_d$ for the minimum current ripple [35]. Here we conduct an exhaustive search as a one-dimensional/line search method to discretized each value of the decision variable, i.e., interleaving shift is evaluated to achieve the extreme value of the objective function, $i_{c,rms}$ here. The detailed algorithm for the current case is presented in Algorithm 1.

**Algorithm 1:** Linear search algorithm for the min. cap ripple current and corresponding interleaving shift

**Data:** Mod. indexes '$m_1, m_2$', load pf angles '$\alpha_1, \alpha_2$'
1 **Init:** $\omega t \leftarrow 0$ , $t_d \leftarrow 0$ `// t_d is interleaving shift`
2 **Compute** '$I_{bat1}$,$I_{bat2}$' for given $m_1, m_2$ and $\alpha_1, \alpha_2$, respectively
3 **while** $t_d \leq 1$ **do**
4  $n \leftarrow 1$
5  **while** $\omega t \leq \frac{\pi}{3}$ **do**
6  $l \leftarrow 1$
7  **Compute** $t_{11}, t_{21}, t_{z1}$ for $inv_1$ and $t_{12}, t_{22}, t_{z2}$ for $inv_2$ `// T_s normalised to '1'`
8  **Compute** output sinusoids $i_{11}, i_{21}$ for $inv_1$ and $i_{12}, i_{22}$ for $inv_2$
9  **for** $k \leftarrow 1$ *to* $K$ **do**
10  **Compute** $i_{dc,1}$ as piece-wise array of $i_{11}, i_{21}, 0$ for given sequence `/* e.g., for sequence` $V_0, V_1, V_2, V_7, V_2, V_1$ $i_{dc,1} = 0$ `for` $\frac{k}{K} \leq 0.5t_{z1}$, $i_{dc,1} = i_{11}$ `for` $\frac{k}{K} \leq 0.5(t_{z1} + t_{11})$ `and so on */`
11  **Compute** $i_{dc,2}$ as piece-wise array of $i_{12}, i_{22}, 0$ for given sequence `/* e.g., for sequence` $V_1, V_2, V_7, V_2, V_1, V_0$ $i_{dc,2} = i_{12}$ `for` $\frac{k}{K} + t_d \leq 0.5t_{12}$, $i_{dc,1} = i_{21}$ `for` $\frac{k}{K} + t_d \leq 0.5(t_{12} + t_{22})$ `and so on */`
12  $i_{c-ms}(k) \leftarrow (i_{dc,1}(k) + i_{dc,2}(k) - I_{bat,1} - I_{bat,2})^2$
13  $i_{c-ms,1}(l) \leftarrow mean(i_{c-ms,1})$
14  $l \leftarrow l + 1$
15  $\omega t \leftarrow \omega t + \Delta\omega t$
16  $i_{c-rms}(n) = \sqrt{mean(i_{c-ms,1}}$
17  $n \leftarrow n + 1$
18  $t_d \leftarrow t_d + \Delta t_d$
19 $i^*_{c-rms} = min(i_{c-rms})$
20 $n^* \leftarrow index(min(i_{c-rms}))$
21 $t^*_d \leftarrow n^* \Delta t_d$
**Result:** Minimized ripple current $i^*_{c-rms}$ and corresponding $t^*_d$

In Algorithm 1, lines 5–16 accomplish the computation of $i_{c,rms}$ for the dual-inverter case, in discretized form as in Equation (18). This computation is performed in an outer loop which traverses the interleave shift $t_d$ within $[0, 1]$ ($T_s$ is normalized to '1') using an increment of $\Delta t_d$. Moreover, synthesis of $i_{dc,2}$ in line 11 of the algorithm can also opt for a

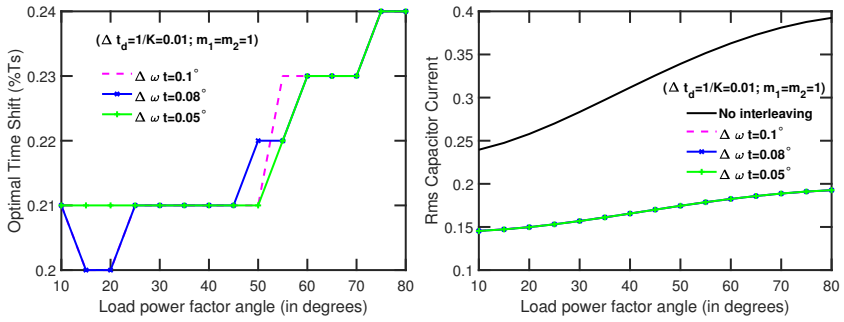
sequence rearrangement as described in the associated comment. The choice of increment $\Delta t_d$ is important for the accuracy of obtained interleaving shift $t_d^*$ corresponding to the minimum $i_{\text{c,rms}}$. Similarly, size of the angular increment $\Delta\omega t$ (line 15 of the algorithm) and sampling size of current '$K$' within an angular segment is also vital for accurate computation of the $i_{\text{c,rms}}$. For this, various values of this incremental sizes can be checked on a one-test case to see the impact on accuracy. This has been performed in Figures 7 and 8 for matching loads on dual-inverters with a two-bit-shifted sequence fed to $i_{DC,2}$. As $\Delta t_d$ and the fraction $\frac{1}{K}$ has to be combined in the algorithm, as depicted in the comment of line 11, they are thus kept the same in this test run, as shown in Figure 7a, for constant $\Delta\omega t$. Here, although changing $\Delta t_d$ to smaller values does change the optimal result within a specific region, the broad region of results remain same. As will be seen, the broad region of interleaving will be of more interest for practical feasibility. Furthermore, the corresponding $i_{\text{c,rms-norm}}$ for closely spaced optimal answers for different $\Delta t_d$ remain similar, as depicted in Figure 7b. Therefore, $\Delta t_d = \frac{1}{K} = 0.01$ is considered a suitable increment for further analysis.




(**a**) (**b**)

**Figure 7.** (**a**) Impact of changing the time shift increment in accuracy of the result in Algorithm 1, (**b**) corresponding to $i_{c,rms}$.

After this, $\Delta\omega t$ is varied for a constant $\Delta t_d$ and $\frac{1}{K}$ in Figure 7c and the corresponding $i_{\text{c,rms-norm}}$ is shown in Figure 7d, where the same trend of a similar broad region with even more similarity in $i_{\text{c,rms-norm}}$ can be observed. Hence, $\Delta\omega t = 0.1°$ is considered sufficient for the subsequent analysis.




(**a**) (**b**)

**Figure 8.** (**a**) The impact of changing the angular increment in accuracy of the result in Algorithm 1, (**b**) corresponding to $i_{c,rms}$.

### *3.2. Numerical Results*

Algorithm 1 is applied for sequence+time interleaving for each of the six possible sequence rearrangements, with the default sequence rearrangement representing time interleaving only. Similarly for sequence interleaving, Algorithm 1 can be used by applying the outer loop with only six possible values of dynamically changing time shifts, instead of the whole range of $t_d$. For instance, if $V_0, V_1, V_2, V_7, V_2, V_1$ is the actual sequence applied, $t_d = 0.5t_z$ represents a one-bit shift, i.e., $V_1, V_2, V_7, V_2, V_1, V_0$ and so on. In other words,

for sequence interleaving, computational burden of the outermost loop can be practically avoided. For any selected $\Delta t_d = \frac{1}{K}$, this computational burden can be approximated as $\mathcal{O}(\frac{1}{\Delta t_d})$ or $\mathcal{O}(K)$.

The proposed numerical algorithm has been run for various load combinations of a dual-inverter system, each representing a specific scenario. These results can be extrapolated to other situations. For each combination, results have been taken for a wide range of load power factors. The following are the five load combination scenarios that have been analysed:

1. Equal loads on both inverters with mod index m = 1 (Figure 9)
2. Equal loads on both inverters with mod index m = 0.5 (Figure 10)
3. Different mod. index on 2 inverters, $m_1$ = 1 and $m_2$ = 0.7 (Figure 11)
4. Equal loads (and m = 1) with 20° power factor angle difference among inveters (Figure 12)
5. Equal loads (and m = 1) but 30° phase difference among inverters (Figure 13)

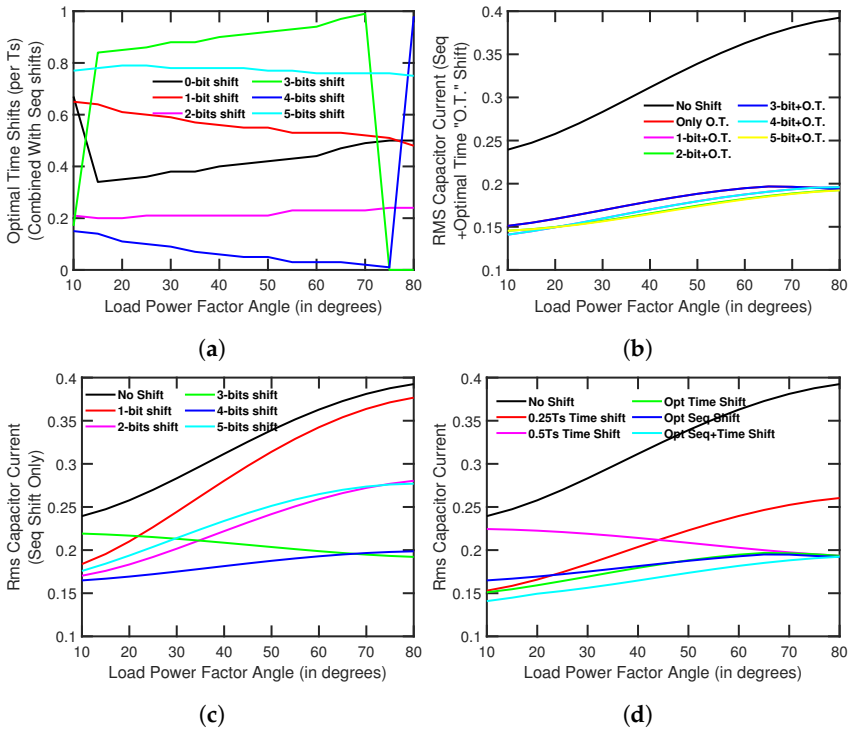



**Figure 9.** For equal load and mod.index = 1. (**a**) Optimal time shifts (combined with seq shifts). (**b**) $i_{c,rms}$ for seq+opt time shifts. (**c**) $i_{c,rms}$ for only seq shifts. (**d**) Comparative $i_{c,rms}$ for different interleaving shifts.

For each case, numerical results contains

(a) Optimal time shifts with and without sequence shift(s);
(b) Corresponding RMS capacitor current (normalized to the combined peak value) for each optimal time shift;
(c) RMS capacitor current (normalized) for only sequence shifts;
(d) Comparison of the min RMS current for only sequence shift, only time shift, and sequence+time shift, along with the RMS current corresponding to standard shifts of $0.5T_s$ and $0.25T_s$.

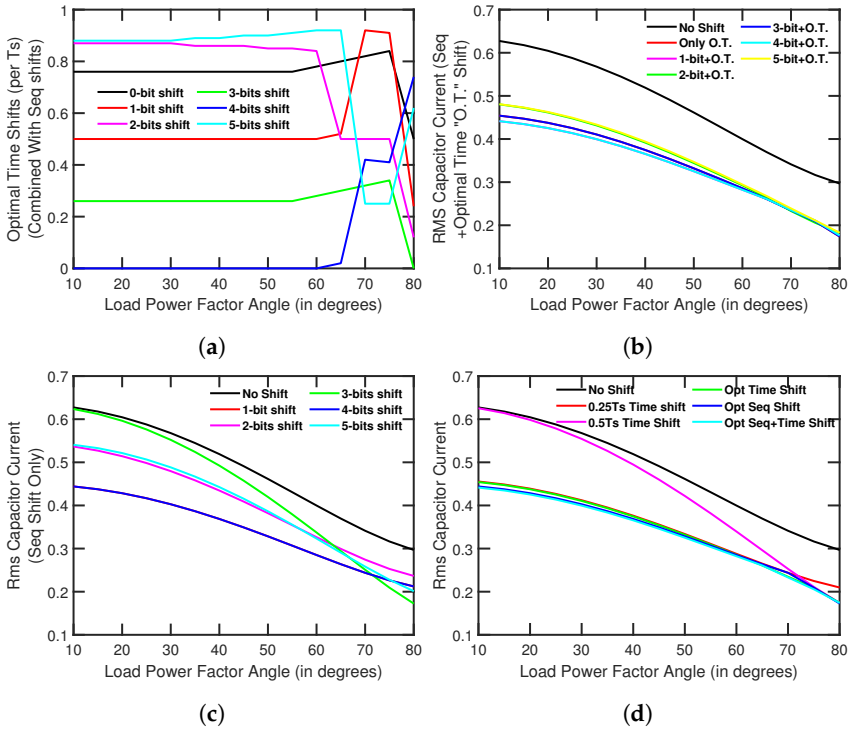



**Figure 10.** For equal load and mod.index = 0.5. (**a**) Optimal time shifts (combined with seq shifts). (**b**) $i_{c,rms}$ for seq+opt time shifts. (**c**) $i_{c,rms}$ for only seq shifts. (**d**) Comparative $i_{c,rms}$ for different interleaving shifts.

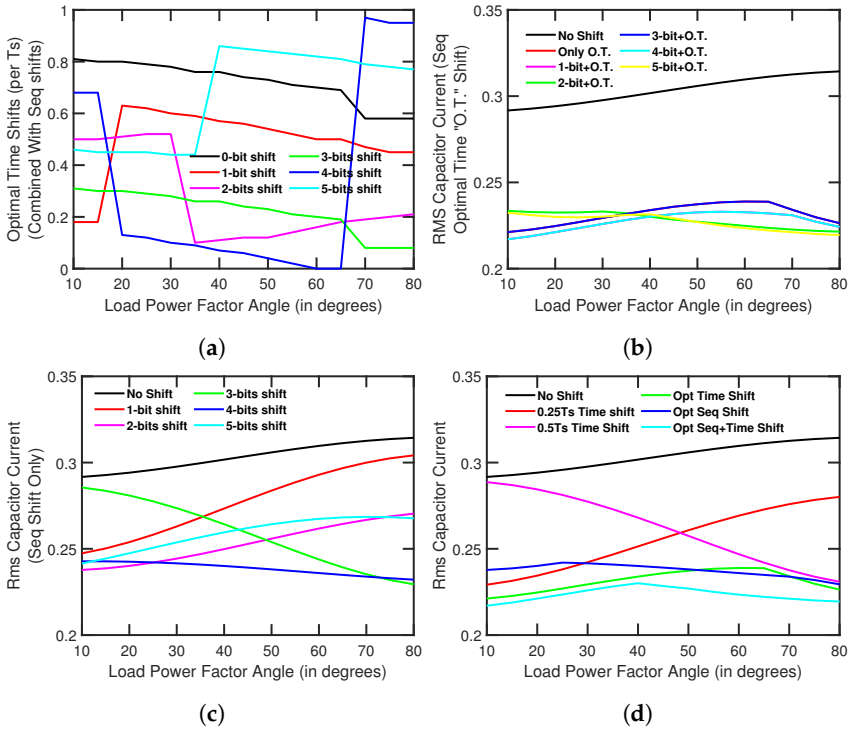



**Figure 11.** For load 1 at mod.index = 1, and load 2 at mod.index = 0.7. (**a**) Optimal time shifts (combined with seq shifts). (**b**) $i_{c,rms}$ for seq+opt time shifts. (**c**) $i_{c,rms}$ for only seq shifts. (**d**) Comparative $i_{c,rms}$ for different interleaving shifts.

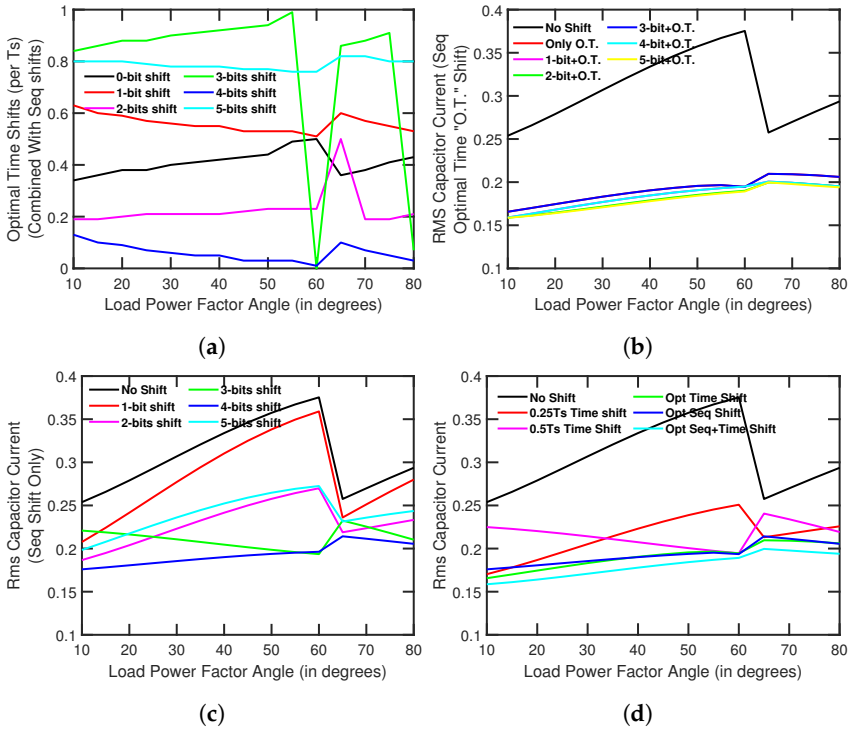



**Figure 12.** For equal load, a mod.index = 1 and a pf angle difference of 20°. (**a**) Optimal time shifts (combined with seq shifts). (**b**) $i_{c,rms}$ for seq+opt time shifts. (**c**) $i_{c,rms}$ for only seq shifts. (**d**) Comparative $i_{c,rms}$ for different interleaving shifts.

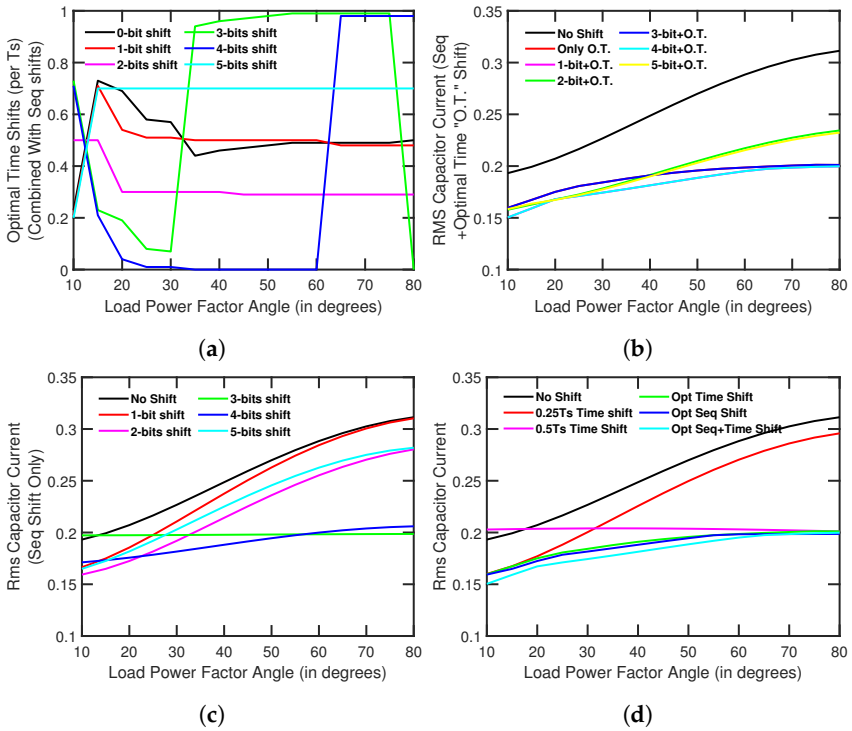



**Figure 13.** For equal load, a mod.index = 1 and a phase difference of 30°. (**a**) Optimal time shifts (combined with seq shifts). (**b**) $i_{c,rms}$ for seq+opt time shifts. (**c**) $i_{c,rms}$ for only seq shifts. (**d**) Comparative $i_{c,rms}$ for different interleaving shifts.

In scenario a of Figures 9–13, it can be observed that, for each of the sequence interleaving, the offset time $t_d^*$ has values close vicinity to specific regions of the load power factors. Hence, from a practical implementation perspective, a staircase set of $t_d^*$ or a constant $t_d^*$,

approximated for instances through linear regression, can be pre-fed to the controller for specific ranges of pf angles and loads.

Scenario b in Figures 9–13 presents the corresponding $i_{c,rms}$ for these optimal time shifts, which are comparably close to one another, at any given load scenario and pf angle. However, the minima of these $i_{c,rms}$ change throughout these load pfs. For applications where mutual load variations are relatively small, such as segmented motor drives, it allows the use of the predetermined value of sequence shift and corresponding approximated $t_d^*$, as described above, to be given to the controller. This will provide a trade-off between optimization and computational complexity. One possible way of such an approximation is shown in Table 4 for the mentioned load cases and pf angle ranges. For cases where multiple sequence shifts gives highly close $i_{c,rms}$ at their respective $t_d^*$, the sequence shift with the most stable $t_d^*$ can be selected. The same is reflected for case 2 in Table 4 via Figure 10b. However, this predetermined look-up table method may not be feasible in a system with dynamically changing loads and mutual phases/pfs, such as multi-motor drives. For which we move to scenario c.

**Table 4.** Sub-optimal approximations for seq+time interleaving for cases presented in Figures 9–13.

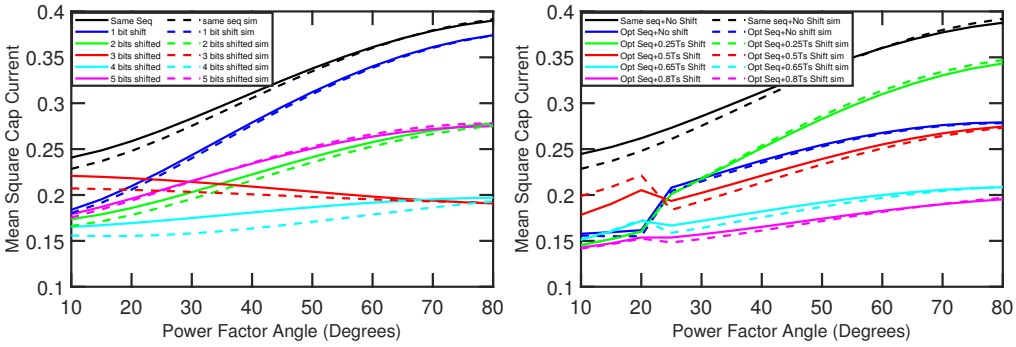
| | Pf Angle Range (deg) | Opt Seq Shift | Opt $t_d$ Range |
|---|---|---|---|
| Case 1: Equal Load, $m_1 = m_2 = 1$ | 10–20° | 4-bits | 10–15% |
| | 20–80° | 5-bits | 75–80% |
| Case 2: Equal Load, $m_1 = m_2 = 0.5$ | 10–60° | 4-bits | 0% |
| | 60–75° | | 40–50% |
| | 75–80° | | 75-80% |
| Case 3: Equal Load, $m_1 = 1$, $m_2 = 0.7$ | 10–20° | 4-bits | 70% |
| | 20–40° | | 5–15% |
| | 40–80° | 5-bits | 75–85% |
| Case 4: Equal Load, $m_1 = m_2 = 1$, pf angle diff of 20° | 10–80° | 5-bits | 75–85% |
| Case 5: Equal Load, $m_1 = m_2 = 1$, phase angle diff of 30° | 10–20° | 2-bits | 50% |
| | 20–80° | 4-bits | 0% |

Scenario c in Figures 9–13 shows normalized $i_{c,rms}$ for only sequence interleaving. This particular scenario has only six discrete possibilities which reduces the overall computational complexity. Furthermore, in all the five cases utilized, the results of 4-bit shifts show consistently good results for almost the entire range of load pfs. This makes it a highly suitable option where reduced computation complexity at the cost of an overall minimization of the objective function can be employed.

To observe the mutual impact of these different types of interleaving, scenario d in Figures 9–13 provides a mutual comparison of sequence interleaving, time interleaving, and seq+time interleaving with no interleaving scenario shown as the base case. In addition, RMS currents corresponding to standard time shifts of $0.5T_s$ and $0.25T_s$, as prescribed in previous works, for dominant harmonic suppression based on Fourier analysis, are also included here to compare our approach with the literature. As per the results, the impact of standard interleaving of $0.5T_s$ and $0.25T_s$, given in the literature, is significantly lower than our proposed methods of optimal interleaving for almost every given load combination. This validates the need for optimization in DC-link quality improvement instead of applying standard shifts. Among the three alternative variants of optimal interleaving we proposed, it can be seen that for all given cases, sequence+time interleaving gives the lowest possible results of $i_{c,rms}$ and therefore DC-link current ripple, while time interleaving and sequence interleaving alone have different load regions of mutual superiority. However, compared to the no interleaving scenario, the improvement is significant for all types of interleaving and their mutual differences are relatively small. In summary, the sequence+time interleaving can be considered the most optimal way of improving DC-link current quality but using only sequence interleaving, a slightly higher ripple value with a much lower computational cost for dynamic loads can be employed.

## 4. Simulation and Hardware Results

To validate the numerically solved optimal interleaving patterns, the simulations have been carried out on a dual-inverter-based AC system in MATLAB/SIMULINK for a similar load pf range used in the numerical solutions. The simulation was tested on a line voltage and three-phase power requirement of 400 V (at mod index m = 1) and 2000 VA, respectively. Symmetric SVPWM, as presented in Table 1 and correspondingly used in the numerical results, was fed to the inverter with Ts = 100 us (fs = 10 kHz). Load impedance magnitude was kept constant for all the power factors and inductive and resistive components were varied accordingly for each pf, so that a similar comparison with numerical results can be accomplished. Results of the first load scenario described above (Figure 9) have been presented for comparative analysis. $i_{c,rms}$ results from these simulations (dashed '–' lines) have been plotted along with their numerical solution counterparts (solid lines with the same colour). For sequence interleaving, all possible combinations have been compared, and the results are shown in Figure 14a.




(**a**) (**b**)

**Figure 14.** Simulation results compared with the numerical results for RMS cap current for (**a**) sequence shifts and (**b**) sequence+discrete time shifts.

These simulated results can be observed to be very close to the numerical results, confirming the validity of the analytical formulation of the DC-link current as well as the associated ripple-minimizing algorithm. Slight differences between the two results may be attributed to the impact of approximating the current as a pure sinusoid for numerical formulation.

For sequence+time interleaving, the method described in Table 4 for approximating the optimal sequence with the corresponding $t_d^*$ was utilized in the simulation. Furthermore, the suitability of the identified $t_d^*$ in Table 4 is depicted by utilizing five different $t_d^*$ of $0T_s$ (no time shift), $0.25T_s$, $0.5T_s$, $0.65T_s$, and $0.8T_s$ on the identified optimal sequence shift, i.e., four-bit shifts for till 20° pf angle and five-bit shifts afterwards for case 1. Figure 14b shows the comparison between the simulation and numerical results. It can be observed, that for five-bit shifts (of pf angles higher than 20°), $t_d^* = 0.8T_s$ which is totally in line with Table 4. For a five-bit-shifted sequence, the optimal time shift range identified is $0.1T_s$–$0.15T_s$ as shown in Table 4, so for our discrete shifts, minimum $i_{c,rms}$ coexist at $t_d = 0T_s, 0.25T_s$ and $0.8T_s$ which is near-optimal if compared with Figure 9. Hence, by selecting a few discrete values of time shift we can obtain a near optimal result. So, this method can be used to apply sequence+time interleaving with reduced computational complexity for near-optimum results. Alternatively, a two-stage process can be used to reach the optimal value by first identifying a close approximation of the optimal time shift and then carrying out a limited exhaustive search. It is pertinent to note that simulations for only time shifts have not been shown here as the method of providing standard time shifts without any sequence rearrangements is already covered in combined sequence+time shift simulations.

For hardware results, two independent inverter systems have been developed. These identical inverter systems employ IGBT hex-bridge inverter modules by Infineon technology along with independent gate drive circuitry. For synchronized operation, both inverters

are controlled by a common STM32-f4 controller, that is used to feed each individual inverter with 10 kHz SVPWM (given in Table 1) with different values of mutual interleaving. In order to incorporate sequence interleaving, a rearranged/shifted sequence of SVPWM has been provided to the second inverter with respect to the first and the corresponding time sections for the three legs of the inverters are varied, while the time interleaving is provided as a counter offset in the controller. Hence, in the sequence+time interleaving, both mechanisms are simultaneously applied, i.e., a counter offset is given to the already rearranged time sections for the inverter legs. The inductive loads comprising the power resistors and the high-frequency inductors both with a current rating of 2 A, are used in a star configuration supplied by the prototype voltage supply rated at 60 V. Two variants of loads were used for different power factors. The hardware setup is shown in Figure 15 and the corresponding results of the DC current waveform are presented for the 20° and 60° in Figures 16 and 17, respectively, for sequence interleaving, and in Figures 18 and 19, for sequence+time interleaving. In these waveforms it can be seen that the overall envelope for the DC-link current, compared to the non-interleaving case (same sequence mentioned in the figures), tends to reduce for different values of interleaving. Furthermore, the envelope for the optimal sequence tends to be the smallest. For instance, in the sequence only interleaving case, in Figures 16 and 17, the envelope for a four-bit-shifted sequence, which is the optimal sequence shift from Figure 9c, appears to be the lowest. The same trend can be seen for sequence+time interleaving as well. Moreover the quantified comparison of these practical results has been performed by computing the $i_{c,rms}$ for each of these waveform and presented in terms of bar graphs in Figure 20a for sequence interleaving and in Figure 20b for sequence+time interleaving. Comparing these bar graphs with Figure 14, the differences in the relative order of magnitude of $i_{c,rms}$ for the different shift values can be observed between the simulation and practical results. These differences can be attributed to the inherent non-linearities and noises associated with the real-life system. However, the relative trend of variation in Figure 20 is similar to that in Figure 14 at respective pf angle values. This shows that the proposed formulation and approach of obtaining the minimized DC-link current ripples as well as mutual comparisons among the sequence and time interleaving are feasible for practical implementation even with the incorporation of practical non-idealities.

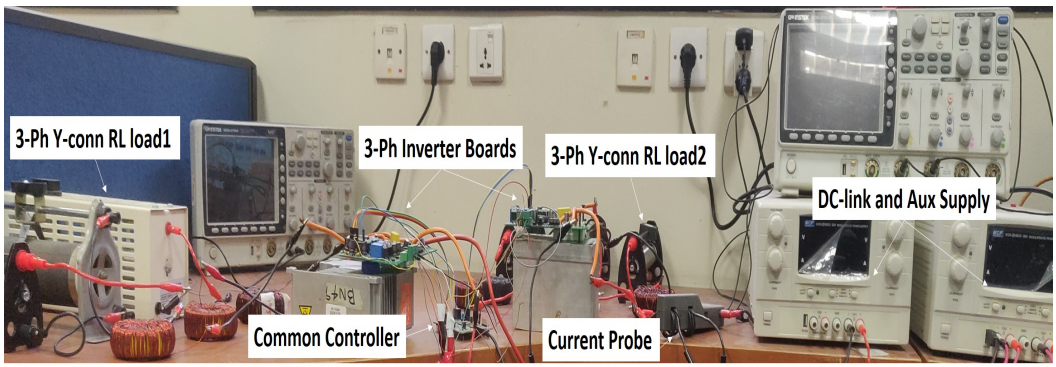



**Figure 15.** Hardware Setup

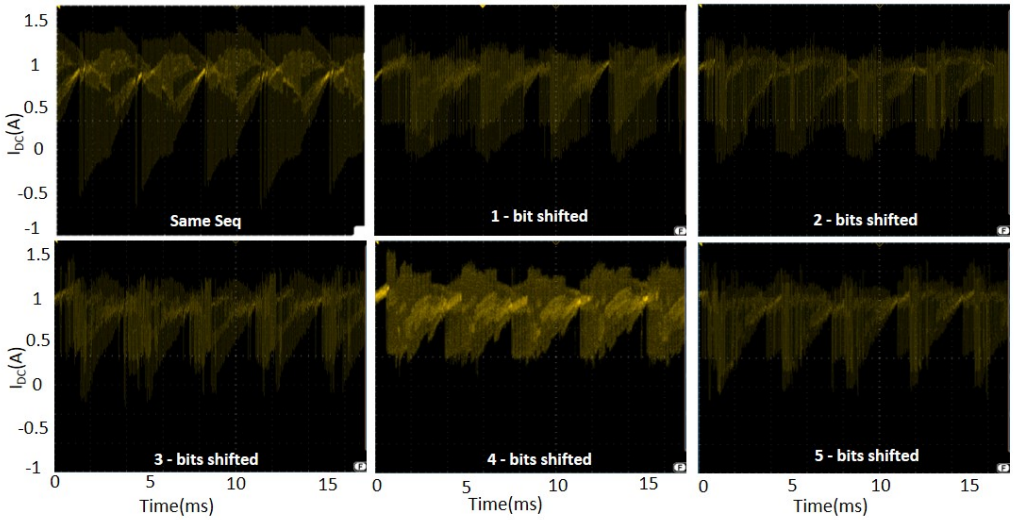



**Figure 16.** Experimental DC−link current for sequence-shifted interleaving at 20° pf angle.

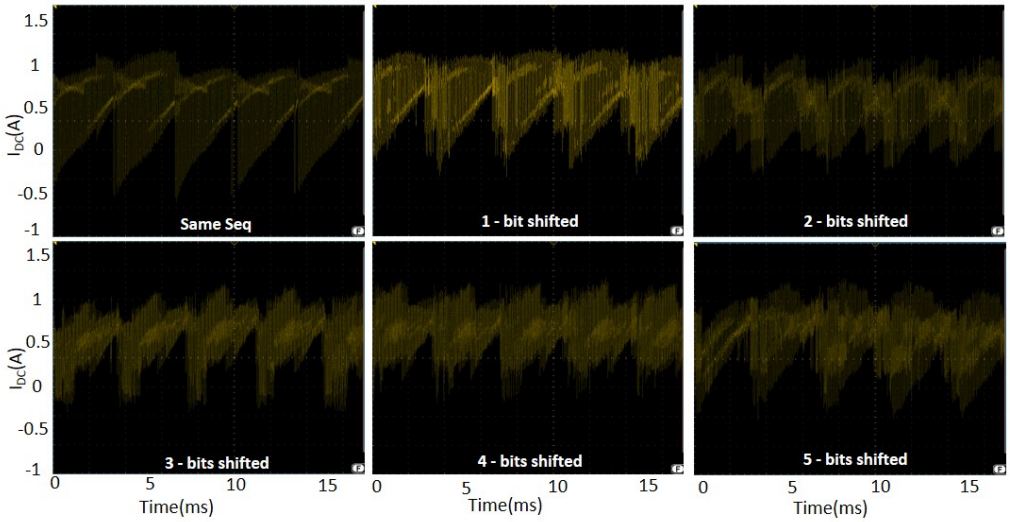



**Figure 17.** Experimental DC−link current for sequence-shifted interleaving at 60° pf angle.

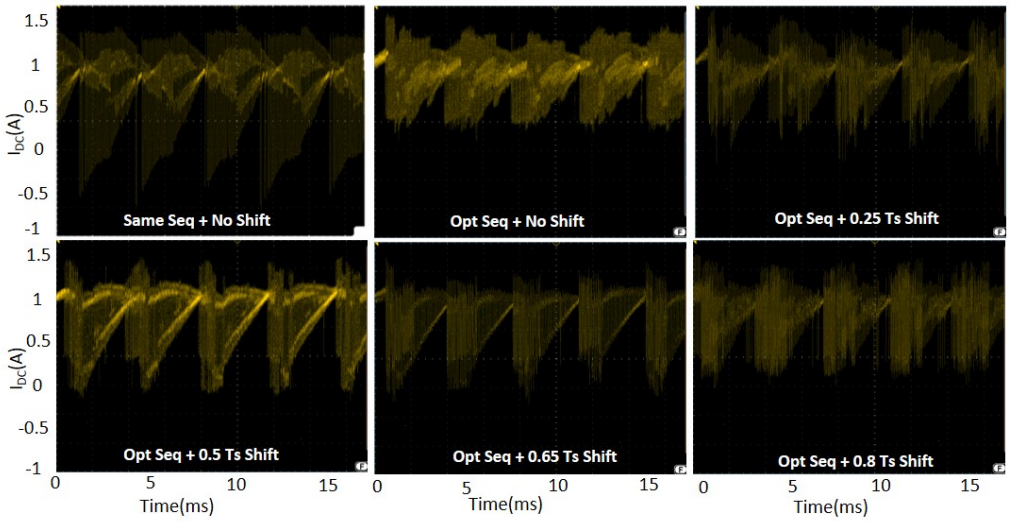



**Figure 18.** Experimental DC−link current for sequence+time-shifted interleaving at 20° pf angle.

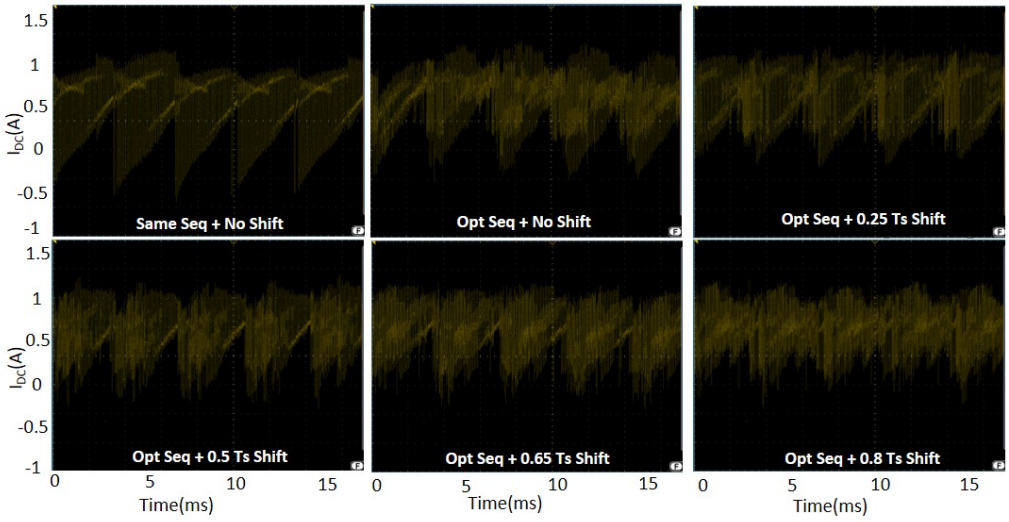
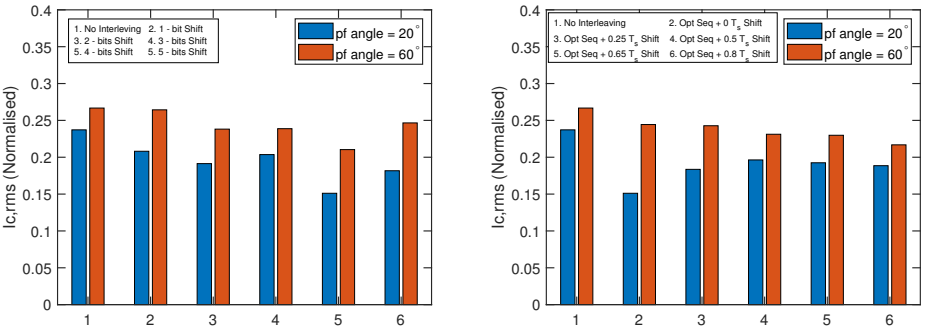



**Figure 19.** Experimental DC−link current for sequence + time-shifted interleaving at 60° pf angle.




(**a**) (**b**)

**Figure 20.** RMS capacitor currents obtained from the hardware results for (**a**) sequence shifts and (**b**) sequence+time shifts.

## 5. Conclusions

A comprehensive evaluation shows that the proposed method of minimization of the DC-link ripple current is effective and practicable compared to the existing concept of standard shifts. As depicted in Section 3.2, the improvement produced by the proposed methods of interleaving is significantly better than the existing static shift methods under a wide region of individual and mutual load variations discussed. Thus, these methods can apply to a large variety of multi-inverter applications where different kinds of load variability are required.

In addition, testing reveals the relative performance merits of sequence-, time- and sequence+time-based interleaving for different ranges of power factors and load characteristics. We find that sequence interleaving is effective in DC-link current quality improvements with a significantly lower computational complexity. In terms of ripple reduction, the combined impact of sequence+time interleaving is better. However, as discussed with Algorithm 1, and then in terms of numerical results, a higher computational burden and a two-stage process of optimization is needed. Furthermore, the time shift values also tend to have variation with changing loads. Hence, sequence+time shifts can provide a higher level of DC-link improvement with added computational cost. A trade-off in computational cost and minimization of the objective function in practical systems can be achieved by a near-optimal approximation of the sequence+time shift with discrete pre-defined values. The pre-defined values can be calculated offline, especially in applications where load variations are low. The sequence-based interleaving has limited permutation shifts and tends to have similar bit shifts for minimum DC-link ripples. Sequence-based interleaving

results in significantly lower computations and memory requirements, for pre-defined values storage, at the expense of slightly reducing quality improvements.

Lastly, our proposed formulation is generally applicable to any variant of conventional or modified space vector-based modulation by replacing the respective sinusoid segments and associated time periods. This paves a way to extend the interleaving concept to existing modulation schemes aiming for different improvement metrics, such as common-mode voltage reduction.

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## Abbreviations

The following abbreviations are used in this manuscript:

| | |
|---|---|
| SVPWM | Space vector pulse width modulation |
| SPWM | Sinusoidal pulse width modulation |
| RMS | Root-mean-square |
| THD | Total harmonic distortion |
| IGBT | Insulated date bipolar transistor |

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