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Design and Implementation of CNFET SRAM Cells by Using Multi-Threshold Technique

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Abstract: This paper presents a CNFET (Carbon Nano-tube FET) based MT (Multi-Threshold)-SRAM (Static Random Access Memory) design based on the leakage reduction mechanism. A multi-threshold logic is employed for reducing the leakage current during read/write operations. Here, the multi-threshold technique is used to insert the high threshold sleep control to the low threshold circuit. The insertion is performed in a serial manner. The high threshold transistors are very useful for deriving the low sub-threshold current. Meanwhile, the low threshold transistors are promising for improving the circuit performance. The high-low threshold transistor pairs are used to change the channel length by modifying the oxide thickness of the transistors. The overall implementation of the Multi-threshold-based SRAM cells are implemented with the help of CNFET in-order to avoid the short channel effect, mobility degradation which is occurred while considering the channel length below 32 nm in CMOS (Complementary Metal Oxide Semiconductor) devices. The paper clearly represents the performance improvement of the proposed SRAM cells with above-mentioned technologies.

Keywords: SRAM; multi-threshold; CNFET; pre-charging; low-power; delay; threshold voltage

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1. Introduction

In many electronic devices and microprocessors, the SRAM (Static Random Access Memory) is commonly used for caches. The SRAM produced better performance compared with the Dynamic Random Access Memory (DRAM). The DRAM capacity is much greater than the static type and it needs more time to refresh itself. This time delay causes the increment of the latency to access the data. In recent electronic devices that are assigned for particular applications such as multimedia, object tracking, video processing, and medicine, the computation process and complexity have been increased and it is also reflected in the power consumption. These devices have unique processors that consumed huge SRAM sub-modules. Hence, the SRAM is one of the much delegated memory modules for power considerations [1]. The limitation of the SRAM power consumption is performed by decreasing V_{dd} supply voltage or V_{th} threshold voltage.

1.1. Basics of CNFET

At nano-meter region of channel length, the CMOS devices will achieve the technological physical limitations. Due to this physical limitation, the failure and defect rate to be much huge in MOSFET devices. Therefore, an emerging developed technology is required to achieve the high performance. Hence, the CNFET is one of the most promising technologies instead of Si-based devices. The reason for taking the CNFET devices over the silicon devices can be justified by,

(1) Effect of Gate oxide thickness: If the gate oxide thickness of CMOS devices decreases, it will increase the quantum capacitance for a variety of gate voltages.
(2) Effect of Temperature: The CMOS behavior and characteristics change with respect to the increase in the temperature rating. The acceptable temperature rating of the Si-CMOS device is 150°. This temperature rating severely affects the V_{th} (threshold voltage). For example, if the temperature increases from 27° to 227°, it will vary the 4.6% variation of the V_{th}. In this case, we definitely stated that the CMOS operates maximum at 150° and device parameter changed at high temperature rate.
(3) Effect of Channel Length (L_{ch}): Channel length is the key factor in CMOS devices. If we are decreasing the channel length, it will reflect in the changes in the packing density. As the channel length of CMOS devices scales down to the nano-meter region, the V_{th} was also scaled and it will increase the leakage power. The increases in the leakage power bring changes in leakage current, which becomes the limiting factor of thinner oxide thickness of 1.5 nm. If the L_{ch} becomes very less, the drain depletion region will enter the source and it will decrease the e^- injection barrier. It automatically degrades the device performance.
(4) Parameter consideration of CMOS & CNFET: Both devices have unique parameter specifications in circuit design. The following Table 1 illustrates the parameter variation of the CMOS and CNFETs.

Table 1. Parameters of Si-CMOS and CNFET.

Parameters	Si-CMOS	CNFET
Vt	0.2–0.5 V	0.293 V, −0.557 V, & −0.293 V
Idlin	$I_D = \mu C_{ox} \frac{W}{L}[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}]$	$I_d = K_n[2(V_{gs} - V_T)V_{ds} - V_{ds}^2]$
Idsat	$I_D = \mu C_{ox} \frac{W}{2L}(V_{GS} - V_{TH})^2$	$I_{d(sat)} = K_n(V_{gs} - V_T)^2$
SS	~70 mV/dec (@ Room Temperature)	61.3 mV/dec
DIBL	$\text{DIBL} = \frac{V_{Th}^{DD} - V_{Th}^{low}}{V_{DD} - V_D^{low}}$	65.65 mV/V

The CMOS-based SRAM cells suffered from short channel effects (SCEs), mobility degradation, etc. when considering the channel length of 32 nm. Hence, the CMOS devices did not produce better performance in 32 nm channel length. This drawback was overcome by introducing the multi-gate devices such as Fin-FET and CNFET.

In recent decades, the CNTs have more attention because of its thermal, electrical and mechanical properties. Based on the ultra long mean-free path, the CNFETs are classified for elastic scattering, which is similar for holes, electrons, easy combination of high-K dielectric materials, and high Fermi velocity characteristics. The fabrication process of the CMOS and CNFET is similar, and the design approaches of CMOS are separated for CNFET based circuit design. Due to the huge current drive capability, less PDP (Power Delay Product), high thermal stability and ballistic transport, the CNFETs have been considered promising devices [2]. Figure 1 shows the layouts of the CNFET where the channel regions are highly doped and less dopant are added to the CNT channel. These are considered the interconnection between the 2 adjacent devices or S/D extended region. The single intrinsic CNT (inset) model is depicted in Figure 1, which is the origin point of the modeling of complete CNFET devices [3].

Figure 2a,b show the CNFET's side and top view, which consist of 6 single walled CNTs considered as the channel material. The CNT is either a semiconducting or metallic material based on the chirality factor. The recent CNFETs give considerable percentage for metallic CNTs (m-CNTs), which short the S/D in CNFETs. This m-CNT is removed by employing the proper function. Here, two important methods incorporated to neglect the unwanted m-CNTs, (1) SCE (Selective Chemical Etching) and (2) VMR (VLSI compatible m-CNT Removal). The above-mentioned two methods eliminate the metallic tube, which is close to 99.9%. A traditional synthesis process of CNFETs approximately produced

113 m-CNT and 2/3 s-CNT (semiconducting CNTs). In recent CNT, growth methodologies reach high amounts (90%) of producing s-CNTs [4]. However, there is no technique available for achieving 100% CNT-growth. Hence, it is an important for adapting the different techniques for removing the m-CNTs like chemical etching process and electrical burning, etc. At the same time, the diameter variation of the CNTs affects the electrical properties such as threshold voltage and drive current. The multiple diameter distribution and mean diameters are observed based on the CNTs production method. During the manufacturing process of the CNFETs, these variations occurred due to doping process and mis-positioned/mis-aligned CNTs in the transistor. This leads to short the CNFETs. However, to date, the CNFETs didn't include this type of source variability [5].

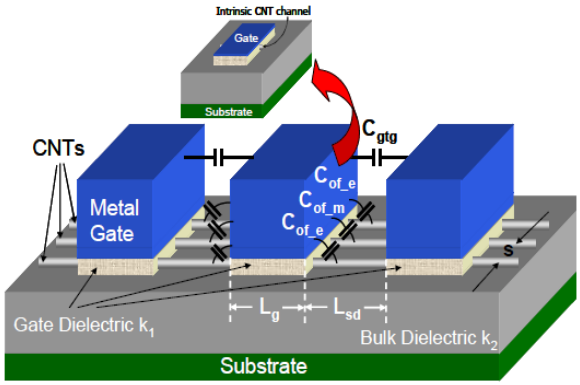


Figure 1. Layout of the CNFET device.

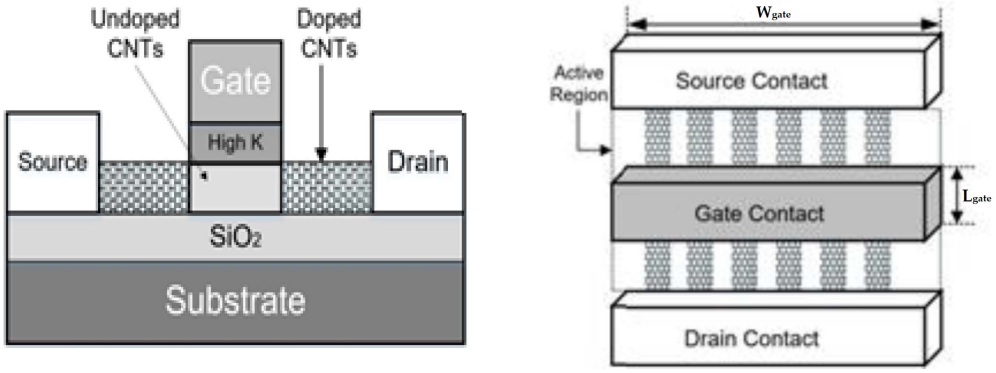


Figure 2. (**a**) Side view of a CNFET, (**b**) Top view of CNFET.

The initial stage of the CNFET fabrication involves the parallel metal strips pre-patterning in SiO_2 substrate. Once the pre-patterning process is completed, CNTs are deposited at the top in a random manner. This CNTs fall around the two metal strips and meet all necessary requirements for basic FET. Here, one metal for the source terminal and another for the drain terminal. The source/drain terminals are made from the chromium/gold materials and SiO_2 is used as the gate oxide.

1.2. CNFET Parameters

(1) CNTs Array: CNT is the hollow nature of a nano-structured cylinder which is made from the carbon atoms. The CNTs have a mono-shell of carbon atoms known as SWCNTs (single-walled CNTs). The CNFET is different from the MOSFET in that it contains the channels built with a parallel of CNTs arrays [2].

(2) Diameter: The CNFET's diameter is defined by the chirality factor (n, m) where n and m are non-negative integers. Based on (n, m), the nature of the CNFET is defined as

either metallic or semiconductor. If we are considering diameter as 1.5 nm, then the chirality factor is equal to (19, 0) [6].

(3) Technology Parameters: The specification of the technology parameters for 32 nm channel length is described in Table 2.

Table 2. Parameters of CNFET.

Parameters	Value
V_{dd}	0.8 V
Gate Length	32 nm
Chirality Factor	(19, 0)
Diameter of PCNFET	1.487 nm
Diameter of NCNFET	0.783 nm

1.3. Existing Methodologies of Designing SRAM Cells

In recent decades, several methodologies boomed for efficient designing of SRAM cells. A high-speed 10T SRAM cell was developed by [7] in FinFET technology at 14 nm channel length. The presented 10T-SRAM cell was approximately 2 times greater than the Six-Transistor HD SRAM cell. Next to this, a low leakage SRAM cell was designed by [8] in which the memory cells were based on the S (Source)-biased inverter. Additionally, two transistors were used in the S-biased inverter to diminish the $I_{leakage}$ current, which results in saving of leakage power up-to 67% when compared with the traditional inverter. The double ended low powers SRAM was constructed by ref. [9], which utilize the low-power stacked inverters for limiting the power dissipation. By introducing cross-coupled inverters with low V_{dd}, the power dissipation is further reduced in the hold mode with power gating techniques.

A low-power single-ended 9T SRAM cell was designed by ref. [10], which countered against LPA and discussed the issue of leakage balance. 7 nm FinFET-based 6T SRAM cell was designed by [11] and the performance comparison was completed with different FinFET devices such as PU (Pull-Up): PD (Pull Down): PG (Pass Gate) transistor ratios to come out suitable devices for LP (low power) and HS (high speed) SRAM applications. The HP SRAM cell was constructed by ref. [12] by using the array of high-bandwidth with 0.0300-µm Intel 4 CMOS technology. The presented 6T SRAM array was compared with 8T SRAM cell for the applications of high-bandwidth memories. By using the 12 nm FinFET technology, the researcher [13] designed an SRAM cell with six transistors. Here, Static Noise Margin (SNM) was used to determine the SRAM cell's stability.

The 8T SRAM cell was designed using a pair of PMOS/NMOS transistors as a diode connection in-order to limit the leakage current [14]. This architecture controlled the amplitude of the current. As Fin-FET devices gave lower V_{th} which is much superior to the gate leakage. The diode-linked NMOS-PMOS was employed to achieve B-S (Bulk-Source) difference to limit the sub-threshold and gate leakages. The diode connected Multiple approaches were utilized for reducing the leakage current. Meanwhile, the amount of leakage power was reduced and increased the performance. The leakage power reduction on SRAM cells is presented by ref. [15]. Here, the authors performed the dual voltage assignment for reducing the leakage power effectively. On the other hand, the memristor based SRAM cell was designed by [16]. Here, the memristor is mainly used for reducing the area consumption compared with the CMOS design without negotiating the functionality of the device. The noise margin was improved in the 7T SRAM cell which had the channel length of 7 nm. By incorporating the technologies like sleep transistors, DTMOS, and MOSFET, the 7T SRAM were designed and also performance analysis was also completed in this method [17].

Dual-rail SRAM with embedded level shifting was designed by [18]. This method was mainly implemented to enhance the dual-rail SRAM's availability because it had more

potential to increase demand in low power applications. At low supply voltage, there was a huge degradation in performance, which couldn't satisfy the high-performance cache necessity in modern computers. The author designed the 6T SRAM based on a comprehensive assessment in 7 nm FinFET technology. Here, the circuit implementation was completed by quantum physics-based device co-optimization. The power gating based FinFET SRAMs were developed by [19] and the method contained three techniques for minimizing the EDP (Energy-Delay Product) and leakage power of 8T and 6T SRAM cells [20].

In recent years, CNFET (Carbon Nano-tube Field Effect Transistor) technology-based circuit design has been raised enormously. The author [21] designed the CNFET-based SRAM cell. The presented design was optimized on the basis of trades such as power efficiency, stability, and performance. The ternary-based two SRAMs were designed by ref. [22], which contain different technologies. In the initial design, the cyclic operation was completed in ternary logic, with a secondary design based on the buffer that was mainly employed for the ternary inverters in both positive and negative cycles.

As we summarized, the previous SRAM cells suffered from leakage. Hence, multi-threshold logic is one of an existing and innovative methodology that uses the low-threshold transistor for designing the circuits. This helps to improve the performance of the circuit in active mode and saves leakage power in the standby mode. Due to ambi-polar properties, there is a possibility of leakage in the CNFET devices. So, this special logic (i.e.,) Multi-Threshold (MT) logic is influenced by the CNFET to reduce leakage while considering the 32 nm channel length of the SRAM cell design.

1.4. Importance of Multi-Threshold (MT) Logic

In VLSI, the power reduction and leakage reduction [23] are mainly aimed at producing the circuit to be more efficient. This power reduction is very important to meet the desired temperature characteristics, increase battery life time for compact devices and reduce the cost of packaging and maintenance.

Multi-Threshold (MT) is also known as the power gating technique, which provides efficient and simple power gating logic by using the low threshold voltage and high-speed transistors for constructing the logic cells and uses the high threshold voltage and less leakage devices as sleep transistors. This sleep transistor (ST) provides higher resistance between the V_{dd} and ground to minimize leakage dissipation. The STs are controlled with the help of sleep control signals. When sleep = 1, the ST in switched OFF during the standby mode which causes the limiting of leakage by ST. The entire leakage of the circuit is limited by the ST's high threshold voltage. During active mode, the sleep signal in '0' state and provides the connection between the real to virtual ground. As a result of this connection, the lower threshold logic gates operate in very high speed. In this active mode, the STs are working like a resistor.

2. Traditional SRAM Cells

2.1. 6T-SRAM Cell

A collection of 6-transistors, along with a sense amplifier, write circuitry, and row and column decoders are used to construct the conventional SRAM cell, and its schematic view is depicted in the Figure 3 [24].

Read Operation: SRAM cell addresses are decoded by the column and row decoders in which the data has to be read. Initially, the BL is pre-charged to V before the read operation starts. Once the word line (WL) is activated, the B is discharged via the M5 transistor. The voltage variation in the BL is very small due to the limited capability of the cell driving current. The small voltage difference across BLs is sensed by the sense amplifier, and finally, whether the value "1" or "0" is stored in the SRAM cell.

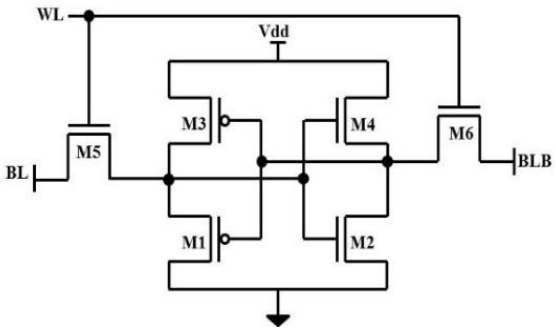


Figure 3. Traditional 6T-SRAM cell [24].

Write Operation: with the help of the external devices, the data has to be stored. The column-row decoders are used for providing the address of the cell. When the WL is enabled, the write function is processed to write the data into the cell, which is fully dependent on the column gate condition. The amount of time consumed by the write operation is less when compared with the reading operation time because the write buffer has a high capability to drive the huge driving current.

2.2. 7T-SRAM Cell

The 7T-SRAM cell is mainly considered for reducing the static power and improvising the read operation. Here, the transistor M7 is connected to form the feedback mechanism in order to boost the high value at the primary inverter and lower value on the secondary inverter, and vice-versa. The read and write operations are performed by M5 and M6 transistors by enabling WS and RS signals, respectively. During the read cycle, the M7 transistor is in ON condition and M7 is OFF in write operation. By resizing the M6 and M7 transistors, the performance of the read cycles is improvised, and the charging of the RB (Read Bit-line) becomes faster. The 7T-SRAM cell configuration is illustrated in Figure 4 [24,25].

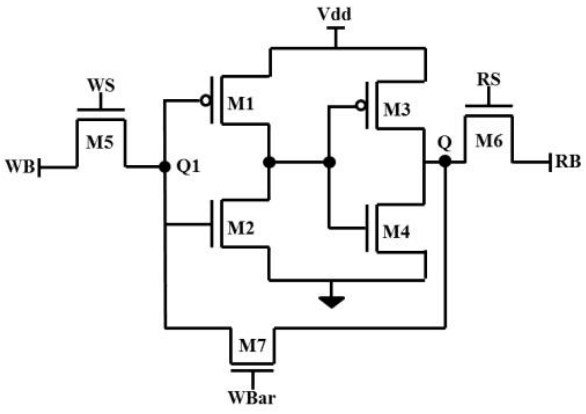


Figure 4. Traditional 7T-SRAM cell.

2.3. 8T-SRAM Cell

Figure 5 illustrates the schematic view of an 8T-SRAM cell. The structure of the 8T-SRAM cell looks like a 6T SRAM cell in which additional 2 transistors are used for separating the internal inverter and WL during read cycle operation. Before initialization of read operation, the RB is pre-charged to the supply voltage V_{dd}. Here, the read cycle is enabled by bit RW whereas RB remains in either logic 1 or logic 0 states, which depends on the Q internal node. The write cycle of the 8T-SRAM is similar to the 6T-SRAM write operation [24].

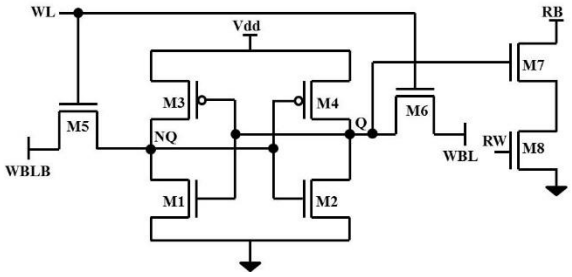


Figure 5. Traditional 8T-SRAM cell.

2.4. 9T-SRAM Cell

The pairs M4–M5 and M1–M3 are used for constructing the internal inverters, whereas one bit information is stored as illustrated in Figure 6. With the aid of WB and transistor M2, the write cycle has been performed. Meanwhile, the bit RB and transistors M6, M7, and M8 are utilized for performing the read cycle. Due to 9T structure, the read cycle data stability has been significantly improved [24].

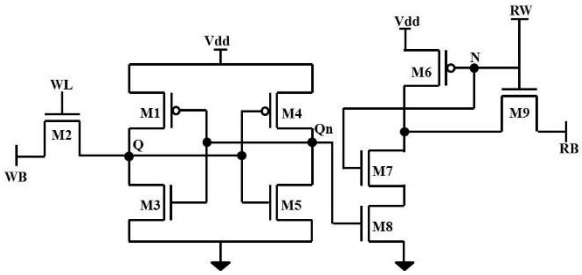


Figure 6. Traditional 9T-SRAM cell.

2.5. Difference between 6T, 7T, 8T and 9T SRAM Cells

The stated 6T, 7T, 8T, and 9T SRAM cells are uniquely designed for particular reason.

- In 6T SRAM cell, the transistor pairs (M1–M3 and M2–M4) are used to form the inverters. In this structure, these transistor pair employed to store the information of bits. The transistors M5 and M6 called as access transistors for performing read and write operations. By selecting, dual bit-lines, the noise margin can be improved.
- In 7T SRAM Cell, an additional feedback transistor is employed for improving the read and write cycle and it also reduces the static power consumption.
- In 8T SRAM Cell, an additional two transistors are used for isolating the inverter pairs from accidental write operation while performing read operation. It produces high noise margin compared with the 6T SRAM Cell.
- During Read cycle of 9T SRAM Cell, the data stability is improved when compared with other SRAM cells.

3. Proposed Multi-Threshold SRAM Cells

3.1. Mathematical Modeling of MT-Logic

A sleep transistor (ST) is either N-type or P-type, and it is mainly employed to shut off or switch on the power supplies to design parts in standby mode. Generally, the P-type ST is used to switch on the V_{dd} supply, and hence is known as a "Header switch". The N-type ST normally controls the V_{ss} supply, so it is known as "Footer switch". The approach of the ST is straight forward; the optimized design of the ST is a challenge due to various effects, such as performance, routability, entire power dissipation, area, and signal/power integrity.

The high quality of the ST design is justified by three important metrics, such as efficiency of the area, IR drop, and switch efficiency. The ST can be optimized in terms of

gate length, width, and body bias, and finger size in order to achieve a high amount of area and switching efficiency, IR drop, and less leakage current.

At the absence of the ST, the delay (T_d) of the single gate is expressed in following Equation (1).

$$T_d = \frac{C_L V_{dd}}{(V_{dd} - V_{tL})\alpha} \tag{1}$$

where C_L represents load capacitance connected at the gate terminal, $V_t{}^L$ is the lower threshold voltage, V_{dd} is the supply voltage, and the velocity saturation index is represented as α. If the ST is present, then the delay of a single gate ($T_d{}^{sleep}$) will be measured with the help of following Equation (2).

$$T_d^{sleep} = \frac{C_L V_{dd}}{(V_{dd} - V_x - V_{tL})\alpha} \tag{2}$$

where V_x is the virtual ground potential. The multi-threshold logic will slow down in the presence of large current spikes, but it speeds up again while performing the transition. In the MT logic, the input vectors robustly influence the delay, and it plays vital role in determining the worst-case of the input for accurate sizing of ST. One more alternative approach also available to size the worst-case input vector is to make the worst-case peak current. Meanwhile, it is necessary to ensure that the virtual ground should be limited within the threshold voltage. To highlight this, the maximum amount of current for input vector transition (00 00 to FF 81) is considered as 1.174 mA (not necessary be a maximum peak current). If the virtual ground is employed, then 50 mV of offset will be induced and it will be produced degradation of 5%. Hence, the circuit can tolerate the degradation of 5% in the presence of ST. Then the ratio of T_d and $T_d{}^{sleep}$ is given in Equation (3).

$$\frac{T_d}{T_d^{sleep}} = 95\% \tag{3}$$

By substituting Equations (1) and (2) in Equation (3), we can get Equation (4).

$$1 - \frac{V_X}{(V_{dd} - V_{tL})} = 95\% \tag{4}$$

Therefore, we can formulate the V_x as shown in Equation (5).

$$V_x = 0.05(V_{dd} - V_{tL}) \tag{5}$$

3.2. Proposed MT-SRAM Cells in CNFET

The proposed design of SRAM cells contains the technique called multi-threshold (MT) technique. In this, the transistor consists of double threshold voltages (V_{th}) to optimize the delay and power. Generally, the multiple threshold voltage lies in the gate terminal of the transistor at which this creates the inversion layer and interface between the oxide and body layer. Therefore, the transistor will quickly switch ON with minimum threshold voltage and also it reduces the critical path clock period. One of the main drawbacks of this lower threshold is that it exhibits huge amount of leakage power. Hence, to limit this leakage current, a transistor with high-threshold voltage is introduced which has the minimum amount of static power. This causes the reduction of static leakage 10 times better than the lower threshold transistors [26].

In this technique, the sleep transistor is used to detach the transistor with lower threshold voltage and it has the high threshold voltage transistor that located in both bottom and top of the circuit. In the proposed design, the MT technique is infused to the traditional SRAM Cells and presented SRAM cells in CNFET are shown in Figures 7–10. The sleep transistor is controlled by the sleep signals. During the active state of the transistor, there is a distortion in the sleep signal which results in the ON condition of the higher

threshold voltage transistor and it supplies the virtual power and lower threshold voltage to be grounded. During the inactive state of the transistor, a step signal is generated and pushes the transistor to higher threshold voltage which moves into the cutoff region. This results in the disconnection of power from the less threshold voltage. Finally, the minimum current exhibited at the region of threshold from power to ground.

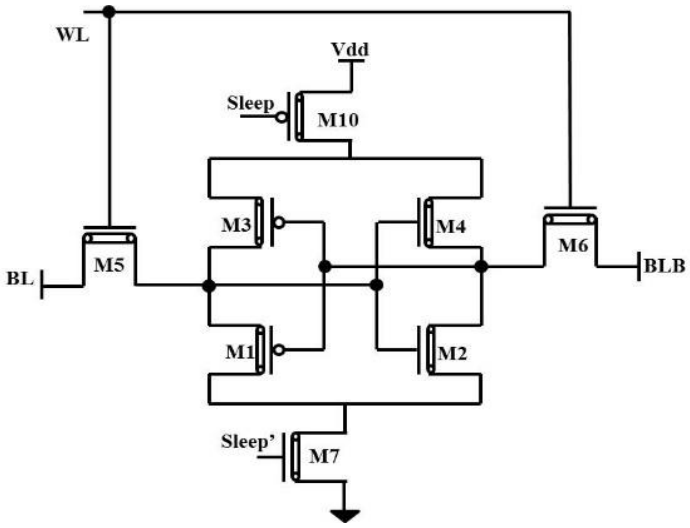


Figure 7. CNFET-Multi-Threshold 6T-SRAM cell.

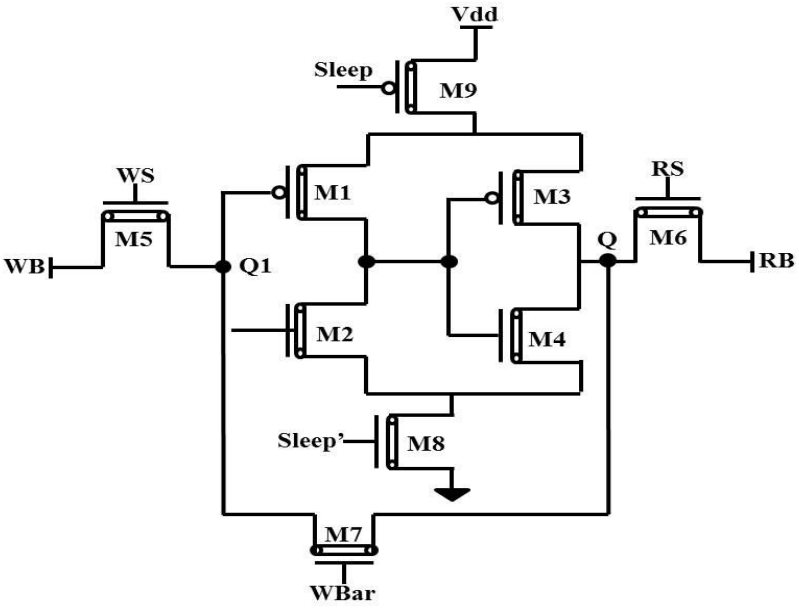


Figure 8. CNFET-Multi-Threshold 7T-SRAM cell.

3.3. Systematic Variability of SRAM Cells

The impact of the variations in the across-field of the transistor terminals will lead to the nominal changes in the width (W) and length (L) fluctuations [27]. The width and length fluctuations are affected the performance of the SRAM cells. But the standard CNFET devices designed with W = 64 nm and L = 32 nm. If we are reducing the channel length less than the 32 nm, it will make the SRAM cells to be more complex and produce inaccurate results. Similarly, if we are increasing the channel length greater than 32 nm, it will produce the Schottky barrier. Due to this effect, we didn't get the accurate results. So, the proposed SRAM cells focused only on 32 nm channel length.

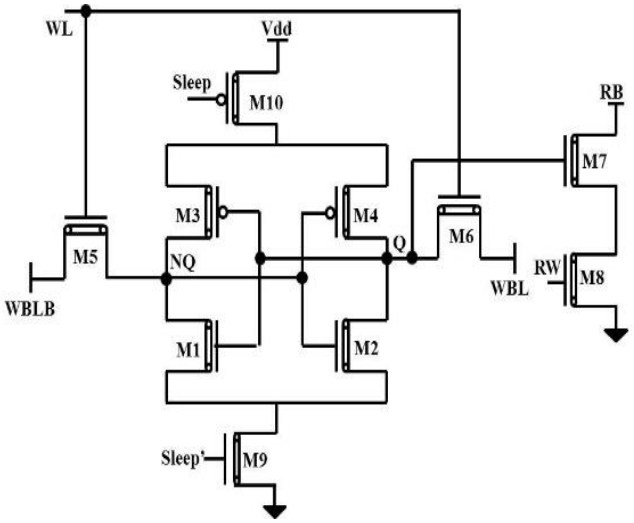


Figure 9. CNFET-Multi-Threshold 8T-SRAM cell.

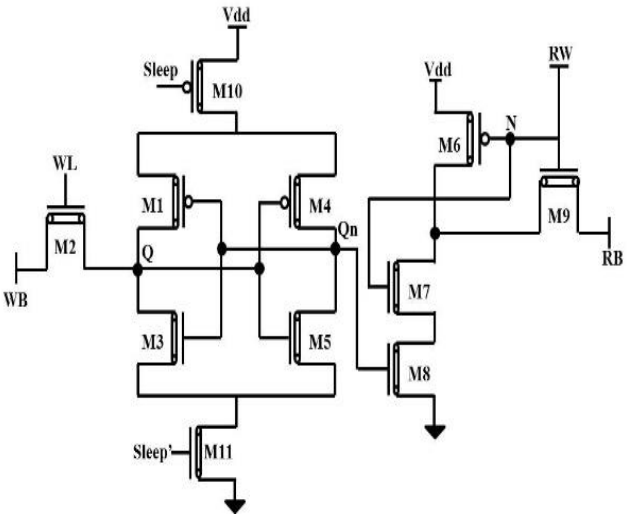


Figure 10. CNFET-Multi-Threshold 9T-SRAM cell.

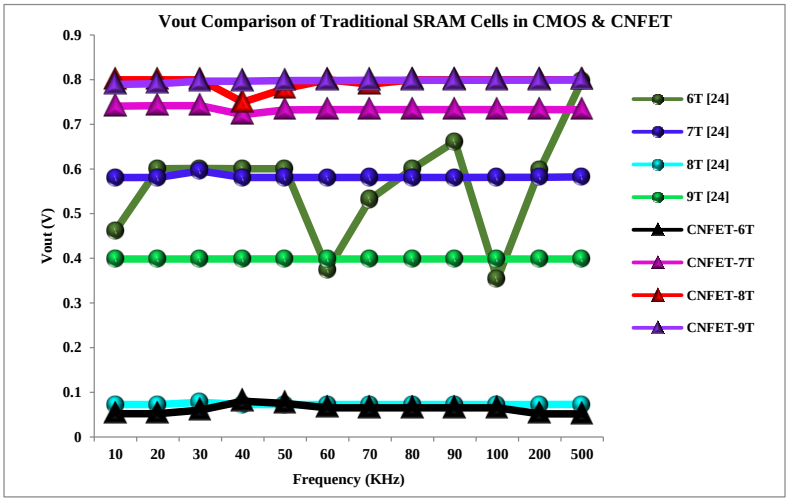
4. Simulation Results

The overall implementations of the existing and proposed methods are implemented in the two different technologies at 32 nm channel length in LTspice and HSpice simulators. The CNFET device can be realized with the help model files available in [28].

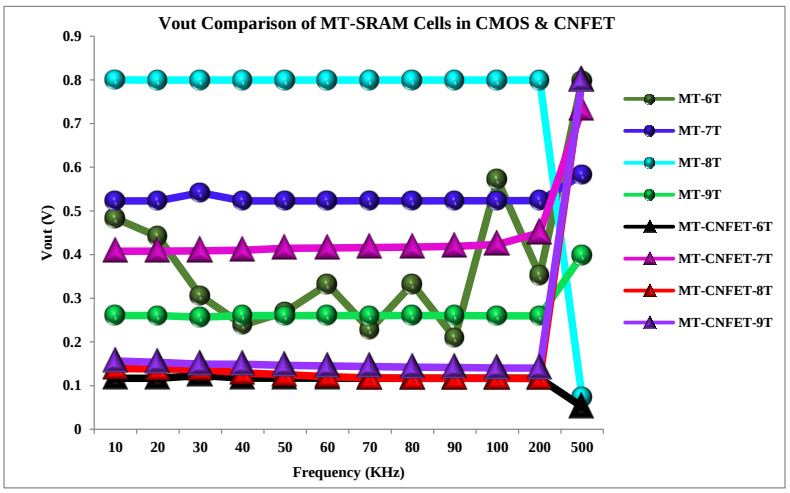
Low power consumption is the ultimate aim in VLSI circuits. To achieve this, we have to measure the power consumption of different SRAM cell and this can be held by parameter P_{avg}. Another important parameter is delay which shows the time taken by the SRAM cells to produce the outputs from input bit-lines. If we achieved less amount of delay, then the SRAM cells will be operated in high-speed. For proving the SRAM cells performance, we calculate V_{out}, I_{avg}, P_{avg}, E_{avg} and delay. For detailed comparison, the design approaches implemented in multiple frequencies varies from 10 KHz–500 KHz.

4.1. Comparison of Vout

The Figure 11a,b show the output voltage comparison of the existing and multi-threshold (MT) SRAM cells. If the read and write operations are performed well in the 6T SRAM cells, they will be automatically reflected to provide a higher output voltage. As a result of this comparison, the proposed CNFET-based 6T SRAM cell performed better, and the following Tables 3 and 4 illustrate the improvement percentages of CNFET-6T and MT-CNFET 6T SRAM along with all other methods.



(**a**)



(**b**)

Figure 11. (**a**) Vout Comparison of Traditional SRAM Cells in CMOS and CNFET. (**b**) Vout Comparison of Proposed MT-SRAM Cells in CMOS and CNFET.

Table 3. Vout Improvement (%)–Traditional CNFET 6T SRAM Cell vs. Other SRAM Cells.

Frequency (KHz)	CMOS-6T [24]	CMOS-7T [24]	CMOS-8T [24]	CMOS-9T [24]	CNFET-7T	CNFET-8T	CNFET-9T
10	89	91	28	87	93	93	93
20	91	91	29	87	93	93	93
30	90	90	22	85	92	92	92
40	87	86	11	80	89	89	90
50	87	87	23	81	90	90	91
60	83	89	10	84	91	92	92
70	88	89	10	84	91	92	92
80	89	89	10	84	91	92	92
90	90	89	10	84	91	92	92
100	82	89	10	84	91	92	92
200	91	91	29	87	93	94	94
500	94	91	29	87	93	94	94

Table 4. Vout Improvement (%)–Proposed MT- CNFET 6T SRAM Cell vs. Other MT- SRAM Cells.

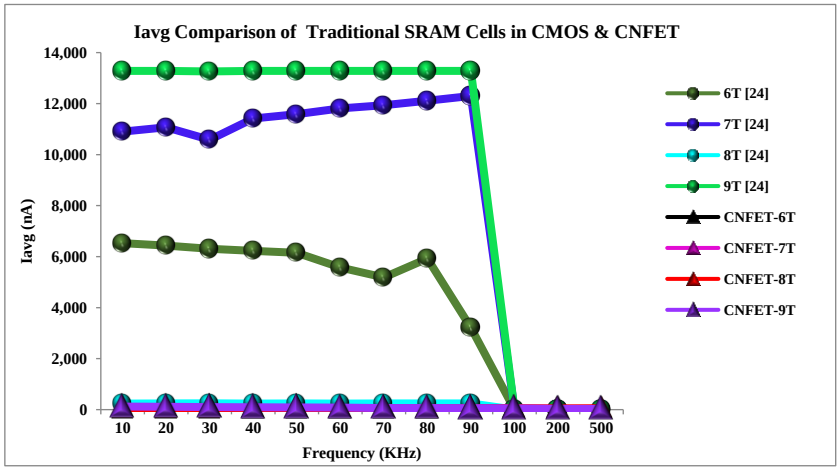
Frequency (KHz)	MT-6T	MT-7T	MT-8T	MT-9T	MT-CNFET-7T	MT-CNFET-8T	MT-CNFET-9T
10	76	78	85	55	71	16	25
20	74	78	85	55	71	15	24
30	60	77	85	52	70	10	17
40	51	78	85	55	71	9	21
50	56	78	85	55	72	6	20
60	65	78	85	55	72	3	19
70	49	78	85	55	72	0.43	19
80	65	78	85	55	72	0.12	18
90	44	78	85	55	72	0.13	18
100	80	78	85	55	72	0.08	17
200	67	78	85	55	74	0.27	17
500	79	78	85	55	76	0.38	17

4.2. Comparison of I_{avg}

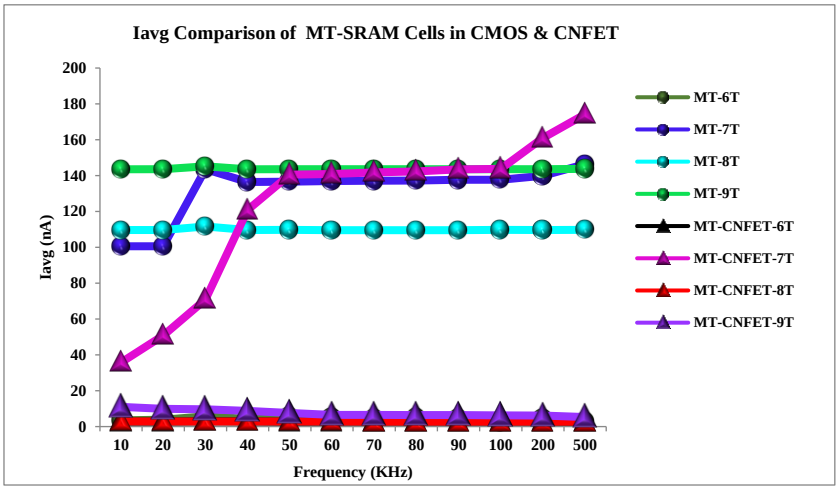
The Figure 12a,b shows the average leakage current comparison of the existing and proposed MT-SRAM cells. In SRAM cells, thickness of the NCNFET gate oxide layer and pull down transistor are increased which results in increasing of the V_{th} (threshold voltage) and reduction in the leakage current. This leakage current depends on the different device parameters and terminal voltages. As a result of this comparison, we found that the existing CMOS based SRAM cells fall in the μA range of the leakage current. But proposed SRAM cells lie in the range of nA. Hence, we clearly stated that the proposed SRAM cells (particularly CNFET-6T and MT-CNFET 6T) produce less leakage, and the following Tables 5 and 6 have shown the improvement percentage.

Table 5. Iavg Improvement (%)–CNFET 6T SRAM Cell vs. Other SRAM Cells.

Frequency (KHz)	CMOS-6T [24]	CMOS-7T [24]	CMOS-8T [24]	CMOS-9T [24]	CNFET-7T	CNFET-8T	CNFET-9T
10	100	100	100	100	83	73	88
20	100	100	100	100	82	73	87
30	100	100	100	100	76	73	85
40	100	100	100	100	75	73	83
50	100	100	100	100	75	73	84
60	100	100	100	100	69	73	82
70	100	100	100	100	69	73	78
80	100	100	100	100	68	72	76
90	100	100	100	100	67	73	74
100	100	100	100	100	67	73	70
200	100	100	100	100	32	72	54
500	99	100	100	100	12	73	48



(**a**)



(**b**)

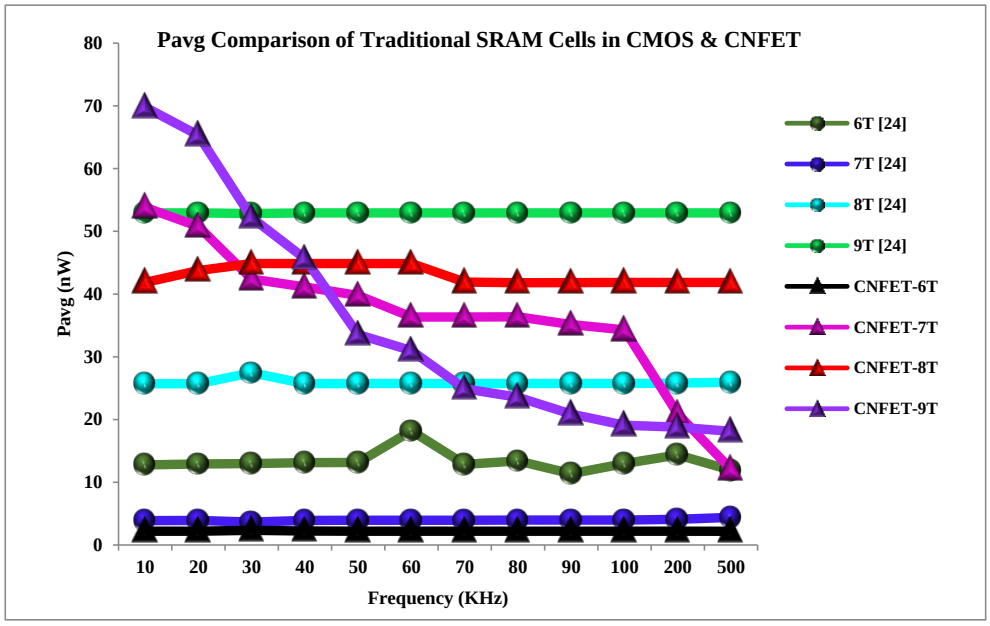
Figure 12. (**a**) Iavg Comparison of Traditional SRAM Cells in CMOS and CNFET. (**b**) Iavg Comparison of Proposed MT-SRAM Cells in CMOS and CNFET.

Table 6. Iavg Improvement (%)–Proposed MT- CNFET 6T SRAM Cell vs. Other MT- SRAM Cells.

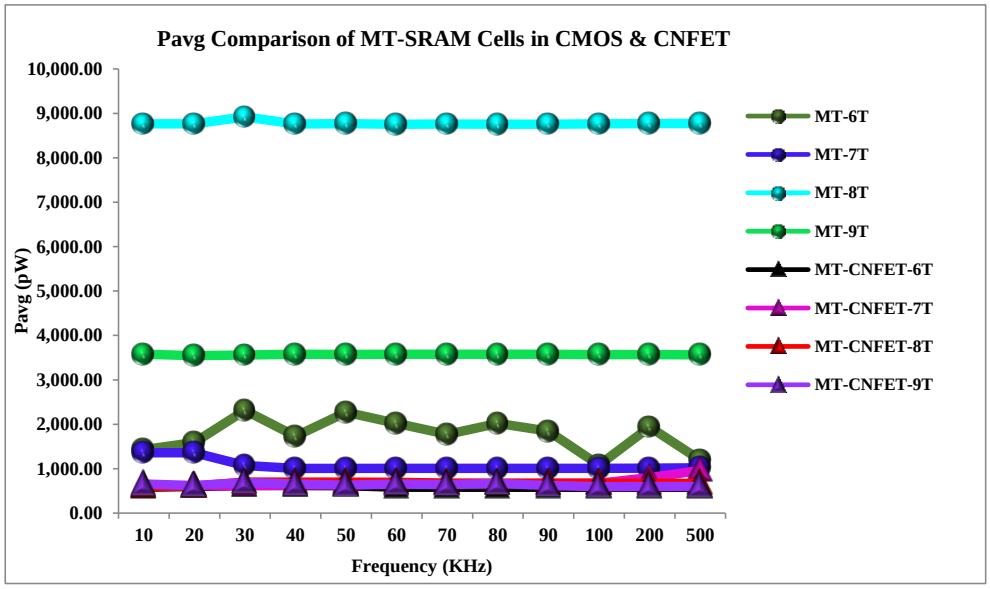
Frequency (KHz)	MT-6T	MT-7T	MT-8T	MT-9T	MT-CNFET-7T	MT-CNFET-8T	MT-CNFET-9T
10	21	97	98	98	92	6	75
20	30	97	98	98	95	5	72
30	49	98	97	98	96	2	70
40	33	98	97	98	98	4	67
50	52	98	98	98	98	5	64
60	45	98	98	98	98	4	58
70	38	98	98	98	98	1	58
80	45	98	98	98	98	1	58
90	41	98	98	98	98	1	57
100	1	98	98	98	98	1	57
200	43	98	98	98	98	0.03	56
500	5	98	98	98	98	5	49

4.3. Comparison of P_{avg}

The Figure 13a,b show the average power comparison of the existing and proposed MT-SRAM cells. Normally, the SRAM cells require less amount of power because it needs small steady state current. Here, the number of transistors is lower for 6T SRAM cell compared with 7T, 8T, and 9T cells. Hence, we have to justify the CNFET 6T SRAM cell consumes less amount of power compared with others. As a result of this comparison, we found that the existing SRAM cells consume much more power when compared with the proposed SRAM cells (particularly CNFET 6T and MT-CNFET 6T), and the following Tables 7 and 8 show the improvement percentage.



(**a**)



(**b**)

Figure 13. (**a**) Pavg Comparison of Traditional SRAM Cells in CMOS and CNFET. (**b**) Pavg Comparison of Proposed MT-SRAM Cells in CMOS and CNFET.

Table 7. Pavg Comparison (%)–CNFET 6T SRAM Cell vs. Other SRAM Cells.

Frequency (KHz)	CMOS-6T [24]	CMOS-7T [24]	CMOS-8T [24]	CMOS-9T [24]	CNFET-7T	CNFET-8T	CNFET-9T
10	83	44	91	96	96	95	97
20	83	44	91	96	96	95	97
30	82	36	91	96	94	95	96
40	83	43	91	96	95	95	95
50	83	44	91	96	94	95	93
60	88	44	91	96	94	95	93
70	83	45	91	96	94	95	91
80	84	45	91	96	94	95	91
90	81	45	91	96	94	95	90
100	83	45	92	96	94	95	89
200	85	46	92	96	90	95	88
500	82	50	92	96	82	95	88

Table 8. Pavg Improvement (%)–Proposed MT- CNFET 6T SRAM Cell vs. Other MT- SRAM Cells.

Frequency (KHz)	MT-6T	MT-7T	MT-8T	MT-9T	MT-CNFET-7T	MT-CNFET-8T	MT-CNFET-9T
10	59	57	93	84	3	3	11
20	62	56	93	83	2	1	3
30	73	42	93	83	0.67	11	10
40	64	38	93	83	2	11	5
50	73	39	93	83	4	12	2
60	71	42	93	84	10	16	11
70	67	42	93	84	12	14	9
80	71	42	93	84	12	14	12
90	68	42	93	84	13	13	6
100	46	42	93	84	13	13	2
200	70	42	93	84	27	13.34	3
500	51	43	93	84	39	13	3

4.4. Comparison of E_{avg}

The Figure 14a,b show the average energy comparison of existing and proposed MT-SRAM cells. If the power consumption of the proposed MT-SRAM cells reduces, it will automatically reflect in the reduction of the energy. As a result of this comparison, we found that the existing SRAM cell consumes much higher energy when compared with the proposed SRAM cells (particularly the CNFET 6T-MT-CNFET 6T), and the following Tables 9 and 10 show the improvement percentage.

4.5. Comparison of Delay

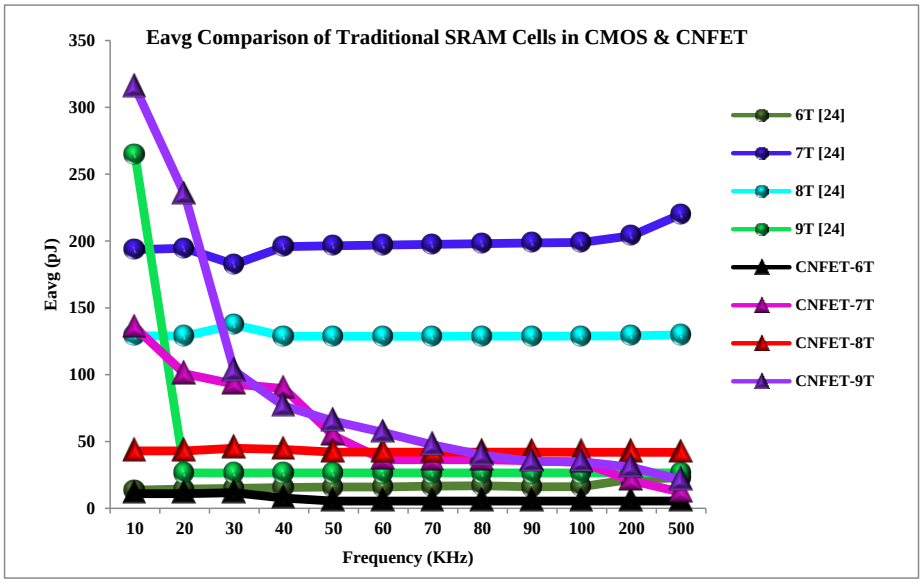
The Figure 15a,b show the average delay comparison of the existing and proposed MT-SRAM cells. Generally, the delay parameter is used for measuring the amount of time required for performing the transition of input bits to the output. The delay is one of the important parameters to justify the high-speed read/write operation of the SRAM cells. In CNFET-Multi-threshold logic, it helps provide very frequent transitions among the input and output bits. As a result of this comparison, we found that the existing

CMOS-based SRAM cells consume much more energy when compared with the proposed SRAM cells (particularly CNFET 6T), and the following Tables 11 and 12 has shown the improvement percentage.

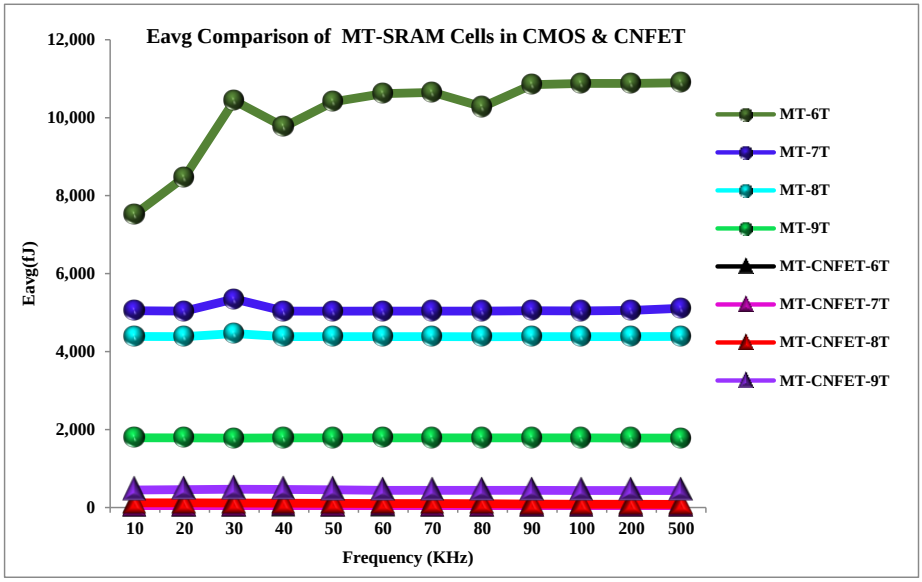
4.6. Justification of 32 nm CNFET Technology

Here, we used standard 32 nm CNFET technology for implementing our proposed MT-SRAM cells. From the experimental results, the 32 nm MT-CNFET SRAM cells work better than CMOS devices. In additionally, we can state that performance effect of the CNFET devices in less than 32 nm and greater than 32 nm channel length (L_{ch}).

By considering the L_{ch} < 32 nm, the complexity of the proposed design increases as well as its tendency to produce inaccurate results. While considering L_{ch} > 32 nm, inaccurate results are produced due to the Schottky barrier effect. That's why, the proposed design mainly focused on the standard 32 nm CNFET technology.



(**a**)



(**b**)

Figure 14. (**a**) Eavg Comparison of Traditional SRAM Cells in CMOS and CNFET. (**b**) Eavg Comparison of Proposed MT-SRAM Cells in CMOS and CNFET.

Table 9. Eavg Improvement (%)–CNFET 6T SRAM Cell vs. Other SRAM Cells.

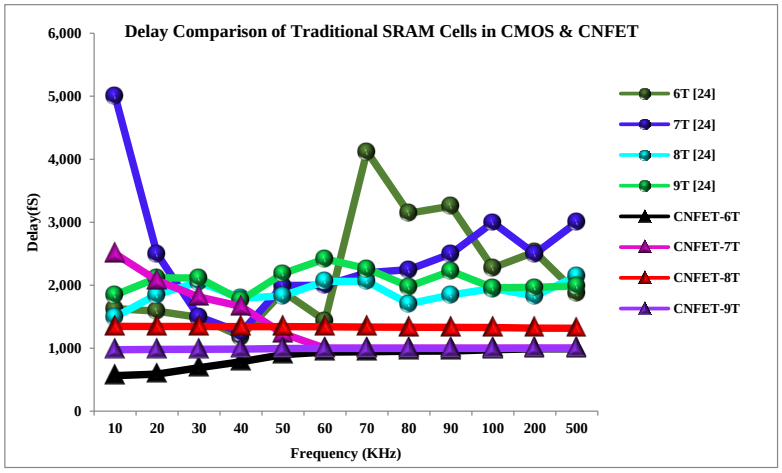
Frequency (KHz)	CMOS-6T [24]	CMOS-7T [24]	CMOS-8T [24]	CMOS-9T [24]	CNFET-7T	CNFET-8T	CNFET-9T
10	19	94	91	96	92	74	97
20	24	94	91	59	89	74	95
30	22	94	91	56	87	74	89
40	51	96	94	71	91	83	90
50	66	97	96	79	90	87	92
60	66	97	96	79	85	87	90
70	67	97	96	79	85	87	88
80	68	97	96	79	85	87	86
90	66	97	96	79	85	87	84
100	66	97	96	79	84	87	84
200	75	97	96	79	74	87	82
500	76	98	96	79	54	87	74

Table 10. Eavg Improvement (%)–Proposed MT- CNFET 6T SRAM Cell vs. Other MT- SRAM Cells.

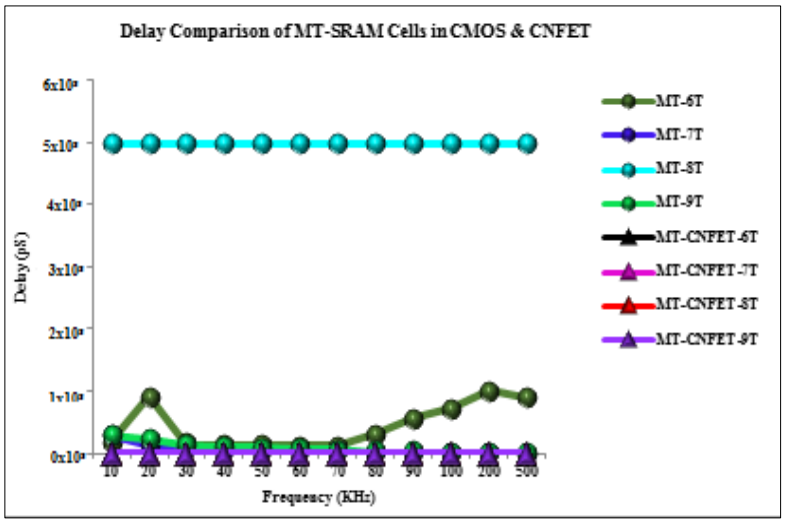
Frequency (KHz)	MT-6T	MT-7T	MT-8T	MT-9T	MT-CNFET-7T	MT-CNFET-8T	MT-CNFET-9T
10	99	99	99	98	13	66	91
20	100	99	99	98	15	66	91
30	100	99	99	98	18.66	66	92
40	100	99	99	98	25	68	92
50	100	99	99	98	29	68	92
60	100	99	99	98	37	70	93
70	100	99	99	98	34	70	93
80	100	99	99	98	17	69	93
90	100	99	99	98	26	67	93
100	100	99	99	98	10	64	93
200	100	99	99	98	2	63.82	93
500	100	99	99	98	6	63	93

4.7. 32 nm CNFET vs. 10 nm CMOS Process

From the above discussion in Section 4.6, we proved that 32 nm standard CNFET device performed well for MT-SRAM cells when compared with the other CNFET devices (i.e., L > 32 nm and L < 32 nm). Once again, a validation proof can be completed for CNFET devices versus 10 nm CMOS devices. The model files for N-type and P-type 10 nm CMOS can be obtained from [29,30] respectively. The following Figure 16a–e graphically compares the MT-SRAM cells in both the devices on the basis of measured parameters and Table 13 shows the improvement percentage of 32 nm CNFET device.



(**a**)



(**b**)

Figure 15. (**a**) Delay Comparison of Traditional SRAM Cells in CMOS and CNFET. (**b**) Delay Comparison of Proposed MT-SRAM Cells in CMOS and CNFET.

Table 11. Delay Improvement (%)–CNFET 6T SRAM Cell vs. Other SRAM Cells.

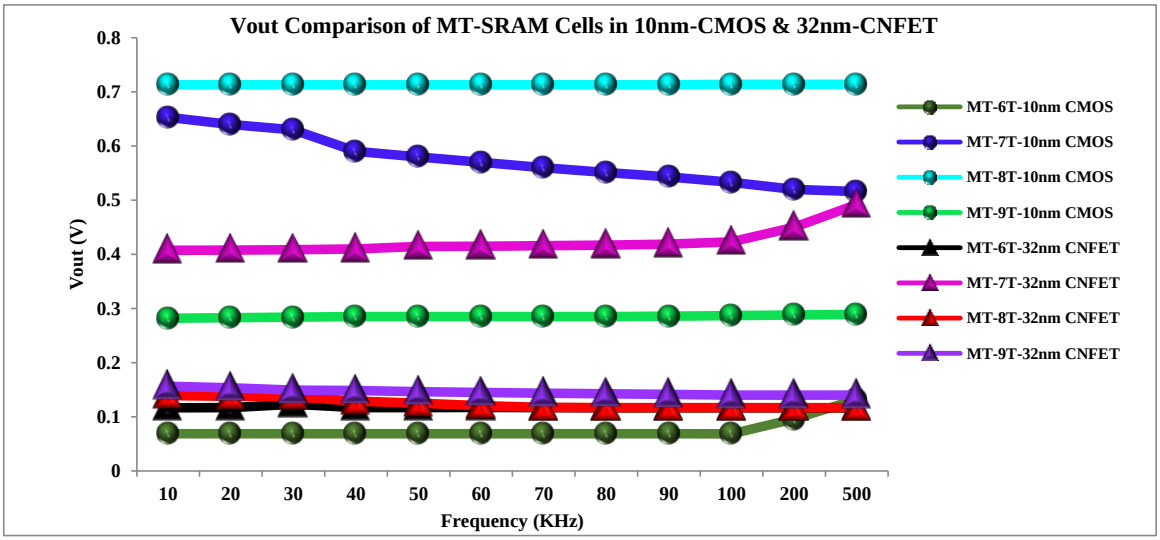
Frequency (KHz)	CMOS-6T [24]	CMOS-7T [24]	CMOS-8T [24]	CMOS-9T [24]	CNFET-7T	CNFET-8T	CNFET-9T
10	65	89	62	69	77	58	42
20	63	77	68	72	72	56	40
30	54	54	66	67	62	49	30
40	34	37	56	56	53	42	20
50	53	55	51	59	27	33	10
60	35	53	54	61	6	30	6
70	77	57	54	58	6	29	5
80	70	58	44	52	5	28	4
90	71	62	48	57	5	28	4
100	57	67	50	50	3	27	2
200	61	60	46	50	1	25	1
500	47	67	54	50	1	25	1

Table 12. Delay Improvement (%)–Proposed MT- CNFET 6T SRAM Cell vs. Other MT-SRAM Cells.

Frequency (KHz)	MT-6T	MT-7T	MT-8T	MT-9T	MT-CNFET-7T	MT-CNFET-8T	MT-CNFET-9T
10	100	100	100	100	73	36	74
20	100	100	100	100	73	34	74
30	100	100	100	100	72.56	32	73
40	100	100	100	100	72	10	72
50	100	100	100	100	70	20	68
60	100	100	100	100	70	3	67
70	100	100	100	100	70	20	63
80	100	100	100	100	71	20	58
90	100	100	100	100	72	3	51
100	100	100	100	100	73	11	35
200	100	100	100	100	72	18.61	16
500	100	100	100	100	72	30	13

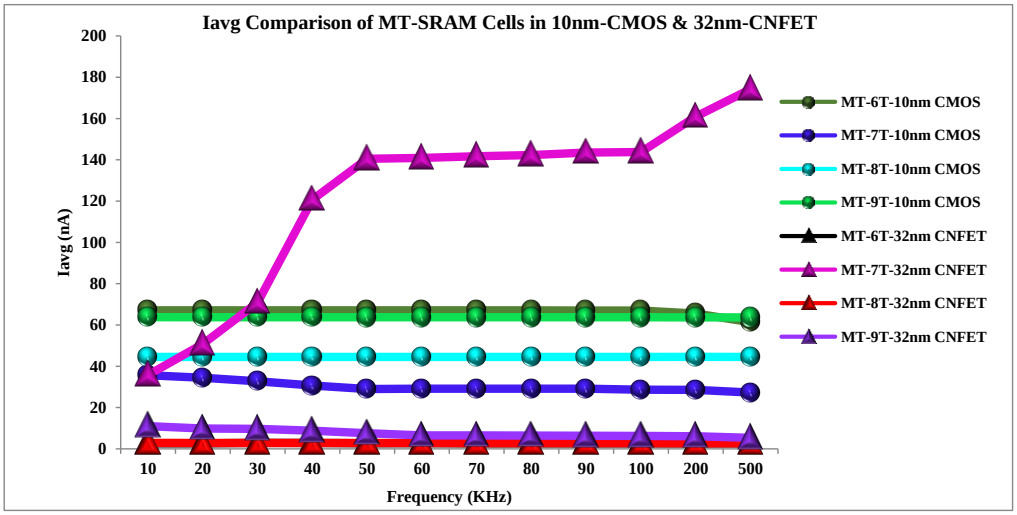
Table 13. Improvement of 32 nm CNFET MT-SRAM Cells over 10 nm CMOS MT-SRAM Cells.

Parameters Taken	10 nm CMOS MT-6T vs. 32 nm CNFT MT-6T	10 nm CMOS MT-7T vs. 32 nm CNFT MT-7T	10 nm CMOS MT-8T vs. 32 nm CNFT MT-8T	10 nm CMOS MT-9T vs. 32 nm CNFT MT-9T
Vout Improvement (%)	60.29	36.27	82.58	48.97
Iavg Improvement (%)	95.86	67.08	93.73	88.18
Pavg Improvement (%)	20.07	97.70	81.65	99.86
Eavg Improvement (%)	4.23	98.16	97.98	87.76
Delay Improvement (%)	96.11	92.27	99.57	93.98



(**a**)

Figure 16. *Cont.*



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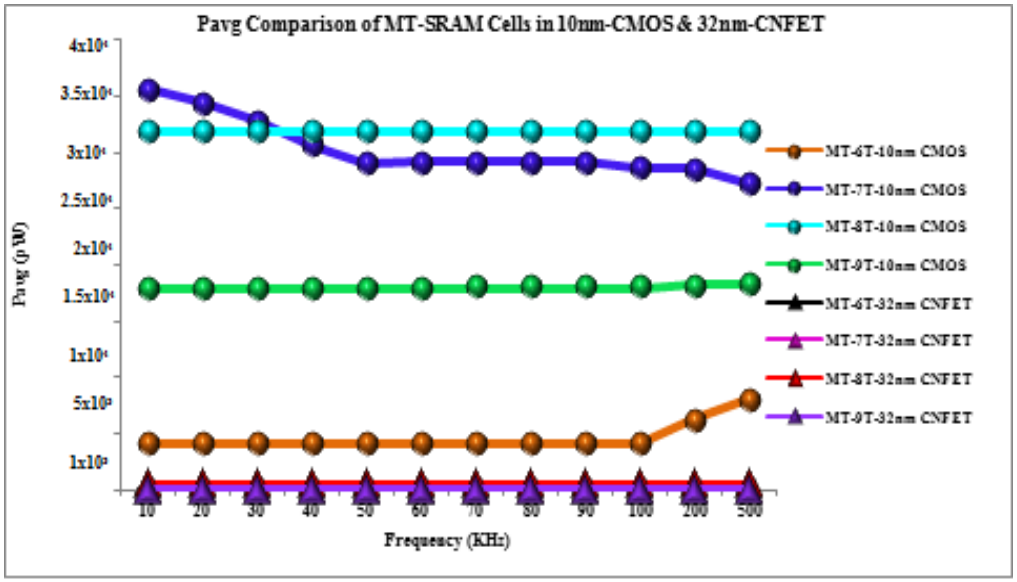
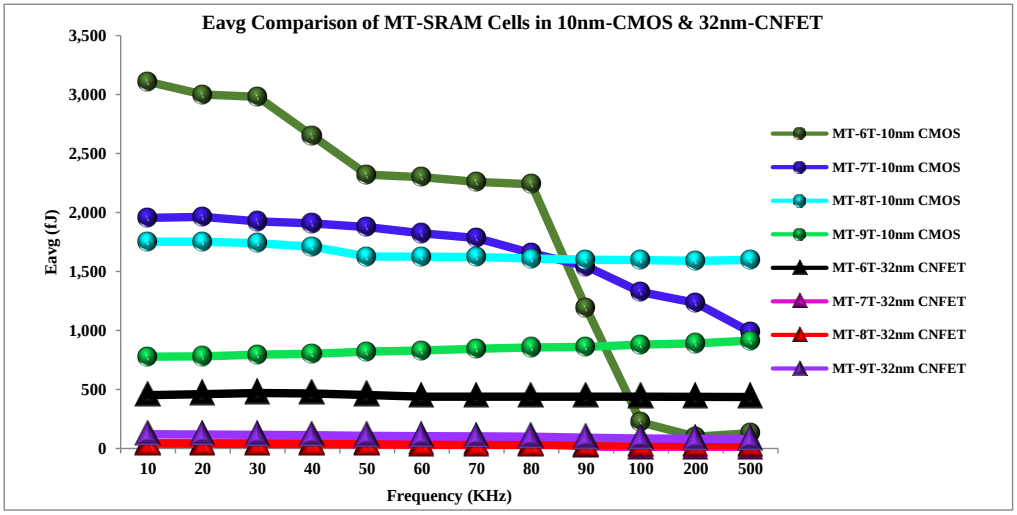
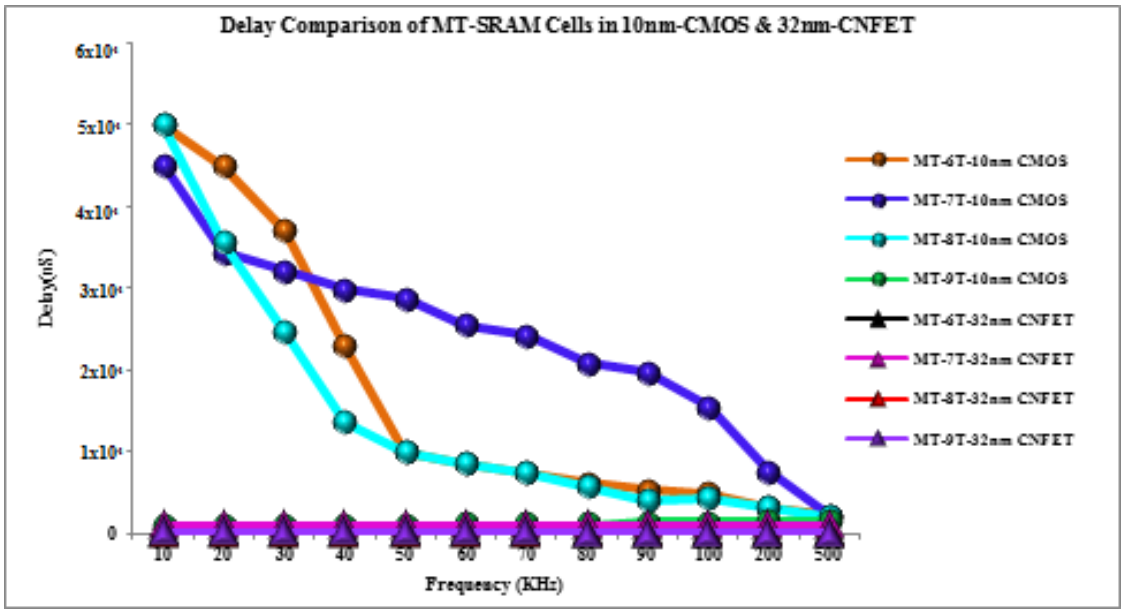


(**c**)



(**d**)

Figure 16. *Cont.*



(**e**)

Figure 16. (**a**) Vout Comparison of Proposed MT-SRAM Cells in 10 nm-CMOS and 32 nm-CNFET. (**b**) Iavg Comparison of Proposed MT-SRAM Cells in 10 nm-CMOS and 32 nm-CNFET. (**c**) Pavg Comparison of Proposed MT-SRAM Cells in 10 nm-CMOS and 32 nm-CNFET. (**d**) Eavg Comparison of Proposed MT-SRAM Cells in 10 nm-CMOS and 32 nm-CNFET. (**e**) Delay Comparison of Proposed MT-SRAM Cells in 10 nm-CMOS and 32 nm-CNFET.

5. Conclusions

The presented paper clearly dealt the lot of designing methods for SRAM design for low power applications. The paper contains both CMOS and CNFET technology-based practical implementations. As a result of this implementation, the CMOS technology does not perform properly when considering the 32 nm channel length. At 32 nm channel length, it produced undesired effects like short channel effect and mobility degradation, etc., This limitation is overcome by CNFET-based SRAM cell design approaches. Hence, the paper proves that CNFET-based Multi-Threshold SRAM design performs better than traditional SRAM cells in CMOS techniques. The proposed design will be further developed by infusing the power reduction techniques.

Author Contributions: Data curation, Methodology, Software, Formal analysis, Conceptualization, Investigation, Writing—original draft, S.K.; Supervision, Validation, Methodology, Resources, Formal analysis, Conceptualization, Investigation, Writing—original draft, C.K.; Visualization, Validation, Resources, Investigation, Writing—review & editing, H.H.F.; Visualization, Validation, Resources, Project administration, Investigation, Writing—review & editing, E.R. All authors have read and agreed to the published version of the manuscript.

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Data Availability Statement: No data except that in the paper.

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Conflicts of Interest: The authors declare no conflict of interest.

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