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An SVPWM Algorithm for a Novel Multilevel Rectifier with DC-Side Capacitor Voltage Balance

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Abstract: The recently proposed novel unidirectional multilevel rectifier, a three single-phase star-connected multilevel rectifier, has the characteristic of having a large number of DC-side capacitors and a complex capacitor voltage balancing control structure under conventional carrier-based phase-shift sine wave pulse-width modulation (SPWM). Hence, a space vector pulse-width modulation (SVPWM) algorithm for the novel multilevel rectifier is proposed in this paper, which can quickly balance the capacitor voltage without an additional voltage balancing control structure. Firstly, it divides the space vectors of the rectifier, then it determines the two basis voltage vectors that synthesize the output reference voltage. After that, based on the analysis of the relationship between switching states and the charge–discharge of capacitors, the final action sequences of redundant vectors are determined according to the principle of keeping the capacitor charge–discharge time consistent. Thus, the capacitor voltages can be automatically balanced without an additional voltage balancing control structure. Finally, simulation and experimental results validated the feasibility and effectiveness of the proposed SVPWM algorithm. The results also show improvements in current quality, capacitor voltage balance and the fluctuation of the neutral point voltage on the DC-link, allowing for further reduction in the overall volume and cost of the rectifier.

Keywords: single-phase; multilevel; space vector pulse-width modulation (SVPWM); capacitor voltage balance

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1. Introduction

Multilevel rectifiers have been widely used and studied because of their advantages in harmonic characteristics, device stress, filter volume, power density and electromagnetic interference [1–3]. The existing multilevel rectifiers are mainly divided into three types: diode-clamped (neutral point clamped, NPC) rectifier [4], flying capacitor (FC) rectifier [5,6] and cascaded H-bridge (CHB) rectifier [7]. These rectifiers are bidirectional power transmission. However, in view of the numerous industrial applications, bidirectional power transmission is not necessary, such as power supplies for aircraft, naval propulsion systems, pumps and blowers, etc. [8–12]. Especially in the medium-voltage (MV) applications, the unidirectional rectifiers have better economic benefits due to the use of fewer active switches, and the lower switching loss of the system, so the system has higher safety and reliability and has attracted many research scientists and engineers to conduct comprehensive research on it.

Ref. [13] discussed the derivation of some of the unidirectional rectifiers from the traditional converters, such as the NPC, FC and CHB converters. The topology in Ref. [14] has the same circuit structure as the 3L-NPC and in which some of active switches are replaced by diodes. Further, the Vienna rectifier in Ref. [15] was proposed which is modified from [14]. Moreover, several multilevel unidirectional rectifiers have been proposed in Refs. [16–19]. Although these rectifiers have lower cost and volume over traditional bidirectional converters, there are still some shortcomings, such as high device stress and

uneven switching loss. Especially in MV applications, its front stage still needs a bulky and expensive line-frequency transformer to achieve voltage step-down, line harmonic-current mitigation and galvanic isolation. So that canceling the line-frequency transformer has become a hotspot in the research of unidirectional rectifiers.

Ref. [20] proposed a 6.6 kV transformer-less motor drive using a five-level clamped pulse-width modulation (PWM) inverter for energy savings of pumps and blowers. In which the diode rectifier and the voltage balancing can be defined as a five-level rectifier. Although the transformer can be canceled in MV scenarios, it is replaced by two bulky inductors and it needs an additional active filter to mitigate the harmonics. Hence, the total volume and cost are still large. Ref. [21] modified the circuit structure in Ref. [20], where the two inductors were replaced by a single coupled inductor. The overall volume is still large. Ref. [22] proposed a unidirectional five-level rectifier which can be used in MV scenarios without transformer at the grid side. Compared with the traditional unidirectional five-level rectifier, there are four switches per phase and it has lower cost and device stress and higher efficiency. It adopts the conventional carrier-based phase-shift PWM method and additional control structure to balance the capacitor voltage on the DC side, so the voltage balancing accuracy and switching loss need to be further improved. Ref. [23] proposed a novel unidirectional three single-phase star-connected five-level rectifier. It can also cancel the transformer to reduce the cost and volume of the system. Compared with the topology in Ref. [22], they both have four switches and eight diodes per phase and can be extended to higher levels, but it can generate more levels on the input side so that the harmonic characteristics and filter volume can be further improved. Similarly, it adopts the conventional carrier-based PWM method and the capacitor voltage balance needs an additional control structure. In general, the rectifiers in Refs. [22,23] have great advantages in device stress, cost, filter volume and power efficiency; they are still in the research and development stage. The conventional carrier-based PWM and additional voltage balance control structure will increase the switching loss of the system and the difficulty of engineering implementation, thus limiting its promotion and application in industrial scenarios.

Considering the complexity and variability of industrial scenarios, it is necessary to further improve the dynamic performance and voltage balancing accuracy. Space vector pulse-width modulation (SVPWM) is widely used in the modulation method of converters because of its easy digital implementation, lower switching loss and harmonic currents, etc. [24–26]. For the multilevel rectifier proposed in Refs. [22,23], this paper takes the unidirectional single-phase five-level as an example to present an SVPWM algorithm with the function of automatically equalizing the capacitor voltage so as to simplify the voltage balance control structure and improve voltage balancing accuracy and dynamic performance of the rectifier. This paper presents a variety of applicable SVPWM sequences, gives a most recommended sequence by comparing the switching loss and midpoint voltage fluctuation range of the system in simulation and presents experimental results. The proposed SVPWM algorithm in this paper is also applicable and can be easily extended to the three-phase or higher level rectifiers in Refs. [22,23].

The rest of this article is organized as follows: The topology and operating principle of the single-phase five-level rectifier are introduced in Section 2. The design of the SVPWM algorithm and different sequences are presented in Section 3. In Section 4, the simulation and experimental results are given to validate the proposed SVPWM algorithm. The main conclusion is drawn in Section 5.

2. Topology and Principle of the Single-Phase Five-Level Rectifier

Figure 1 shows the topology of a single-phase five-level rectifier, which consists of a diode bridge rectifier and a five-level DC/DC unit. AC grid voltage is u_s. The filter inductance at the AC side is L, which has the function of boosting voltage. The AC inductive current is i_L. The diode bridge rectifier consists of four common diodes D_1, D_2, D_3 and D_4. PWM driving signals of switches T_1, T_2, T_3 and T_4 are represented by S_1, S_2, S_3

and S_4, respectively. When $S_{i\ (i=1,2,3,4)} = 1$, the corresponding power switch is on. When $S_{i\ (i=1,2,3,4)} = 0$, the corresponding power switch is off. D_5, D_6, D_7 and D_8 are freewheeling diodes with voltage-clamped functions. The voltages of C_1, C_2, C_3 and C_4 are represented by u_{c1}, u_{c2}, u_{c3} and u_{c4}, respectively. The DC load voltage is u_{dc}.

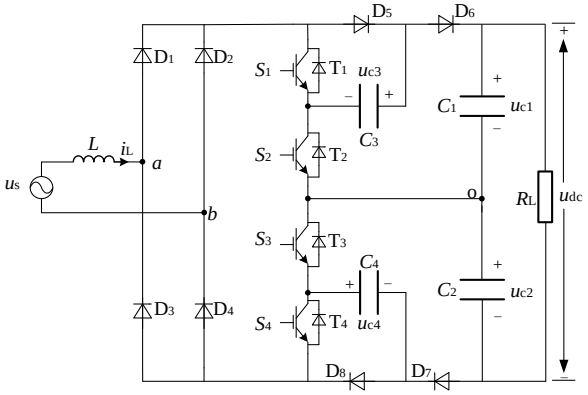

Figure 1. Topology of single-phase five-level rectifier.

Taking a power frequency cycle as an example. The principle of the single-phase five-level rectifier is introduced as follows.

Taking the point O on the DC-link as the reference point, the output level u_{ao} from the point a on the AC-side port to the point O is analyzed.

If $i_L > 0$:

When both switches T_1 and T_2 are off, $u_{ao} = u_{dc}/2$.

When only one of the switches T_1 and T_2 is on, $u_{ao} = u_{dc}/4$.

When both switches T_1 and T_2 are on, $u_{ao} = 0$.

If $i_L < 0$:

When both switches T_3 and T_4 are off, $u_{ao} = -u_{dc}/2$.

When only one of the switches T_3 and T_4 is on, $u_{ao} = -u_{dc}/4$.

When both switches T_3 and T_4 are on, $u_{ao} = 0$.

Accordingly, the voltage u_{ao} outputs five levels, $-u_{dc}/4$, $-u_{dc}/2$, 0, $u_{dc}/4$, $u_{dc}/2$. Therefore, the port voltage u_{ab} can output nine levels, $-u_{dc}$, $-3u_{dc}/4$, $-u_{dc}/2$, $-u_{dc}/4$, 0, $u_{dc}/4$, $u_{dc}/2$, $3u_{dc}/4$, u_{dc}. Table 1 shows the relationship between output levels and switching states in detail.

Table 1. The relationship between output level and switching states.

$(S_1S_2S_3S_4)$	u_{ao} $(i_L > 0)$	u_{ao} $(i_L < 0)$	u_{ab} $(i_L > 0)$	u_{ab} $(i_L < 0)$
0000	$u_{dc}/2$	$-u_{dc}/2$	u_{dc}	$-u_{dc}$
1000	$u_{dc}/4$	$-u_{dc}/2$	$3u_{dc}/4$	$-3u_{dc}/4$
0100	$u_{dc}/4$	$-u_{dc}/2$	$3u_{dc}/4$	$-3u_{dc}/4$
0010	$u_{dc}/2$	$-u_{dc}/4$	$3u_{dc}/4$	$-3u_{dc}/4$
0001	$u_{dc}/2$	-$u_{dc}/4$	$3u_{dc}/4$	$-3u_{dc}/4$
1100	0	$-u_{dc}/2$	$u_{dc}/2$	$-u_{dc}/2$
0110	$u_{dc}/4$	$-u_{dc}/4$	$u_{dc}/2$	$-u_{dc}/2$
0011	$u_{dc}/2$	0	$u_{dc}/2$	$-u_{dc}/2$
1010	$u_{dc}/4$	$-u_{dc}/4$	$u_{dc}/2$	$-u_{dc}/2$
0101	$u_{dc}/4$	$-u_{dc}/4$	$u_{dc}/2$	$-u_{dc}/2$
1001	$u_{dc}/4$	$-u_{dc}/4$	$u_{dc}/2$	$-u_{dc}/2$
1110	0	$-u_{dc}/4$	$u_{dc}/4$	$-u_{dc}/4$
1011	$u_{dc}/4$	0	$u_{dc}/4$	$-u_{dc}/4$
0111	$u_{dc}/4$	0	$u_{dc}/4$	$-u_{dc}/4$
1101	0	$-u_{dc}/4$	$u_{dc}/4$	$-u_{dc}/4$
1111	0	0	0	0

Since the front stage of the topology is diode uncontrolled rectification, the current flow path at the DC side has nothing to do with the positive or negative half cycle of the AC voltage, but only with the switching on or off at the DC side. Taking the positive half cycle of the AC voltage as an example, the current flow paths under different switching states are shown in Figure 2.

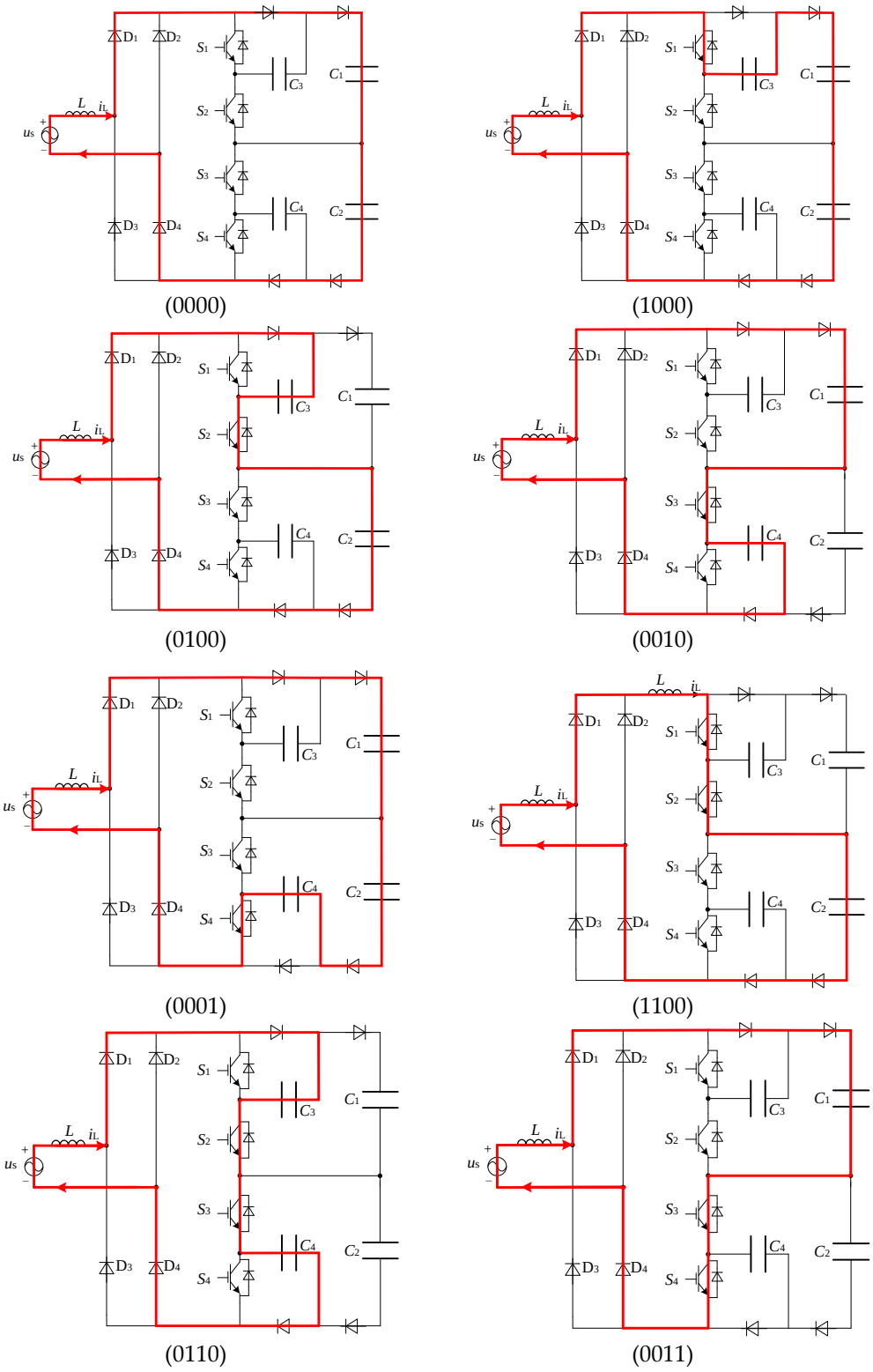

Figure 2. *Cont.*

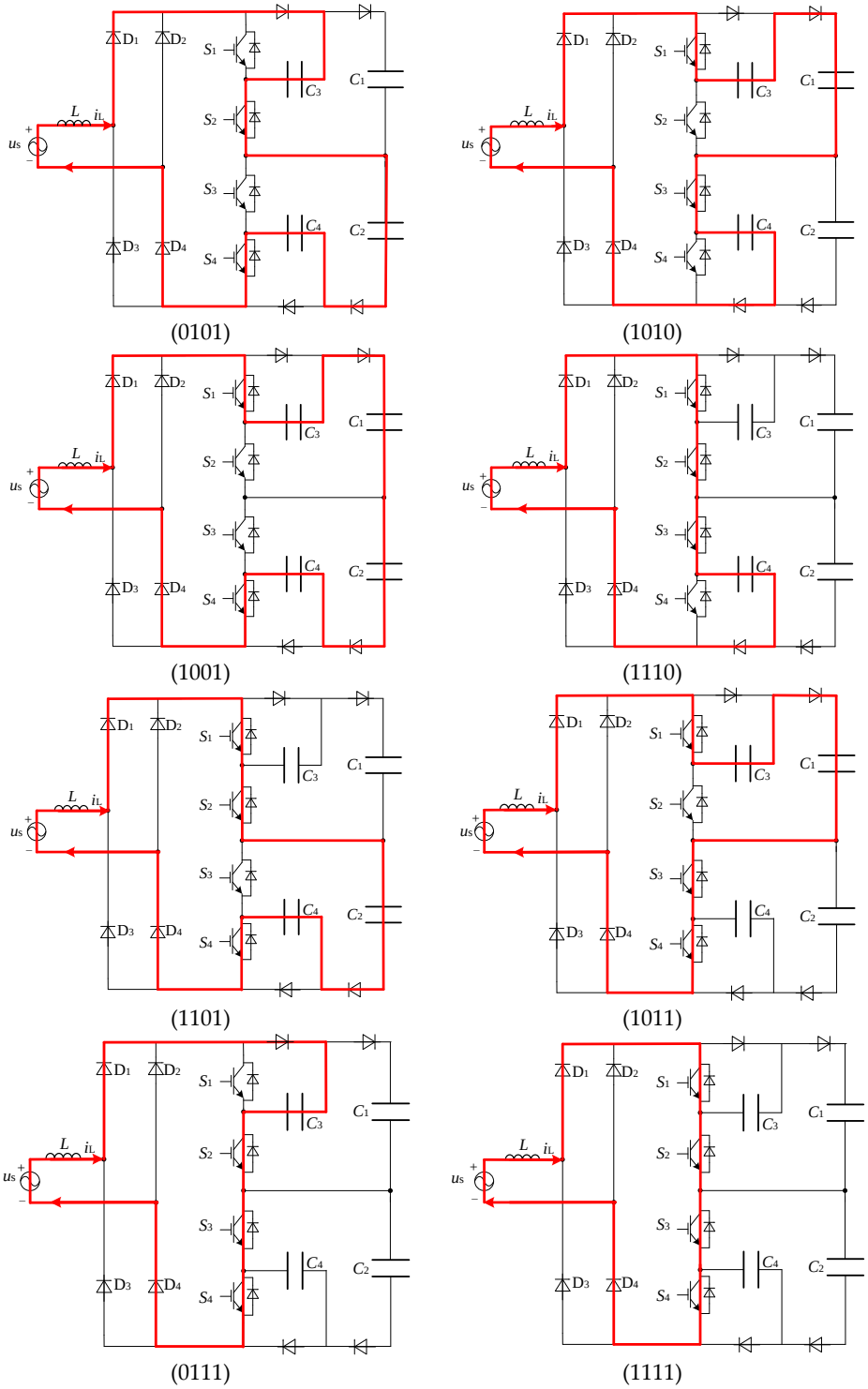

Figure 2. Modal analysis of single-phase five-level rectifier in the positive half cycle of voltage.

3. The Proposed SVPWM Algorithm for Single-Phase Five-Level Rectifier

3.1. Sector Division and Selection of Basis Synthetic Voltage Vector

According to the nine levels of output voltage u_{ab}, input current direction at the AC side and 16 switching states, the space vector diagram of the single-phase five-level rectifier is divided into 8 sectors, I, II, III, IV, V, VI, VII, VIII. Figure 3 shows the space vector diagram of the rectifier. The boundary of sector I corresponds to voltage vectors $\boldsymbol{V}_4$ and $\boldsymbol{V}_3$. The case is similar for the rest of sector boundaries in Figure 3 and it will not be repeated here.

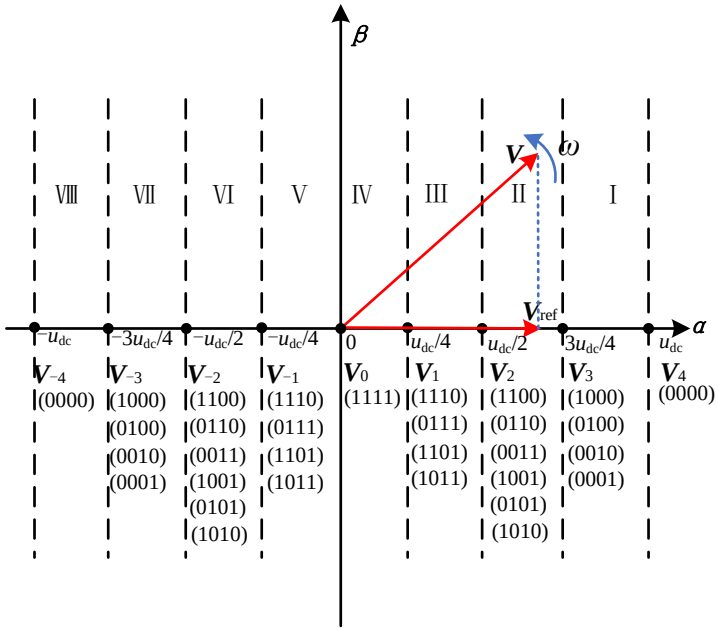

Figure 3. Space vector diagram for the single-phase five-level rectifier.

As shown in Figure 3, $\boldsymbol{V}$ is a virtual vector with angular velocity ω rotating counterclockwise. The projection on the α axis of $\boldsymbol{V}$ is the output reference voltage vector $\boldsymbol{V_{ref}}$ of the rectifier. Considering the different input current directions at the AC side, the single-phase five-level rectifier has a total of thirty-one space voltage vectors. Except for the zero vector (1111), each switching state corresponds to two voltage vectors with different directions and the same length.

All voltage vectors are defined according to Figure 3. $\boldsymbol{V}_4$ and $\boldsymbol{V}_{-4}$ (0000) are long vectors. $\boldsymbol{V}_3$ and $\boldsymbol{V}_{-3}$ are medium-long vectors, in which (1000), (0100), (0010) and (0001) are redundant vectors. $\boldsymbol{V}_2$ and $\boldsymbol{V}_{-2}$ are medium vectors, in which (1100), (0110), (0011), (1001), (0101) and (1010) are redundant vectors. $\boldsymbol{V}_1$ and $\boldsymbol{V}_{-1}$ are short vectors, in which (1110), (0111), (1101) and (1011) are redundant vectors. $\boldsymbol{V}_0$ is a zero vector.

Before selecting the basis synthetic voltage vector, the sector to which the reference voltage vector $\boldsymbol{V_{ref}}$ belongs should be judged first. The sector judgment rules and the selection of the basis synthetic voltage vector are as follows:

If $\boldsymbol{V_{ref}} \geq 3u_{dc}/4$, select vectors $\boldsymbol{V}_4$ and $\boldsymbol{V}_3$ for synthesis in sector I.

If $3u_{dc}/4 > \boldsymbol{V_{ref}} \geq u_{dc}/2$, select vectors $\boldsymbol{V}_3$ and $\boldsymbol{V}_2$ for synthesis in sector II.

If $u_{dc}/2 > \boldsymbol{V_{ref}} \geq u_{dc}/4$, select vectors $\boldsymbol{V}_2$ and $\boldsymbol{V}_1$ for synthesis in sector III.

If $u_{dc}/4 > \boldsymbol{V_{ref}} \geq 0$, select vectors $\boldsymbol{V}_1$ and $\boldsymbol{V}_0$ for synthesis in sector IV.

When $\boldsymbol{V_{ref}} < 0$, the sector judgment is similar to the above rules with $\boldsymbol{V_{ref}} \geq 0$ and is easy to understand from Figure 3.

After determining the sector to which $\boldsymbol{V_{ref}}$ belongs and selecting the basis synthetic vector, the existence of the relevant redundant vector makes the selection of the basis vector more flexible. When selecting redundant vectors, the influence of each vector on the charge and discharge of each DC-side capacitor should be considered, so as to better maintain the voltage balance between capacitors. Table 2 shows the relationship between different switching states, namely different voltage vectors, and the charge–discharge of DC-side capacitors.

Table 2. The relationship between switching states and the charge–discharge of DC-side capacitors.

$(S_1S_2S_3S_4)$	C_1	C_2	C_3	C_4
0000	Null	Null	Null	Null
1000	Null	Null	Discharge	Null
0100	Discharge	Charge	Charge	Null
0010	Charge	Discharge	Null	Charge
0001	Null	Null	Null	Discharge
1100	Discharge	Charge	Null	Null
0110	Null	Null	Charge	Charge
0011	Charge	Discharge	Null	Null
1010	Charge	Discharge	Discharge	Charge
0101	Discharge	Charge	Charge	Discharge
1001	Null	Null	Discharge	Discharge
1110	Null	Null	Null	Charge
1011	Charge	Discharge	Discharge	Null
0111	Null	Null	Charge	Null
1101	Discharge	Charge	Null	Discharge
1111	Null	Null	Null	Null

"Null" means neither charging nor discharging.

3.2. Determine the SVPWM Sequence and Vector Action Time

After determining which basis vectors are composed of $\boldsymbol{V_{ref}}$ in each sector, the specific SVPWM sequence is determined based on the principle that the capacitors recover balance as soon as possible.

In sector I, there is no redundant vector for $\boldsymbol{V_4}$, and only the redundant vectors of $\boldsymbol{V_3}$ need to be reasonably configured. According to the relationship between redundant vectors and the charge–discharge of each capacitor in Table 2, select (0000) as the first vector. Considering the minimum switching times per switching cycle, conduct in the order of (0000) → (1000) → (0100) → (0010) → (0001) → (0000).

In sector II, the redundant vectors of $\boldsymbol{V_3}$ and $\boldsymbol{V_2}$ need to be reasonably configured. According to the relationship between redundant vectors and the charge–discharge of each capacitor in Table 2, select (1010) as the first vector. Considering the minimum switching times per switching cycle, conduct in the order of (1010) → (1000) → (0100) → (0010) → (0001) → (0101).

In sector III, the redundant vectors of $\boldsymbol{V_2}$ and $\boldsymbol{V_1}$ need to be reasonably configured. According to the relationship between redundant vectors and the charge–discharge of each capacitor in Table 2, select (1010) as the first vector. Considering the minimum switching times per switching cycle, conduct in the order of (1010) → (1110) → (1101) → (1011) → (0111) → (0101).

In sector IV, there is no redundant vector for $\boldsymbol{V_0}$, and only the redundant vectors of $\boldsymbol{V_1}$ need to be reasonably configured. According to the relationship between redundant vectors and the charge–discharge of each capacitor in Table 2, select (1111) as the first vector. Considering the minimum switching times per switching cycle, conduct in the order of (1111) → (1110) → (1101) → (1011) → (0111) → (1111).

In sector V, the switching states of the redundant vectors of $\boldsymbol{V_1}$ and $\boldsymbol{V_{-1}}$ are the same; that is, the charge–discharge impact on the DC-side capacitors is the same. For this reason, the same SVPWM sequence as sector IV is selected to synthesize $\boldsymbol{V_{ref}}$.

In sector VI, the switching states of the redundant vectors of $\boldsymbol{V_1}$ and $\boldsymbol{V_{-1}}$, $\boldsymbol{V_2}$ and $\boldsymbol{V_{-2}}$ are the same; that is, the charge–discharge impact on the DC-side capacitors is the same. The same SVPWM sequence as sector III is selected to synthesize $\boldsymbol{V_{ref}}$.

In sector VII, the switching states of the redundant vectors of V_3 and V_{-3}, V_2 and V_{-2} are the same; that is, the charge–discharge impact on the DC-side capacitors is the same. The same SVPWM sequence as sector II is selected to synthesize V_{ref}.

In sector VIII, the switching states of the redundant vectors of V_4 and V_{-4}, V_3 and V_{-3} are the same; that is, the charge–discharge impact on the DC-side capacitors is the same. The same SVPWM sequence as sector I is selected to synthesize V_{ref}.

SVPWM-1:
Sector I: (0000) → (1000) → (0100) → (0000) → (0001) → (0010).
Sector II: (1010) → (1000) → (0100) → (0101) → (0001) → (0010).
Sector III: (1010) → (1110) → (1101) → (0101) → (0111) → (1011).
Sector IV: (1111) → (1110) → (1101) → (1111) → (0111) → (1011).
Sector V: (1111) → (1110) → (1101) → (1111) → (0111) → (1011).
Sector VI: (1010) → (1110) → (1101) → (0101) → (0111) → (1011).
Sector VII: (1010) → (1000) → (0100) → (0101) → (0001) → (0010).
Sector VIII: (0000) → (1000) → (0100) → (0000) → (0001) → (0010).
SVPWM-2:
Sector I: (0000) → (1000) → (0100) → (0000) → (0001) → (0010).
Sector II: (1100) → (1000) → (0100) → (0011) → (0001) → (0010).
Sector III: (1100) → (1110) → (1101) → (0011) → (0111) → (1011).
Sector IV: (1111) → (1110) → (1101) → (1111) → (0111) → (1011).
Sector V: (1111) → (1110) → (1101) → (1111) → (0111) → (1011).
Sector VI: (1100) → (1110) → (1101) → (0011) → (0111) → (1011).
Sector VII: (1100) → (1000) → (0100) → (0011) → (0001) → (0010).
Sector VIII: (0000) → (1000) → (0100) → (0000) → (0001) → (0010).
SVPWM-3:
Sector I: (0000) → (1000) → (0100) → (0000) → (0001) → (0010).
Sector II: (1001) → (1000) → (0100) → (0110) → (0001) → (0010).
Sector III: (1001) → (1110) → (1101) → (0110) → (0111) → (1011).
Sector IV: (1111) → (1110) → (1101) → (1111) → (0111) → (1011).
Sector V: (1111) → (1110) → (1101) → (1111) → (0111) → (1011).
Sector VI: (1001) → (1110) → (1101) → (0110) → (0111) → (1011).
Sector VII: (1001) → (1000) → (0100) → (0110) → (0001) → (0010).
Sector VIII: (0000) → (1000) → (0100) → (0000) → (0001) → (0010).
SVPWM-4 (hybrid):
Sector I: (0000) → (1000) → (0100) → (0000) → (0001) → (0010).
Sector II: (1001) → (1000) → (0100) → (0110) → (0001) → (0010).
Sector III: (1001) → (1110) → (1101) → (0110) → (0111) → (1011).
Sector IV: (1111) → (1110) → (1101) → (1111) → (0111) → (1011).
Sector V: (1111) → (1110) → (1101) → (1111) → (0111) → (1011).
Sector VI: (1010) → (1110) → (1101) → (0101) → (0111) → (1011).
Sector VII: (1010) → (1000) → (0100) → (0101) → (0001) → (0010).
Sector VIII: (0000) → (1000) → (0100) → (0000) → (0001) → (0010).

For sequence SVPWM-1, Figure 4 shows the conduction sequence and output of the four switches in each sector, respectively:

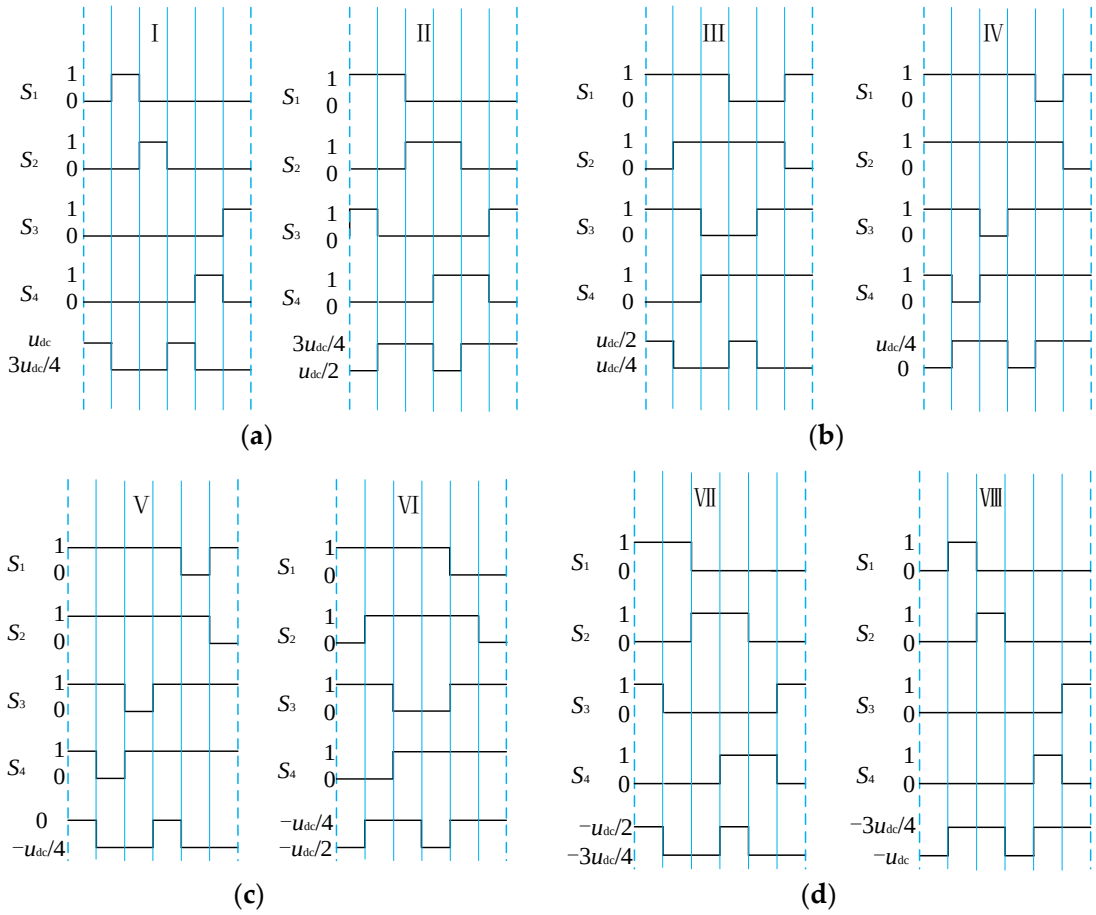

Figure 4. Switching states and output level corresponding to the SVPWM-1. (**a**) Sector I, II. (**b**) Sector III, IV. (**c**) Sector V, VI. (**d**) Sector VII, VIII.

For other diagrams of SVPWM sequences given in this paper, the analysis method is similar to the above, and will not be shown here one by one.

As for the action time of each basis synthetic vector, it is calculated according to the volt-second principle, and the relevant formulas are shown as follows:

$$\begin{cases} \boldsymbol{V}_{\mathrm{x}} T_{\mathrm{x}} + \boldsymbol{V}_{\mathrm{y}} T_{\mathrm{y}} = \boldsymbol{V}_{\mathrm{ref}} T_{\mathrm{s}} \\ T_{\mathrm{x}} + T_{\mathrm{y}} = T_{\mathrm{s}} \end{cases} \tag{1}$$

$$\begin{cases} T_{\mathrm{x}} = \dfrac{|V_{\mathrm{ref}} - V_{\mathrm{y}}|}{|V_{\mathrm{x}} - V_{\mathrm{y}}|} T_{\mathrm{s}} \\ T_{\mathrm{y}} = T_{\mathrm{s}} - T_{\mathrm{x}} \end{cases} \tag{2}$$

where the action time of the basis synthetic vectors $\boldsymbol{V}_{\mathrm{x}}$ and $\boldsymbol{V}_{\mathrm{y}}$ are T_{x} and T_{y}, respectively. The switching cycle is T_{s}. It is necessary to ensure that the action time between the redundant vectors of each basis synthetic vector is equal so as to realize the voltage balance between the DC-side capacitors.

4. Simulation and Experimental Results

In this section, the simulation and experimental results of a single-phase five-level rectifier prototype are presented to verify the effectiveness and feasibility of the proposed SVPWM algorithm. The system parameters applied in the simulation are listed in Table 3.

Table 3. System parameters.

Parameters	Value
The AC grid voltage u_s/V	220
The AC inductance L/mH	3
DC-link reference voltage u_{dc}/V	400
Load resistance $R_{L/}\Omega$	100
Fundamental frequency f_0/Hz	50
Switching frequency f_s/kHz	5
DC-side capacitor C_1/μF	1100
DC-side capacitor C_2/μF	1100
DC-side capacitor C_3/μF	40
DC-side capacitor C_4/μF	40

4.1. Simulation Results

Figure 5 shows the sector judgment curve of $\boldsymbol{V_{ref}}$ under the SVPWM algorithm proposed in this paper. Meanwhile, the waveforms of grid voltage u_s, inductive current i_L, port input voltage u_{ab}, and the voltage u_{ao} from point "a" on the AC side to point "o" on the DC side under the SVPWM algorithm proposed in this paper are shown in Figure 6. According to Figures 5 and 6, the feasibility of the proposed SVPWM algorithm and the given sequences are verified.

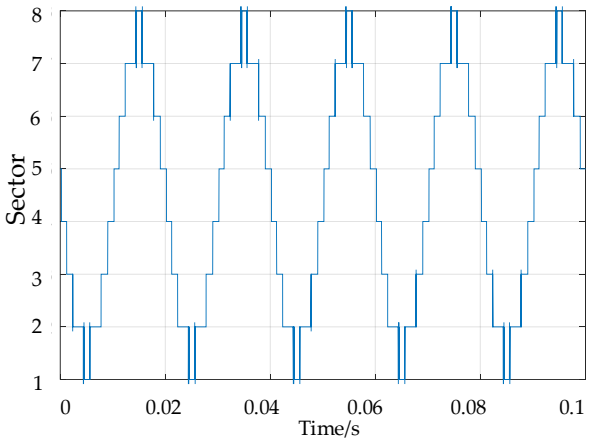

Figure 5. Sector judgement of rectifier during steady-state operation.

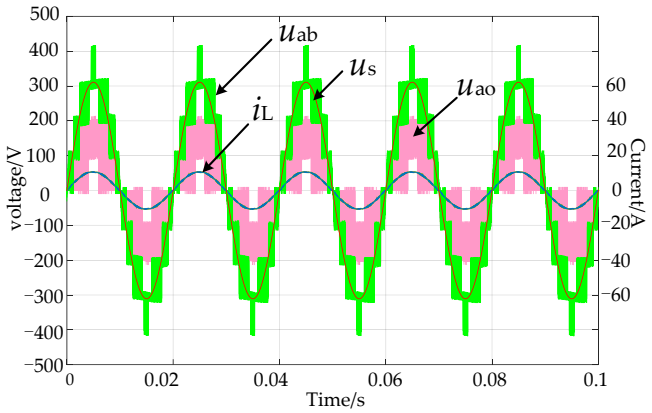

Figure 6. Voltage and current at AC side of rectifier during steady-state operation.

Figure 7 shows the voltage and current at the AC side under the conventional carrier-based phase-shift SPWM and the SVPWM algorithm with different SVPWM sequences proposed in this paper. It can bet seen from the figure that the unit power factor operation can be realized under the conventional carrier-based phase-shift SPWM and the SVPWM algorithm and the harmonic distortion rate of input current i_L is lower under the SVPWM algorithm.

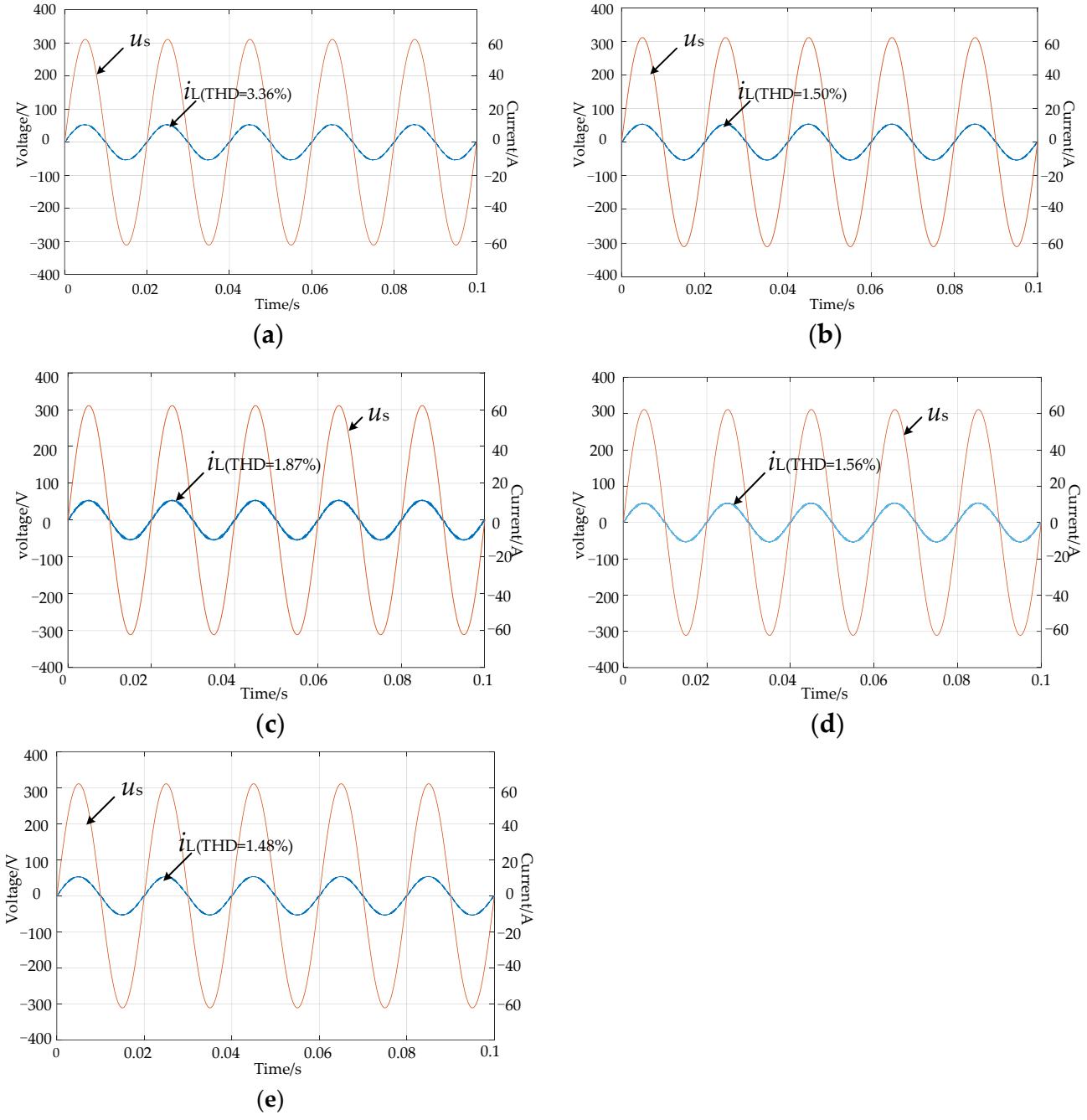

Figure 7. Grid voltage and inductive current under different modulation methods during steady-state operation. (**a**) SPWM. (**b**) SVPWM-1. (**c**) SVPWM-2. (**d**) SVPWM-3. (**e**) SVPWM-4(hybrid).

Figure 8 shows the voltages of DC-side capacitors C_1 and C_2 during steady-state operation of the rectifier under conventional carrier-based phase-shift SPWM and the SVPWM proposed in this paper. Figure 9 shows the corresponding DC-side midpoint voltage fluctuation Δu_{c12}. It can be seen from the curves that both SPWM and SVPWM

can achieve the stable output of DC-link voltage. However, through comparison, it can be found that under the SVPWM algorithm proposed in this paper, especially under the SVPWM-4 sequence, the neutral point voltage Δu_{c12} is significantly reduced by about 60%, which reduces the transmission loss of the DC-link voltage to a certain extent and provides space for reducing the capacitance C_1 and C_2.

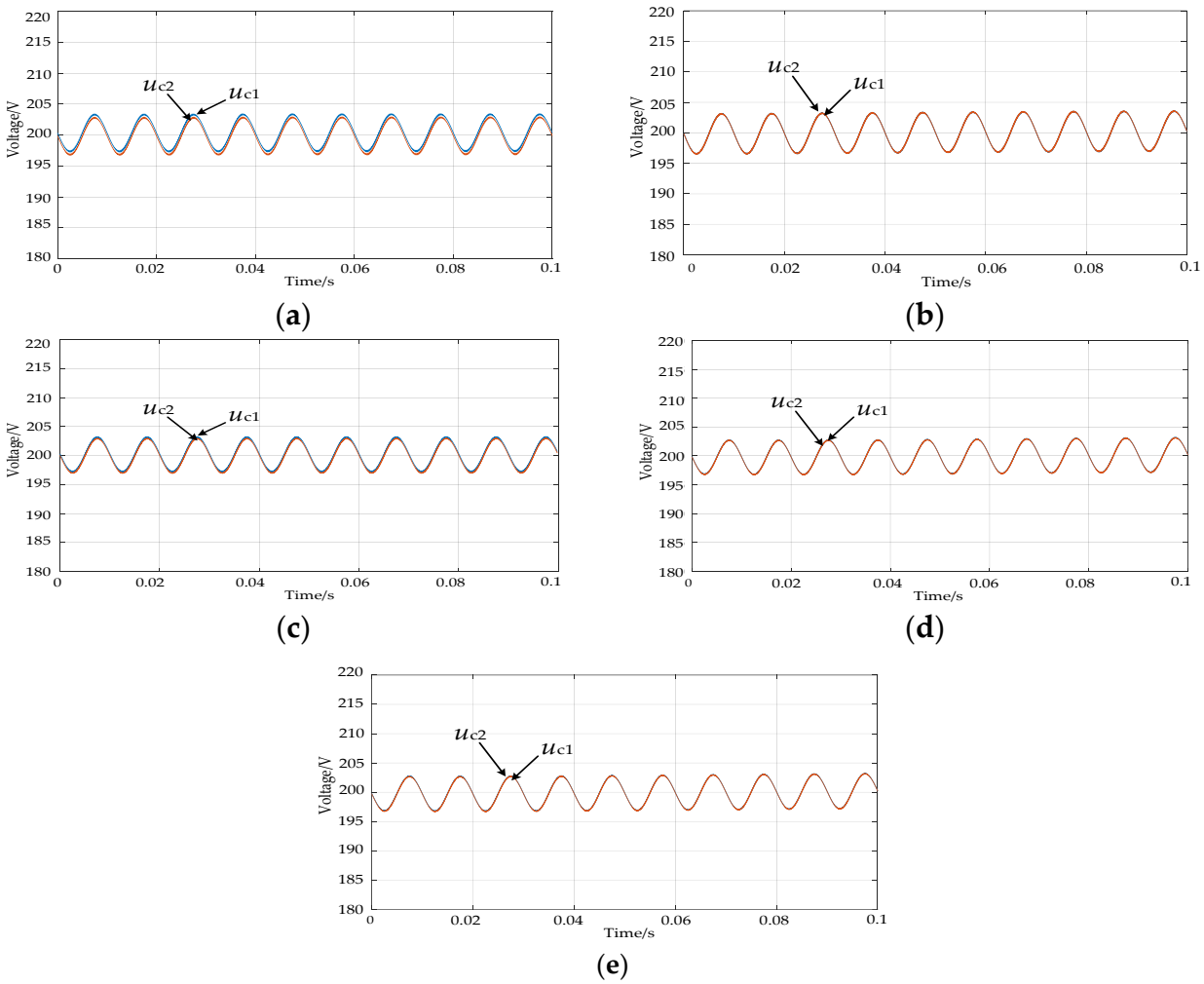

Figure 8. The voltages of u_{c1} and u_{c2} under different modulation methods during steady-state operation. (**a**) SPWM. (**b**) SVPWM-1. (**c**) SVPWM-2. (**d**) SVPWM-3. (**e**) SVPWM-4(hybrid).

Figure 10 shows the voltages of flying capacitors C_3 and C_4 under the conventional carrier-based phase-shift SPWM and the SVPWM proposed in this paper. Figure 11 shows the voltage fluctuation Δu_{c34} between the two flying capacitors C_3 and C_4. It can be seen from the figures that both SPWM and SVPWM can realize the charge and discharge of flying capacitors, and the voltage value is stable at about 1/4 of the reference voltage. Moreover, through comparison, it can be found that under the SVPWM algorithm proposed in this paper, especially under the SVPWM-4, the voltage fluctuation Δu_{c34} is greatly reduced by about 98%. This advantage provides space for further reducing the size of flying capacitors, and has certain economic benefits. It is proved that the SVPWM algorithm proposed in this paper can not only realize better AC-side current quality, but also greatly reduce the volume and cost of the single-phase five-level rectifier, which has better engineering application and promotion value.

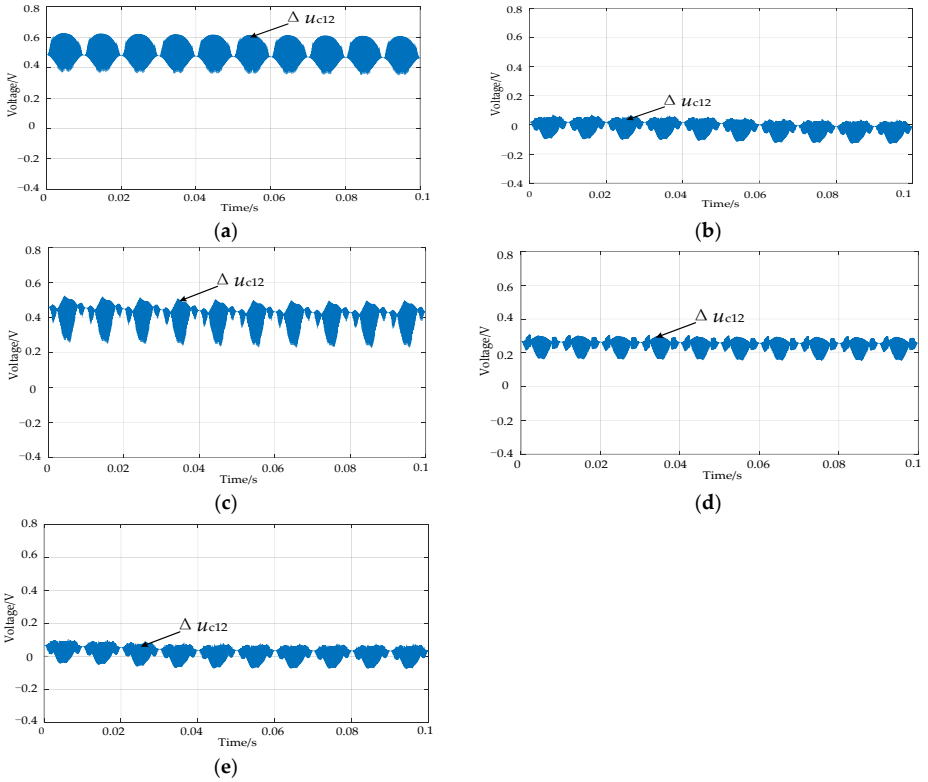

Figure 9. The voltage fluctuation of Δu_{c12} under different modulation methods during steady-state operation. (**a**) SPWM. (**b**) SVPWM-1. (**c**) SVPWM-2. (**d**) SVPWM-3. (**e**) SVPWM-4(hybrid).

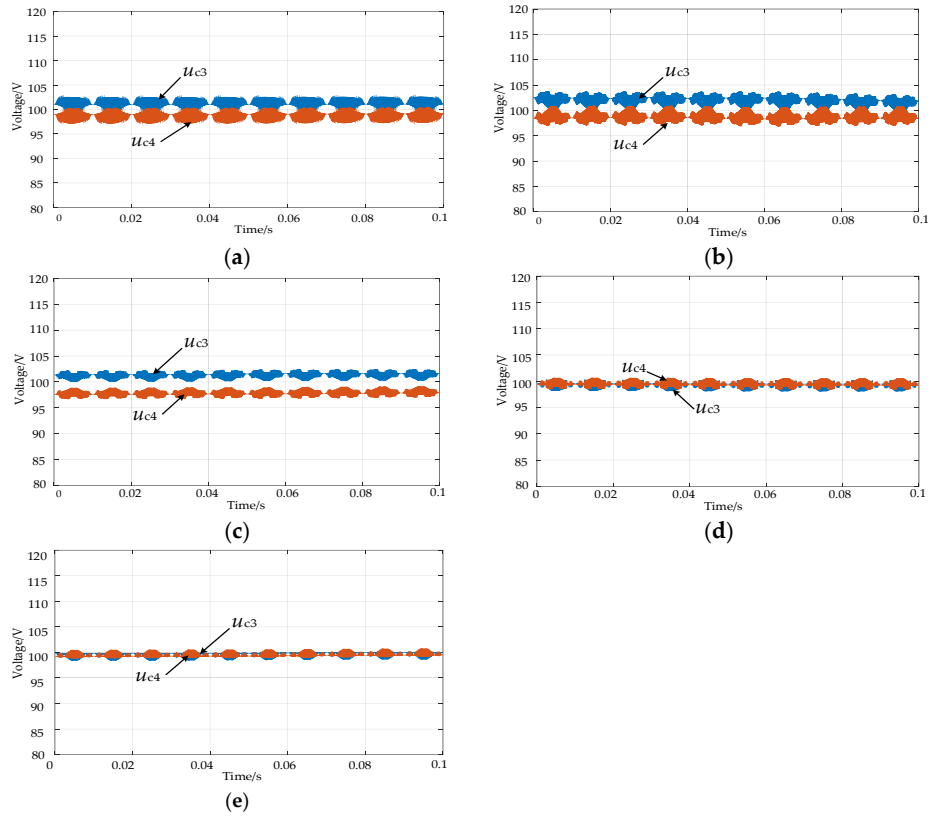

Figure 10. The voltages of u_{c3} and u_{c4} under different modulation methods during steady-state operation. (**a**) SPWM. (**b**) SVPWM-1. (**c**) SVPWM-2. (**d**) SVPWM-3. (**e**) SVPWM-4(hybrid).

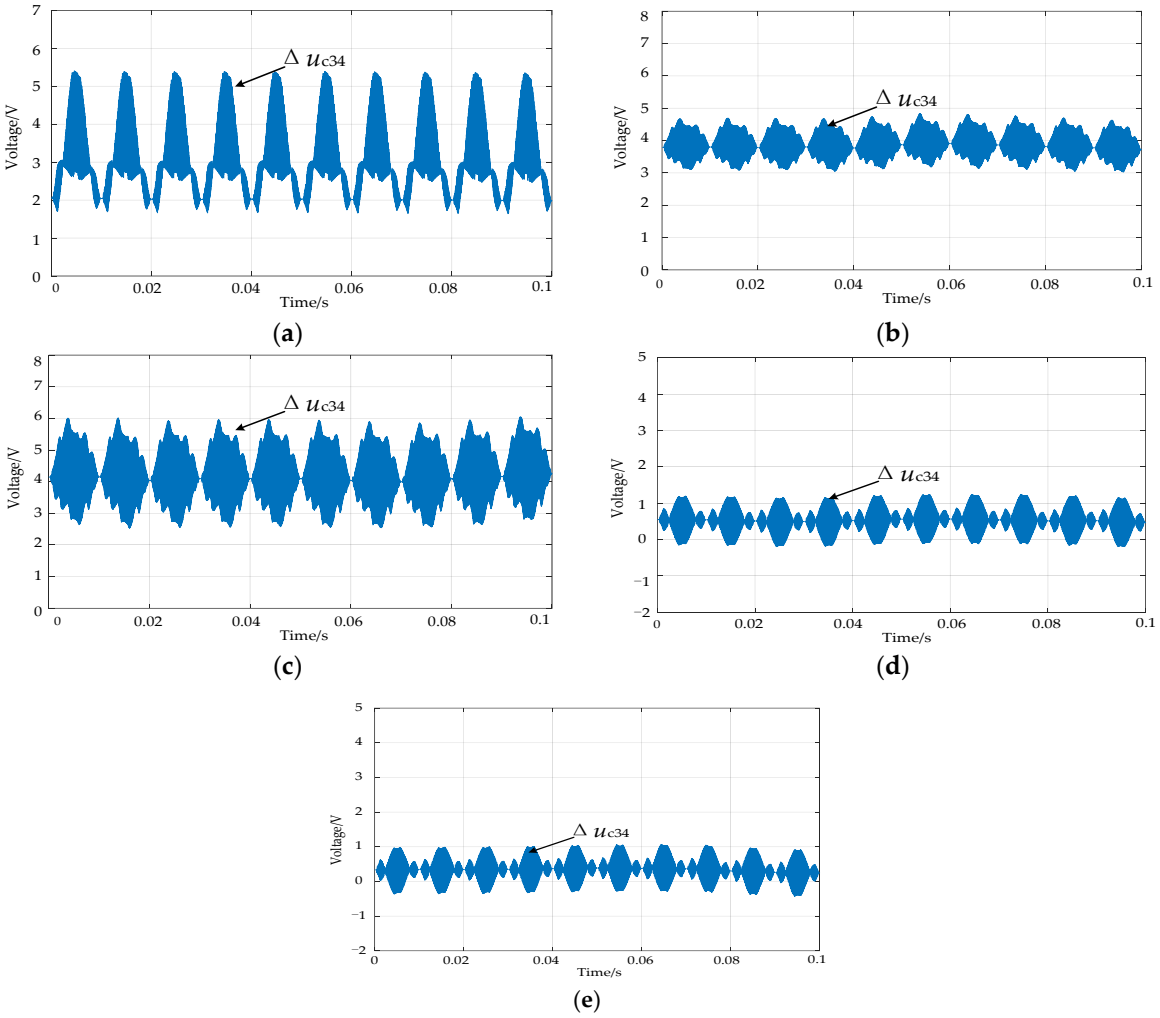

Figure 11. The voltage fluctuation of Δu_{c34} under different modulation methods during steady-state operation. (**a**) SPWM. (**b**) SVPWM-1. (**c**) SVPWM-2. (**d**) SVPWM-3. (**e**) SVPWM-4(hybrid).

4.2. Experimental Results

In order to verify the proposed SVPWM algorithm for a single-phase five-level rectifier with DC-side capacitor voltage balance, a down-scaled prototype, as shown in Figure 12, was built. The power supply used was a programmable AC power supply, Chroma 61503, while the oscilloscope was Tektronix DPO 3054. The controller used was TMS320F28335 DSP from Texas Instruments. In the experimental test, a reduced power level was used, with an effective input voltage of 110 V on the AC side, and a desired DC-link voltage of 200 V. Furthermore, all other parameters are consistent with the simulation section, as shown in Table 3. Meanwhile, this section only selects SVPWM-4 sequence with the best overall performance to verify the effectiveness and feasibility of the SVPWM algorithm proposed in this paper. The main experimental results are as follows.

Figure 13 shows the AC-side voltage and current, the total DC-link voltage u_{dc} as well as the port voltage u_{ab}. Nine-level port voltage u_{ab} and sinusoidal AC-side current can be realized. Moreover, the total DC-link voltage can be stabilized near the desired value with a small voltage ripple.

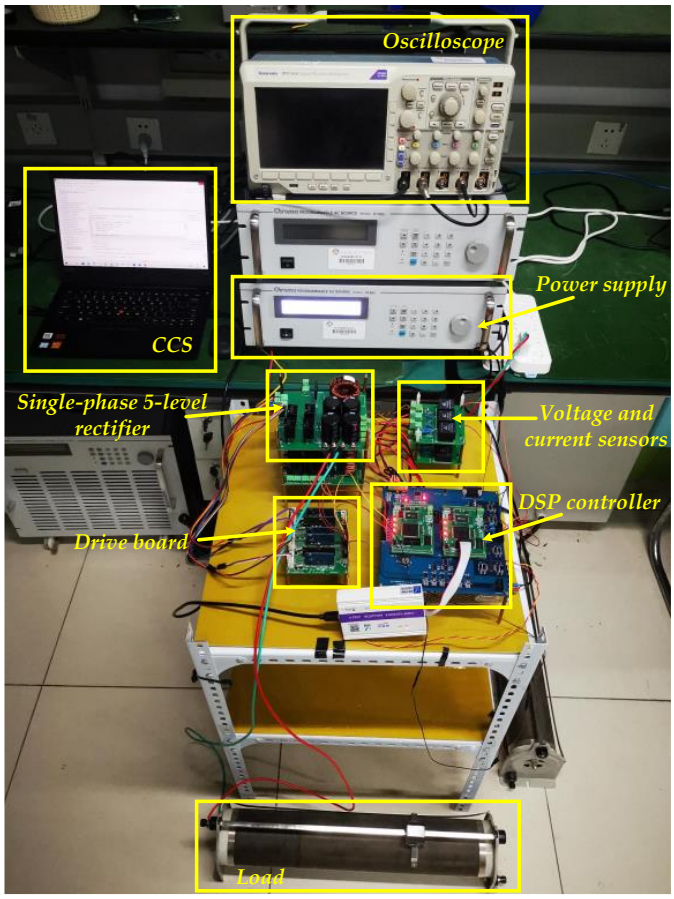

Figure 12. The prototype of single-phase five-level rectifier.

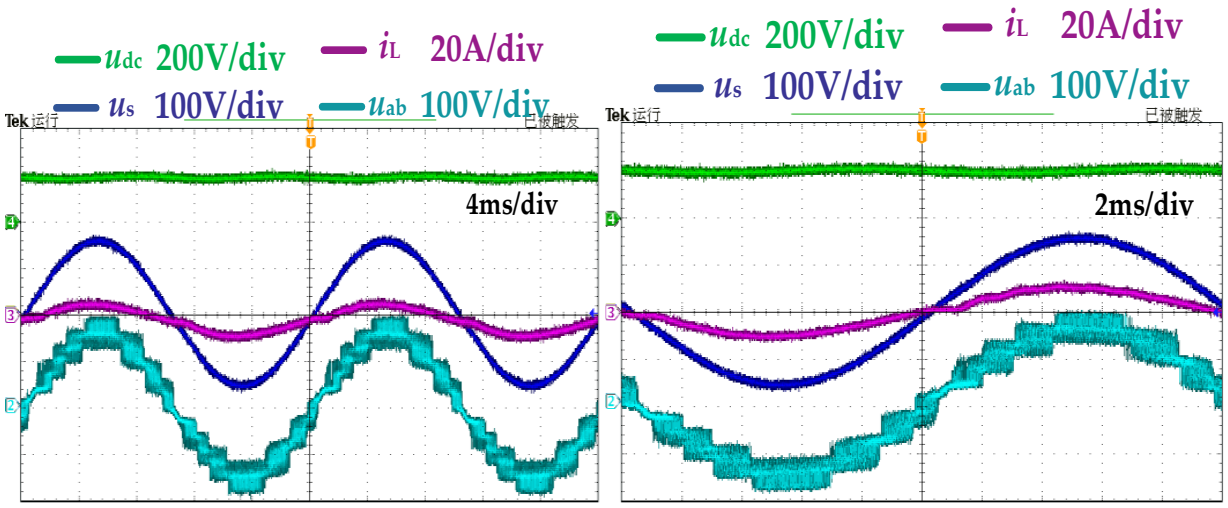

Figure 13. Experimental results of current i_L and voltages u_s, u_{dc} and u_{ab}.

Figures 14 and 15, respectively, show the AC-side voltage u_s and current i_L as well as the DC-side capacitor voltages u_{c1} and u_{c2} under the load suddenly changing from 100 Ω to 50 Ω and 50 Ω to 100 Ω. It can be seen that the capacitor voltages is still well balanced, which verifies the effectiveness of the proposed SVPWM algorithm.

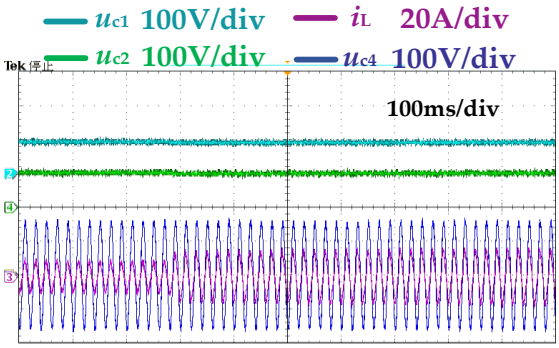

Figure 14. Experimental results of current i_L and voltages u_s, u_{c1} and u_{c2} with load suddenly changing from 100 Ω to 50 Ω.

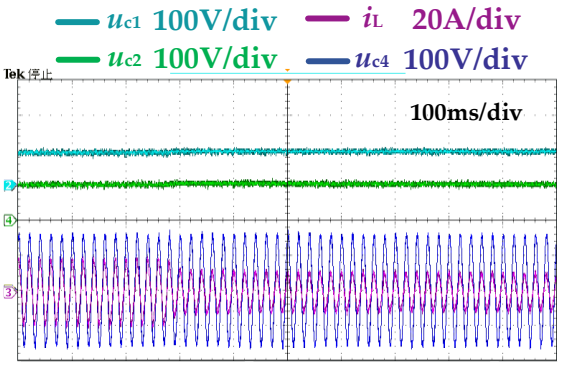

Figure 15. Experimental results of current i_L and voltages u_s, u_{c1} and u_{c2} with load suddenly changing from 50 Ω to 100 Ω.

Figure 16 shows the DC-side capacitor voltages u_{c1}, u_{c2}, u_{c3} and u_{c4}. It can be found that the DC-side capacitor voltages can be well balanced. The voltages u_{c1} and u_{c2} can be stabilized near the desired value with small voltage ripple. In addition, the voltages u_{c3} and u_{c4} can be stabilized near half of the voltage u_{c1} or u_{c2} with smaller voltage ripple. Moreover, the voltage fluctuations between u_{c1} and u_{c2}, u_{c3} and u_{c4} are well suppressed under the proposed SVPWM algorithm. Therefore, Figures 13–15 prove the feasibility and effectiveness of the SVPWM algorithm proposed in this paper for single-phase five-level rectifier. Meanwhile, we have also provided a comparison table with the previous work to highlight the achievements of this paper, which is shown in Table 4.

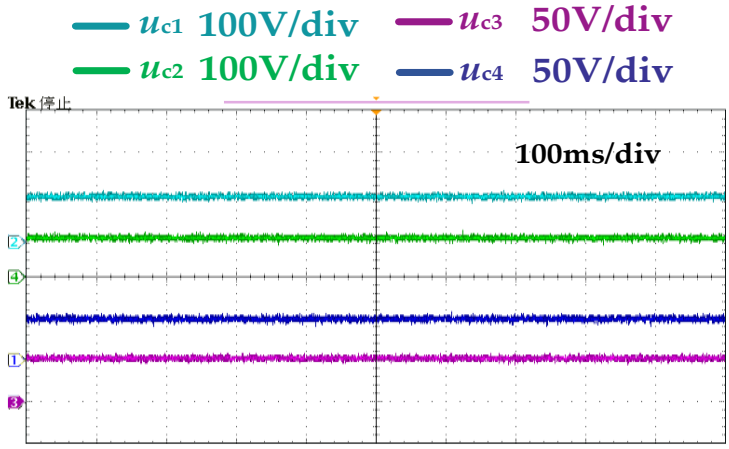

Figure 16. Experimental results of voltages u_{c1}, u_{c2}, u_{c3} and u_{c4}.

Table 4. Comparison with the previous work.

	The Previous Work	This Paper
1	Propose the novel multilevel rectifier	Sort out the principle and give a space vector diagram
2	Adopt carrier-based phase-shift SPWM	Propose a specific SVPWM algorithm
3	Need additional voltage balancing control	Actively balancing capacitor voltage without additional voltage balancing control
4	Current quality (THD%) on the AC side is about 3.3%	Current quality (THD%) on the AC side is about 1.5%
5	The fluctuation of the neutral point voltage on the DC-link is large	The fluctuation of the neutral point voltage on the DC-link is reduced by about 60% compared to the SPWM
6	Voltage difference between two flying capacitors is large	Voltage difference between two flying capacitors is reduced by about 98% compared to the SPWM

5. Discussion

Aiming at the inherent disadvantages of a large number of single-phase five-level DC-side capacitors and complex capacitor voltage balance control, an SVPWM algorithm for improving the DC-side capacitor voltage balance is proposed in this paper. Finally, the simulation and experimental results verify the correctness and effectiveness of the proposed SVPWM algorithm. Moreover, this paper also gives several SVPWM sequences, and highlights its advantages through the comparative analysis with the conventional carrier-based phase-shift SPWM. Meanwhile, the given sequences are summarized, and a sequence with the best performance is recommended. It is of great significance for the promotion and application of the single-phase five-level rectifier in practical engineering, and can be easily extended to the higher levels of the three-phase rectifiers in Refs. [22,23].

6. Conclusions

In this paper, we propose an SVPWM algorithm for the recently proposed novel unidirectional multilevel rectifier. Compared with the conventional carrier-based phase-shift SPWM, it can balance the DC-side capacitor voltage better without requiring additional complex capacitor voltage balancing control structures. Furthermore, the flexibility of the proposed SVPWM algorithm is demonstrated through different sequence selections, providing ideas for higher-level SVPWM algorithm research in both three-phase and single-phase unidirectional rectifiers. Additionally, it provides theoretical support for practical engineering applications and lays a solid foundation for the research of upper control strategies for this type of unidirectional rectifier. These contributions will facilitate further studies in other fields, such as nonlinear control strategies and thermal losses.

Author Contributions: Conceptualization, D.Y. and H.C.; methodology, D.Y. and C.W.; software, D.Y.; validation, D.Y., H.C., C.W. and C.T.; writing—original draft preparation, D.Y.; writing—review and editing, D.Y., H.C., C.W. and C.T. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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