electronics

MDPI

Article

Design of 6 GHz Variable-Gain Low-Noise Amplifier Using Adaptive Bias Circuit for Radar Receiver Front End

Hyungseok Nam [1,†], Dang-An Nguyen [1,†], Yanghyun Kim [2] and Chulhun Seo [1,*]

[1] Department of Information and Telecommunication Engineering, Soongsil University, Seoul 06978, Republic of Korea
[2] Department of Electronic Engineering, Soongsil University, Seoul 06978, Republic of Korea
* Correspondence: chulhun@ssu.ac.kr
† These authors contributed equally to this work.

Abstract: This paper presents a variable-gain low-noise amplifier (VGLNA) based on an adaptive bias (ADB) circuit for the radar receiver front end. The ADB circuit processes the signal separated by a coupler at the LNA output port. First, the ADB circuit rectifies the coupled signal into positive DC voltage through a rectifier, which is then inverted to control a junction-gate field-effect transistor (JFET). The voltage-controlled current of JFET flows through a voltage-divider network and finally produces the DC biasing voltage for the BJT base termination, which decreases with the increase in the input RF power. The proposed VGLNA operates automatically in high gain at low input power and low gain at high input power, providing a wider dynamic range as compared to the constant-bias counterpart. For validation, a prototype is fabricated and measured at 6 GHz. As observed, the base biasing voltage generated by the ADB circuit is changed from 858 mV to 798 mV as the input power increases from −50 dBm to 0 dBm. As a result, the dynamic range represented by the input P1dB point (IP1dB) has an increase of 6.5 dB, while LNA still maintains a high gain of 15.15 dB at low input power.

Keywords: adaptive bias (ADB) circuit; variable gain low noise amplifier (VGLNA); voltage controlled resistor; JFET; diode; radar receiver

Citation: Nam, H.; Nguyen, D.-A.; Kim, Y.; Seo, C. Design of 6 GHz Variable-Gain Low-Noise Amplifier Using Adaptive Bias Circuit for Radar Receiver Front End. *Electronics* **2023**, *12*, 2036. https://doi.org/10.3390/electronics12092036

Academic Editors: Mohammad Maktoomi, Tutku Karacolak, Mohamed Helaoui and Syed Azeemuddin

Received: 3 April 2023
Revised: 25 April 2023
Accepted: 26 April 2023
Published: 27 April 2023

1. Introduction

The radar systems are an electromagnetic system for the detection and location of the objects, and a low-noise amplifier (LNA) is considered a key component in its receiver front end [1–3]. Radar applications require a LNA, which can well process both weak and strong echos of the received signal. Specifically, in the case of an incoming weak signal, the LNA should provide high gain and minimum additive noise to increase the signal-to-noise ratio (SNR) of the signal. In contrast, for short-distance objects with high-power input signal, it is expected to operate at a low gain, which can exhibit good linearity or a wide dynamic range to avoid the saturation of the receiver chain. Therefore, a mechanism of gain control is necessary in the LNA design to achieve both these two objectives simultaneously, which cannot be solved with the common fixed-gain LNAs. In addition, in the case of sensing platforms, variable-gain LNAs (VGLNAs) research is essential because gain problems may occur depending on distance [4–6].

The VGLNAs have been developed for achieving a wide dynamic range as well as covering the entire detection range without the receiver signal saturation [7–13]. In [7,8], the authors proposed a method known as current steering, which controls gain through reducing the bias current and transconductance of the cascoded transistors. Another method is using an extra digital signal [9–11]. However, the use of the external control signal can increase receiver complexity and cause additional power consumption from digital circuits. Authors in [12] presented an automatic mechanism of gain control using an analog signal inside the circuit without external excitation. Nevertheless, the requirement of

a multi-transistor adaptive biasing circuit leads to high design complexity, a large occupying area, and low accuracy in the discrete-circuit implementation. In [13], gain is automatically adjusted by a Gilbert-cell-based topology. However, this structure is also complicated and not suitable for discrete-circuit deployment.

In this paper, a single-ended VGLNA on the discrete-circuit implementation of a bipolar junction transistor (BJT) is designed with an extended dynamic range for a military radar receiver front-end at 6 GHz, which is in the C-Band, with the advantages of long-distance detection and low atmospheric attenuation, as compared to a higher frequency band. The VGLNA deploys a novel adaptive-biasing (ADB) circuit, which adopts a small part of the output analog signal to control gain in an automatic manner without another additional signal. The proposed ADB network is mainly a combination of a AC-DC converter and a resistive divider, which is one of the resistors realized by the equivalent ohmic operation of a junction field effect transistor (JFET). The main principle is to use the DC load signal from the rectifier to manipulate the equivalent resistor r_d of the JFET source as JFET operates in the ohmic region. Following the design method, the dynamic range of LNA is extended significantly in comparison with that of the fixed-gain counterpart. It is also important to note that our research focuses on investigating and implementing the printed circuit board (PCB)-level LNA that relies on discrete components. PCB-level LNAs with ADB circuits have not been extensively studied, but the discrete circuits can offer advantages in terms of high performance, low complexity, and manufacturing cost compared to the integrated circuits.

2. Extended Dynamic Range with Lower Biasing Base Voltage

The generic schematic of a BJT-based LNA is shown in Figure 1a, where the active device is voltage-biased with two DC sources, i.e., V_{b0} and V_{DD} for base and collector terminations, respectively. For single-frequency operation, the dynamic range is commonly characterized by the input 1 dB compression point (IP1dB), which determines the input power at which LNA gain is dropped by 1 dB. In radar detection applications, it is always desirable to extend the IP1dB of LNA for processing near-distance objects with strong reflections in the linear region. The increase in the dynamic range, referred to as the increase in IP1dB, relates intimately to the decrease in the base biasing voltage V_{b0}, which can be demonstrated by considering the variation of BJT transconductance within small-to-large signal regimes. Assuming V_t is the thermal voltage, transconductance g_m is highest with small-signal driving, approximating I_{c0}/V_t and reducing as the input signal grows large. The large-signal transconductance G_m associated with the input signal magnitude is then given by [14]

$$G_m \equiv \frac{I_{c1}}{V_{b1}} = \frac{\alpha_f I_{ES} e^{V_{b0}/V_t}}{V_t} \cdot f(x) \tag{1}$$

$$f(x) = \frac{2\hat{I}_1(x)}{x}, x \equiv \frac{V_{b1}}{V_t} \tag{2}$$

$$V_{be} = V_{b0} + V_{b1} cos\omega_0 t, \tag{3}$$

where I_{ES} denotes the saturated current, x is the base signal voltage amplitude, and f_x is independent of V_{b0} and is defined as in [14]. It is clear that G_m decreases with the increase in x or the signal magnitude V_{b1}. Additionally, the amplitude of G_m depends on V_{b0} as described in (1). The slope of G_m with respect to x is negative and can be calculated as follows:

$$\frac{dG_m}{dx} = \frac{\alpha_f I_{ES} e^{V_{b0}/V_t}}{V_t} \cdot f'(x). \tag{4}$$

From (4), with the independence of $f(x)$ on V_{b0}, and assuming that the V_{b0}^1 is greater than V_{b0}^2, then $\left|\frac{dG_m}{dx}\right|_{V_{b0}=V_{b0}^1}$ becomes larger than $\left|\frac{dG_m}{dx}\right|_{V_{b0}=V_{b0}^2}$. In other words, G_m in the case of the biasing voltage V_{b0}^1 is dropped quicker than G_m with V_{b0}^2. As a result, IP1dB is higher with lower biasing voltage V_{b0} as intuitively illustrated in Figure 1b. The gain curve with respect to V_{b0}^1 is more steep and descends to its IP1dB at a lower input power point, i.e., $\text{IP1dB}_{G^1} < \text{IP1dB}_{G^2}$. However, LNA is also required to provide high gain to amplify the weak signals for long-distance detection to increase SNR, which is only obtained with high V_{b0}, for example, V_{b0}^1 instead of V_{b0}^2 in Figure 1b. Therefore, in order to achieve two targets concurrently, i.e., a wide dynamic range for processing the entire detection range without receiver saturation and a high initial gain for the weak signal amplification, a mechanism for changing the LNA gain according to the input power level has become a reliable approach and has been widely used in the radar detection applications. In this paper, the principle of reducing the base biasing voltage V_{b0} with the increase in input power is used to design the VGLNA.

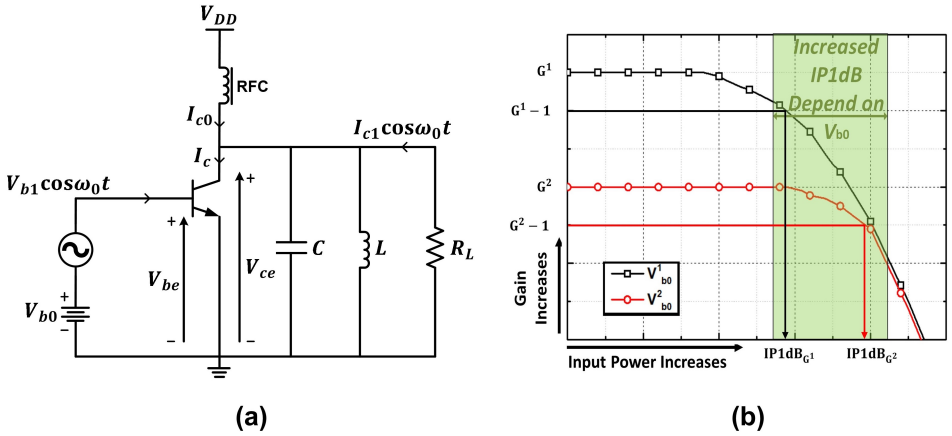

Figure 1. (**a**) Generic LNA schematic with a bipolar transistor, and (**b**) input P1dB at different biasing point V_{b0}.

3. VGLNA Design with ADB Circuit

The proposed VGLNA structure is shown in Figure 2, which commonly consists of input and output matching networks (MNs) to provide noise and power matchings for low noise figure (NF) and high gain. Specifically, the input MN is designed to match an intermediate impedance between noise and power impedances, which can provide a balanced performance of NF and gain, simultaneously, even in the whole variation range of V_{b0}.

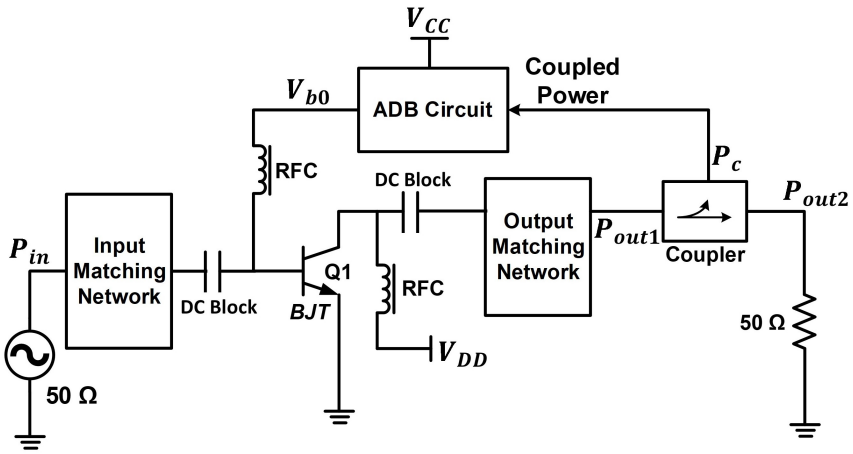

Figure 2. Block diagram of the proposed VGLNA.

Instead of biasing the base terminal of BJT with a fixed DC source, LNA deploys an ADB circuit, which takes a small power proportion of the output signal through a coupler to generate a DC voltage V_{b0} for base biasing. As expected, the output DC voltage V_{b0} from the ADB circuit relates inversely to the input power, i.e., as the input power grows, V_{b0} reduces, and such variation leads to an extension of IP1dB.

The detail schematic of the proposed ADB circuit is shown in Figure 3. This network deploys an AC-DC converter, which rectifies the coupled signal into DC positive voltage V_R. The rectifier topology utilizes a Schottky diode in a shunt, which was investigated in [15,16]. The RF coupled power P_c is initially delivered through a rectifier input matching network to obtain a maximum signal across the diode. Then, the diode rectifies the negative half cycle of the signal, and the overall energy is stored in C_1. The combined network of a RF choke and C_L acts as a DC-pass filter, which smooths the rectified voltage. The DC output voltage V_R determines the positive terminal of the inverse source V_i and creates negative voltage V_G on the other side to control the JFET current flowing in a voltage divider network. Finally, the voltage divider yields V_{b0}, exhibiting an inverse variation with the coupled signal power as shown in Figure 3.

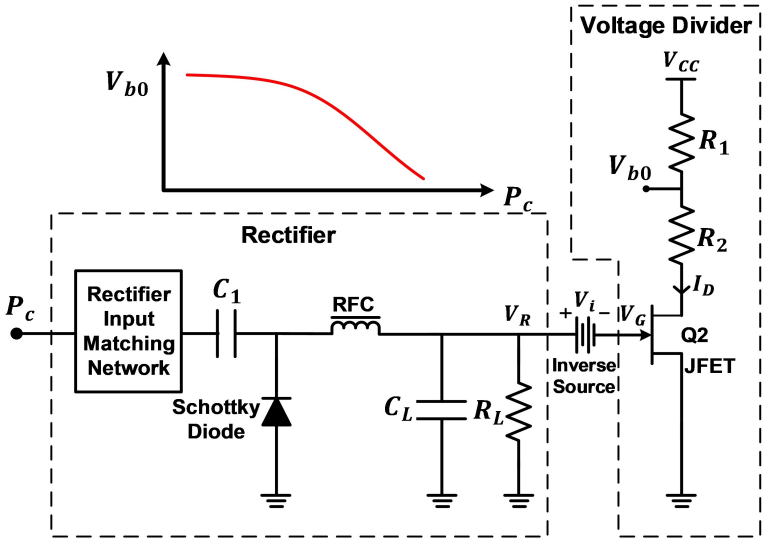

Figure 3. Schematic of the proposed ADB circuit.

In order to clarify the relation between the resulting voltage V_{b0} and the input power P_{in}, it is assumed that the coupler has the coupling coefficient of β(dB) and LNA exhibits an initial gain of G(dB). The coupled power P_c(dB) is calculated as follows:

$$\begin{aligned} P_c &= P_{out1} - \beta \\ &= P_{in} + G - \beta. \end{aligned} \tag{5}$$

From (5), P_{in} and P_c are in the same variation, and an increase in P_{in} leads to an increase in V_R as a result of the AC-DC converting process of the rectifier [15]. The DC inverse source V_i then generates V_G with the following relation:

$$V_G = V_R - V_i. \tag{6}$$

For a depletion-mode JFET, the value of V_i must be higher than V_R to yield a negative value of V_G for controlling the JFET current, which is calculated at different operating regions as follows [17]:

$$I_D = I_{DSS}\left[1 - \frac{V_G}{V_P}\right]^2 \tag{7}$$

for saturation region and

$$I_D = 2I_{DSS}\left[(1+\frac{V_G}{V_P})(\frac{V_{DS}}{V_P}) - (\frac{V_{DS}}{V_P})^2\right] \tag{8}$$

for the ohmic region, where I_{DSS} is the maximum saturation current, and V_P is the pinched-off voltage. If JFET operates in the saturation region, I_D is independent of V_{DS} as in (7), and apart from satisfying (7), I_D must abide by Kirchhoff's voltage law in the voltage divider network as follows:

$$\begin{aligned} V_{CC} &= I_D(R_1+R_2) + V_{DS} \\ &= I_D R_1 + V_{b0}. \end{aligned} \tag{9}$$

Because V_G is an increasing function of V_R, then an increment of P_{in} leads to higher I_D, and V_{b0} will be reduced through the decrease in V_{DS} to satisfy (9). As another case of ohmic region, I_D is dependent of V_{DS}, and JFET acts as a variable resistor r_d, whose resistance value is defined as

$$r_d = \frac{V_{DS}}{I_D} = \frac{r_0}{(1-\frac{V_G}{V_P})^2}, \tag{10}$$

where r_0 denotes the drain resistance at zero gate bias, i.e., $V_G = 0$. The voltage divider is then composed of three resistors (R_1, R_2, and r_d). As a result, V_{b0} can be calculated as follows:

$$V_{b0} = V_{CC}\frac{R_2 + r_d}{R_1 + R_2 + r_d}. \tag{11}$$

It can be seen from (10) and (11) that V_{b0} has the same variation with r_d and reduces with the increase in V_G. In general, any operating region of JFET, the voltage divider can produce V_{b0} exhibiting an opposite variation with V_G as well as the input power level. Because the required base biasing voltage V_{b0} is quite small for a BJT, just around $0.8V$ practically, JFET is predicted to operate in the ohmic region. Additionally, the values of R_1, and R_2 should be set such that at the starting time with $V_G = -V_i$, the maximum V_{b0} must be in the appropriate base–voltage range of the chosen BJT.

4. Implementation, Simulation and Experiment

For verification, the LNA is implemented on the Taconic TLY substrate ($\epsilon_r = 2.2$, $H = 0.8$ mm) with a realistic BJT model operating at 6 GHz. Figure 4 shows the entire schematic of the proposed VGLNA. The input and output MNs deploy L-type sections of transmission lines (TLINs) to provide accurate noise and power matches for low noise figure (NF) and high gain, respectively. The RF chokes used in Figures 2 and 3 are substituted by $\lambda/4$ TLINs for minimizing losses at 6 GHz. The model and value of the components are listed in Table 1 for simulation and measurement.

Table 1. Component models and values (implementation on 0.8-mm Taconic TLY-5) for simulation.

Components	Model/Value	Components	Model/Value
Q_1	BFP840FESD	TL_{i1}	$L = 5.0$, $W = 1.3$ mm
Q_2	LS26VNS	TL_{i2}	$L = 0.5$, $W = 1.3$ mm
Schottky Diode	BAT15-03W	TL_{o1}	$L = 2.8$, $W = 1.3$ mm
Coupler	DCW-6-722+	TL_{o2}	$L = 4.2$, $W = 1.3$ mm
DC Block	C08BL-2.4nF	TL_{ir1}	$L = 8.6$, $W = 1.0$ mm
C_{bypass}	C08BL-2.4nF	TL_{ir2}	$L = 2.4$, $W = 1.0$ mm
V_{CC},V_{DD}	1.8 V	C_{Lr}	C08BL-2.4 nF
V_i	2.4 V	R_{Lr}	5 kΩ
R_1	200 V	R_2	164 Ω

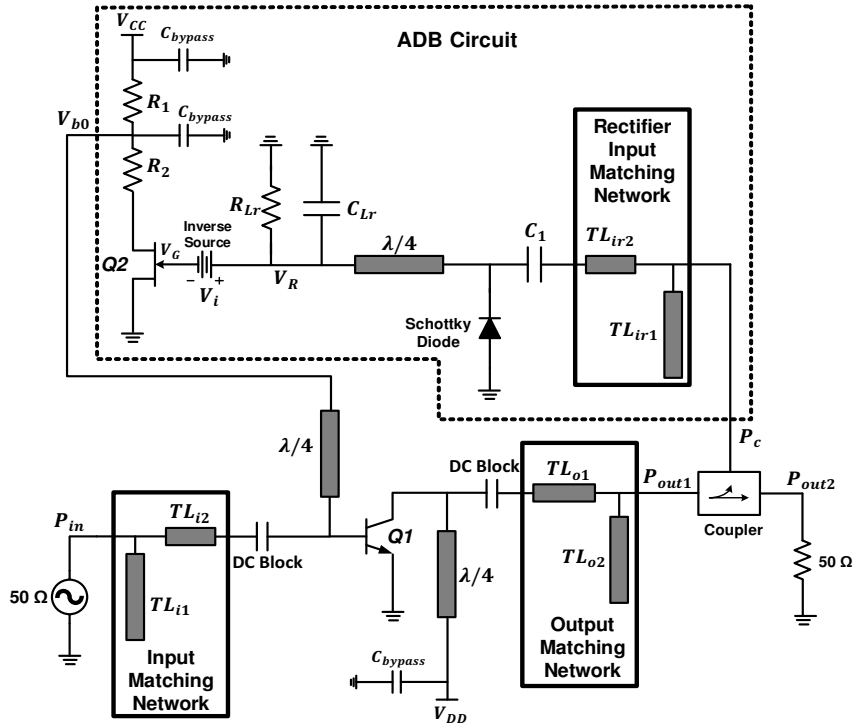

Figure 4. The overall schematic of the proposed VGLNA.

The stability factor μ of the proposed VGLNA is shown in Figure 5, which is higher than 1 within a tested wide bandwidth (5–7 GHz), indicating stable operation at the target frequency.

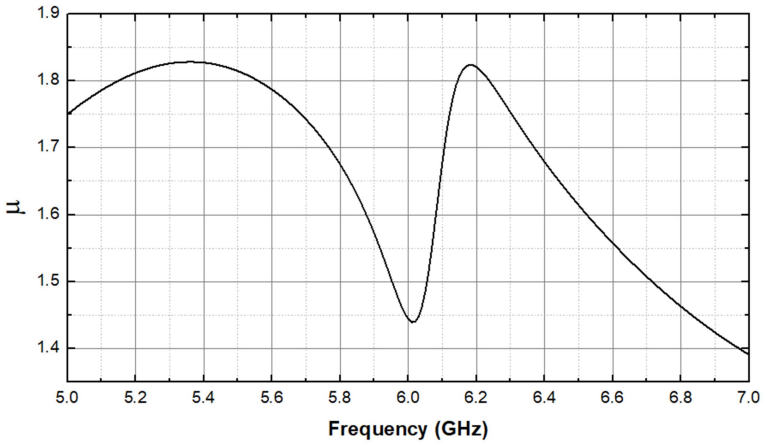

Figure 5. Stability factor (μ factor) of the proposed VGLNA.

Figure 6 presents the variation of P_c, V_R, V_G, and V_{b0} according to the input power P_{in} spreading from -50 dBm to 0 dBm. It can be seen that the coupled power P_C exhibits a positive slope with P_{in} and a high-enough value at $P_{in} > -30$ dBm so that the rectifier can detect and rectify the wave. As a result, V_R increases to the highest value of 1.9 V at $P_{in} = 0$ dBm; with $V_i = 2.4$ V, V_G changes from -2.4 V to -0.5 V during the input power range. This voltage controls the JFET current and generates the biasing voltage V_{b0} within a range from 873 mV to 837 mV as P_{in} increases. To determine the IP1dB gain of the proposed VGLNA, fixed-bias LNA version of the same BJT is simulated at several different values of V_{b0} in the extracted range. The biasing voltage V_{b0} is first assigned to the highest value of the V_{b0} range, and its IP1dB is extracted. Then, this IP1dB is mapped to the V_{b0} range to determine the corresponding V_{b0}. Subsequently, the LNA is operated at that new V_{b0}

with a new IP1dB. The process is repeated until the IP1dB gain is obtained as summarized in Figure 7. As shown in Figure 8a, with the adaptive-gain mechanism, the IP1dB gain is extended by 2.5 dB, while also achieving a high gain of around 16.6 dB at a low input power, which exhibits a clear advantage as compared to the fixed-bias counterpart at only $V_{b0} = 0.873$ V.

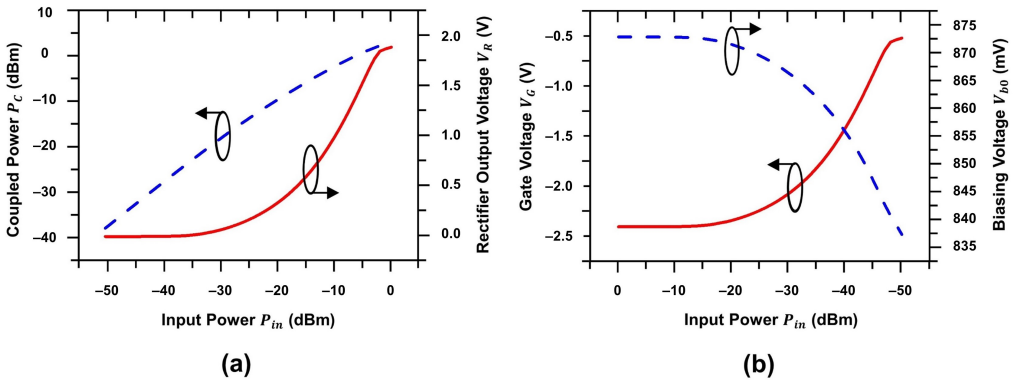

Figure 6. (**a**) Simulated coupled voltage P_C and rectifier output voltage V_R, and (**b**) simulated gate voltage V_G and biasing voltage V_{b0}.

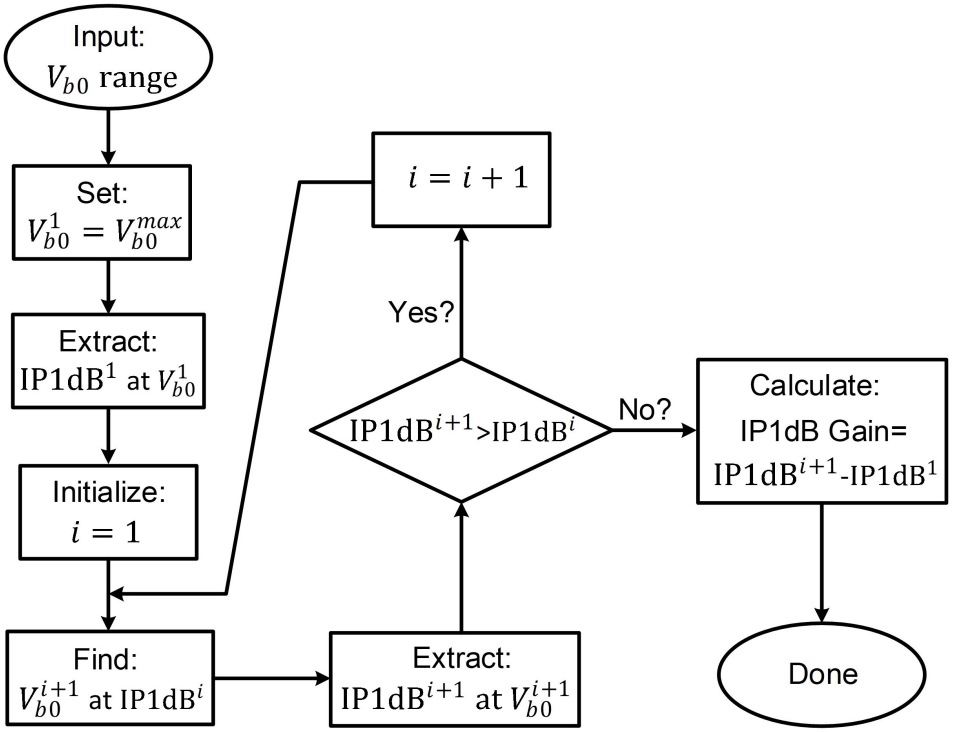

Figure 7. Procedure of IP1dB gain extraction from a V_{b0} range.

For experimental validation, a prototype is fabricated and tested. The circuit layout is shown in Figure 8b. We use a total of three DC power supplies, i.e., V_{DD}, V_{CC}, and V_i. A network analyzer is used first for measuring the S-parameters of the VGLNA. In this test, the initial gain of the VGLNA and its frequency response are observed. Then, the prototype is measured with a spectrum analyzer and a continuous-wave generator at the target frequency of 6 GHz to verify the adaptive gain behavior of the LNA. The trace of V_{b0} is performed thanks to a digital multimeter, which is used to calculate the IP1dB gain. Finally, the VGLNA experiences a noise analysis to determine its NF, which is important for practical radar applications.

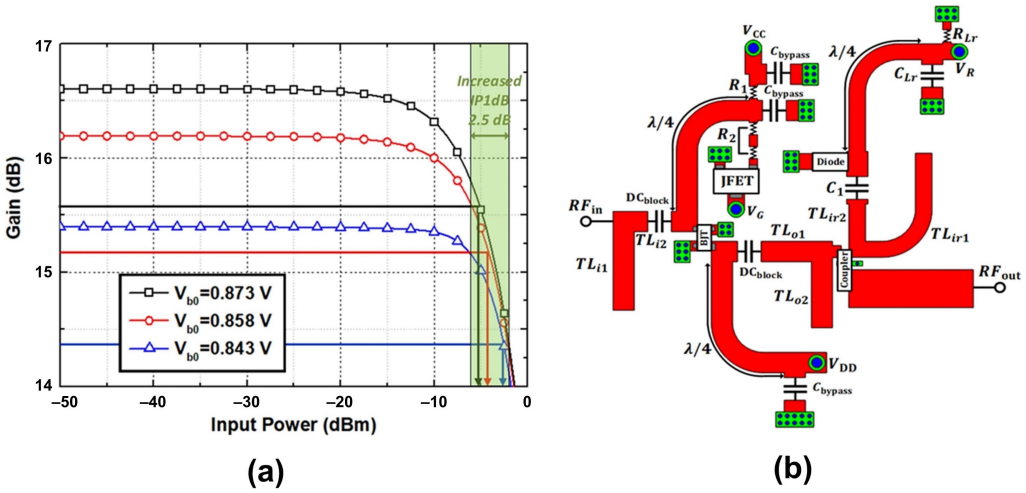

Figure 8. (**a**) Simulated IP1dB gain of the proposed VGLNA at 6 GHz, and (**b**) layout for VGLNA fabrication.

4.1. S-Parameters

The S-parameters measurement setup is shown in Figure 9a, where three DC power supplies are $V_{CC}, V_{DD} = 1.8$ V, and $V_i = 2.4$ V as in the simulation. The analysis of S-parameters is performed by a network analyzer N5230C, and the results at -50 dBm excitation are shown in Figure 9b. As observed, the reflection coefficients S_{11}, S_{22} are about -27 dBm and -8 dBm, respectively, at 6 GHz, confirming good impedance matching at the input and output terminals for power transmission. The transmission coefficient S_{21} of the proposed VGLNA is achieved at 15.5 dB, denoting a high gain during the small-signal regime at the design frequency. The proposed LNA also exhibits an initial high gain across a very wide bandwidth, i.e., over 10 dB within a bandwidth from 0.5 GHz to 7.2 GHz, which is expected to operate well at different frequency bands. In addition, the VGLNA is compact, with its dimension shown in Figure 9c.

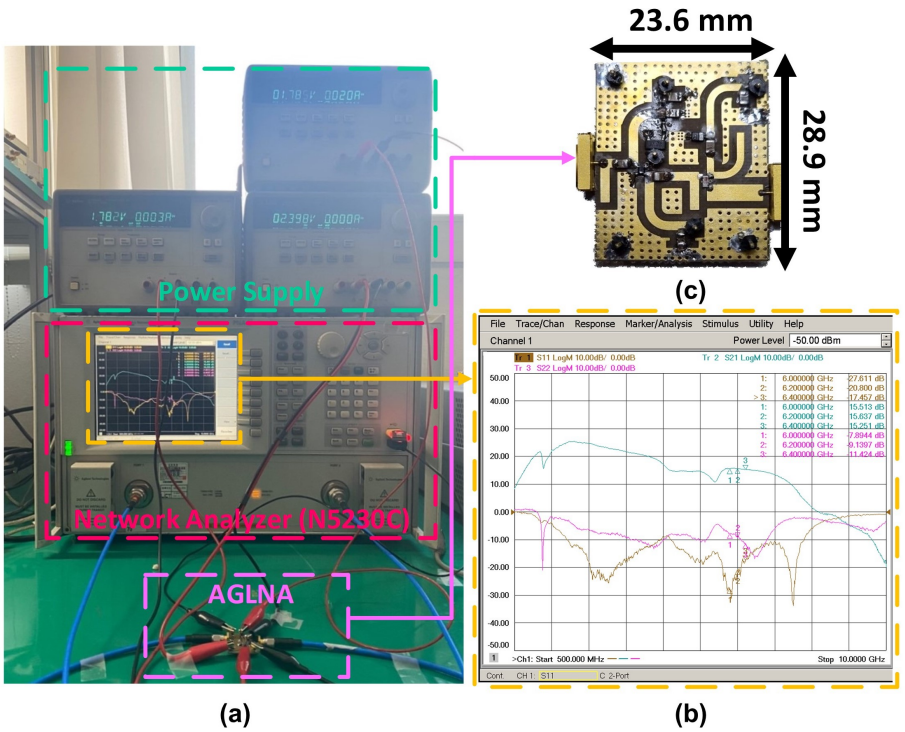

Figure 9. (**a**) S-parameter measurement setup, (**b**) measurement results, and (**c**) circuit photograph.

4.2. IP1dB Gain and Linearity

In order to evaluate IP1dB gain of our VGLNA at the target frequency, the prototype is measured under a signal generator and a spectrum analyzer. Similar to the S-parameters measurement setup, the circuit is applied with the same DC supplying voltages. A digital multimeter is used to measure the biasing voltage V_{b0} across the different input power levels. By sweeping the input power from −50 dBm to 0 dBm, a graph of gain and output power versus the input power is shown in Figure 10a. Note that these gain and output powers have different values from V_{b0}. The results show a similar tendency to the simulation ones, and it can be seen that the VGLNA always exhibits a gain of >10 dB within the overall input range. There is a slight difference in the initial gain between the two measurement schemes, i.e., using the S-parameters network analyzer and using the spectrum analyzer; due to their accuracy, there is instability in the cable loss and device characteristics. The overall range of V_{b0} is shown in Figure 10b. Increasing the input power from −50 dBm to 0 dBm, the observed voltage delivered to the base for biasing decreases from 858 mV to 798 mV. As a result, the DC collector current decreases, denoting a gain reduction mechanism in the LNA operation. It should also be noted that the similarity of the 1.2 dB lower measured gain (in comparison with the simulated gain while simulated) and the measured collector currents is due to the insertion loss of the coupler, which is not modeled accurately in the simulation.

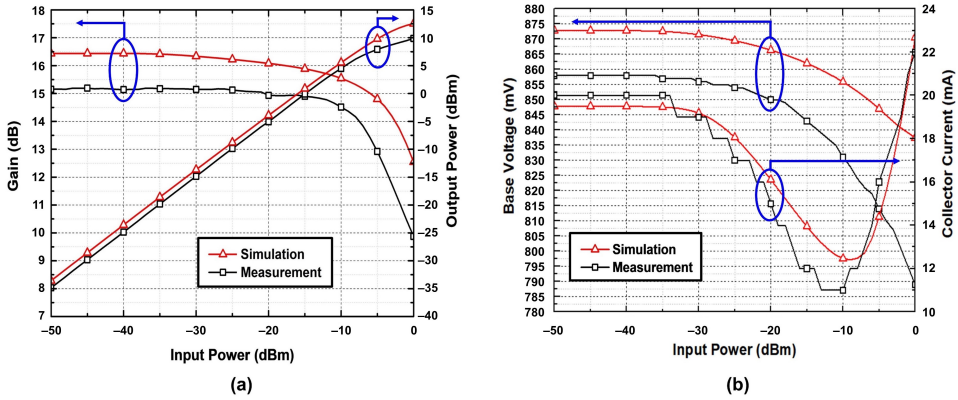

Figure 10. (**a**) Measured gain and output power versus input power, (**b**) Base voltage and collector current measurement results based on input power.

Finally, the IP1dB gain of the proposed VGLNA is determined by the steps described in Figure 7 with a measured range of V_{b0} shown in Figure 10b thanks to a fixed-bias prototype. The operation of three gain modes with respect to three different V_{b0} is shown in Figure 11a. It can be seen that IP1dB is −8 dBm, −4 dBm and −1.5 dBm with V_{b0} of 858 mV, 824 mV, and 810 mV, respectively, and it is confirmed that VGLNA using the ADB circuit operates with an extended IP1dB of 6.5 dB as compared to a counterpart with fixed V_{b0} of 858 mV.

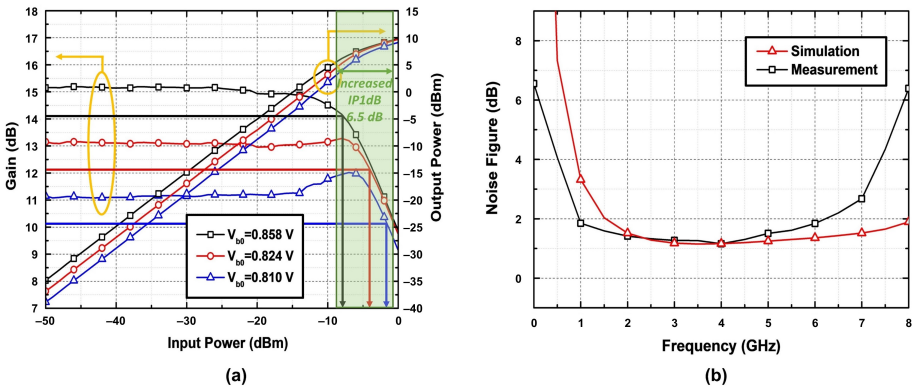

Figure 11. (**a**) IP1dB gain based on fixed-bias circuit operations, (**b**) measured noise figure.

4.3. Noise Figure

The noise figure is a very important aspect when assess an LNA design. In addition of JFET and the diode components, the noise figure performance of the proposed design is apparently degraded as compared to the single-BJT LNA. Applying the same supplying voltages, the VGLNA exhibits a measured NF of 1.8 dB at 6 GHz as shown in Figure 11b, which is in a good agreement with the simulated one. It is also noted that the lowest NF is not recorded at the target frequency because the input matching network is designed at the intermediate impedance in order to provide a good balance between NF and power performance.

5. Conclusions

In this paper, a variable-gain single-stage LNA is realized successfully for radar-detection applications, aiming at increasing the IP1dB of the high and fixed gain LNA one. The proposed LNA deploys a novel ADB circuit to produce a biasing voltage for BJT. This operation is automatic, providing a high gain at a low-power signal and a lower gain as the signal grows. The operation is verified, showing that IP1dB is extended by 6 dB as the input power increases from −50 dBm to 0 dBm. Compared to the common fixed gain LNA, the proposed VGLNA has the clear advantage of not only achieving a high gain at a low-power signal but having a wider linear processing region. With this ADB deployment, the VGLNA exhibits a compact size of 23.6 mm × 28.9 mm and a low NF of 1.8 dB, which is suitable for practical radar applications. A comparison among the state-of-the-art designs is summarized in Table 2. For an accurate comparison, three figures of merit (FOMs) are used as defined in Equations (12)–(14), which are presented [18]. The proposed VGLNA has the highest FOM2 and FOM3.

$$\text{FOM1}[dB/mW] = \frac{\text{Gain}[dB]}{\text{P}_{\text{DC}}[mW]} \tag{12}$$

$$\text{FOM2}[mW^{-1}] = \frac{\text{Gain}[abs]}{(\text{NF-1})[abs] \cdot \text{P}_{\text{DC}}[mW]} \tag{13}$$

$$\text{FOM3}[-] = \frac{\text{Gain}[abs] \cdot \text{IP1dB}[mW] \cdot \text{f}_{\text{c}}[GHz]}{(\text{NF-1})[abs] \cdot \text{P}_{\text{DC}}[mW]} \tag{14}$$

Table 2. Performance comparison with other state-of-the-art works.

Ref.	This Work	[7]	[8]	[12]	[19]
Center Freq. (GHz)	**6**	73.5	60	77.5	9.25
Gain (dB)	**15.2**	14	18.9	16	20.7
NF (dB)	**1.8**	N/A	6.06	10.5	3.26
IP1dB (dBm)	**−1.5**	N/A	−11.2	−28	−5
P_{DC} (mW)	**39.6**	36	45	57	75
FOM1 (dB/mW)	**0.38**	0.39	0.42	0.28	0.28
FOM2 (1/mW)	**0.28**	N/A	0.06	0.01	0.13
FOM3 (−)	**1.2**	N/A	0.29	0.001	0.38
VGA Method	**ADB**	Current Steering	Digital	ADB	Digital
Techn.	**Discrete Circuit**	90 nm CMOS	65 nm CMOS	65 nm CMOS	55 nm CMOS

Author Contributions: Conceptualization, H.N., D.-A.N. and Y.K.; methodology, H.N. and D.-A.N.; software, H.N. and D.-A.N.; validation, H.N., Y.K., D.-A.N. and C.S.; formal analysis, D.-A.N. and Y.K.; investigation, H.N., D.-A.N. and Y.K. resources, C.S.; data curation, H.N. and Y.K.; writing—original draft preparation, H.N., D.-A.N. and Y.K. writing—review and editing, Y.K. and C.S.; visualization, H.N. and D.-A.N.; supervision, Y.K. and C.S.; project administration, Y.K. and C.S.; funding acquisition, C.S. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by the National Research Foundation of Korea (NRF) Grant funded by the Korea government (Ministry of Science and ICT (MSIT)) under Grant 2017R1A5A1015596.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Skolnik, M.I. *Introduction to Radar System*; McGraw-Hill Education: New York, NY, USA, 2002.
2. Lacomme, P.; Marchais, J.C.; Hardange, J.P.; Normant, E. *Air and Spaceborne Radar Systems*; An Introduction; SPIE: Philadelphia, PA, USA, 2001.
3. Kuo, W.-M.; Liang, Q.; Cressler, J.D.; Mitchell, M.A. An X-band SiGe LNA with 1.36 dB mean noise figure for monolithic phased array transmit/receive radar modules. In Proceedings of the IEEE Radio Frequency Integrated Circuits Symposium (RFIC), San Francisco, CA, USA, 11–13 June 2006.
4. Chen, Z.; Zheng, T.; Luo, J. Octopus: A practical and versatile wideband MIMO sensing platform. In Proceedings of the 27th Annual International Conference on Mobile Computing and Networking (MobiCom), New Orleans, LA, USA, 25–29 October 2021.
5. Ding, R.; Jin, H.; Xiang, D.; Wang, X.; Zhang, Y.; Shen, D.; Su, L.; Hao, W.; Tao, M.; Wang, L.; et al. Soil Moisture Sensing with UAV-Mounted IR-UWB Radar and Deep Learning. *Proc. ACM Interact. Mob. Wearable Ubiquitous Technol.* **2023**, *7*, 1–25. [CrossRef]
6. Zhao, R.; Woodford, T.; Wei, T.; Qian, K.; Zhang, X. M-cube: A millimeter-wave massive MIMO software radio. In Proceedings of the 26th Annual International Conference on Mobile Computing and Networking (MobiCom), London, UK, 21–25 September 2020.
7. Kuo, C.-C.; Tsai, Z.-M.; Tsai, J.-H.; Wang, H. A 71–76 GHz CMOS variable gain amplifier using current steering technique. In Proceedings of the IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Atlanta, GA, USA, 15–17 June 2008.
8. Kao, K.-Y.; Lu, D.-R.; Kao, J.-C.; Lin, K.-Y. A 60 GHz variable gain low-noise amplifier with low phase variation. In Proceedings of the International Symposium Radio-Frequency Integration Technology, Taipei, Taiwan, 24–26 August 2016.
9. Liu, H.; Zhu, X.; Boon, C.C.; He, X. Cell-based variable-gain amplifiers with accurate dB-linear characteristic in 0.18 µm CMOS technology. *IEEE J. Solid-State Circuits* **2015**, *50*, 586–596. [CrossRef]
10. Hsieh, Y.-K.; Kuo, J.-L.; Wang, H.; Lu, L.-H. A 60 GHz broadband low-noise amplifier with variable-gain control in 65 nm CMOS. *IEEE Microw. Wirel. Compon. Lett.* **2011**, *21*, 610–612. [CrossRef]
11. Min B.-W.; Rebeiz, G.M. Ka-Band SiGe HBT low phase imbalance differential 3-bit variable gain LNA. *IEEE Microw. Wirel. Compon. Lett.* **2008**, *18*, 272–274. [CrossRef]
12. Jang, J.; Oh, J.; Kim, C.; Hong, S. A 79-GHz adaptive–gain and low noise UWB radar receiver front-end in 65-nm CMOS. *IEEE Trans. Microw. Theory Technol.* **2016**, *64*, 859–867. [CrossRef]
13. Liu, C.; Yan, Y.-P.; Goh, W.-L.; Xiong, Y.-Z.; Zhang, L.-J.; Madihian, M. A 5-Gb/s automatic gain control amplifier with temperature compensation. *IEEE J. Solid-State Circuits* **2012**, *47*, 1323–1333. [CrossRef]
14. Vidkjaer, J. *RF-Circuits*; Class Notes for the Course: RF Communication; 2000. Available online: https://dokumen.tips/documents/rf-communication-2-chap5-power-and-nonlinear-rf-amplifiers-rf-communication.html?page=1 (accessed on 25 April 2023).
15. Nguyen, D.-A.; Seo, C. A compact and high-efficiency design of 0.915/2.45 GHz dual-band shunt-diode rectifier for wireless power transfer. *IEEE Microw. Wirel. Compon. Lett.* **2022**, *32*, 915–918. [CrossRef]
16. He, Z.; Lin, H.; Liu, C. A novel class-C rectifier with high efficiency for wireless power transmission. *IEEE Microw. Wirel. Compon. Lett.* **2020**, *30*, 1197–1200. [CrossRef]
17. Floyd, T.L. *Electronic Devices: Electron Flow Version*, 9th ed.; Prentice Hall: Hoboken, NJ, USA, 2011.
18. Linten, D.; Thijs, S.; Natarajan, M.I.; Wambacq, P.; Jeamsaksiri, W.; Ramos, J.; Mercha, A.; Jenei, S.; Donnay, S.; Decoutere, S. A 5-GHz fully integrated ESD-protected low-noise amplifier in 90-nm RF CMOS. *IEEE J. Solid-State Circuits* **2005**, *40*, 1434–1442. [CrossRef]
19. Gao, H.; Li, N.; Li, M.; Wang, S.; Zhang, Z.; Kuan, Y.C.; Yu, X.; Gu, Q.J.; Xu, Z. A 6.5-12 GHz balanced variable gain low-noise amplifier with frequency-selective non-foster gain equalization technique. In Proceedings of the IEEE/MTT-S International Microwave Symposium, Los Angeles, CA, USA, 4–6 August 2020.