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Implementation of Buck DC-DC Converter as Built-In Chaos Generator for Secure IoT

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Abstract: Resource-constrained but widely deployed IoT devices require a new approach to ensure secure and reliable communications. That is why, in recent years, the paramount effort has been applied in lightweight cryptography. Because of its unpredictable nature, chaos is regarded as a potential candidate in cryptographic applications. Chaos mode of operation is observed not only in deliberately designed oscillators but also in switching DC-DC converters, which are part of almost every embedded design. The use of a built-in chaos source may improve performance, energy consumption, PCB area, and cost of IoT devices. In this research, the regions of robust chaos were identified using numerical analysis, and the performance of a real buck DC-DC converter under peak-current-mode control was studied experimentally. It was shown that a compensating ramp acts as a switch between different operating regimes. Despite minor performance degradation, chaos mode can be used for secure communications in IoT networks.

Keywords: bifurcations; chaos; DC-DC converters; nonlinear dynamics; voltage ripples

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1. Introduction

Interconnected heterogeneous devices form the so-called Internet of Things (IoT), and wireless sensor networks (WSN) have already become ubiquitous in different areas of human life, starting with industrial applications and ending with wearable gadgets. The terms IoT and WSN are often used interchangeably; in most cases, it is extremely hard to distinguish between them. Both concepts have the same layered structure: application, middleware, network or communication, and perception layers [1]. A low-energy embedded device or node containing either sensors or actuators is located at the perception layer. Nowadays, many IoT ecosystems, including sensor nodes, base stations (gateways), data storage and management cloud services, and software for smartphones and desktop computers, are commercially available. The main benefit of WSN use is up-to-date information about parameters of interest ranging from the temperature in refrigerators to CO_2 concentration in an office or an athlete's heart rate. Further analysis of the collected information allows one to take action and keep the parameter of interest within acceptable margins. At the perceptional layer of any WSN ecosystem is a sensor node [1], which, in most cases, is a low-cost device with limited energy and performance. Physical dimensions and weight are other factors that determine the low performance of a sensor node. Limited computational resources of a node complicate or eliminate the application of conventional security measures [2]. As a result, WSNs become vulnerable to different kinds of security risks. According to [2], IoT threats can be classified into three groups:

(1) Hardware trojans. These are modifications to the electronic circuit during the production stage at some subsidiary manufacturing companies. Results of the malicious inclusions in the original IC can range from the leakage of sensitive information to the complete breakdown of an IoT device;

(2) Software threats. Typical software attacks include using vulnerable IoT devices to form a botnet by installing a malicious program on the device. Created botnet can be further exploited in denial of service (DoS) or distributed DoS attacks. Also, IoT devices may be subjected to different kinds of spoofing;
(3) Data in transit (communications layer of the IoT network). These threats are mainly associated with eavesdropping/sniffing, which becomes a simple task in the case of non-encrypted data. Moreover, in the case of replay and man-in-the-middle attacks, an attacker is located between the transmitter and receiver and can either capture packets of information and replay them later or alter the data being sent.

A comprehensive literature review of IoT security and threats-related articles was presented in [3], where the lack of encryption is also mentioned as important but not the only factor violating the security of IoT networks.

Among all the layers of the IoT system, the perception or edge layer is the most resource-restricted and, therefore, most vulnerable. Another risk arises from the fact that many nodes can be located in distinct areas, allowing an attacker to capture the node and perform a side-channel attack. The technique uses side signals like the consumed current of the node circuit to determine the encryption secret keys [4]. A detailed example of such an attack on the lightweight cryptography algorithm SIMON12 implemented in FPGA was presented in [5]. It is evident that data collected by a sensor node, stored in it for some time, and later sent over a wireless communication channel must be protected by means of appropriate encryption techniques. Moreover, proper authentication techniques must be implemented even in low-end embedded devices to ensure protection against malicious/modified IoT devices operating in the network.

The implementation of chaos as a potential solution to resource-constrained communication devices has been studied extensively in recent decades [6]. There are two methods of using chaos in data protection: as the source of a random number generator for data encryption [7] and secure modulation schemes, as presented in [8]. Both methods employ a chaos oscillator, either in the form of an analog circuit or a digital version that can be implemented on a processor or FPGA [9]. Digital chaotic signals are obtained using chaotic maps or systems of differential equations that mimic some real-world electronic oscillator. Even the simplest chaos oscillators require at least three reactive and one nonlinear element accompanied by some resistors. Operational amplifiers are often used in various proposed chaos oscillators. It means an extra PCB area and energy is required to implement chaos-based secure schemes in the IoT device. However, the chaos phenomenon was also observed in the switch-mode DC-DC converters found in every embedded device. Thus far, the chaos-mode operation in switching voltage converters was considered unwanted, causing performance degradation and even leading to failure [10]. Nevertheless, benefits from incorporating existing sources of randomness initiate the need for more profound research of chaotic regimes in switching DC-DC converters.

The main goal of this research is to estimate the performance of a switching buck DC-DC converter operating in a chaotic mode. Output voltage ripple and efficiency were chosen as the main characterizing parameters of the working converter. Initially, in-depth numerical analysis was performed to determine the conditions for robust chaos. Input voltage, load current, and reference current in a feedback loop were chosen as the bifurcation parameters. After that, the validity of the mathematical model was verified in an experimental study, together with the measurements of the converter's efficiency and output voltage ripples.

This paper is organized as follows. Section 2 is devoted to the numerical analysis of the buck DC-DC switching converter under peak-current-mode control to determine the regions of chaos-mode operation. Results of the experimental verification of the converter in different modes of operation are presented in Section 3. The summary and conclusions are provided in Section 4.

2. Buck Converter Model and Numerical Analysis

2.1. The Buck Converter under Current-Mode Control

Three basic types of switching voltage converters formed of two semiconductor switches, a single inductor, and a capacitor are buck (step-down), boost (step-up), and buck-boost. These converters allow one to achieve almost any voltage level needed by the design. This study is devoted to the synchronous buck converter under peak-current-mode control (PCMC). The power stage circuit diagram and the main control blocks are shown in Figure 1. It was determined that such a converter operates in chaotic mode when the duty cycle exceeds 50% with an excluded compensation ramp signal [10]. The research was performed with a converter operating in a continuous current mode that determines the division of one switching cycle into two subintervals with the corresponding subcircuits defined by combinations of switching elements. The chaotic mode of operation is assumed to be something dangerous to the converter and is avoided in practical applications. However, this particular regime is a built-in chaos oscillator that can be employed for data encryption. The main concern is the reliability and safety of the converter working in chaotic mode. Another problem is the degradation of the main converter parameters, namely output voltage ripple, and efficiency.

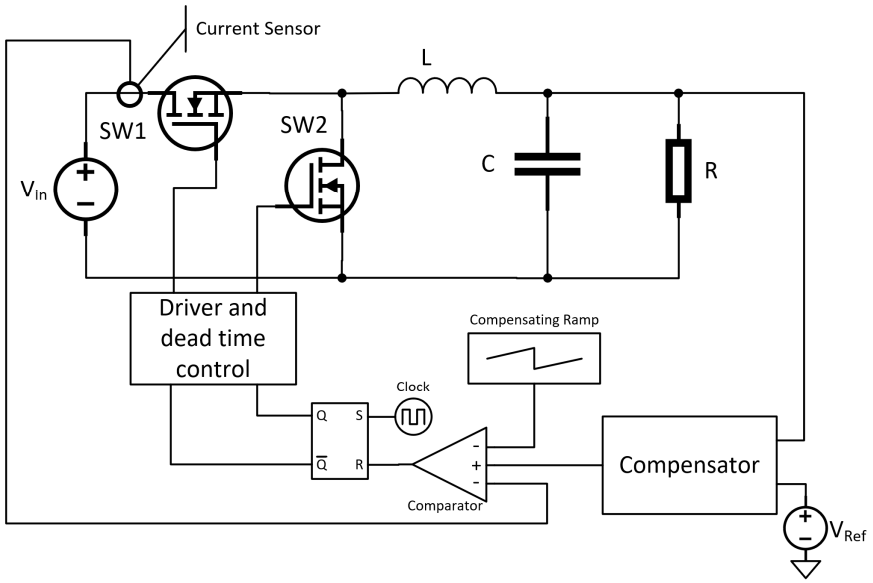


Figure 1. Block diagram of the buck converter under peak-current-mode control.

2.2. The Discrete-Time Model and Numerical Simulations

2.2.1. Discrete-Time Model of the Buck Converter

The numerical analysis of the dynamics of the converter under study requires derivation of the model, which can predict the nonlinear behavior of the circuit.

The converter's operation is determined by two configurations, defined by the arrangement of the respective combinations of switches (SW_1 = ON, SW_2 = OFF and SW_1 = OFF, SW_2 = ON). The different system of differential equations describes each circuit configuration.

$$t_1 : \ SW_1 = \text{ON}, \ SW_2 = \text{OFF} \begin{cases} \frac{di_L}{dt} = -\frac{1}{L} v_C + \frac{1}{L} V_{in}, \\ \frac{dv_C}{dt} = \frac{1}{C} i_L - \frac{1}{RC} v_C, \end{cases} \tag{1}$$

$$t_2 : \ SW_1 = \text{OFF}, \ SW_2 = \text{ON} \begin{cases} \frac{di_L}{dt} = -\frac{1}{L} v_C, \\ \frac{dv_C}{dt} = \frac{1}{C} i_L - \frac{1}{RC} v_C, \end{cases} \tag{2}$$

where i_L is the current through the inductor L, v_C is the voltage across the output capacitor, and V_{in} is the input DC voltage. The location of the L, C, and R components in the schematic of the buck converter is shown in Figure 1.

The main control signals defining the fast–scale dynamics of the current loop are shown in Figure 2.

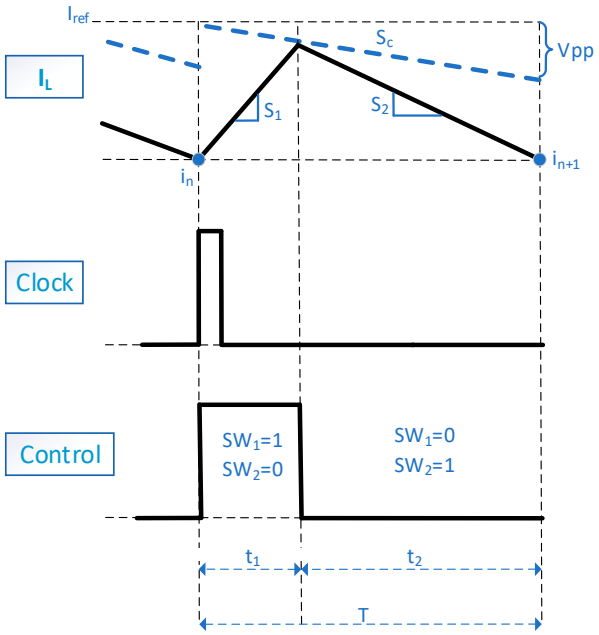


Figure 2. Control signals of the buck converter under PCMC.

Every period, clock signals change the position of switches, turning SW_1 ON and SW_2 OFF. This forces the inductor current i_L to rise with the slope $S_1 = (V_{in} - V_{out})/L$. The reference current I_{ref} in conjunction with the compensation ramp with the slope $S_c = V_{pp}/T$ defines the value of the switching threshold of the comparator. When the i_L reaches the value $I_{ref} - S_c \times t_1$, the comparator output signal forces the SW_1 to turn OFF and SW_2 to turn ON. This leads to the falling of the inductor current with the slope $S_2 = (-V_{out})/L$ until the next clock signal toggles the position of both switches. The buck converter operates in continuous conduction mode (CCM), where the instantaneous current through the inductor is always above zero, and the switching cycle consists of two subintervals, namely t_1 and t_2.

Solving systems of differential equations is a time- and resource-demanding task, especially when it involves analyzing millions of periods. Thus, the general practice is obtaining discrete-time models, enabling analysis simplification and significantly decreasing computation times. In this study, we used a modification of the iterative map obtained in [10], supplementing it with the compensation ramp always present in all practical PCMC converters.

It is assumed that in the case of the high-output capacitance value, the output voltage ripples can be neglected, and the output voltage $V_{out} = v_n$ (capacitor voltage) is almost constant. The inductor current rises linearly, and it is possible to express the rise time during the switching cycle n from Equation (1):

$$t_1 = \frac{I_{ref} - i_n}{\frac{V_{in} - v_n}{L} + S_c}, \tag{3}$$

where t_1 is SW_1 ON time, i_n is the inductor current at the beginning of the nth switching cycle, I_{ref} is the reference signal of the current loop, and S_C is the slope of the compensating ramp.

When $t_1 \geq T$, during the entire switching period, SW_1 conducts the current, and the discrete model of the buck converter is represented as follows:

$$i_{n+1} = e^{\alpha T}(c_1 \cos(\beta T) + c_2 \sin(\beta T)) + \frac{V_{in}}{R} \tag{4}$$

$$v_{n+1} = e^{\alpha T}(c_3\cos(\beta T) + c_4\sin(\beta T)) + V_{in}, \quad (5)$$

where

$$\alpha = -\frac{1}{2RC},\ \beta = \sqrt{\frac{1}{LC} - \frac{1}{4R^2C^2}},$$

$$c_1 = i_n - \frac{V_{in}}{R},\quad c_2 = \frac{1}{\beta}\left[\frac{V_{in} - v_n}{L} - \alpha\left(i_n - \frac{V_{in}}{R}\right)\right],$$

$$c_3 = v_n - V_{in},\ c_4 = \frac{\alpha}{\beta}(v_n + V_{in}) + \frac{i_n}{\beta C}.$$

When $t_1 < T$, switch SW_1 is in OFF during the $t_2 = T - t_1$ interval, and it is possible to obtain the discrete iterative mapping model of the converter:

$$i_{n+1} = e^{\alpha(t_2)}\lceil k_1\cos(\beta(T - t_2)) + k_2\sin(\beta(t_2))\rceil, \quad (6)$$

$$v_{n+1} = -Le^{\alpha(t_2)}[(k_1\alpha + k_2\beta)\cos(\beta(t_2)) + (k_2\alpha - k_1\beta)\sin(\beta(t_2))], \quad (7)$$

where

$$k_1 = I_{ref}, k_2 = -\frac{1}{\beta L}\left(v_C(0) + \alpha L I_{ref}\right),$$

$$v_C(0) = e^{\alpha t_1}(c_3\cos(\beta t_1) + c_4\sin(\beta t_1)) + V_{in}.$$

As a result, Equations (3)–(7) form the complete two-dimensional discrete-time model of the buck converter under peak-current-mode control with compensating ramp.

2.2.2. Numerical Simulation Results

The numerical analysis aims to detect the potential regions of nonlinear oscillations of the converter in the parameter space and identify the possible pathways to chaos.

The investigation is based on constructing the two-parameter bifurcation diagram (map), defining the periodicity of the regime. As the compensation ramp is introduced to eliminate all subharmonic oscillations and ensure the stable operation of the converter, Sc = 0 in this study makes the system as unstable as possible. The parameters of the buck converter under test, corresponding to the practically viable values of the commonly used devices, are shown in Table 1.

Table 1. Parameters of the buck converter under test.

Parameter	Values
V_{in}	6 . . . 12 V
I_{ref}	2 . . . 4 A
R	2 Ω
L	2.2 μH
C	391 μF
f	0.5 MHz
S_c	0 V/s

First, we introduce the bifurcation map in the $I_{ref} - V_{in}$ plane in Figure 3.

The obtained map demonstrates that for large values of the input voltage, the system exhibits stable period-1 operation for the whole range of the reference current values. As we decrease the input voltage, the period-1 region shrinks, and the transition to period-2 oscillations and chaos can be observed. A straight line from point (2.9; 6) to (4; 8.3) defines the border or the chaotic region. Thus, any combination of the I_{ref} and V_{in}, lying to the right of the defined borderline, ensures chaotic oscillations of the converter. Two different chaotic regions with distinct properties examined in the following explanation are marked as Ch1 and Ch2.

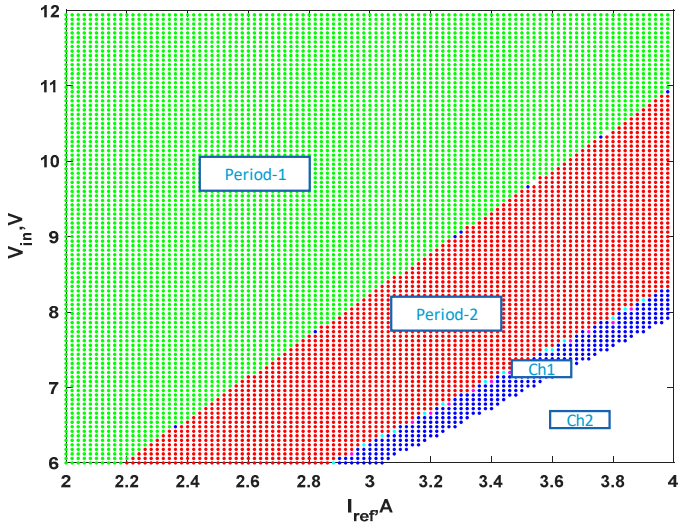
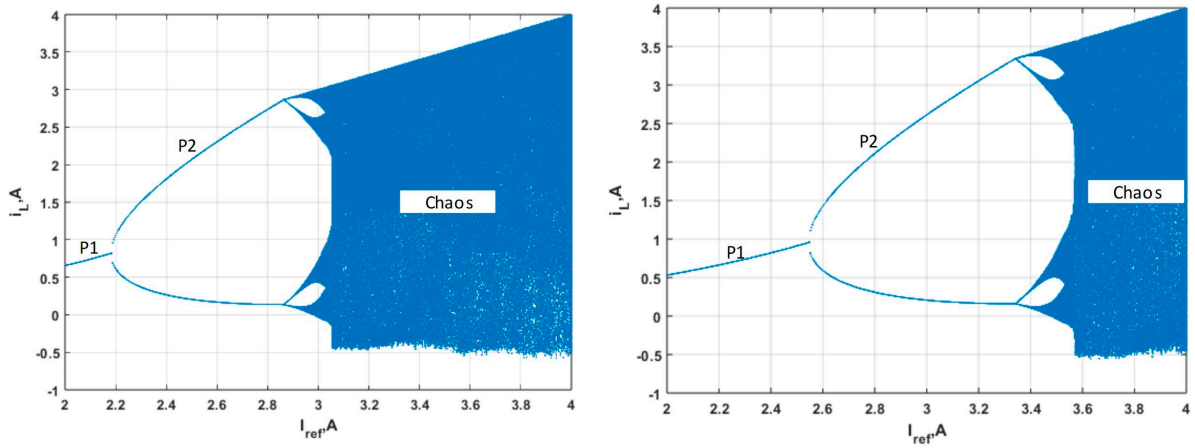


Figure 3. The bifurcation map of the buck converter without compensation ramp. V_{in} = 6–12 V; I_{ref} = 2–4 A; R = 2 Ω; L = 2.2 µH, C = 391 µF; f = 0.5 MHz, S_c = 0 V/s.

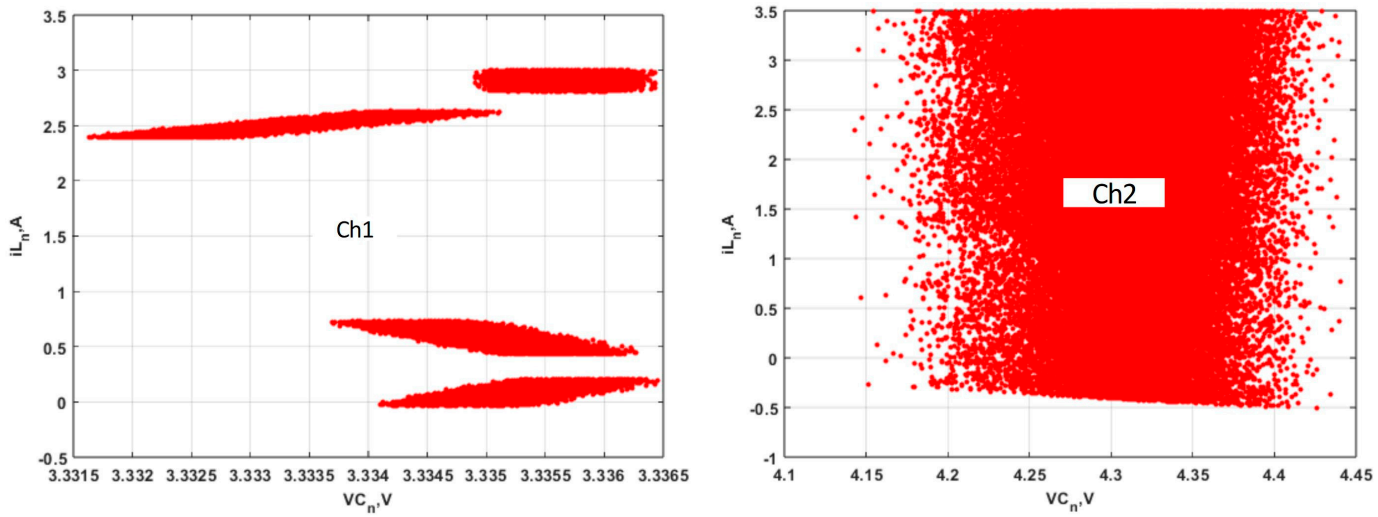
It is necessary to construct the bifurcation diagrams and obtain the iterative maps showing the shape of attractors to ascertain that the dynamics of the converter ensures robust chaos in the defined region.

As the cross-section of the map, two bifurcation diagrams are obtained for V_{in} = 6 V and V_{in} = 7 V, which are shown in Figure 4. The main observation from both diagrams is the apparent transition from period-1 (P1) to period-2 (P2) regimes with the subsequent chaotization without the classical period-doubling cascade. No coexisting attractors or periodic windows can be identified, so the obtained chaotic mode is robust. One more distinguishing feature of the diagrams is that there are no one-piece chaotic attractors for I_{ref} = (2.85–3.05) for V_{in} = 6 V and I_{ref} = (3.35–3.58) for V_{in} = 7 V. While being chaotic, the operation is still forming around four distinct regions. This is demonstrated better in Figure 5a, where the discrete-time attractor Ch1 is shown. This kind of chaotic motion has low application potential in practice, as the regime will look like subharmonic oscillations. Additionally, the range of voltages on the x-axis indicates that it would be challenging to differentiate between two closely positioned values, especially when using standard off-the-shelf ADCs. Another full-scale chaotic attractor for I_{ref} = 3.5 A is demonstrated in Figure 5b, showing a practically viable source of chaotic oscillations.



(**a**) (**b**)

Figure 4. The bifurcation diagrams for (**a**) V_{in} = 6 V and (**b**) V_{in} = 7 V (I_{ref} = 2–4 A; R = 2 Ω; L = 2.2 µH, C = 391 µF; f = 0.5 MHz, S_c = 0 V/s). P1 stands for period-1 mode of operation, and P2 for period-2.



(**a**) (**b**)

Figure 5. Attractors for V_{in} = 6 V and (**a**) I_{ref} = 3 A and (**b**) I_{ref} = 3.5 A; for (**a**,**b**) R = 2 Ω; L = 2.2 μH, C = 391 μF; f = 0.5 MHz, S_c = 0 V/s.

Thus, returning to the reference bifurcation map in Figure 3, only the Ch2 region, represented by a one-piece wide chaotic attractor, is of practical importance.

2.2.3. The Effects of the Compensation Ramp

The compensation ramp is implemented in most modern DC-DC converter controllers as the tool for eliminating subharmonic oscillations. It was demonstrated in the previous subsection that it is possible to ensure the transition to chaos, varying V_{in} and I_{ref} values in the predicted parameter range. However, this leads to changes in the output voltage levels, affecting the load. Therefore, it is highly advantageous to incorporate a parameter that enables the transition between chaotic and non-chaotic modes of operation. The compensation ramp for the current-mode controlled converter is the most obvious choice. Thus, we fix the converter's parameters, including the V_{in} = 6 V, and obtain the bifurcation map, depicting the changes in the dynamics in the $I_{ref} - S_c$ plane (see Figure 6).

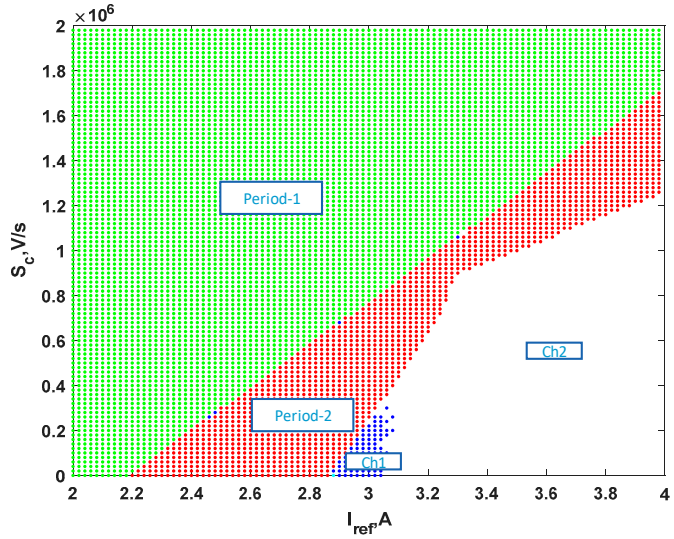


Figure 6. The bifurcation map of the buck converter with compensation ramp. V_{in} = 6 V; I_{ref} = 2–4 A; R = 2 Ω; L = 2.2 μH, C = 391 μF; f = 0.5 MHz, S_c = 0–2 × 10^6 V/s.

Like in the map in Figure 3, we can observe the region of period-1 operation and transition to small-scale (Ch1) or larger-scale (Ch2) chaotic attractors through the period-2 regime. We can see that the increase in the compensation ramp leads to the widening of the stable period-1 region. This is demonstrated by means of two bifurcation diagrams obtained for $S_c = 0.2 \times 10^6$ V/s and $S_c = 1 \times 10^{-6}$ V/s, shown in Figure 7. The increase in the S_c value also leads to a steeper transition from periodic to large chaotic mode without the formation of small-scale multi-piece chaotic attractors.

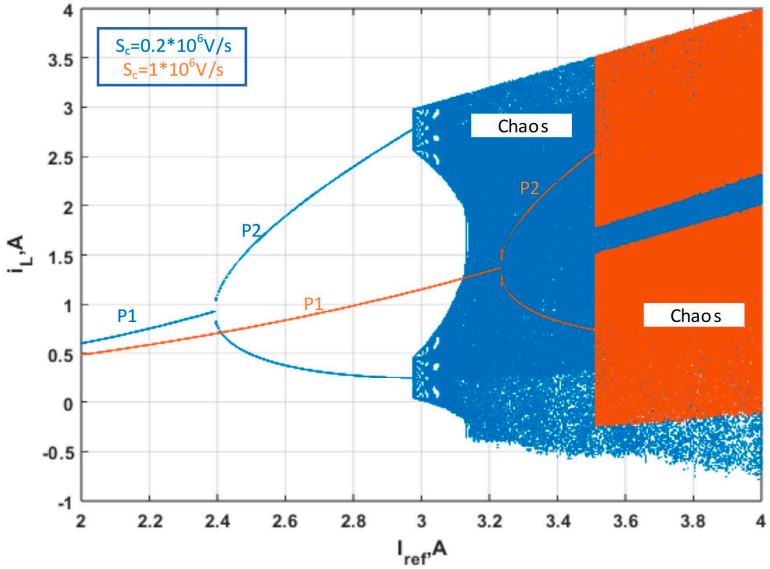


Figure 7. The bifurcation diagrams for $S_c = 0.2 \times 10^{-6}$ V/s and $S_c = 1 \times 10^6$ V/s. $V_{in} = 6$ V; $I_{ref} = 2$–4 A; $R = 2$ Ω; $L = 2.2$ µH, $C = 391$ µF; $f = 0.5$ MHz. P1 stands for period-1 mode of operation, P2 for period-2.

To ensure switching between chaotic and period-1 modes without affecting the output voltage, we should fix the value of I_{ref}, corresponding to the chaotic region without a ramp, and change the S_c. The exemplary bifurcation diagram for $I_{ref} = 3.4$ A, demonstrating the proposed approach, is shown in Figure 8.

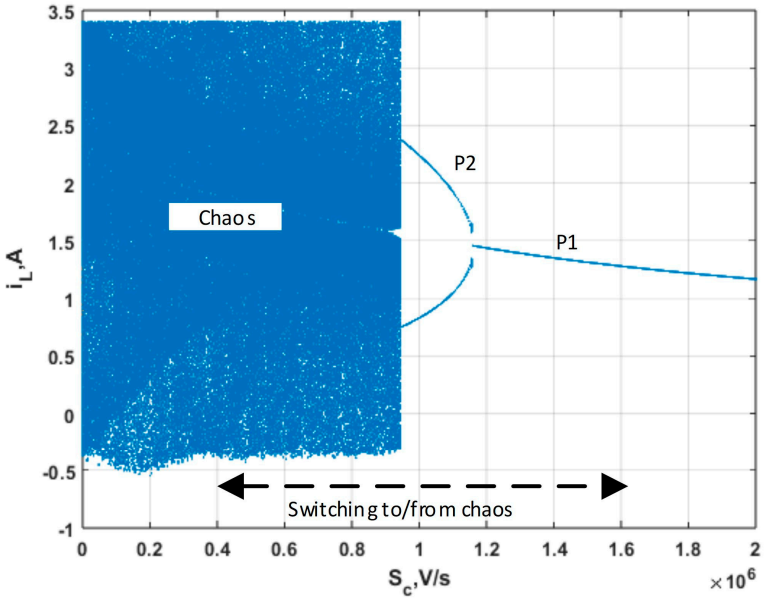


Figure 8. The bifurcation diagram for $I_{ref} = 3.4$ A. $V_{in} = 6$ V; $R = 2$ Ω; $L = 2.2$ µH, $C = 391$ µF; $f = 0.5$ MHz, $Sc = 0$–2×10^6 V/s. P1 stands for period-1 mode of operation, and P2 for period-2.

In this case, it is possible to implement switching between qualitatively different modes of operation, varying the value of S_c. For example, the transition from chaos to stable period-1 operation is ensured by changing S_c from 0.4×10^6 V/s to 1.6×10^6 V/s.

It should be noted that the obtained numerical results served as a reference for further experimental research given in the following sections, which allowed the investigation of the effects of the predicted regimes on the main parameters of the switching power converter.

3. Experimental Results and Analysis

After the numerical analysis, the laboratory measurements were performed. The main goals for the measurements were to detect regions of chaotic operation mode, study the influence of chaotic mode on the output voltage ripples and converter efficiency, as well as evaluate the use of a ramp generator signal for switching the converter from period-1 to chaotic mode and back, as it was shown in the numerical analysis.

The Microchip's CIP Hybrid Power Starter Kit was used for the laboratory measurements. This kit is a synchronous buck converter that can be configured in three different feedback loop modes using the PIC16F1779 hybrid microcontroller. The synchronous buck converter accepts input voltage from 6 V to 16 V, providing the maximum output power of 25 W with up to 8 A load. During the measurements, the CIP Hybrid Power Starter Kit was configured to operate in peak-current-mode control mode. The kit schematic in the PCMC configuration can be seen in Figure 9.

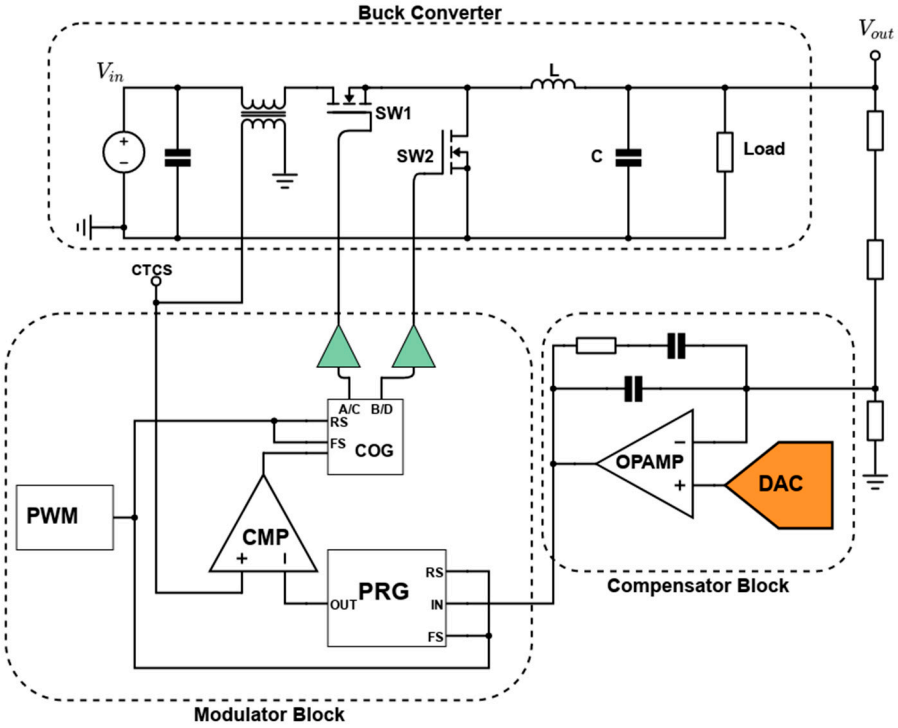


Figure 9. CIP Hybrid Power Starter kit in peak-current-mode control configuration.

Compared to the block diagram of the PCMC buck converter in Figure 1, the reference voltage V_{ref} was applied using a digital-to-analog converter (DAC) in the compensator. The current sensing transformer was used to obtain the current signal CTCS shown in Figure 9 for the modulator block. The clock signal, in turn, was provided by the PWM block.

To prevent the short-circuit state where both switches are "ON", the rising-edge dead time in the complementary output generator (COG) was set to 15 ns, and the falling-edge dead time was set to 60 ns. The programmable ramp generator (PRG) was turned off and bypassed to obtain a chaotic mode of operation.

3.1. Methodology

Measurements of the output voltage ripples and the current sensor signal were implemented to construct phase plots using the setup shown in Figure 10. The SMA connector was soldered in parallel to the output capacitor of the converter to minimize the effect of noise on the measurements of the output voltage ripples. Because the voltage ripples have a small amplitude compared to the output signal DC component, the ripple signal amplifier with a flat frequency response, wide band, and a gain of 16 was used for the measurements.

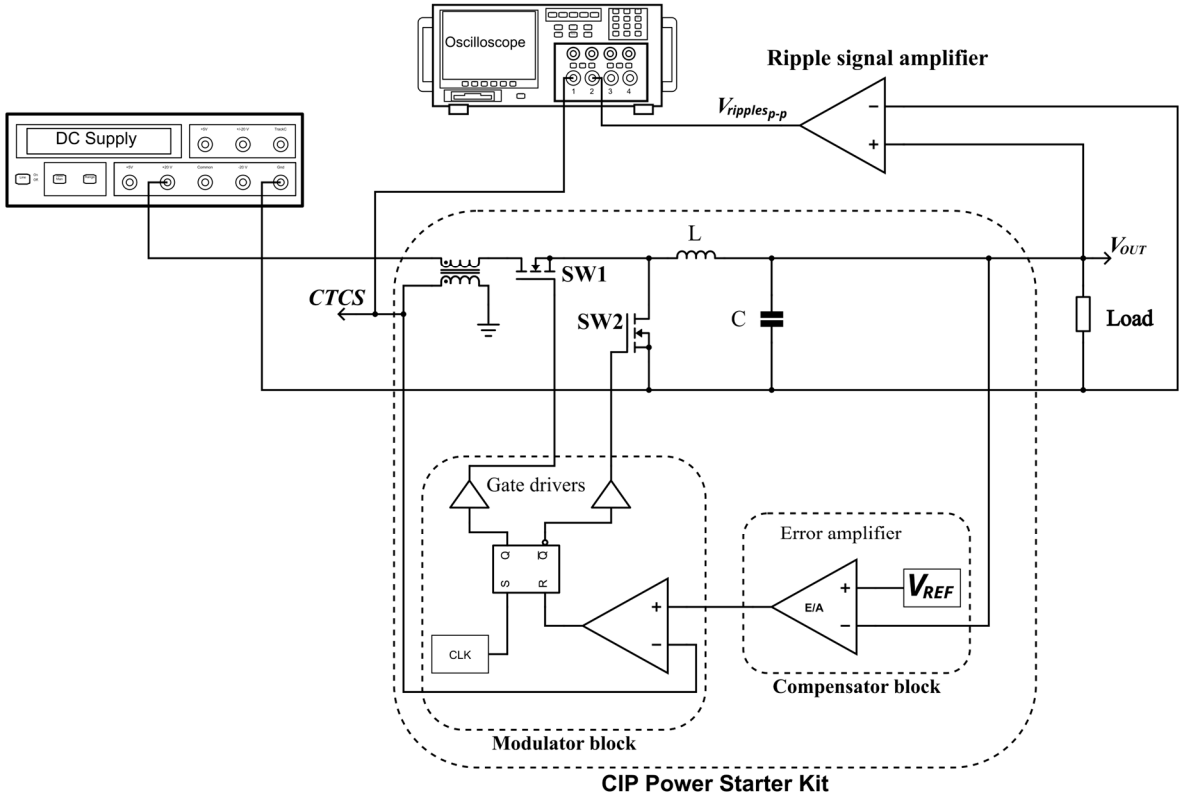


Figure 10. Output voltage ripple measurement setup.

The Analog Discovery Pro oscilloscope ensured signal acquisition with increased measurement accuracy. The average values of 500 acquisitions were calculated to obtain the average value of peak-to-peak output voltage ripples. After the signal data were obtained, MATLAB was used for noise filtering and constructing output voltage ripple waveforms, autocorrelation functions, and phase plots.

First, we provide a series of experiments to identify the possibilities of ensuring chaotic modes of operation in the buck converter under PCMC. The following parameters of the converter were used during the experiments: $f_{sw} = 500$ kHz; $R_{load} = 2\ \Omega$; $V_{in} = 8$ V; $L = 2.2$ µH; $C = 391$ µF.

To examine the converter's operation modes evolution in response to variations in the reference voltage V_{ref}, the phase plots can be constructed using the output voltage ripple signal ($V_{ripples}$) and high-side transistor current sensor signal (V_{CTCS}). The resulting phase plots for the reference voltages of 2.5 V, 3.0 V, 3.5 V, and 3.8 V are shown in Figures 11–14.

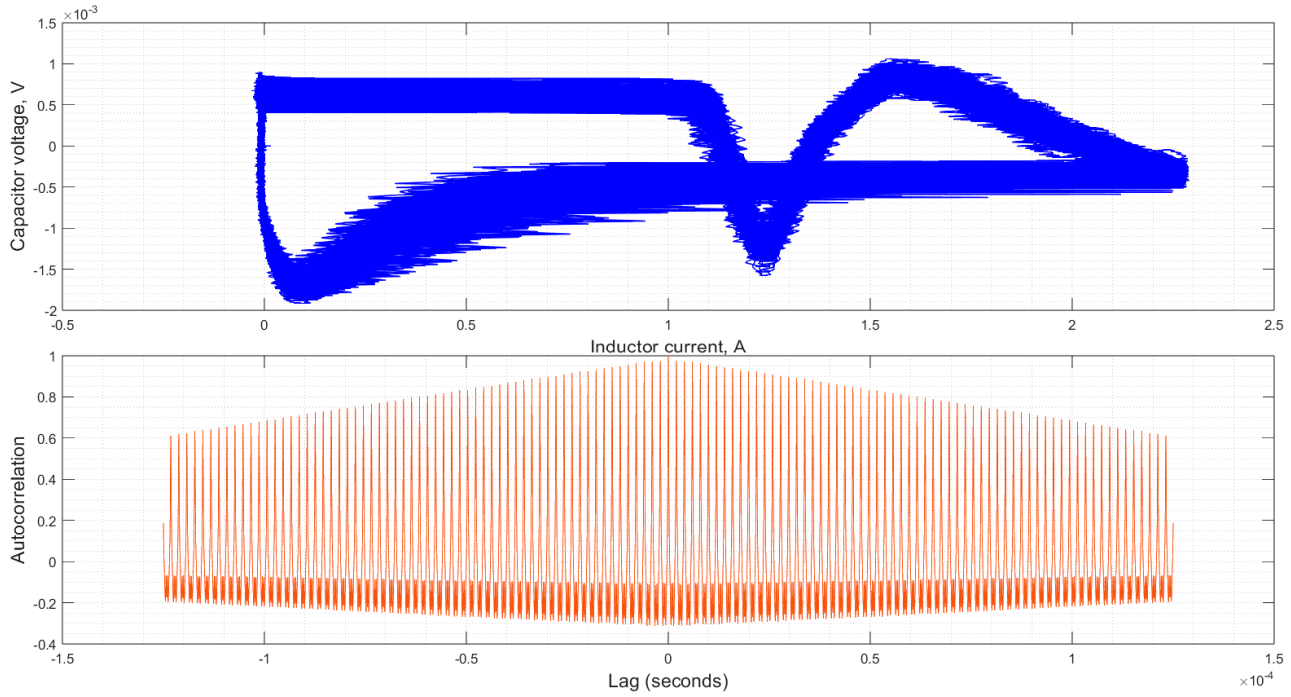


Figure 11. Phase plot and autocorrelation function of the output voltage ripple ($V_{ref} = 2.5$ V).

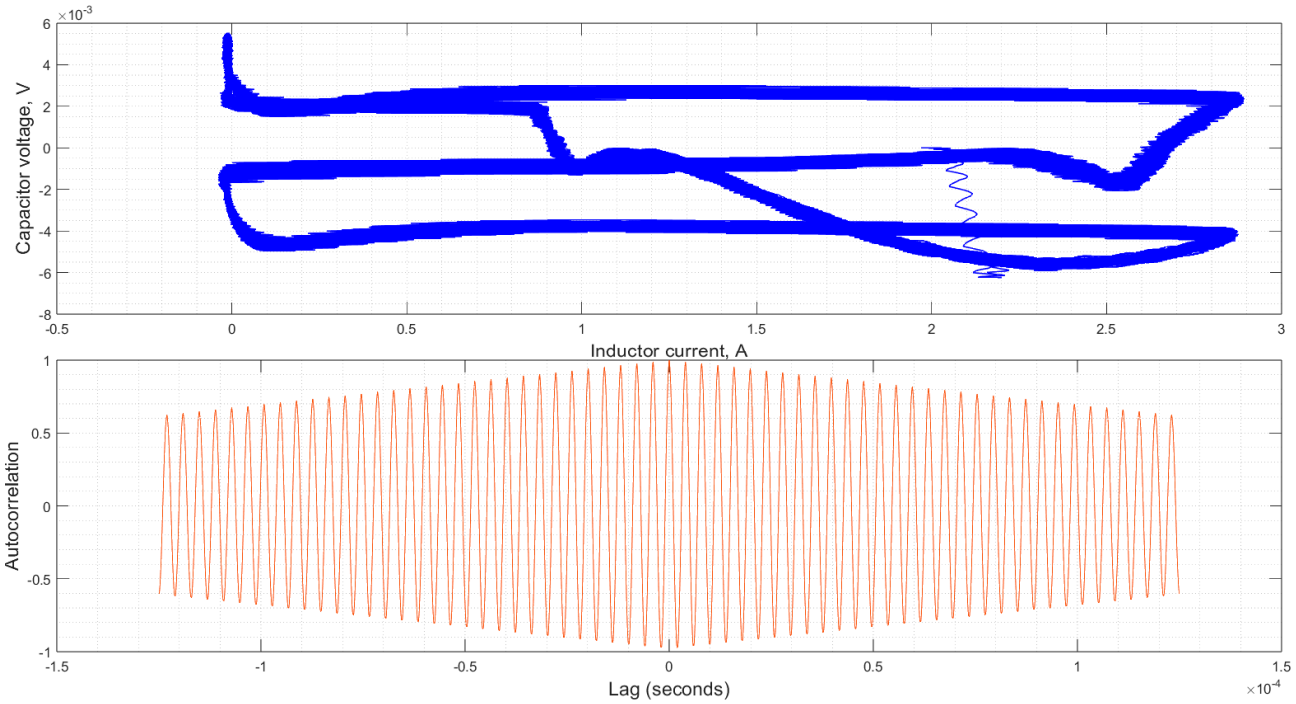


Figure 12. Phase plot and autocorrelation function of output voltage ripple ($V_{ref} = 3.0$ V).

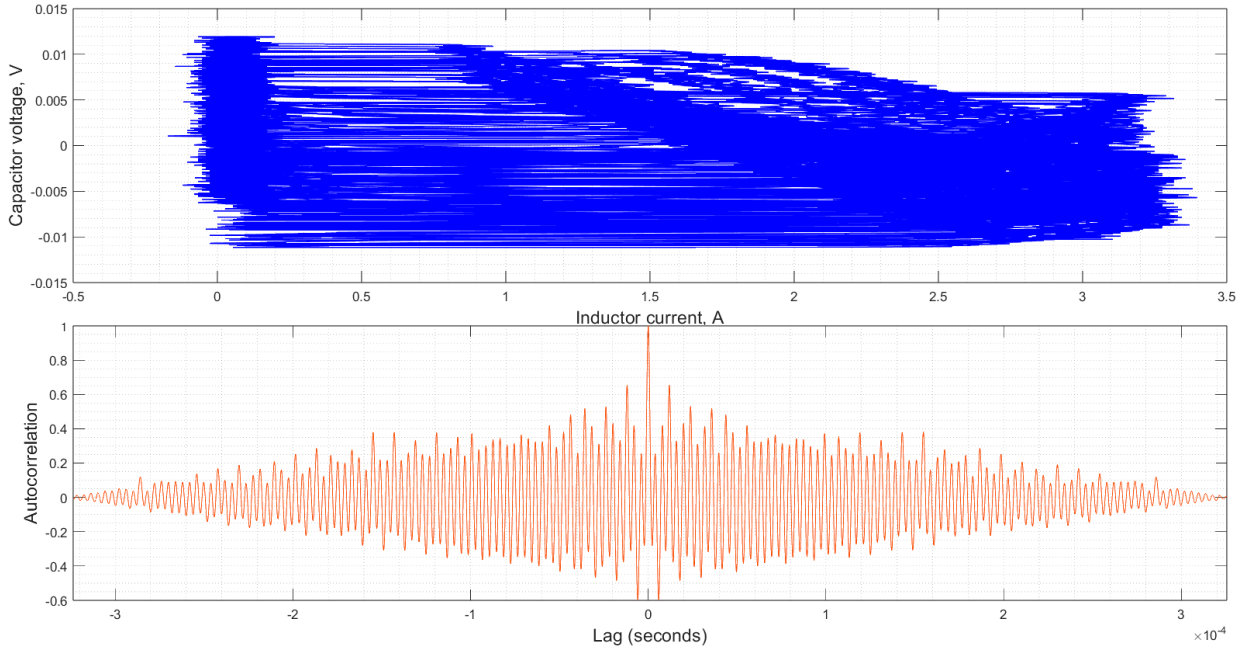


Figure 13. Phase plot and autocorrelation function of output voltage ripple ($V_{ref} = 3.5$ V).

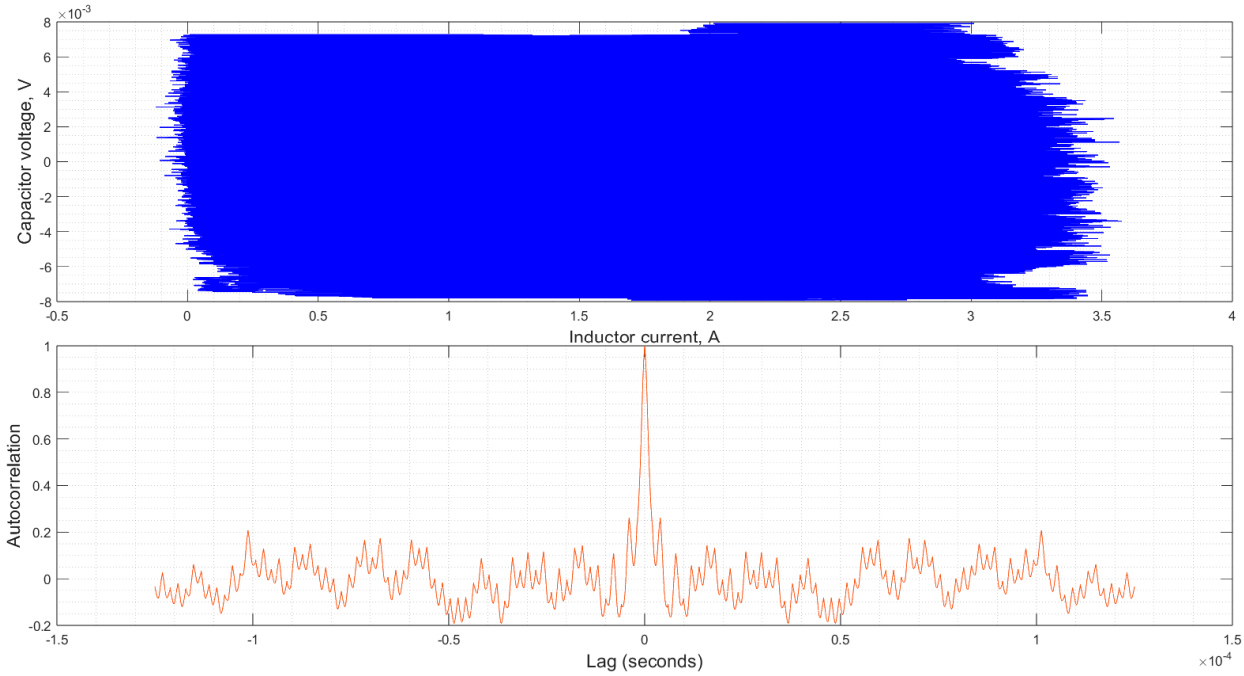


Figure 14. Phase plot and autocorrelation function of output voltage ripple ($V_{ref} = 3.8$ V).

Figures 11–14 reveal that the phase plot for period-1 operation mode in Figure 11 can be readily differentiated from the phase plot for period-2 mode in Figure 12, and the phase plot for period-2 mode can be distinguished from the phase plot for period-N mode in Figure 13. However, the differences between the phase plot for period-N mode in Figure 13 and the chaotic phase plot in Figure 14 are minor. Consequently, the autocorrelation function was employed to identify the operation mode.

In order to showcase the unique characteristics of each operation mode's autocorrelation functions and to make a comparison with the phase-plots-based approach, MATLAB was employed. The resulting phase plots and autocorrelation functions for the reference voltages of 2.5 V, 3.0 V, 3.5 V, and 3.8 V are shown in Figures 11–14.

Upon inspecting the autocorrelation function in Figure 11, decreasing amplitude peaks with a 2 µs period are evident, whereas in Figure 12, similar peaks with a 4 µs period can be discerned, indicating the period doubling. Analyzing the autocorrelation function in Figure 13, it is noticeable that the period of the peaks increased, accompanied by variations in peak amplitudes, which is characteristic of the period-N operation mode. In contrast, when analyzing the autocorrelation function in Figure 14, it is evident that the peaks exhibit significantly reduced amplitudes compared to the 0 s lag peak, indicating a negligible autocorrelation in the waveform and typifying the chaotic nature of the waveforms. Thus, the autocorrelation function appears to be a reliable tool for the apparent detection of periodic and chaotic modes.

The measurement arrangement depicted in Figure 15 was employed to assess the converter's efficiency. Two Instek GDM-8245 digital multimeters were utilized for measuring input and output currents, while the Analog Discovery Pro was used for measuring input and output voltage average values.

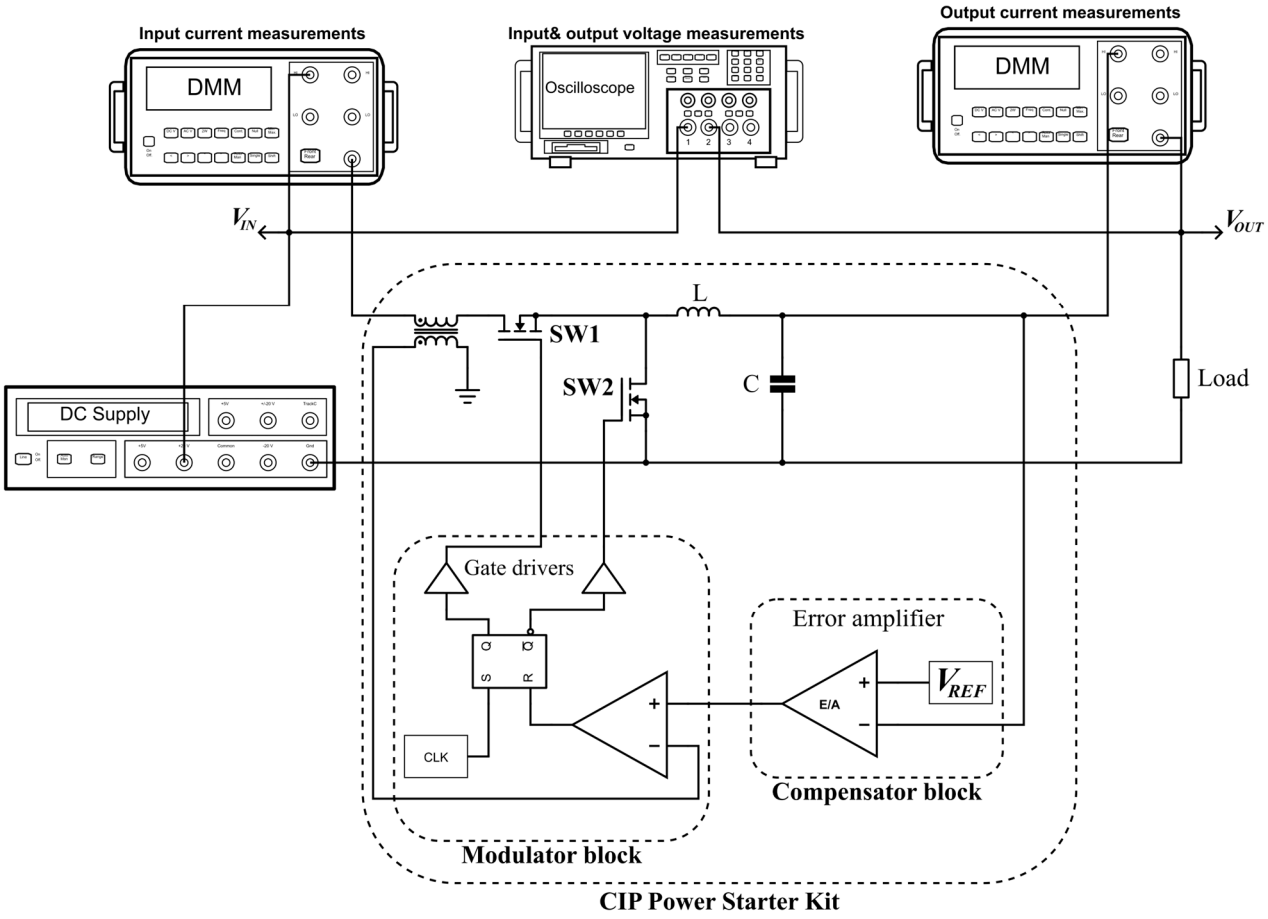


Figure 15. Efficiency measurement setup.

3.2. Effects on Output Voltage Ripples

3.2.1. $V_{in} - V_{ref}$ Measurements

First, we provide the experimental study on the effects of different modes of operation on the output voltage ripples of the converter, which is one of the main quantitative characteristics of the device.

From the inspection of the graph in Figure 16 and data from Table 2, it can be seen that the increase in V_{ref} results in the gradual transition from period-1 to a chaotic mode of operation. It can be concluded that the rise in V_{ref} results in the increase in the output voltage ripple amplitude and the expansion of operation mode boundaries with an increase in V_{in}.

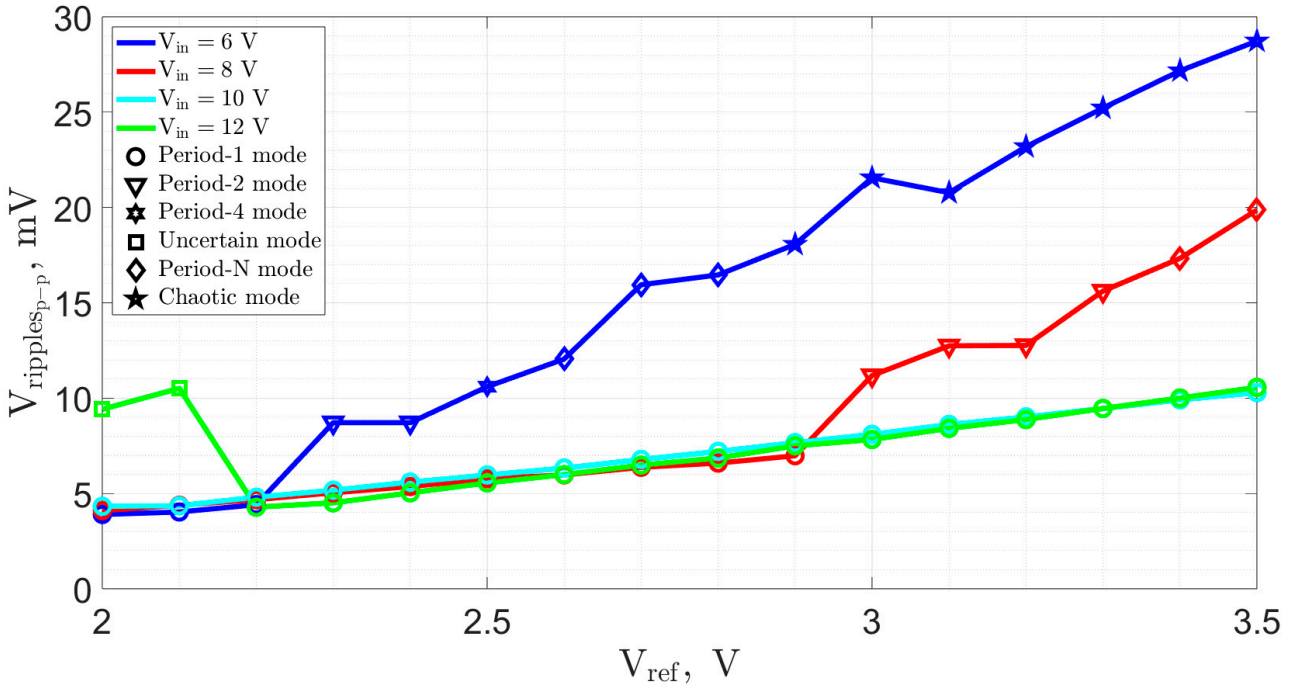


Figure 16. The dependence of output voltage ripples on $V_{in} - V_{ref}$ changes.

Table 2. The dependence of output voltage ripples on $V_{in} - V_{ref}$ changes.

Mean Output Voltage Ripples					
V_{ref} (V)↓	V_{in} = 6 V	V_{in} = 8 V	V_{in} = 10 V	V_{in} = 12 V	Period-1
2	3.90	4.10	4.32	9.42	Period-2
2.1	4.03	4.38	4.35	10.51	Period-4
2.2	4.41	4.68	4.80	4.28	Period-N
2.3	8.71	5.04	5.17	4.51	Chaos
2.4	8.71	5.36	5.59	5.03	Uncertain regime
2.5	10.60	5.77	5.96	5.55	
2.6	12.05	5.97	6.33	5.99	
2.7	15.95	6.37	6.78	6.48	
2.8	16.46	6.59	7.21	6.86	
2.9	18.07	6.98	7.66	7.50	
3	21.56	11.19	8.10	7.83	
3.1	20.78	12.75	8.62	8.41	
3.2	23.19	12.76	9.01	8.88	
3.3	25.22	15.62	9.45	9.46	
3.4	27.17	17.33	9.91	10.00	
3.5	28.73	19.87	10.29	10.57	

Further data analysis revealed a potential correlation between the variations in output voltage ripples and specific operation modes. In other words, certain operation modes exhibited characteristic ranges of output voltage ripples. However, some deviations of output voltage ripple ranges were observed with the variation of input voltage values. Because of these deviations, for example, for $V_{in} = 6$ V, the range of output voltage ripples that are typical for period-N mode intersected with the range of output voltage ripples that are typical for period-2 mode for $V_{in} = 8$ V. This occurred because of the expansion of operation mode boundaries, as mentioned earlier.

In addition, some parameter combinations caused uncertain behavior, which resulted in a transition from chaotic operation mode to period-1 mode after some time. This type of operation mode, connected to the possible coexistence of various attractors, should be avoided, as it may result in unforeseen dynamics changes and jeopardize the overall security of the interconnected system.

3.2.2. $R_{load} - V_{ref}$ Measurements

Next, we analyzed the dependence of the output voltage ripples in the $R_{load} - V_{ref}$ plane, marking the transitions to subharmonic and chaotic modes of operation.

After analysis of the graph in Figure 17 and Table 3, it can be seen that the increase in V_{ref} results in the gradual transition from period-1 to a chaotic mode of operation. As in the previous study, raising the value of V_{ref} leads to the increase in output voltage ripple amplitude. It could also be observed that the increase in R_{load} leads to the shift of the transition boundaries between different qualitative behaviors.

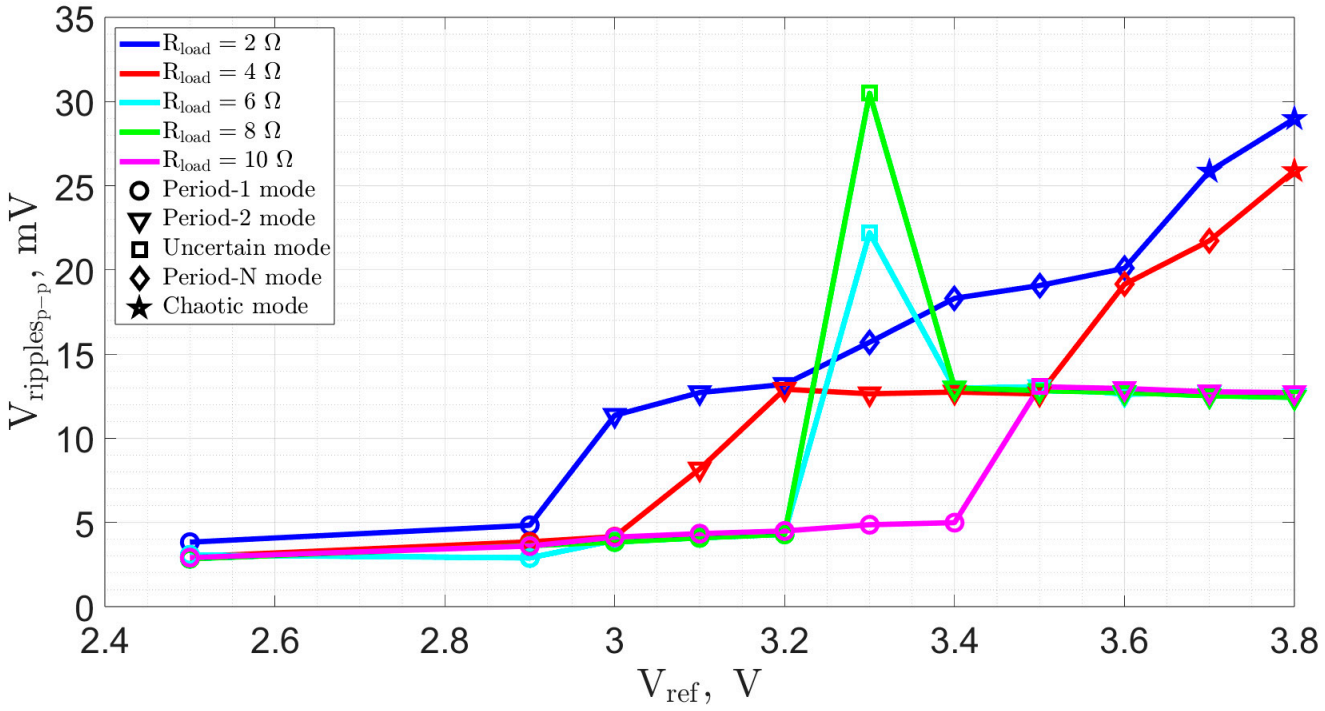


Figure 17. The dependence of output voltage ripples on $R_{load} - V_{ref}$ variation.

Table 3. The dependence of output voltage ripples on $R_{load} - V_{ref}$ changes.

	Mean Ripple Voltage Amplitude (Peak to Peak) for Parameters $R_{load} - V_{ref}$ (mV)					
V_{ref} Values (V) ↓ / **R_{load} Values (Ω) →**	**2**	**4**	**6**	**8**	**10**	
2.5	3.83	2.97	3.07	2.84	2.91	Period-1
2.9	4.83	3.85	2.90	3.63	3.60	Period-2
3	11.36	4.16	3.94	3.84	4.13	Period-N
3.1	12.72	8.18	4.25	4.09	4.34	Chaos
3.2	13.20	12.92	4.38	4.30	4.50	Uncertain regime
3.3	15.70	12.64	22.21	30.49	4.87	
3.4	18.32	12.75	12.97	12.99	4.99	
3.5	19.08	12.64	13.07	12.84	13.06	
3.6	20.09	19.15	12.62	12.72	12.96	
3.7	25.86	21.74	12.71	12.72	12.76	
3.8	28.98	25.89	12.54	12.43	12.71	

Further data analysis shows that the transition to subharmonic and chaotic modes of operation changes the slope of the graphs, leading to a steeper rise in the output voltage ripples. If one wants to force the converter to serve as a source of chaotic oscillations, the degradation of the output voltage characteristics should be considered. As in the previous study, the same parameter combinations caused the uncertain behavior of the converter.

3.2.3. Measurements Data Comparison to Numerical Analysis

After measurement data were obtained, the results were compared to the numerical study. The goal was to identify the regions in the parameter space exhibiting different dynamical patterns. In order to do that, the reference current was obtained from the current sensor signal. Then, the obtained value, the input voltage, and the operation mode were compared to the bifurcation map in Figure 3. The comparison of results is summarized in Table 4.

Table 4. Measurements data comparison to numerical analysis results.

V_{in} = 6 V		
V_{ref}, V	I_{ref}, A	Num. analysis mode
2	2.13	Period-1
2.4	2.82	Period-2
2.7	3.02	Period-N (Group 0)
3.5	3.38	Chaos
V_{in} = 8 V		
V_{ref}, V	I_{ref}, A	Num. analysis mode
2.5	2.70	Period-1
3.2	3.72	Period-2
3.5	3.93	Period-N (Group 0)
3.8	4.47	Chaos
V_{in} = 10 V		
V_{ref}, V	I_{ref}, A	Num. analysis mode
2.2	2.51	Period-1
2.6	2.92	Period-1
3	3.29	Period-1
3.5	3.72	Period-2

As can be seen from Table 4, there is an excellent agreement between the numerical model and the actual buck schematic regarding the operation mode transitions. However, from the obtained data for the V_{in} = 10 V and V_{ref} = 3.5 V parameter combination, the converter operated in period-1 mode, but the numerical analysis showed period-2 mode. This disagreement is possible because, according to the Figure 3 bifurcation map, the converter operation is close to the period-2 mode transition for this combination of parameters.

3.3. Effects on Efficiency

Next, the experimental study on the effects of different modes of operation on the converter's efficiency was undertaken. This study is essential to ensure that the efficiency differences between the converter operating in period-1 and chaotic modes are as minor as possible, which can be crucial in most converter applications, including secure data transmission using WSN nodes. Afterward, we compared converter efficiency in chaotic mode both with and without compensation ramp. This analysis allowed us to draw conclusions regarding the differences in efficiency between period-1 and chaotic mode operations and evaluate the possible application of the ramp signal as a switch between period-1 and chaotic mode.

3.3.1. $V_{in} - V_{ref}$ Measurements

First, we analyzed the converter's efficiency change as the values of the $V_{in} - V_{ref}$ parameters changed, marking the transitions similarly to the output voltage ripple measurements.

After examination of the graph presented in Figure 18, it can be seen that the increase in V_{ref} results in the gradual transition from period-1 to a chaotic mode of operation. Further study of the presented graph revealed an increase in converter efficiency with an increase in V_{ref}. A closer analysis of the constructed graphs showed that the $V_{ref} - \eta$ dependency is nearly linear with negligible deviations for all V_{in} values. Analyzing the influence of operation modes on converter efficiency deviations, it can be seen that the effect is insignificant even in chaotic mode. This leads to the conclusion that utilizing a chaotic mode of operation will not result in sudden deviations in the converter's efficiency.

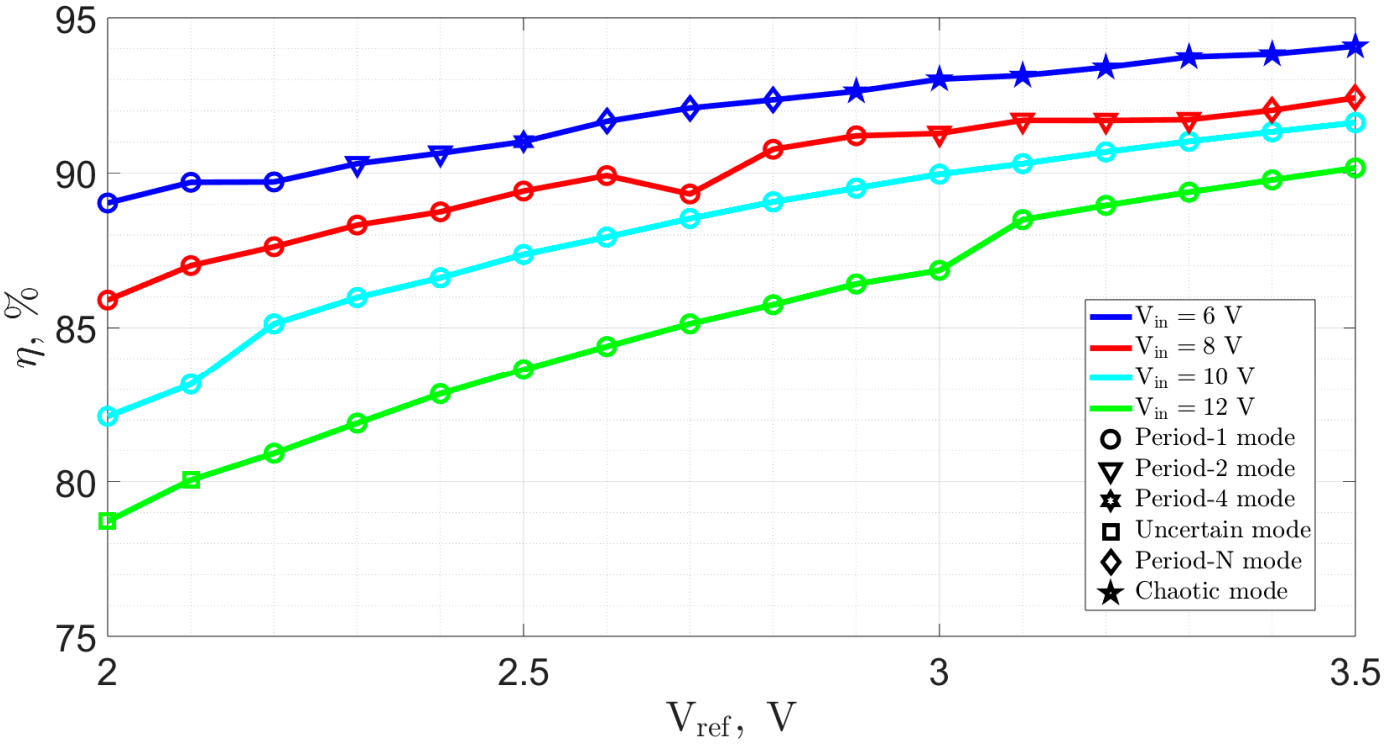


Figure 18. Efficiency dependence on $V_{in} - V_{ref}$ changes.

3.3.2. $R_{load} - V_{ref}$ Measurements

After that, we assessed how changes in the $V_{in} - V_{ref}$ parameters impacted the converter's efficiency.

Analysis of the graph in Figure 19 shows the gradual transition from period-1 to chaotic mode of operation with the increase in V_{ref}. Further inspection indicates an increase in converter efficiency with an increase in V_{ref}. A closer analysis of the constructed graphs shows that the dependence $V_{ref} - \eta$ is almost linear. However, there are some significant deviations present for $R_{load} = 6$ to 10 Ω. For $R_{load} = 6$ Ω, the drop in efficiency was observed at $V_{ref} = 3.4$ V; $R_{load} = 8$ Ω at $V_{ref} = 3.6$ V; and $R_{load} = 10$ Ω at $V_{ref} = 3.7$ V.

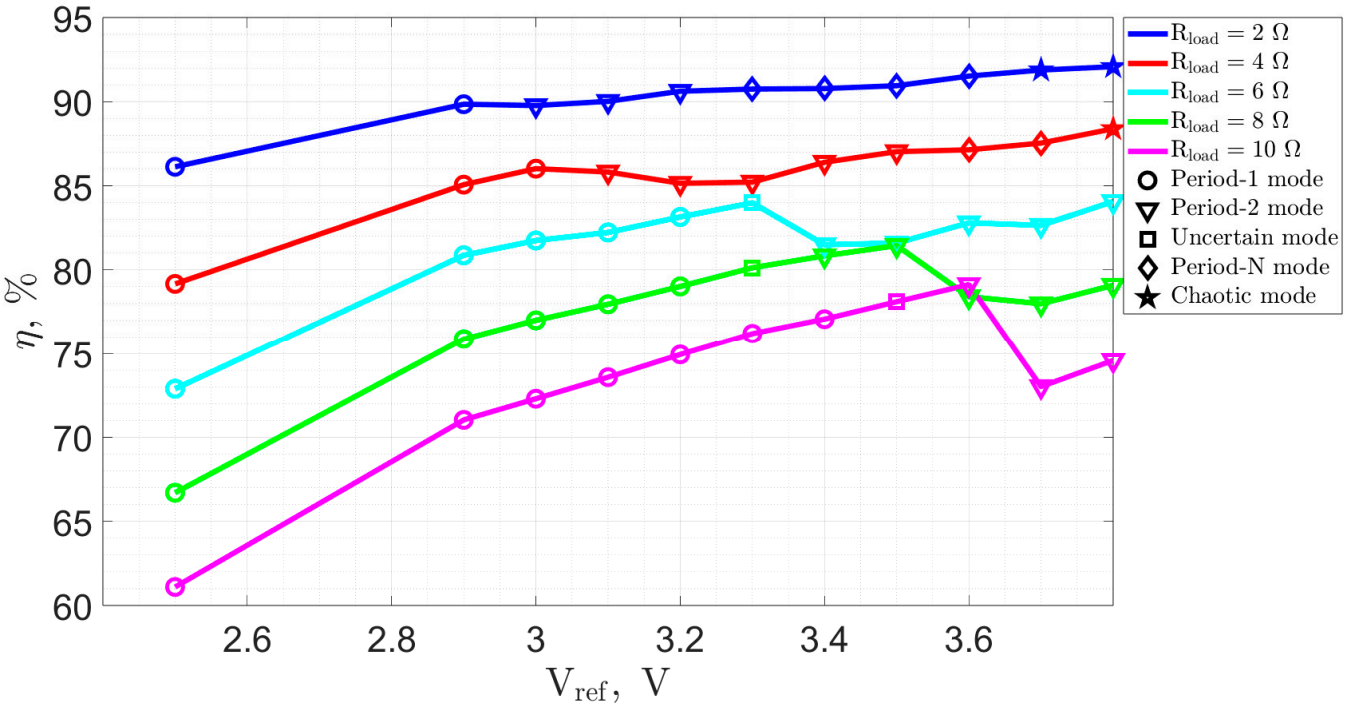


Figure 19. Efficiency dependence on $R_{load} - V_{ref}$ changes.

3.3.3. Efficiency Comparison between Period-1 Operation Mode and Chaotic Mode

Next, the programmable ramp generator (PRG) was used to compare the efficiency of the buck converter operating in the period-1 mode to the buck converter operating in the chaotic mode. The measurements of the efficiency of the converter in chaotic operation mode for both $R_{load} - V_{ref}$ and $V_{in} - V_{ref}$ groups were performed using the obtained chaotic mode parameter combinations from the previous measurements with PRG turned off. Subsequently, to obtain period-1 operation mode with the same parameters, the PRG was turned on. The methodology of these measurements was the same as in the efficiency measurements shown in Section 3.1. For the $R_{load} - V_{ref}$ group comparison, the parameters of the system were as follows: $V_{in} = 8$ V, $f_{sw} = 500$ kHz, $V_{ref} = 3.8$ V, $R_{load_1} = 2\,\Omega$, and $R_{load_2} = 4\,\Omega$. For the $V_{in} - V_{ref}$ group, in turn, the parameters of the system were as follows: $V_{in_1} = 6$ V, $V_{in_1} = 8$ V, $f_{sw} = 500$ kHz, $V_{ref_1} = 3.5$ V, $V_{ref_2} = 3.8$ V, and $R_{load} = 2\,\Omega$. The measurement results are summarized in Tables 5 and 6.

Table 5. Efficiency comparison for chaotic (PRG turned off) and period-1 (PRG turned on) modes ($R_{load} - V_{ref}$ group).

	R_{load}, Ω	V_{ref}, V	I_{in}, A	V_{in}, V	I_{out}, A	V_{out}, V	η, %	η, % (PRG Turned Off)
With PRG turned on	2	3.8	1.804	7.7172	2.593	5.0219	93.535%	92.330%
	4	3.8	1.022	7.844	1.461	5.0175	91.443%	89.077%

Table 6. Efficiency comparison for chaotic (PRG turned off) and period-1 (PRG turned on) modes ($V_{in} - V_{ref}$ group).

	R_{load}, Ω	V_{ref}, V	I_{in}, A	V_{in}, V	I_{out}, A	V_{out}, V	η, %	η, % (PRG Turned Off)
With PRG turned on	2	3.5	2.055	5.6817	2.385	4.6126	94.220%	94.021%
	2	3.8	1.804	7.7172	2.593	5.0219	93.535%	92.330%

Analysis of the data presented in Tables 5 and 6 reveals a slight decrease in efficiency in chaotic operation mode compared to the period-1 mode. Although the efficiency decrease was about 2.4% at maximum in the current results, this impact, together with the increase in voltage ripple amplitude, could adversely affect the circuit powered by the switching converter in chaotic mode for the extended time period. Nonetheless, the generated chaotic waveform could be used for secure communication if turned on for the data transmission periods using the ramp signal generator.

4. Conclusions

The primary focus of this study was to investigate how operation modes evolve in the buck converter when circuit parameters are altered. The analysis involves examining the impact of subharmonic and chaotic modes on the essential power conversion characteristics. The modified model of the PCMC buck converter was initially analyzed using numerical simulations to identify the regions exhibiting subharmonic and chaotic behavior. Consequently, laboratory measurements using the Microchip's CIP Hybrid Power Starter Kit in the PCMC configuration were taken to study the effects of different operation modes on the output voltage ripples and efficiency of the converter. After that, an efficiency comparison was performed for the buck converter operating in the period-1 mode and the chaotic mode, respectively.

The numerical analysis demonstrated the presence of a one-piece wide chaotic attractor region and the possibility of switching between the different operation modes using the compensation ramp. The laboratory measurements revealed the increase in output voltage ripple amplitude with an increase in V_{ref} for both the $R_{load} - V_{ref}$ and $V_{in} - V_{ref}$ groups. The obtained results show an excellent agreement between the numerical model and the real buck schematic regarding the operation mode transitions. Consequently, the exploration of the effect of the parameter changes on the efficiency of the converter demonstrated the nearly linear $V_{ref} - \eta$ dependency with a minor efficiency drop in the chaotic mode compared to the periodic mode of operation.

In summary, the research indicates that the buck converter holds the potential for generating chaotic signals. However, sustained operation in chaotic mode over extended periods may lead to efficiency degradation and an undesirable rise in voltage ripple amplitude, negatively impacting the circuit powered by the switching converter. A possible solution for that is to employ chaotic mode only during data transmission periods, utilizing the ramp signal generator for switching between period-1 mode and chaotic mode.

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