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Interface Contact Thermal Resistance of Die Attach in High-Power Laser Diode Packages

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Abstract: The reliability of packaged laser diodes is heavily dependent on the quality of the die attach. Even a small void or delamination may result in a sudden increase in junction temperature, eventually leading to failure of the operation. The contact thermal resistance at the interface between the die attach and the heat sink plays a critical role in thermal management of high-power laser diode packages. This paper focuses on the investigation of interface contact thermal resistance of the die attach using thermal transient analysis. The structure function of the heat flow path in the T3ster thermal resistance testing experiment is utilized. By analyzing the structure function of the transient thermal characteristics, it was determined that interface thermal resistance between the chip and solder was 0.38 K/W, while the resistance between solder and heat sink was 0.36 K/W. The simulation and measurement results showed excellent agreement, indicating that it is possible to accurately predict the interface contact area of the die attach in the F-mount packaged single emitter laser diode. Additionally, the proportion of interface contact thermal resistance in the total package thermal resistance can be used to evaluate the quality of the die attach.

Keywords: die attach; interface contact thermal resistance; thermal management; transient thermal analysis; structure function; high-power laser diode

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1. Introduction

High-power laser diodes have been widely used for solid-state laser pumping, as well as a direct high-power light source for industrial, research, and medical applications [1,2]. With the development of laser diodes, the requirement for power has continued to increase and the heat in the die has been generated. According to statistics, the failure of electronic devices caused by excessive temperature currently accounts for approximately 55%, being a major reason for electronic device failure [3]. Therefore, it is evident that thermal effects have become an issue that cannot be ignored in the development of high-power laser diodes, and effective removal of heat in order to maintain a safe junction temperature is the key to thermal management of high-power laser diode packages.

Thermal management is crucial for high-power laser diodes. With the development of laser diodes, electro-optical conversion efficiency can increase to 50~70%, but there is still 30~50% of electrical energy being converted into thermal energy. High-power laser diode chips have a small size and high output power, resulting in a great heat flux density during operation. For instance, when the thermal load power of a single emitter chip increases to 10 W, the internal heat flux density will exceed to 1500 W/cm^2, which is equivalent to the magnitude of heat flux density on the surface of the sun [4]. If such a high heat flux density cannot be efficiently dissipated, the junction temperature will rapidly increase. The

rising chip temperature significantly affects the performance of the laser diodes, leading to degradation of lifetime and electro-optical efficiency, as well as an increase in threshold current and wavelength redshift. Therefore, thermal management is vital to maintain a safe junction temperature during the operation for high-power laser diodes.

Thermal resistance is the primary parameter for evaluating thermal management of electronic devices [5]. Packaging technology is the post-processing technique for fabrication of laser diodes, which mainly includes heat sink design, solder preparation, sintering, and bonding. Sintering involves soldering the chip onto the heat sink, while bonding entails connecting electrode leads from the chip to the heat sink, typically using gold wires with a diameter of 30 um to form the current path. To enhance heat dissipation performance, the laser chip is epi-down mounted onto a substrate, which is the p-side connection. The packaging thermal resistance of high-power laser diodes is composed of chip thermal resistance R1, interface contact thermal resistance between chip and solder R2, solder thermal resistance R3, interface thermal resistance between solder and submount R4, submount thermal resistance R5, and heat sink thermal resistance R6, as Figure 1 shows. Analyzing the package thermal resistance is of great significance for better thermal management of high-power laser diodes.

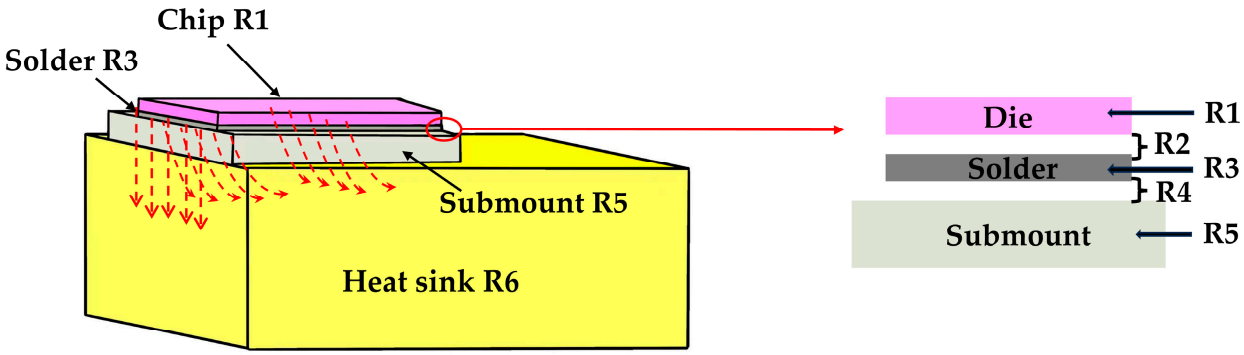


Figure 1. Schematic diagram of high-power laser diode package thermal resistance.

Thermal management has a vital impact on the thermal performance of high-power laser diodes, making the evaluation of precise thermal resistance essential. It should be noted that numerous studies on the thermal characteristic of laser diode packages have been conducted by other research groups. For instance, Wipiejewski. T et al. measured the thermal resistance of vertical-cavity laser diodes by comparing the emission wavelength shift versus dissipated power to the wavelength shift as ambient temperature was changed [6]. Chang. J et al. researched the effect of solder void size and location on the thermal resistance of power devices using three-dimensional (3-D) finite element modeling [7]. Maciej. Kuc and Otiaba. KC et al. focused on thermal analysis of the size of the diamond heat sink and on the thickness of the solder [8,9]. Ma. X et al. studied the relationship between chip size and thermal resistance of the C-mount packaged single emitter diode laser through a wavelength shift experiment [10]. Ni. Y et al. investigated the heat dissipating performance of laser diodes packaged by silicon carbide (SiC) ceramic submount, compared with aluminum nitride (AlN) ceramic submount. The thermal resistance was measured using the structure function method [11].

Although the aforementioned studies provide vital information on the package thermal resistance of laser diodes, they were more concentrated on the impact of chip size, solder void, heat sink, and submount materials on thermal resistance [6–11]. There are few papers researching the influence of interface between the chip and solder or solder and heat sink on package thermal resistance in high-power laser diodes. Previous research [6,10] mostly measured the overall thermal resistance between the heat-generating chip and heat-dissipating heat sink using the wavelength shift experiment, which could not obtain the thermal resistance of each layer in the laser diodes' packaged structure. Thus, more studies are needed for an in-depth understanding of the precise measurement of interface

thermal resistance in the die attach for package thermal management. This article firstly utilizes the finite element method (FEM) to conduct steady-state thermal characteristic simulations on F-mount packaged high-power single emitter laser diodes, analyzing the mechanism of interface thermal resistance which affects the thermal properties of the chip, and then, measures the interface thermal resistance using T3ster thermal resistance testing measurement. Finally, combining the results of measurement with simulation, we can forecast and estimate the interface contact area and package quality of single emitter laser diodes in the real working environment. These findings have great reference significance for further improving the reliability and performance stability of high-power laser diodes.

2. Materials and Methods

2.1. Simulation of F-Mount Packaged Single Emitter

Interface contact thermal resistance of the die attach is crucial for the thermal management of high-power laser diodes. At present, Indium solder and Gold-Tin solder are commonly used in laser diode packages. In the die attach process, the laser chip is epi-down mounted onto the submount, and the liquid AuSn alloy will flow and fill the burrs on the surface of the chip metal layer or heat sink layer when the soldering temperature increases to 320 °C [12]. However, due to the poor flatness of the heat sink's surface, large particles produced during the chip metallization, impurities in solder, pressure applied during sintering and poor wettability of the die attach, gaps, and voids may form at the contact interface. When thermal flow passes through the interface, incomplete contact of the interface results in a sudden decrease in the heat transfer channel, leading to the shrinkage of thermal flow, thus causing significant temperature difference and interface thermal resistance between the chip or heat sink and solder. Interface contact thermal resistance is related to the roughness of the interface and the interface contact area. Generally, to ensure that the laser diode can operate normally, the wettability of the solder should not be too poor. Hence, in the following simulation, we analyze the impact of contact interface area of 80%, 85%, and 90% on interface contact thermal resistance in the die attach of high-power laser diode packages.

To investigate interface thermal resistance and the interface contact state in the die attach, we establish a calculation model and a finite element calculation format based on the multi-point contact model. From a microscopic perspective, the actual contact interface is composed of numerous randomly distributed micro-protrusions with various shapes. When conducting finite element simulations, directly adopting this random surface model would result in a significant increase in computational scale and workload, potentially reaching an unacceptable level. In order to better simulate the actual contact interface of laser diodes, we use regular micro-protrusions with the same characteristic parameters, such as cuboids, cylinders, frustums, spheres, etc., to approximate random rough surfaces. In terms of rapidity and feasibility of calculation, using cuboids or cylinders is more convenient. Moreover, it can better match the measurement results of the surface roughness of the structure (for example, the height of a convex rectangle can be determined by the surface roughness parameter Ra) [13]. Additionally, due to the small size of the microcontact, the computational workload would be very large if three-dimensional modeling were conducted. The increase in computational accuracy would be insignificant compared to a two-dimensional model. Therefore, this study adopts a two-dimensional plane model to simulate the contact interface. The microcontacts on the interface are approximated by multiple rectangular protrusions with a periodic distribution, as Figure 2 shows.

Figure 2 shows the main structural parameters of the calculation model, including the height t, width b, and the gap width a of the rectangular convex body, in addition to the actual size of the chip, solder, and heat sink. The determination methods for these parameters are as follows: the contact between two rough surfaces is equivalent to the contact between a completely smooth surface and a rough surface. The height t of the contact protrusions is taken as the average of the surface roughness (Ra1 and Ra2) of

the two interfaces. The gap width depends on the contact area between the solder and the chip or heat sink. During the Ansys finite element simulation, in order to facilitate analysis and calculation, it is common to model the chip and its internal structure using a simplified rectangular stack structure [14–17]. The research object of this study is the F-mount packaged single emitter diode laser with a cavity length of 2 mm. Figure 3 shows the schematic diagram of the single emitter epitaxial structure. Table 1 presents the specific parameters of the finite element computational model.

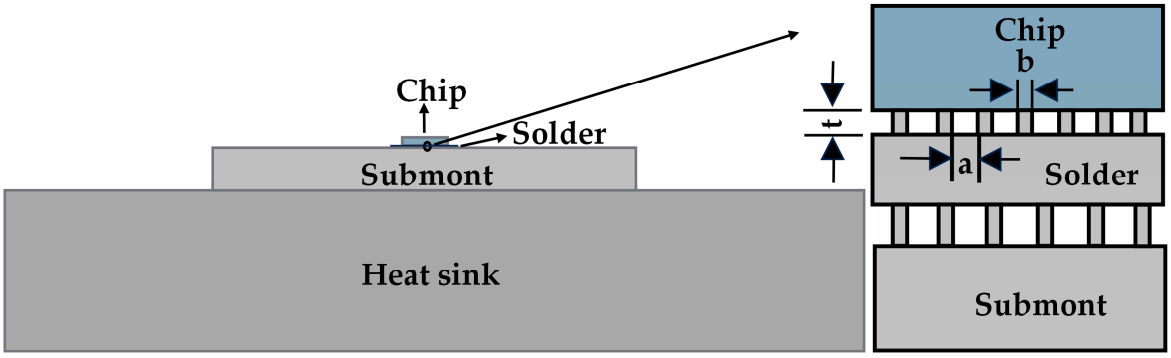


Figure 2. Computational model of the thermal contact resistance based on multipoint contact model.

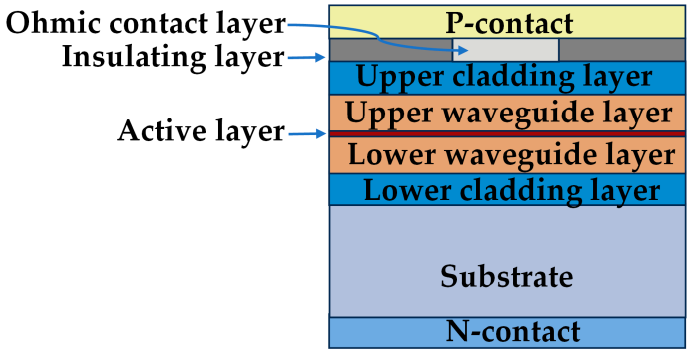


Figure 3. Schematic diagram of single emitter epitaxial structure.

Table 1. Material specification of high-power laser diode package.

Layer		Material	W × L × H (mm)	Thermal Conductivity (W/m·K)
Die	N-contact	Au	0.5 × 2 × 0.0007	315
	Substrate	GaAs	0.5 × 2 × 0.1	46
	Lower cladding layer	$Al_{0.5}GaAs$	0.5 × 2 × 0.0011	11
	Lower waveguide layer	$Al_{0.33}GaAs$	0.5 × 2 × 0.0006	12.04
	Active layer	$Al_{0.12}Ga_{0.795}In_{0.085}As$	0.5 × 2 × 0.000008	4
	Upper waveguide layer	$Al_{0.33}GaAs$	0.5 × 2 × 0.0004	12.04
	Upper cladding layer	$Al_{0.5}GaAs$	0.5 × 2 × 0.0011	11
	Insulating layer	SiO_2	0.2 × 2 × 0.00015	46
	Ohmic contact layer	GaAs	0.15 × 2 × 0.00015	1.28
	P-contact	Au	0.5 × 2 × 0.0004	315
Solder		AuSn	0.9 × 4.75 × 0.005	57
Submount		AlN	5 × 4.75 × 0.4	120
Heat sink		Cu	14 × 5.25 × 2.5	398

In this section, we conducted steady-state thermal simulation calculation for interface thermal resistance of the die attach, utilizing the multipoint contact thermal resistance calculation model established in the previous section. Regarding the numerical model, we

made some reasonable assumptions. Firstly, we assume that all heat power is concentrated in the active layer during the operation of the laser diode [18,19]. Subsequently, the chip surface, as well as the sides of the thermal sink, are considered adiabatic [20], and the heat dissipation capacity at the bottom of the heat sink is assumed to be infinite. In the simulation calculation, the governing equation for the steady-state temperature field we employ is $\nabla^2 T + \frac{q_v}{\lambda} = 0$ (where ∇ is the Laplace operator, λ is the thermal conductivity, and q_v is the internal heat source). The corresponding boundary conditions are $T = \overline{T}$ (in the $\partial\Omega_1$) and $n \cdot q = \overline{q}$ (in the $\partial\Omega_2$). The surface roughness of the chip P-side gold layer and the solder were measured to be 0.8 um and 0.25 um, respectively, while the AlN heat sink exhibited a surface roughness of 0.5 um. Considering that the height of the contact protrusions is the average of the surface roughness values Ra1 and Ra2 of the two interfaces, the height at the chip–solder interface was determined to be 0.525 um, with a width of 0.5 um. Similarly, the height of the contact protrusions at the solder–heat sink interface was calculated to be 0.375 um, with a width of 0.5 um.

For the simulation, we first set the initial contact area between the chip and solder, as well as between the solder and heat sink interfaces, to be 80%. The thermal boundary condition applied in the simulation model involved a thermal power density of 1.11×10^{15} W/m^3 in the active layer and a constant temperature boundary condition of 22 °C at the bottom of the heat sink. These parameters were crucial in the simulation setup, ensuring accurate representation of the thermal behavior at the interfaces. The simulation results will provide valuable insights into the interface thermal resistance and contribute significantly to the advancement of our understanding in this field.

2.2. Experiment of F-Mount Packaged Single Emitter

2.2.1. T3ster Interface Contact Thermal Resistance Testing

The most widely used method for measuring the chip temperature of high-power laser diodes is the junction voltage measurement method, also known as the forward voltage method. This approach relies on the nearly linear relationship between the temperature of the junction temperature region and the forward voltage, making it a reliable technique for temperature estimation [21,22]. The chip's active region temperature can be deduced by measuring the voltage of the laser diode. However, due to the variations in laser diode types and manufacturing processes, this linear relationship needs to be calibrated in advance using a low current method. In this method, the laser diode operates under a current from the working current source for a sufficiently long duration (typically 600 s), ensuring a steady-state operational regime. The laser diode is then switched from the working state to the measuring state to measure the forward voltage. This method has been validated by Liu et al., confirming that the temperature change over time under cooling conditions has a complementary relationship with that under heating conditions [23]. Therefore, by mathematically inverting the transient cooling curve, the transient temperature rise curve can be derived. Due to its simplicity and effectiveness, this method is commonly utilized for temperature measurement in high-power semiconductor lasers (LED, IGBT etc.) [24–26].

The utilization of the structure function theory was introduced as an enhancement to the junction voltage thermometry method, enabling fast calculation of the device package thermal resistance. In 1997, V. Szekely et al. pioneered the application of the structure function in thermal analysis based on the Cauer network model [27]. This approach involved measuring the transient thermal response curves of the device during heating or cooling, from which parameters related to the thermal resistance and thermal capacitance were extracted [28]. By discerning the physical differences among different material layers, crucial parameters such as thermal resistance and heat capacity could be acquired, particularly at the interfaces between material layers. The structure functions serve as a tool to map the cumulative thermal capacitances of the heat flow path in relation to the thermal resistances, extending from the junction to the ambient environment. By examining the derivative of this function, the differential structure is represented as a function of cumulative thermal resistance. Notably, local peaks and valleys in these functions indicate transitions to new

materials or changes in surface areas within the heat flow path, offering valuable insight into the thermal behavior and material transitions within the package.

In this experiment, we determined the transient thermal response curve of a single emitter using the commercial T3ster transient thermal tester (SIMUCAD Info Tech Co., Ltd., Shanghai, China), which offers a remarkable time resolution of 1 us and a high-temperature measurement accuracy of 0.01 °C. The experimental subjects consisted of two F-mount packaged single emitter laser diodes, each with a cavity length of 2 mm, as Figure 4 depicts. Initially, the single emitters were placed directly on a cold plate for testing, allowing us to observe the cumulative structure function. Subsequently, thermal grease was applied on the cold plate, and the transient response curve was measured under the same conditions as the first test to obtain the structure function. In the laboratory setup, the LD heating current was maintained at 3 A, with a heating duration of 80 s and a test current of 20 mA. The temperature of the cooling plate was precisely controlled at 20 °C using a Peltier-based temperature controller. This meticulous experimental procedure ensured accurate measurements and reliable data for the analysis of the thermal behavior of the single emitter laser diodes.

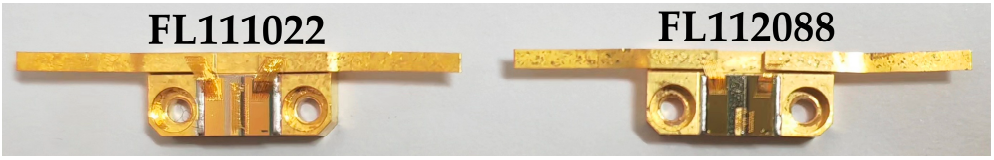


Figure 4. Schematic diagram of two F-mount packaged single emitter laser diodes.

2.2.2. CW Power-Averaged Wavelength Measurement of the Overall Thermal Resistance

The interface contact thermal resistance of the die attach is one crucial parameter of thermal management in high-power laser diode packages. However, there has been relatively limited research conducted on interface thermal resistance of solders in high-power laser diode packages. Both simulation and experimental fields in this area remain largely unexplored. This paper aims to quantitatively measure interface contact thermal resistance utilizing the T3ster thermal resistance testing experiment. To enhance the credibility and accuracy of this experimental data, we also performed a wavelength shift experiment to measure the thermal resistance of an F-mount packaged single emitter diode laser.

This method is based on the wavelength change under continuous wave (CW) operation of an F-mount packaged single emitter [29]. Figure 5 shows the setting up of the experimental equipment. Figure 6a shows data obtained by measuring the wavelength vs. heat sink temperature with a constant drive current of 1.4 A, revealing a wavelength heat coefficient of 1.55 nm/W. Figure 6b shows the measurement results of power-averaged wavelength vs. heat power with a heat sink temperature of 20 °C, indicating wavelength shifts of 0.285 nm/K toward longer wavelengths. By using equation $R = (\Delta\lambda/\Delta P)/(\Delta\lambda/\Delta T)$, the thermal resistance of the laser diode was calculated to be 5.4 K/W.

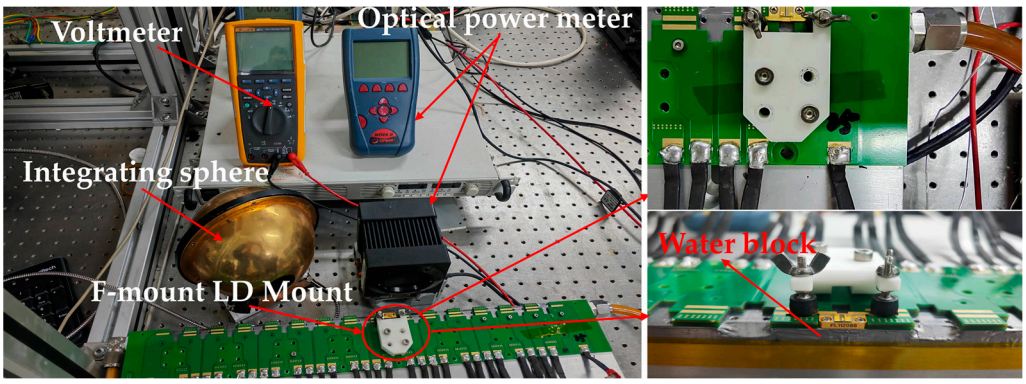
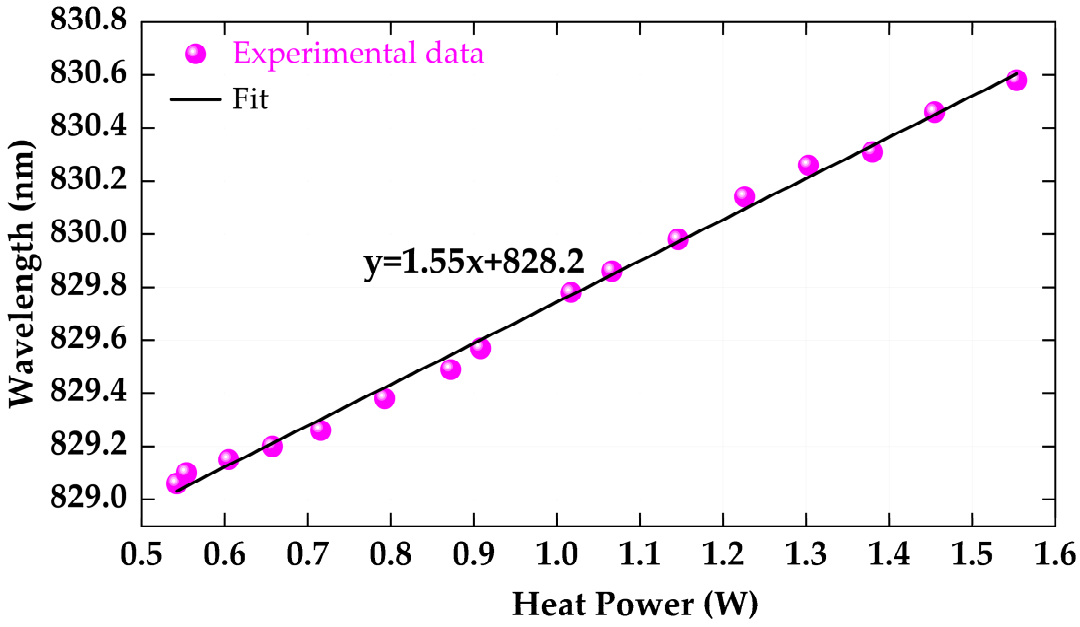
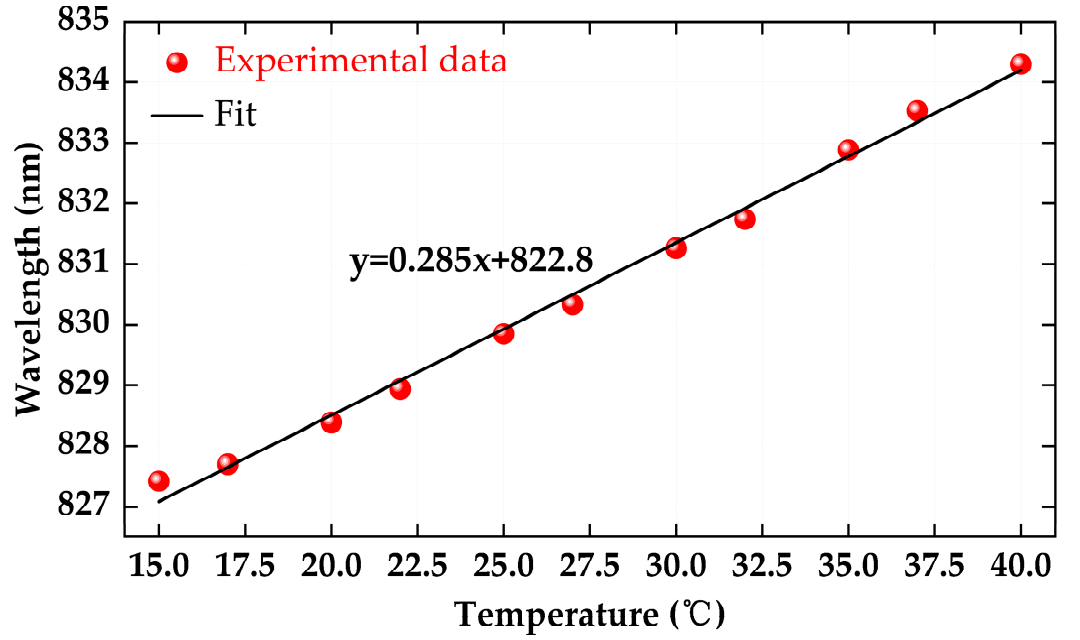


Figure 5. Test setup for power-averaged wavelength measurement.



(**a**)



(**b**)

Figure 6. Measured results of wavelength shift method: (**a**) Wavelength varies with heat power of the single emitter; (**b**) Wavelength varies with temperature of the single emitter.

3. Results

3.1. Simulation of the Interface Contact Thermal Resistance

Figure 7 illustrates the case of an interface contact area setting at 80%, the temperature distribution contour plot for the overall structure, and the local contact protrusions. Figure 4 shows that due to the presence of interface contact thermal resistance, there are significant temperature disparities on both sides of the chip–solder contact interface and the solder–heat sink contact interface. Specifically, the temperature difference at the chip–solder interface contact measures 1.8 °C, while at the solder–heat sink interface contact, it amounts to 2.8 °C. The interface thermal resistance between the solder layer and the chip or heat sink of a given material and thickness is profoundly influenced by the wettability of the solder

layer between the chip and the heat sink. Consequently, this study delves into the impact of the contact area between the solder layer and the chip or heat sink on the interface thermal resistance and thermal performance. To investigate this, the contact area of the die attach is varied at 80%, 85%, 90%, respectively. Table 2 outlines the different contact areas of the interface thermal resistance in the simulation.

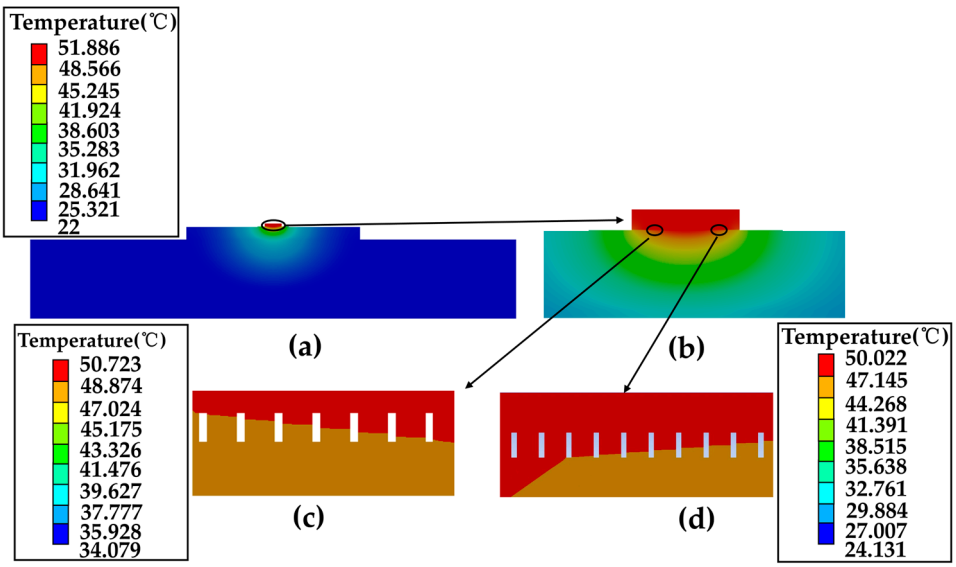


Figure 7. Temperature field of the computational model: (**a**) The overall structure; (**b**) The local contact protrusions; (**c**) Interface of the chip and solder; (**d**) Interface of the solder and heat sink.

Table 2. Thermal resistance of each layer for single emitter in simulation.

		Thermal Resistance (K/W)						
		Chip	**R1**	**Solder**	**R2**	**Submount**	**Heat Sink**	R_{thjc}
Simulation	80%	0.41	0.47	0.42	0.55	0.81	0.57	3.23
	85%	0.37	0.40	0.50	0.49	0.77	0.45	2.98
	90%	0.36	0.34	0.57	0.42	0.75	0.44	2.88

3.2. T3ster Interface Contact Thermal Resistance Testing

In this experiment, Figure 8a illustrates the cumulative structure functions of FL111022 under two distinct experimental conditions. The two curves exhibit exceptional repeatability up to 2.93 K/W. However, beyond 2.93 K/W, the curves diverge. This divergence occurs because the internal thermal resistance and thermal capacitance characteristics within the same single emitter lasers remain constant. However, once the heat flow reaches the backside of the heat sink, the structure functions separate due to the presence of different thermal conductive materials. By identifying the position of the separation point in the structure function, we can determine the overall thermal resistance from the chip to the heat sink of the single emitter, which amounts to R_{thjc} = 2.93 K/W. For various laser diodes, it is challenging to ensure the consistency of voids, thickness uniformity, and wetting properties of the solder layer during the packaging process. Consequently, the thermal resistance of the solder layer or heat sink layer may vary. Figure 9a displays the cumulative structure functions of the single emitter FL112088, where the curve diverges after 2.52 K/W, indicating an overall thermal resistance of 2.52K/W. By delineating the region of slope change and the positions of peak-trough in the curve, different material layers can be classified, as Figures 8b and 9b illustrate. This classification enables the acquisition of the thermal resistance of each layer and the interface thermal resistance in the die attach, as Table 3 details. These findings provide valuable insights into the material characteristics and thermal behavior within the single emitter.

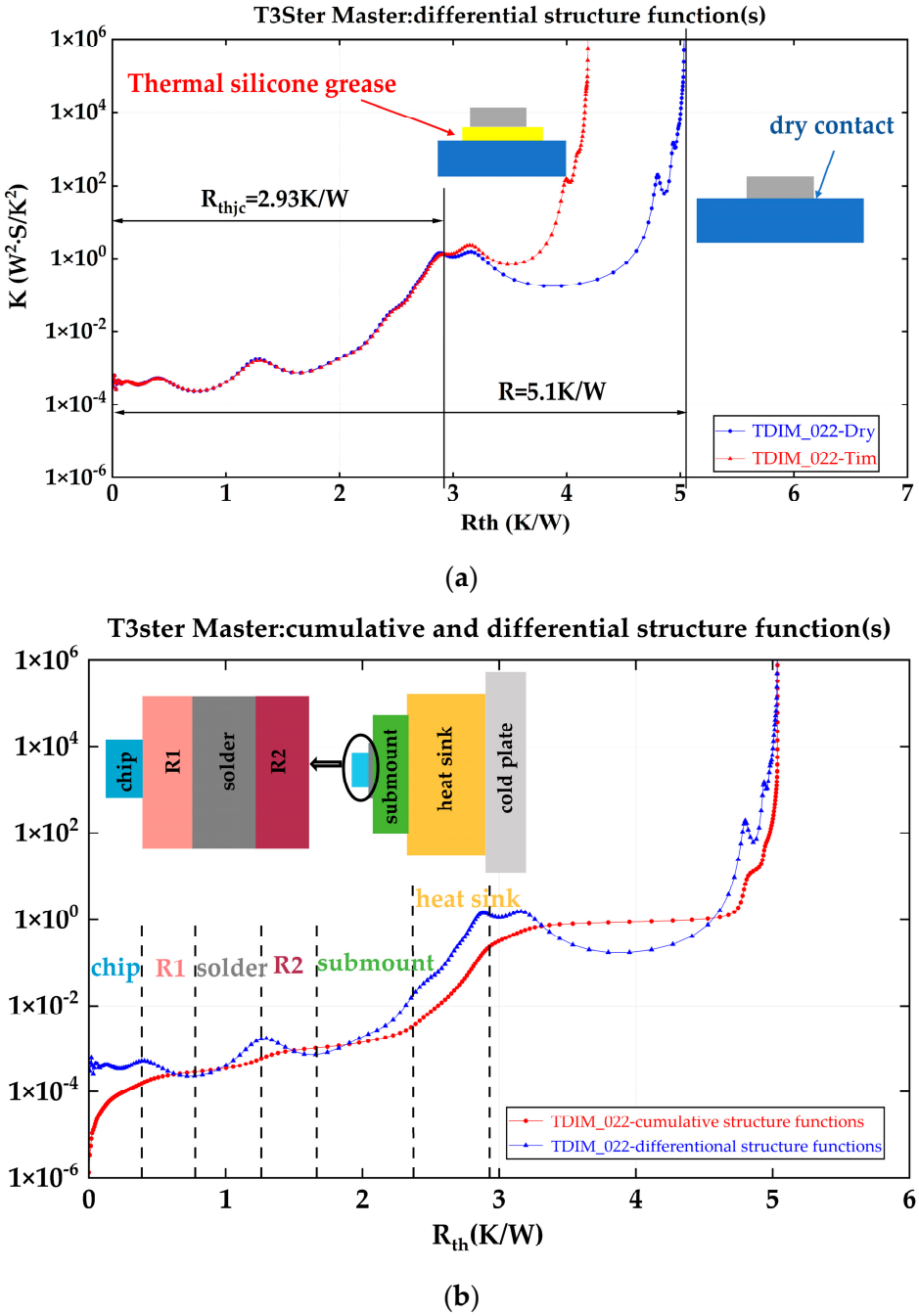


Figure 8. Measured cumulative and differential structure functions for FL111022 single emitter: (**a**) Differential structure functions with two interface contact conditions; (**b**) Structure functions with the dry contact of the single emitter.

Table 3. Thermal resistance of each layer for single emitter in the experiment.

		Thermal Resistance (K/W)						
		Chip	**R1**	**Solder**	**R2**	**Submount**	**Heat Sink**	**R_{thjc}**
T3ster	FL111022	0.386	0.381	0.525	0.36	0.761	0.511	2.93
	FL112088	0.331	0.33	0.42	0.35	0.689	0.4	2.52

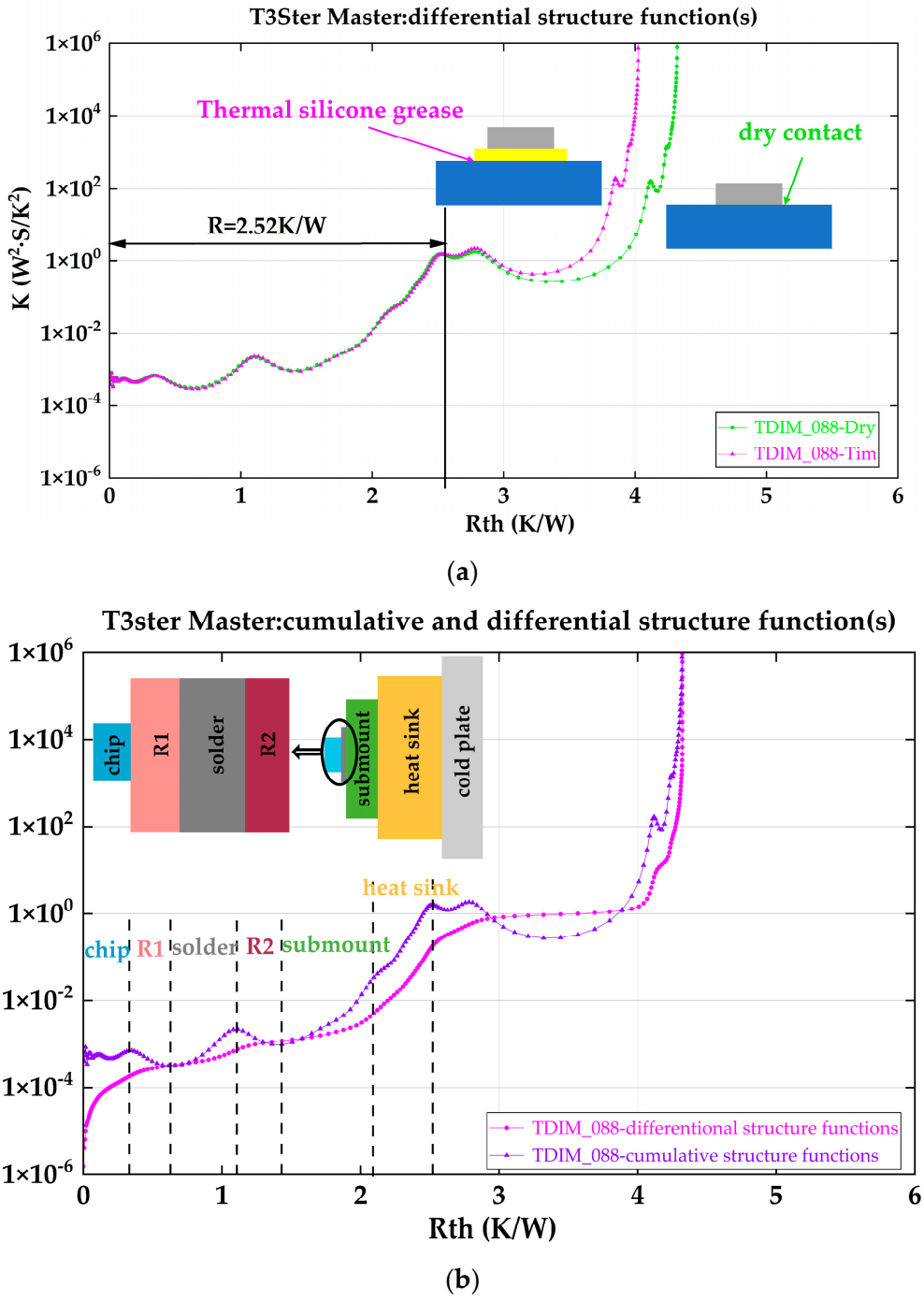


Figure 9. Measured cumulative and differential structure functions for FL112088 single emitter: (**a**) Differential structure functions with two interface contact conditions; (**b**) Structure functions with the dry contact of the single emitter.

3.3. CW Power-Averaged Wavelength Measurement of the Overall Thermal Resistance

In the wavelength measurement, we calculate the overall thermal resistance of the laser diode to be 5.4 K/W. However, this value does not solely represent the thermal resistance from the chip to the heat sink. In this experimental setup, the single emitter is placed on a temperature-controlled fixture and dissipates heat through the water cooler, as Figure 8 shows. The entire heat dissipation path includes the water block, aligning with the heat dissipation path in the forward voltage method with dry contact, as Figure 6a depicts. Therefore, the thermal resistance measured by the wavelength drift method, R = 5.4 K/W, is basically consistent with the thermal resistance measured by the forward

voltage method in the device's dry contact state (including the water block), which is R = 5.1 K/W, as Figure 6a shows. The slight difference in thermal resistance may arise from the slightly varied thermal resistance of the water block in the two experimental setups. This alignment demonstrates the accuracy and practicality of the forward voltage method and the structural function theory. It also underscores the effectiveness of using structural function analysis for evaluating interface thermal resistance in the die attach, showcasing it as a powerful experimental method.

4. Discussion

Table 4 summarizes the consequence derived from T3ster testing and finite element simulation. Upon analyzing the simulation results, it becomes evident that the interface thermal resistance of the die attach gradually decreases as the interface contact area between the solder and chip or solder and heat sink increases. This phenomenon arises because a large interface contact area implies good wettability of the solder between the chip and heat sink, resulting in fewer voids on the surface between the chip or heat sink and solder. As a result, the temperature differential between different interfaces diminishes, leading to a reduction in thermal resistance. This reduction is advantageous for efficient heat dissipation.

Table 4. Thermal resistance of each layer for single emitter between experiment and simulation.

		Thermal Resistance (K/W)						
		Chip	**R1**	**Solder**	**R2**	**Submount**	**Heat Sink**	**R_{thjc}**
T3ster	FL111022	0.386	0.381	0.525	0.36	0.761	0.511	2.93
	FL112088	0.331	0.33	0.42	0.35	0.689	0.4	2.52
Simulation	80%	0.41	0.468	0.42	0.547	0.814	0.571	3.23
	85%	0.368	0.405	0.50	0.494	0.771	0.45	2.98
	90%	0.36	0.345	0.59	0.417	0.75	0.44	2.88

Upon comparing the experimental results with the simulation data, it was found that when the contact area of the die attach is 90%, the error between the simulated interface thermal resistance and the experimental test is only 2.8%. Similarly, with a contact area of 85%, the error between the simulated junction to heat sink of thermal resistance and the experimental result is only 1.7%. The simulated interface thermal resistance aligns closely with the T3ster testing results, indicating that the optimal solder interface contact area for single emitters to operate and emit light properly and stably under actual working conditions is between 85% and 90%. This finding serves as a valuable prediction for the interface contact situation for high-power single emitter diode lasers.

Figure 10 shows the distribution of simulated and experimental thermal resistance for each layer within the overall thermal resistance. The pie chart reveals that when the interface contact area is 80%, the simulation of the solder interface thermal resistance constitutes 33.4% of the total thermal resistance. In the T3ster testing experiment, the proportion of interface thermal resistance decreases to 25.3%. This clearly indicates that during actual packaging processes, the quality of the solder interface can be evaluated based on the proportion of interface thermal resistance of the die attach in the overall thermal resistance. For instance, poor wettability between the chip and solder (or solder and heat sink), or the presence of voids on the solder layer's surface result in higher corresponding interface thermal resistance. This, in turn, leads to a larger share in the total thermal resistance. Consequently, by optimizing specific parameters in the soldering process, such as enhancing solder uniformity and infiltration, both packaging quality and heat dissipation characteristics can be improved. Additionally, this optimization opens up the possibility of non-destructively detecting potential defects in the high-power laser diode packaging process.

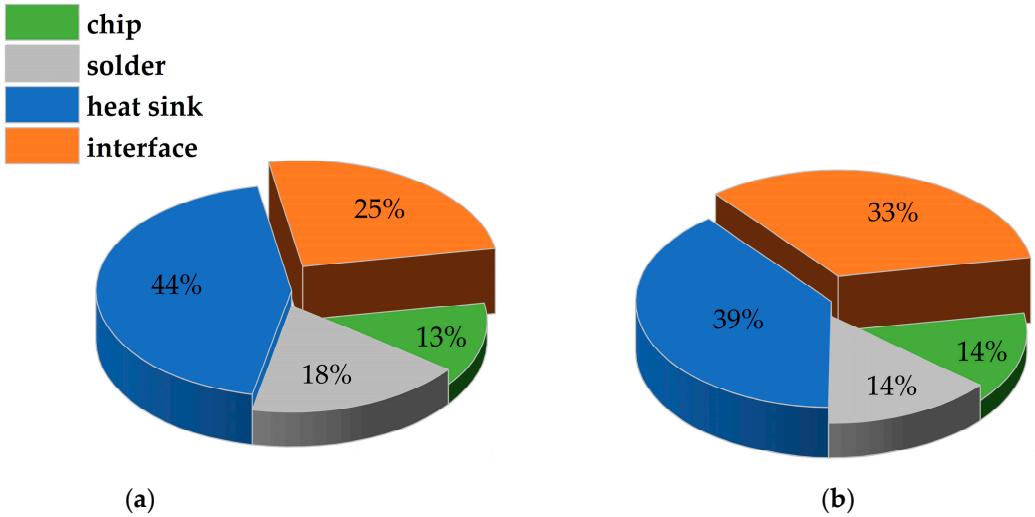


Figure 10. Distribution of simulated and experimental values of thermal resistance for each layer: (**a**) T3ster testing for FL111022; (**b**) Simulation for contact area of 80%.

The consistency of simulated and measured results establishes the significance of interface contact thermal resistance of the die attach in thermal management of high-power laser diode packages. Furthermore, it is evident that the current single emitter diode laser packing structure and process are rational, and this detection technology has the potential to be applied for assessing the thermal resistance of laser diodes packaged with Indium solder in future work. Likewise, this technology could be utilized to identify possible defects, such as voids, in the laser diode package procedure. The discrepancy between the simulation and experiment of the interface thermal resistance between the solder and heat sink may be attributed to the configuration of the interface contact shape. This article provides a thorough analysis and validation of the impact of the interface contact area on interface thermal resistance and device thermal performance. However, it does not delve into the effect of altering the geometric shape of the contact area on the interface thermal resistance of the die attach. Therefore, future research can explore various geometric shapes and comprehensively analyze the interface thermal resistance of the die attach.

5. Conclusions

In this paper, we have investigated interface contact thermal resistance of the die attach in high-power F-mount packaged single emitter laser diodes. Through T3ster thermal resistance testing experiment, interface thermal resistance between the chip and solder of 0.38 K/W is determined, while the resistance between the solder and heat sink is 0.36 K/W. Finite element simulation revealed that the chip–solder interface thermal resistance is 0.345 K/W and the solder–heat sink interface thermal resistance is 0.417 K/W when the interface contact area is 90%. By comparing the simulation results with the T3ster testing results, we can predict that the interface contact area of a single emitter under actual operating conditions ranges from 85% to 90%. Additionally, by considering the proportion of interface thermal resistance in the overall thermal resistance, the quality of the die attach can be evaluated, defects in laser diode packages can be identified, and the subsequent packaging process can be optimized. This research also verifies the accuracy and practicality of T3ster thermal resistance testing experiments through CW power-averaged wavelength measurement, highlighting the effectiveness and convenience of using the forward voltage method and structural function analysis for interface thermal resistance assessment in high-power laser diode packages.

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