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Designing a Twin Frequency Control DC-DC Buck Converter Using Accurate Load Current Sensing Technique

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Abstract: In this paper, a buck DC-DC converter with the proposed twin frequency control scheme (TFCS) and accurate load current sensing (ALCS) was designed and implemented with 0.18 µm CMOS technology for a supply voltage ranging from 2.0 to 3.0 V, which is compatible with state-of-the-art batteries (NiCd/NiMH: 1.1–2 V, Li-Ion: 2.5–4.2 V). The proposed converter yields a peak efficiency of about 92.7% with a load current of 30 mA. Furthermore, it only occupies a silicon area of 1.3 mm^2. The proposed buck converter is dedicated for smartphone applications whereby it spends most of its time in idle, low load conditions.

Keywords: DC-DC converter; twin frequency control; load sensing; buck converter; smartphone application

Citation: Kok, C.L.; Siek, L. Designing a Twin Frequency Control DC-DC Buck Converter Using Accurate Load Current Sensing Technique. *Electronics* **2024**, *13*, 45. https://doi.org/10.3390/electronics13010045

Academic Editor: Anna Richelli

Received: 1 December 2023
Revised: 18 December 2023
Accepted: 19 December 2023
Published: 20 December 2023

1. Introduction

Modern 4G smartphones are embedded with a high-speed multi-core processor, gigabytes of flash memory, high-resolution color display, 3G/4G and Bluetooth wireless communication devices [1]. Therefore, the quiescent power consumption of a smartphone is comparable to a laptop or a handheld tablet. Furthermore, new modern applications such as live video streaming require a constant utilization of an LED backlight display or cloud computing services, which will no doubt increase the total power consumption drastically [2]. All of the above enhanced functionalities of a 4G smartphone will heighten the pressure on the battery lifetime and escalate the urgency for a more efficient power management system [3]. However, the NiCd/NiMH and Li-ion batteries, which are widely used to provide a source of power, are very limited in supplying the energy and power demands for the wide variety of applications found in a smartphone. This is supported by a recent research study which has shown that its energy density has only doubled over the past decade from 300 to 600 Whr/liter [4]. Hence, the viable solution is to reduce the overall battery power consumption by improving the power efficiency of the power management unit (PMU) in a smartphone.

For the past few years, there have been numerous interesting research works [5,6] which have presented various power consumption usage models for 3G/4G smartphones. Modern power management systems in smartphones [7] are used to generate a constant or variable output voltage supply from battery sources which have a wide input range variation, e.g., NiCd/NiMH, 1.1–2 V, or Li-Ion, 2.5–4.2 V [8,9]. Power converters (buck/boost) are indispensable building blocks found in a part of the power management unit (PMU) of a smartphone, as shown in Figure 1. Their objectives are to supply a well-regulated supply voltage to the different group core modules [1] found in a smartphone. A full illustration of the PMU of a smartphone can be found here [10].

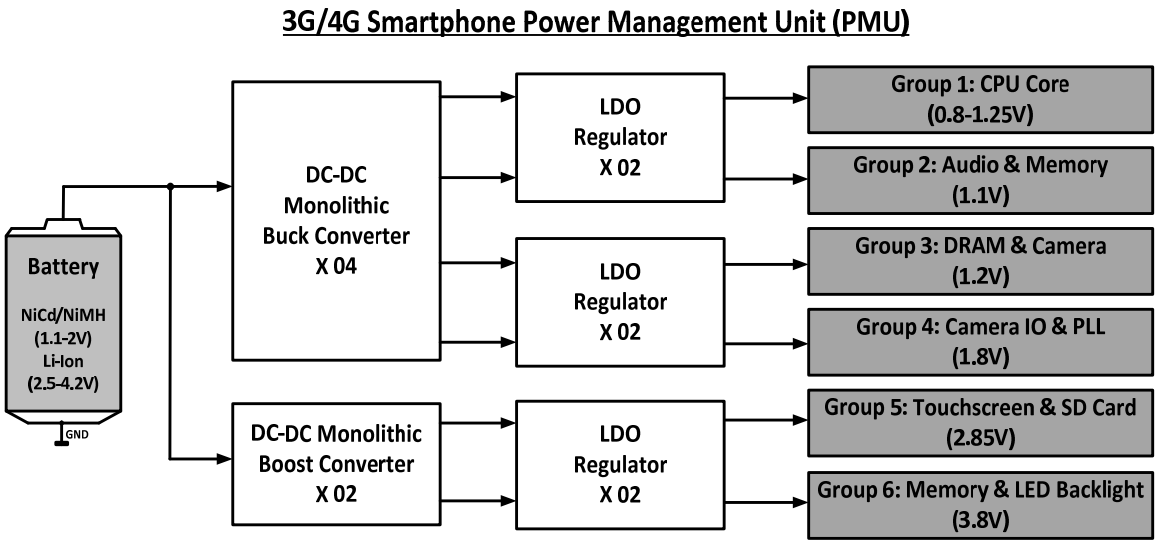

Figure 1. A vital part of the 3G/4G smartphone power management unit (PMU).

The key to prolonging the battery lifetime is to improve the power efficiency of the DC-DC converter. Since a smartphone spends most of its time in the low load condition [2], numerous research works [11–14] have already aimed to improve the light-load efficiency as the core priority. Though the new circuit implementation is novel, improvements in power efficiency are minimal, and the proposed circuit techniques are relatively complex. One of the more interesting works proposed [15] a width-switching scheme whereby the width of the respective power transistors can be altered according to the load current demand. However, the light-load efficiency falls below 80% for <20 mW of load power. In another study [16], pulse-skipping modulation (PSM) was added in between PWM and PFM to ensure a seamless transition of the power efficiency curve from a low to high load current. This technique is well known as the tri-hybrid mode converter, which can deliver high efficiency for a wide load range. On the other hand, it has drawbacks, too. Whenever it transits to PSM mode, load regulation is always sacrificed, and the power conversion efficiency is only maximized in several load conditions. Lastly, tri-hybrid mode control requires several modulators with complex-mode switching circuits, which may lead to stability issues, e.g., inductor runaway.

Hence, in this current research work, a twin frequency control scheme (TFCS), together with an accurate load current sensing block (ALCS), are proposed to achieve high efficiency under a low load condition (<50 mW) regardless of the process/power transistor variation as well as the source voltage or load current variation. This is compatible with the fact that smartphones drive these ranges of power load levels during their idle conditions. For proof of concept, a monolithic buck converter with the proposed TFCS and ALCS are implemented and tested. Furthermore, a conventional PWM/PFM buck controller is implemented to provide a good comparison with our proposed work. The design and measurement details are presented in this paper in the following structure: Section 2 discusses the operation of the system and block level design. Section 3 presents the experimental results, followed by a discussion and comparison with the state-of-the-art works, as summarized in Table 1. Finally, the conclusion will be shown in Section 4.

Table 1. Performance summary and comparison.

	Unit	TPEL [17]	JSSC [18]	TCAS I [19]	This Work
Year	-	2017	2018	2022	2023
Technology	µm	0.13 (CMOS)	0.13	0.18 (BCD)	0.18 (CMOS)
Input Voltage	V	2.2~3.3	1.8~3.3	2.7~4.7	2.0~3.0
Output Voltage	V	1.7	1.2	1.6	1.25
Peak Efficiency@Load Current	%	90.4@10 mA	84.0@100 µA	92.1@10 mA	92.7@30 mA
External Inductor	µH	3.0	18	4.7	47.0
External Capacitor	µF	3.0	0.056	4.7	10.0
Frequency	kHz	2500	3000–5500	4000	250
Chip Silicon Area	mm^2	0.656	0.2576	0.55	1.3
Power Transistors Implemented in This Work:					
Size	Unit	M_N	$\frac{21{,}168\ m}{0.35\ m}$	M_P	$\frac{35{,}672\ m}{0.30\ m}$
Finger Width	µm	19.6	-	19.6	-
No. of Fingers	-	60	-	91	-
Multiplier	-	18	-	20	-
Channel Resistance	mΩ	$R_{on,n}$	80	$R_{on,p}$	95
Bonding Wire Resistance [1]	mΩ	$R_{bond,n}$	200	$R_{bond,p}$	200
Total Resistance [2]	mΩ	$R_{overall,n}$	280	$R_{overall,p}$	295
Total Gate Capacitance [3]	pF	C_{gn}	477.8	C_{gp}	574.3

[1] Wire bonding performed using A*STAR IME—Au (Gold) Wire (1 mil diameter and 650 mA/cm). [2] Impedance and inductance for a bonding wire per unit cm are 1 Ω and 10 nH, respectively. [3] Post layout extraction, including bond pads (performed using Calibre). Other remarks: process has 6 metal layers (EMI: M1–M5 → 1 mA/µm, M6 → 5.34 mA/µm at 30 °C).

2. Proposed Twin Frequency Control DC-DC Buck Converter

Our proposed work, shown in Figure 2, consists of a twin frequency control scheme (TFCS), an accurate load current sensing (ALCS) block, a switched capacitor (SC) integrator, two deadtime controllers and the power train stage. In general, the output voltage, V_{out}, gives important information about the load current, and this will be sensed by the proposed load current sensing block to produce a sensing voltage, V_{sense}. Furthermore, this voltage, in turn, is compared with a 4-bit thermometer code ADC to produce a 4-bit signal (S_0, S_1, S_2 and S_3). This gives an accurate indication of the load current level drawn by the output of the DC-DC converter. The 4-bit signal goes through the TFCS, which yields two non-overlapping clocks to control the switches in the switched-capacitor integrator and also a clock frequency to reset the integration cycle. In other words, it is meant to define the switching period of the buck converter. The integrated voltage, V_{int}, monitors V_x, which gives an indication of the output load current and its corresponding voltage level. The integrated voltage, V_{int}, can be derived as follows:

$$V_{\text{int}} = \frac{1}{R_{eq}C_2}\int_0^T V_x dt \tag{1}$$

$$= f_{\phi_{A/B}} \cdot \frac{C_1}{C_2}\int_0^{Int_1 T_s} V_x dt \tag{2}$$

$$\therefore V_{\text{int}} = f_{\phi_{A/B}} \cdot \frac{C_1}{C_2} \cdot V_{BATT} \cdot Int_1 \cdot T_S \tag{3}$$

where V_{int} is the integrated voltage and the output of the SC integrator. $f_{\varnothing_{A/B}}$ is the frequency of the switches in the SC integrator, and $\frac{C_1}{C_2}$ is the ratio of the capacitor, which gives the gain of the amplifier. V_{BATT} refers to the input voltage of the DC-DC buck converter. Int_1 and T_s refer to the integration and switching period of the converter, respectively.

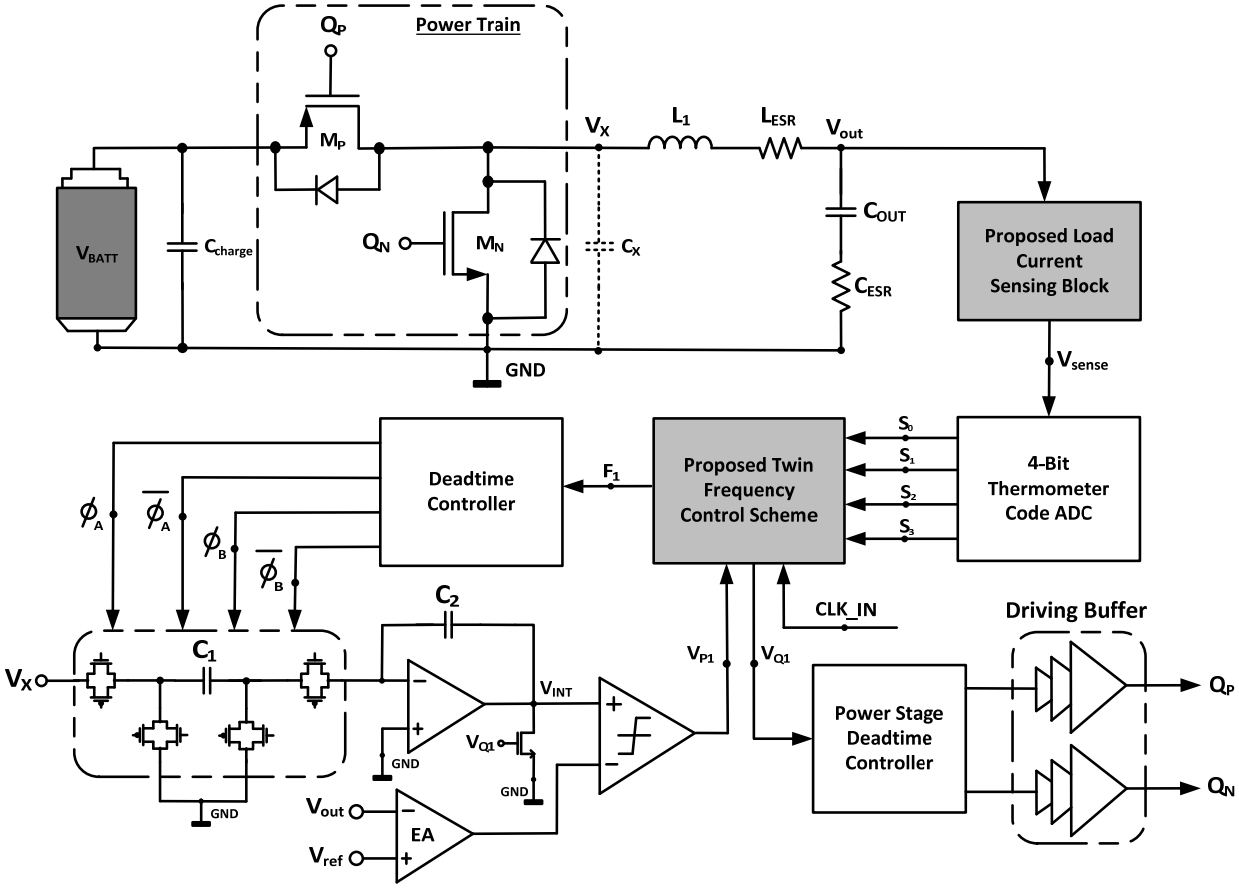

Figure 2. Proposed twin frequency control DC-DC buck converter using accurate load current sensing technique.

With reference to Equation (3), it is evident that the ratios of capacitors are constant under any circumstances such as heavy or light load. The remaining parameters, except V_{BATT}, are variables which will change according to the DC load power drawn by the output of the converter. Specifically, in a light load condition, the above-mentioned 4-bit signal (S0, S1, S2 and S3) will activate the proposed TFCS. This will alter the switching frequency of the DC-DC converter and the corresponding switches in the SC integrator. Hence, the switching losses of the buck converter will be significantly reduced in a low current load condition. This will improve the power efficiency for the load range (<50 mW) where the smartphone is idling.

2.1. Proposed Accurate Load Current Sensing (ALCS) Block

The proposed ALCS, shown in Figure 3, is an extension and improvement to a prior work [20]. A more in-depth analysis with regard to the prior work of current sensing techniques will be presented in Appendix A. It is used to sense the load current and gives an output sense voltage, V_{sense}, via the sensing resistor, R_{sense}. This voltage level is proportional to the load current level. Transistors M_{P1}–M_{P4} and M_{N1}–M_{N3} form a current conveyor structure where negative feedback is employed, which forces the node voltage V_1 to be equal to V_2 at a balanced state equilibrium. If the V_2 node increases, the drain voltage of the MP3/the gate voltage of M_{P1} will increase since the transistor M_{N1} will force

the mirrored current going through M_{N3} to be the same. This action allows for a larger net current to go through M_{P2}, which becomes mirrored over to M_{P3}. Hence, the gate voltage of M_{P3} decreases, which pulls node voltage V_3 down. This constitutes negative feedback and forces V_2 to be equal to V_1. At the same time, the cascode pair, M_{P5} and M_{P6}, is included to increase the output impedance of the current mirror formed by M_{P7} and M_{P8}. This will ensure a more accurate mirroring of the current, behaving more like an ideal current source. Thus, transistors M_{N6}–M_{N7} are stacked on top of M_{N4}–M_{N5} to form a diode-connected configuration. This is at the expense of M_{N4}–M_{N5} being biased in the linear triode region, with a larger transistor length value.

$$I_S = \frac{V_{out} - V_1}{R_S} \tag{4}$$

$$I_{S1} = \frac{V_{out} - V_2}{R_{load1}} \tag{5}$$

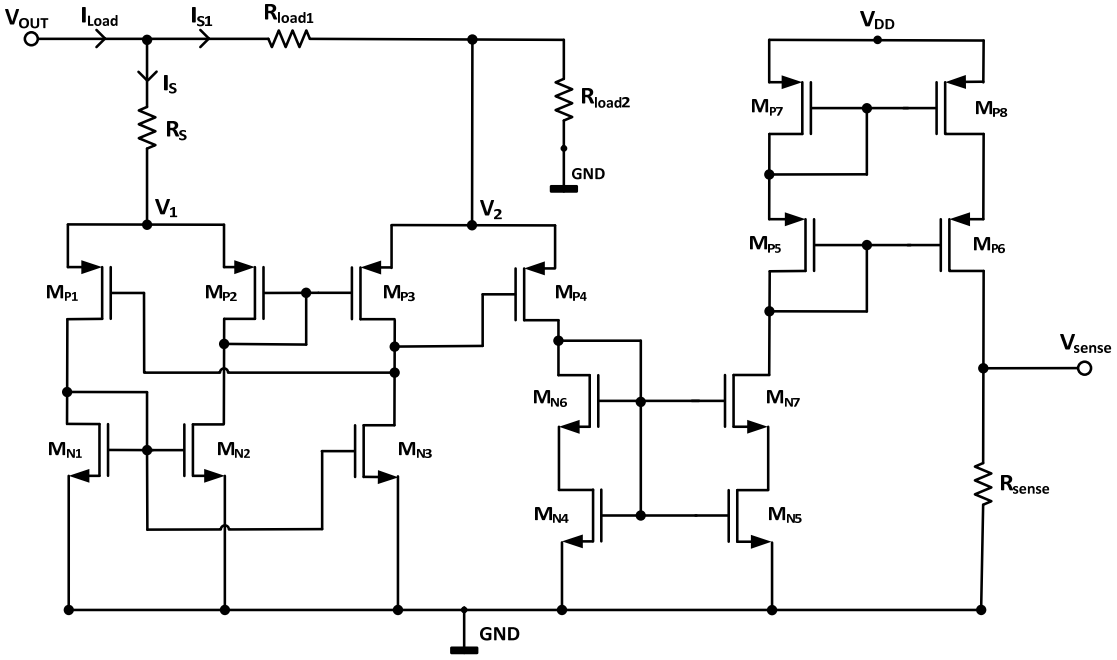

Figure 3. Accurate load current sensing (ALCS) block.

Assume V_1 to be equal to V_2:

$$I_S = \frac{I_{S1} \cdot R_{load1}}{R_S} \tag{6}$$

$$I_{Load} = I_S + I_{S1} \tag{7}$$

Substitute Equation (6) into (7) to obtain

$$I_{Load} = I_{S1}[1 + \frac{R_{load1}}{R_S}] \tag{8}$$

The output voltage, V_{out}, can be derived as follows:

$$V_{out} = I_{S1} \cdot \{R_{load1} + R_{load2} - \frac{R_{load1}}{R_S} \cdot R_{load2}\} \tag{9}$$

If the ratio of the resistance $R_{load1}/R_S << 1$, Equation (8) becomes

$$I_{Load} \approx I_{S1} \tag{10}$$

At the same time, Equation (9) is simplified as

$$\therefore V_{out} \approx I_{Load} \cdot R_{load,total} \tag{11}$$

whereby $R_{load,total} = R_{load1} + R_{load2}$.

The above derivation proves that the two passive resistors, R_{load1} and R_{load2}, contribute to the total load resistance without excessive power dissipation, which will degrade the power efficiency of the overall DC-DC buck converter. Furthermore, the current, I_s, going through R_s is negligible, having minimal impact on the overall power efficiency. Hence, the sense voltage, V_{sense}, can be derived to be

$$V_{sense} = \frac{1}{2} \cdot I_S \cdot R_{sense} \tag{12}$$

Substituting Equation (6) into (12) obtains the following:

$$V_{sense} = \frac{1}{2} \cdot [\frac{R_{sense} \cdot R_{load1}}{R_S}] \cdot I_{S1} \tag{13}$$

If the ratio of the resistance $R_{load1}/R_S = N_1$,

$$V_{sense} = A_1 \cdot I_{Load} \tag{14}$$

where $A_1 = \frac{1}{2} \cdot N_1 \cdot R_{sense}$ is a constant.

The above derivation of the sense voltage, V_{sense}, can be used to provide a voltage that is proportional to the load current. The power dissipation across the passive sensing resistor, R_{sense}, is negligible as the current, I_s, going through it is minimal. However, this sensing technique may have some drawbacks.

The above derivation and working operation assume that the output voltage, V_{out}, is a constant value. But, in fact, there are some AC ripples riding on it. This is caused by the product of the inductor current ripple and the ESR of the output filtering capacitor. Thus, to ensure a more accurate load current sensing capability, the inductor value is made relatively larger to reduce the ripples riding on the output voltage. Furthermore, trimming techniques are employed for the resistor, R_{sense}, as its value may differ by ±20% after the process of die fabrication. Therefore, careful consideration has to be taken into account when designing the next block as the resistor's value due to the process, and the voltage supply and temperature (PVT) variation should never exceed the 1-bit resolution of the ADC stage. The W/L sizing of each transistor is shown in Table 2.

Table 2. Transistor Sizing (W/L) Ratio.

Transistor No	W/L Sizing
M_{P1} to M_{P4}	4 µm/10 µm
$M_{N1,}$ $M_{N2,}$ M_{N3}	2 µm/10 µm
$M_{N4,}$ $M_{N5,}$ M_{N7}	1 µm/5 µm
M_{N6}	1 µm/20 µm
M_{P5} to M_{P8}	2 µm/10 µm

2.2. Four-Bit Thermometer Code ADC

The 4-bit thermometer code ADC, shown in Figure 4, is employed to compare the sense voltage, V_{sense}, with four voltage levels (V_{r0}, V_{r1}, V_{r2} and V_{r3}) to generate a 4-bit

thermometer code signal (S_0, S_1, S_2 and S_3). This gives vital information about the current load level. There are basically four different levels (0001, 0011, 0111 and 1111) which correspond to four different light load conditions. The resolution of the load current level can be improved at the expense of increasing the no. of comparators in the ADC, which will increase conduction and switching losses that may degrade the power efficiency. Hence, there exists a tradeoff between better resolution and power efficiency.

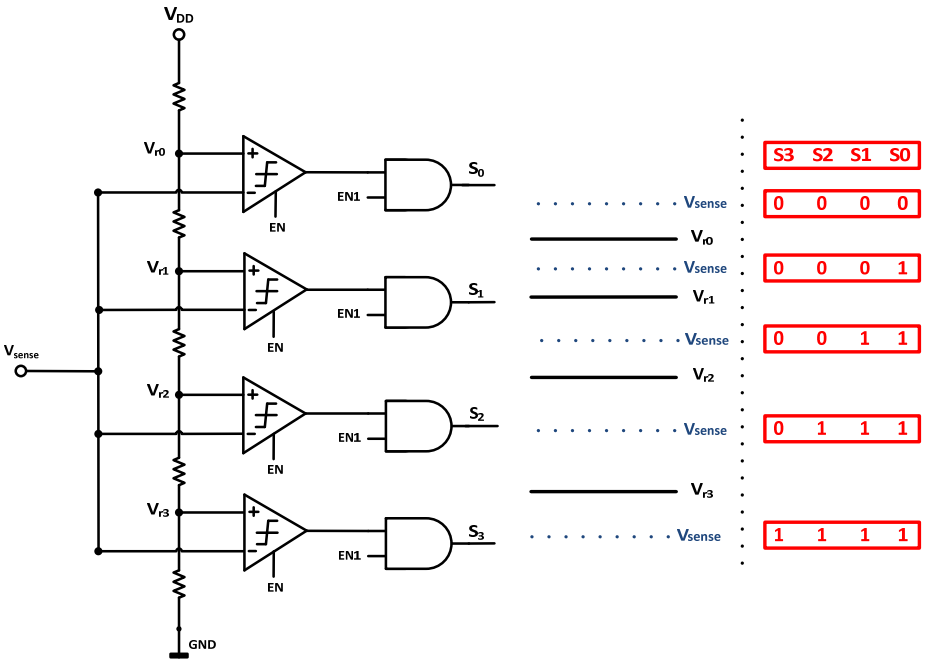

Figure 4. Four-bit thermometer code ADC.

2.3. Proposed Twin Frequency Control Scheme (TFCS)

The proposed TFCS, shown in Figure 5, is used to progressively alter the switching frequency of the buck controller and the integration cycle according to the load current, which is embedded in the 4-bit signal level (S_0, S_1, S_2 and S_3). There are only four possible signal levels (0001, 0011, 0111 and 1111) which correspond to four different load current levels in the light, idle condition of a smartphone (<40 mA). As mentioned, the resolution of the load current level can be improved further, but at the expense of increased power consumption. Hence, there exists an optimum value for the no. of levels of load current associated with the signal generated by the thermometer code ADC.

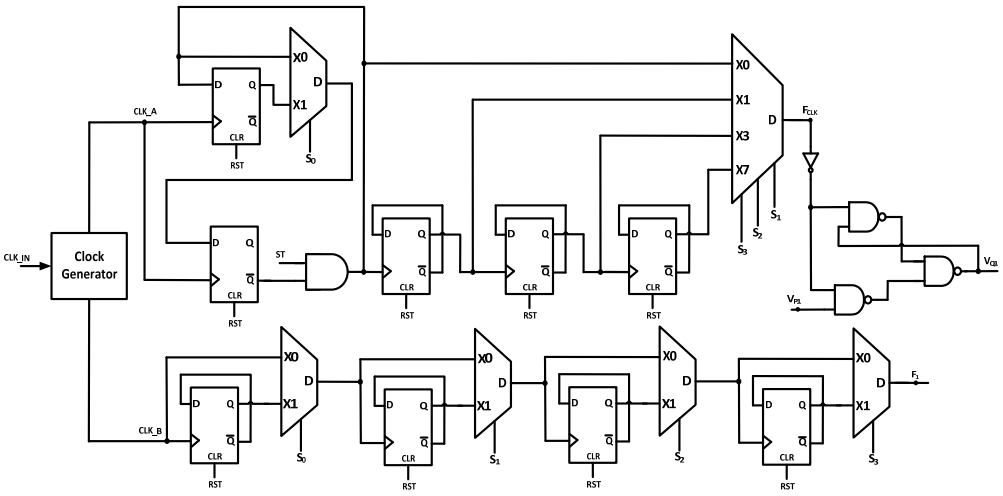

Figure 5. Proposed twin frequency control scheme (TFCS).

2.4. Power Train

The power train consists of one PMOS (M_P) and NMOS (M_N) device, as shown in Figure 2. Both are 3.3 V transistors, which have a thicker gate oxide and occupy a much larger area than a regular transistor. Considering the power NMOS transistor, M_N, the total power loss comprises the sum of the switching and conduction loss as follows:

$$P_{total\_loss} = C_{gdn} \cdot W_N \cdot V_N^2 \cdot f_S + C_{gsn} \cdot W_N \cdot V_N^2 \cdot f_S + (C_{gdn} + C_{dbn}) \cdot W_N \cdot V_{BATT}^2 \cdot f_S + \frac{I_N^2 \cdot R_{on,N}}{W_N} \quad (15)$$

whereby C_{gdn}, C_{gsn} and C_{dbn} refer to the respective parasitic capacitance per unit width of the device, V_{BATT} is the input voltage to the buck converter, f_s refers to the switching frequency of the power train, $R_{on,N}/W_N$ is the on-resistance per unit width, I_N refers to its RMS current and V_N is the gate voltage of the power NMOS transistor. Thus, the optimum width, $W_{opt,N}$, can be calculated when the switching loss is equal to the conduction loss, given by

$$W_{opt,N} = \sqrt{\frac{I_N^2 \cdot R_{on,N}}{C_{gdn} \cdot V_N^2 \cdot f_S + C_{gsn} \cdot V_N^2 \cdot f_S + (C_{gdn} + C_{dbn}) \cdot V_{BATT}^2 \cdot f_S}} \quad (16)$$

The optimized width for both the power NMOS and PMOS is shown in Figure 6, where the graph of the switching loss intersects the conduction loss. The graph plot is based on the highest load current of 40 mA and a switching frequency of 1 MHz. The aspect ratio and the on-resistance of the power transistors are shown in Table 1. In addition, the on-resistance and input parasitic capacitance required to calculate the conduction and switching loss, respectively, are the sum of the simulation results and a theoretical calculation of the resistance/capacitance of metal routing/contact/via and the silicon area occupied by the layout of the power train. Since the optimized width was finalized, it is now vital to find the best layout structure of the power train for our research application.

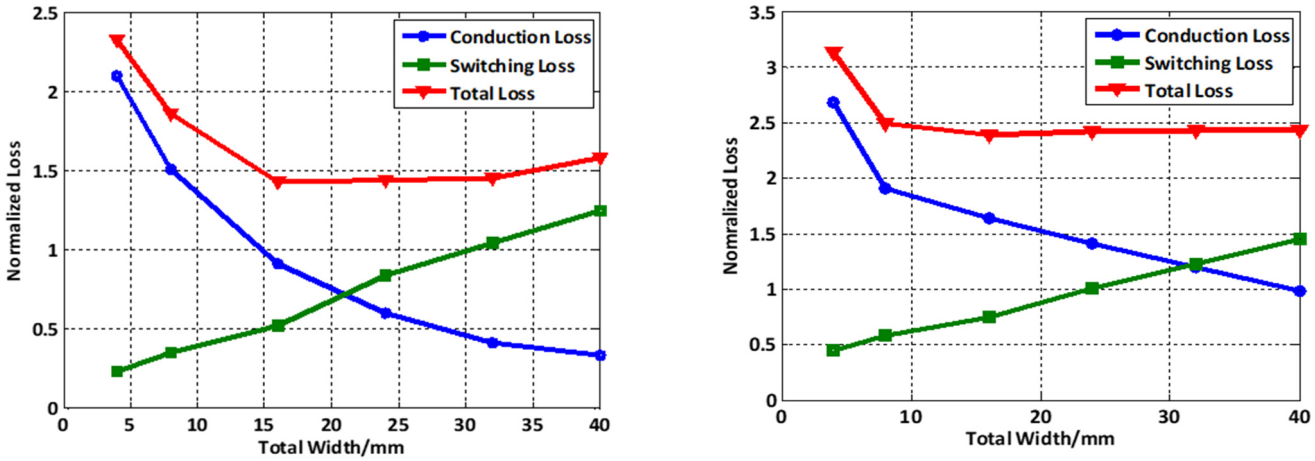

Figure 6. Optimized sizing of (**a**) NMOS power transistor; (**b**) PMOS power transistor.

The efficiency of the power train is vital and depends largely on the layout structure, which is a compromise between the total gate charge (Q_g) and the on-resistance (R_{on}) of the power transistors [21]. This is because the area (W·L) of the power transistor is proportional to the total gate capacitance but inversely proportional to the on-resistance of the power transistor. Recent research [22] proves that power transistors, which do not take into account the resistance and parasitic capacitance of metal routing, will have an error variation of more than 50% in the calculation of Q_g and R_{on}. This is because the impact of the parasitic capacitance and resistance from layers of metal interconnection is

extremely dependent upon the layout style of the power transistors and the positioning of its external source/drain connections. At the same time, the R_{on} value is greatly affected by the distributed parasitic resistance associated with metal interconnects to the source and drain terminals. Many past research efforts [23–25] aimed at improving and optimizing the layout of the power transistor to minimize the parasitic resistance and capacitance.

Traditionally, power transistors were designed with a multi-finger layout structure to maximize the channel width per unit area, which increases the current handling capability. On the other hand, a regular waffle layout structure was introduced [24] to further optimize the width per area ratio by having four neighboring transistors, enclosing a centralized localized one. However, the above-mentioned layout structure does not yield the best optimum tradeoff between the total gate capacitance (Q_g) and the on-resistance (R_{on}). Thus, in a recent research work, there was an interesting proposal for a hybrid waffle layout structure [26,27], which proves that it can best optimize the tradeoff between the area, total gate charge and on-resistance.

However, in this research work, the above-mentioned hybrid waffle layout may not be suitable, as this buck converter is not operating at an extremely high frequency (>100 MHz). Hence, our proposed layout is a tapered/matrix structure, as shown in Figure 7, as it can provide a more uniform distribution of the DC current among the fingers of the transistor. In addition, the fingers of the power transistor are designed in a diagonal way, which will reduce the on-resistance and equalize the flow of current on the opposite side of the device. Furthermore, the nos. of fingers and multipliers for each power transistor are optimized, as shown in Table 1, so as to balance the tradeoff between the total gate charge and parasitic interconnection resistance. One of the drawbacks is that there is a "hotspot" at the corner, furthest away from the center of the power train. During measurement testing, this "hotspot" may increase the on-resistance of the power transistor, leading to an increase in the heat dissipation and ultimately degrading the power efficiency. Therefore, the die package must be thermally enhanced to avoid the overheating of the silicon die chip or create other reliability issues. However, for our work, it focuses on a smartphone idling state (low load power); hence, the above-mentioned drawback may not be significant.

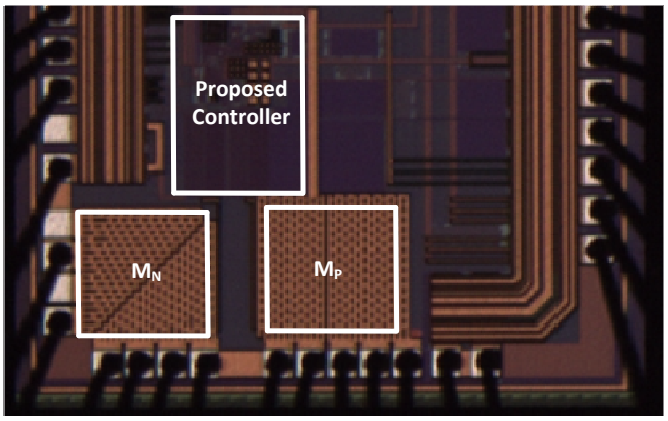

Figure 7. Die photo of the buck converter with proposed TFCS and ALCS.

3. Experimental Results

A buck DC-DC converter with the proposed TFCS and ALCS was implemented with 0.18 µm 1P6M CMOS technology with an area of 1.3 mm^2. The micrograph of the chip is shown in Figure 7. The 2~3 V input and 1.25 V output buck converter utilizes an off-chip SMD 47 µH inductor (Coilcraft Shielded 1812PS Series) with a DCR of <1.0 Ω and a self-resonant frequency (SRF) of 17 MHz. A relatively larger value of an inductor value is selected to reduce the inductor ripple to <50% of the maximum load current. Furthermore, an output off-chip SMD ceramic 10 µF filtering capacitor (AVX Hi-Cap MLCC) has an estimated ESR of ~0.5 Ω. The capacitor type is chosen to be an SMD ceramic capacitor since it is the most inexpensive type compared to tantalum or aluminum electrolytic ones.

However, the tradeoff comes with the relative larger value of ESR, which will lead to a larger peak-to-peak ripple riding on the output voltage of the buck converter. Thus, relatively larger values of the inductor and capacitor are chosen so as to mitigate the ripple problem. Furthermore, this helps to yield a more accurate sensing of the load current, as previously mentioned. Take note that the choice for the type of capacitor varies, depending on the application specification. A prototype of the buck converter with the TFCS and ALCS chip is also presented in Figure 8. It can be observed that our proposed work uses the DIP package with 48 leads. During testing, this is held tightly by the adjustable socket shown in Figure 8.

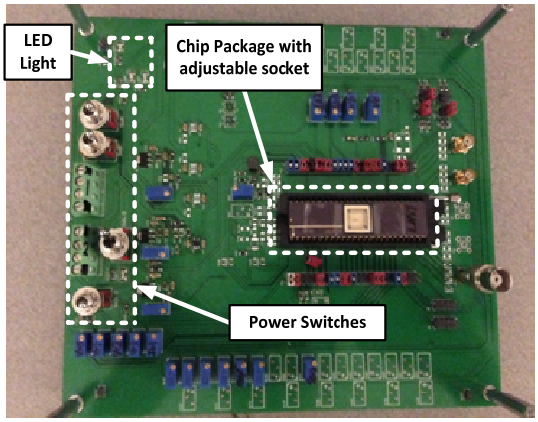

Figure 8. Prototype of a buck converter with proposed TFCS and ALCS.

The performance evaluation is carried out in three general steps: (1) the performance of our proposed TFCS and ALCS is examined in light loading conditions, (2) a comparison of the power efficiency is made between our proposed work and the conventional PWM/PFM controller and (3) the design specification and performance comparison are summarized in Table 1. The proposed TFCS and ALCS allow the frequency to be reduced under different low load conditions. It achieves a peak efficiency of 92.7%, operating at 250 kHz with V_{BATT} = 2 V, V_{OUT} = 1.25 V and I_{LOAD} = 30 mA, as shown in Figure 9. The top waveform is the voltage V_x, while the bottom one shows the integrated voltage V_{int}. This proves that our proposed TFCS and ALCS buck converter is stable and achieved high efficiency under the low load condition. However, taking a closer look at the V_x waveform, there is a significant interval whereby there are body diode conduction losses which degrade the power efficiency. This is because our proposed buck converter uses a fixed deadtime controller. One of our current and future works has therefore included a novel deadtime controller. Furthermore, from Figure 9, it is evident that our proposed controller does not enter DCM operation in a light load condition. The rationale is that for DCM operation, the node, V_x, will oscillate when both the power transistors are idling. This is due to the existence of the LC tank formed by the inductor and the parasitic capacitance at that node. Thus, this will incur additional power losses. Recent research efforts have included another free-wheeling switch [9,28,29] to dampen the sub-harmonic oscillation. However, this will incur an additional silicon area, as the aspect ratio of the additional switch is comparable to the size of a power transistor. Furthermore, it adds complexity to the circuit design, as another control signal has to be included to determine the turning on/off of this free-wheeling switch. Therefore, our proposed work uses a relatively larger inductor value to reduce the ripple at the output voltage of the buck converter while operating in CCM mode. This will allow the proposed ALCS to work ideally, as any undesirable voltage ripple will cause inaccuracies in the sense voltage, V_{sense}. This can be considered a minimal tradeoff for our proposed TFCS and ALCS buck converter compared to other research studies in the literature.

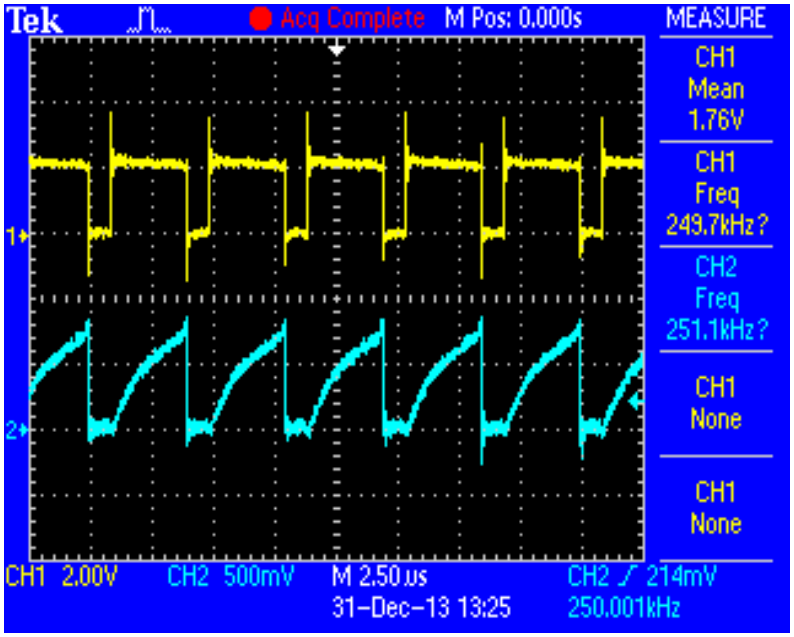

Figure 9. Peak efficiency achieved—waveform of V_x and V_{int} (V_{BATT} = 2 V, V_{out} = 1.25 V, Freq = 250 kHz and I_{load} = 30 mA).

Figure 10 shows the power efficiency between our proposed TFCS and ALCS converter and a conventional PWM/PFM controller under varying load conditions. A peak efficiency of about 92.7% can be achieved when our proposed buck converter is operating at 250 kHz with a 2.0 V input voltage and a 30 mA load current. It can be observed that the efficiency degrades when the input voltage is higher. This is because the buck converter has to dissipate more energy to bring it down to the same output voltage.

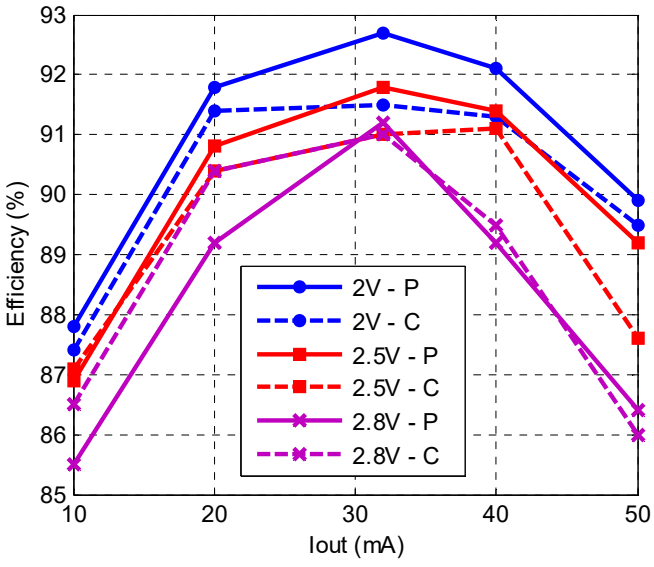

Figure 10. Power efficiency of the proposed TFCS and ALCS buck converter and the conventional PWM/PFM controller under different loading conditions (P—Proposed Work; C—Conventional Work).

The efficiency improvement graph, shown in Figure 11, compares our proposed work with the latest state-of-the-art work [28]. This shows that our improvement in power efficiency ranges approximately from 4 to 6% across a 10~50 mA load current. Our proposed specification and performance are summarized in Table 1. It clearly shows that the proposed TFCS and ALCS technique yields an improvement in the power efficiency

(4~6%) compared to some of the latest state-of-the-art research work [17–19]. However, one drawback is the fact that the external inductor and capacitor are relatively larger in our proposed work so as to achieve a smaller peak-to-peak output voltage ripple for a more accurate sensing of the load current. The measured line and load regulation for our proposed work are about 21 mV/V and 0.53 mV/mA, respectively. The output voltage recovery time subjected to a sudden load change from no load to full load is <20 µs.

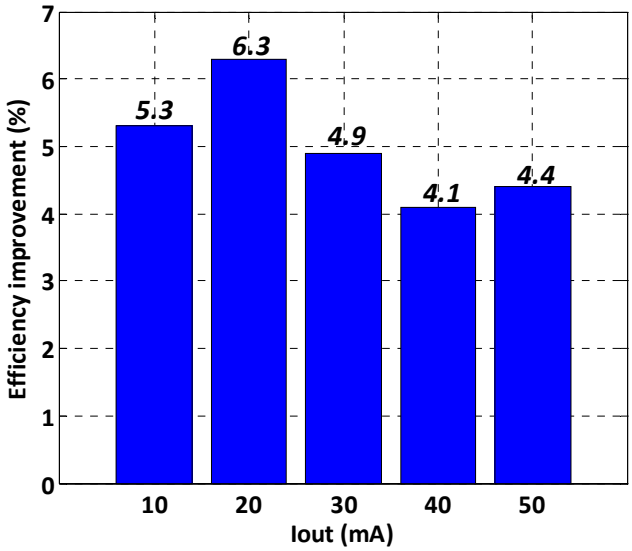

Figure 11. Efficiency improvement of the proposed TFCS and ALCS buck converter compared to the latest state-of-the-art work [28].

4. Discussion and Conclusions

One area of improvement is to use the MOSFET segmentation technique proposed in [30–32], which can help to further improve the power conversion efficiency. At the same time, our proposed work is not optimized for deadtime control; hence, there is ongoing current research into designing a deadtime controller to minimize body diode conduction loss, which will improve efficiency. This ongoing work into deadtime control is a continuation of this proposed work. In addition, the simulation results for the power efficiency of our proposed work are about 2~3% better than our testing results. The rationale for this margin is due to the power loss in the resistance of the Au (Gold) wire bonding, the DIP package leads and the resistance in the traces of the PCB board. Careful consideration, recommended by [33], has been taken into account when designing the PCB board so that important power/ground lines have as short but as wide a trace as possible to minimize unnecessary power losses. Overall, our proposed TFCS and ALCS indeed yield an efficiency improvement over some of the latest research works, though with a relatively larger external inductor and filtering capacitor. At last, a buck DC-DC converter with the proposed TFCS and ALCS has been designed and implemented with 0.18 µm 1P6M CMOS technology, occupying an area of 1.3 mm^2. It yields a peak efficiency of about 92.7% when the buck converter is operating at 250 kHz with a 2.0 V input voltage and a 1.25 V output voltage with a load current of 30 mA. The proposed buck converter is implemented and dedicated for smartphone application, whereby it spends most of its time under idle, low load conditions.

5. Future Work

One aspect of future work is to design and implement envelope tracking, which is important for smartphone applications, whereby it uses 3G/4G technology. For the proposed work in this thesis, it focuses more towards achieving higher power efficiency by optimizing body diode conduction, reverse inductor current and better delivery for a wide range of load currents. The next aspect of future work includes working on the circuit block

of the battery charger, which comprises the detection mechanism for a low battery shelf life. Another aspect of future work will focus on the safety aspect of the DC-DC converter, which consists of over-current and over-voltage protection circuits. In addition, since the power transistors are drawing a huge amount of current and causes the overheating of the PCB board, thermal management has to be employed to ensure long-term reliability. This also includes employing on-chip temperature sensors to detect hot-spots during chip measurement. The final aspect of future work is to design on-chip LDO regulators, which can be used for silicon-on-chip (SoC) integration and yet be able to yield high PSR values at frequencies above 10 MHz.

Author Contributions: Conceptualization, C.L.K.; Supervision, L.S. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Data Availability Statement: Data are contained within the article.

Acknowledgments: Our team would like to express our deepest gratitude to Global Foundries and the Singapore Economic Development Board (EDB) for supporting our research work.

Conflicts of Interest: The authors declare no conflict of interest.

Appendix A

Sensing the inductor current in a buck converter is an important function of the DC-DC controller. Its current-sensing circuit should be easy to implement without increasing the form factor. Furthermore, the current sensor has to be fast for a high-switching frequency DC-DC converter in order to reduce the inductor size. Past research works yielded many interesting current sensing techniques. One of them is to sense the on-resistance of the power transistor directly [34], but the drawback lies in the fact that the resistance value may change significantly by ±30% due to the PVT variation during the fabrication of the die. Hence, this technique is unreliable. Another work [35] instead proposed a novel self-learning technique to sense the instantaneous induct current via the parasitic resistance (DCR) of the inductor. One of the benefits include minimal power losses and thus makes it applicable to varying loading conditions. In addition, it completely eliminates unnecessary losses by not introducing any additional passive components in the power line. However, it requires a very complex circuit implementation, which occupies a large silicon area overhead. At the same time, the more widely used approach is based on the sensing of the current [36–38] that passes through the power transistor. It employs the use of matched current mirrors and a high gain amplifier to mirror a fraction of the current going through the respective power transistor to the sensing transistor. However, one of its disadvantages is that its accuracy is poor, as it depends heavily on the matching performance of the current mirror in the ohmic region. Furthermore, channel-length modulation and process mismatch will induce an error of >15% [39]. On the other hand, there is a proposed use of a current offset cancellation technique [40] to further improve the accuracy of current sensing. However, one of its minor drawbacks is the relatively larger quiescent current required to provide the driving capability, which leads to a degradation in the power efficiency. Hence, it suffers an imminent tradeoff between speed and accuracy. Some other techniques employ the advantage of the availability of a bipolar transistor in the BiCMOS process [41] to enhance the accuracy of its current sensing capability. This, however, proves to be too costly to implement. There is also a filter approach, which senses the current in a continuous mode [42] by applying an inductor voltage across a tuned low-pass filter and by sensing the filter current. One of its advantages is that it has minimal switching noise, but its inherent accuracy is highly dependent on the DCR of the inductor and the tuning accuracy of the filter, which may lead to a variation of >±20%. One of the more recent works [19] uses a tri-mode operation (PFM, PWM and DGM) to handle a 100,000× load range. It works on the fact that by reducing the comparator current, a delay-based hysteresis window adaptive to the load current is generated, thereby reducing the total

switching power loss. However, this converter is implemented in 0.18 um BCD technology, which is too costly for us to handle, and the power efficiency seems to degrade drastically under very light load conditions (<100 μA). At the same time, there are other converters which are capable of providing a wide load range with good efficiency and consuming a very low quiescent current, which will no doubt be the major power consumption in sensing or low load mode [17,18,43–48].

However, in our proposed TFCS and ALCS DC-DC buck converter, it employs a very accurate ALCS circuit, which is an extension and improvement to the prior work [20]. It is able to achieve high accuracy in the current sensing at the tradeoff of a slightly higher quiescent power consumption and a larger inductor value so as to minimize the output voltage ripple, which will lead to inaccuracies in the sensing voltage, V_{sense}.

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