MDPI

Article

Parasitic-Based Model for Characterizing False Turn-On and Switching-Based Voltage Oscillation in Hybrid T-Type Converter

Amir Babaki [1], Mohammad Sadegh Golsorkhi [1,*], Nicklas Christensen [2], Mehdi Baharizadeh [1], Stefan Behrendt [3], Jesco Beyer [4] and Thomas Ebel [1]

[1] Centre for Industrial Electronics (CIE), Institute of Mechanical and Electrical Engineering, University of Southern Denmark, 6400 Sonderborg, Denmark; amirbabaki@sdu.dk (A.B.); smbaharizadeh@sdu.dk (M.B.); ebel@sdu.dk (T.E.)
[2] Danfoss Drives A/S, 6300 Grasten, Denmark; nicklas.christensen@danfoss.com
[3] Semikron Danfoss, Husumer Straße 251, 24941 Flensburg, Germany; stefan.behrendt@semikron-danfoss.com
[4] FuE-Zentrum FH Kiel GmbH, Schwentinestr. 24, 24149 Kiel, Germany; jesco.beyer@fh-kiel.de
* Correspondence: golsor@sdu.dk; Tel.: +45-65507529

Abstract: High frequency and high voltage switching converters utilizing wide bandgap semiconductors are gaining popularity thanks to their compactness and improved efficiency. However, the faster switching requirements gives rise to new challenges. A key issue is the increased oscillation of the drain–source voltage caused by the switching action of the complementary switch in the same phase or change of state of the other phase switches. The voltage stress caused by these oscillations can damage the switch. Furthermore, the high dv/dt during turning-on of one switch might result in false turn-on of the complementary switch due to the miller effect. In this paper, these issues are investigated in a T-type converter through analytical and experimental analysis. Based on the proposed analytical approach, simple and cost-wise solutions utilizing an optimum design of gate driver circuits and circuit layout modifications can be developed to cope with the aforementioned issues. A comprehensive analytical model of the converter with consideration of parasitic capacitances and inductances is developed. By performing sensitivity analysis on the model, the effect of the parasitic parameters on the drain–source voltage oscillation and gate–source voltage amplitude in case of false turn-on is studied. The validity of the model is then assessed through numerical simulations and experimental results.

Keywords: AC/DC power converters; SiC MOSFET; power electronics; switching model; voltage oscillation

Citation: Babaki, A.; Golsorkhi, M.S.; Christensen, N.; Baharizadeh, M.; Behrendt, S.; Beyer, J.; Ebel, T. Parasitic-Based Model for Characterizing False Turn-On and Switching-Based Voltage Oscillation in Hybrid T-Type Converter. *Electronics* **2024**, *13*, 1808. https://doi.org/10.3390/electronics13101808

Academic Editor: Fabio Corti

Received: 21 March 2024
Revised: 25 April 2024
Accepted: 30 April 2024
Published: 7 May 2024

Copyright: © 2024 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https://creativecommons.org/licenses/by/4.0/).

1. Introduction

Silicon carbide (SiC) semiconductors favor faster switching, lower switching loss and lower turn-on voltage compared with the traditional silicon technology [1–3]. The fast-switching capability of the SiC switches provide the opportunity for developing power electronic converters with high switching frequency and high voltage ratings. Through boosting the switching frequency, the passive components of the converters can be shrunk, hence offering compact and high power density converter design [4,5]. Thanks to the high switching capability of SiC, they can be used in resonant converters, which are widely employed in various applications like electric vehicle battery chargers [6], drive systems [7], and V2X power converters [8]. Furthermore, SiC semiconductors are able to maintain higher junction temperature, which makes them suitable candidates for the compact power electronic converters in integrated motor drive applications [9]. Electro-thermal modeling of SiC-based converters for different power range has been studied in the literature [10–12] in order to improve the thermal performance of such converters.

Despite the aforementioned superior characteristics, the application of SiC semiconductors in high voltage/high frequency converters creates new issues [13]. On the one

hand, the voltage overshoot across the switch's drain–source terminals is higher due to the ultrafast switching (high dV/dt) [14]. The voltage overshoot stresses the switch and can damage the switch if it exceeds the switch voltage rating. On the other hand, unintentional voltage oscillations across the gate–source of a switch during turning-on of another switch might give rise to false turn-on [15,16]. SiC switches are more prone to such false turn-on due to the lower turn-on threshold voltage [17]. False turn-on contributes to cross conduction across two switches in a leg, which increases the losses and might even result in switch failure due to overcurrent [18]. Both drain–source voltage overshoot and false turn-on issues are dependent on the parasitic capacitances and inductances in the circuit layout.

In addition to the abovementioned issues, another challenge is associated with three-phase compact converters which are used in high-power, high-frequency application [19]. In this case, a change in the switching state of switches in one phase gives rise to drain–source voltage oscillations in the switches of the other phases [20,21]. This may have a negative impact on the switch voltage blocking and load current quality. This issue elevates in the case of three-phase PMs, which increase the power density through compact design [22]. In such a compact design, the mutual inductance/capacitance between each two phases of the three-phase converter are intensified, hence elevating the cross-phase voltage oscillations [23]. These oscillations can be mitigated using an active/passive snubber circuit [24,25].

The former issue, false turn-on, can be mitigated using an active Miller clamp technique in the gate driver [26,27]. However, this solution requires a gate driver design specific to the switch characteristics, which increases the cost [28]. Additionally, the reliability of this approach may be compromised depending on the circuit layout [29,30]. An extra isolated voltage source can be connected to the gate–source capacitor during the switch turn-off to maintain the gate–source voltage at less than the turn-on threshold [31]. Despite the improved reliability, the mentioned protection circuit is not cost effective [31]. The drain–source voltage overshoot can be limited within the safe range using a snubber circuit [32–34]. However, the conventional snubber configurations cannot be used in high-frequency applications because of the limitation in power loss and switching speed [35–37]. In practice, the issues associated with the voltage overshoot may be resolved slightly in the converter design stage by employing suitable SiC switches as well as a low parasitic power module (PM) and a PCB layout design [38,39].

Prior to introducing costly solutions such as snubbers, modified gate driver designs, and special circuit layouts, it is important to clarify the necessity of such solutions. A compact electrothermal model has been presented in [40] to characterize the SiC switch, where the whole circuit parasitic effects was not fully considered. Experimental characterization of the SiC switch and its body diode is also presented in [12] using a double pulse test setup, as well as a temperature-dependent physical thermal model in [41]. Although, the mentioned approaches are usable to precisely switch characteristic detection, proposing a general circuit model to determine the impact of the non-optimal layout parameters on the voltage stress and oscillation across the pre-characterized SiC switch is of interest. This paper proposes an analytical study of the mentioned issues to help quantify the drain–source voltage overshoot and gate–source voltage oscillations. The analytical results provide a baseline for assessment of the safe converter operation despite the presence of the drain–source voltage overshoot and the possibility of false turn-on. Based on the proposed analytical approach, simple and cost-wise solutions utilizing an optimum design of gate driver circuits and circuit layout modifications can be developed. This way, the cost of the converter can be reduced without compromising the performance.

The specific contributions of the paper are as follows.

- A general switching model of three-phase hybrid T-Type converter, consisting of SiC MOSFETs and Si IGBTs, is developed, which has not been studied before. This type of front-end converter is chosen due to the comparison results yielded from [42]. All possible effective parasitic components, which are modeled as stray inductances and

switch intrinsic capacitors, are considered in the model. This makes a comprehensive model to be applied to other power electronic converter types.

- Unlike the conventional analytical model of the converter, sensitivity analysis is carried out here to investigate the impact of parasitic capacitances and inductances on the damping and natural oscillation frequency of the switch drain–source and gate–source voltages, simultaneously. This way, the most critical parasitic parameters affecting voltage overshoot and false turn-on are determined using the same analytical model.
- Regarding the proposed built compact converter, a new issue has been raised which is affecting the voltage oscillation characteristics across the switch. Accordingly, the effect of the switching in one phase on the drain–source voltage of the switches in the other phases is investigated in detail by simulating the equivalent circuit model, which was not completely focused in the literature.
- Simulation and experimental results have been carried out to verify the analytical model.

The rest of the paper is organized as follows. The possibility of false turn-on and drain–source voltage oscillation in a T-type converter with consideration of different modulation scenarios is investigated in Section 2. In Section 3, a detailed analytical model of one of the phases of the T-type converter is derived. In Section 4, the analytical model is analyzed to identify the sensitivity of damping and natural oscillation frequency on the parasitic parameters. In Section 5, the single-phase model is extended to three phases to analyze the impact of switching in one phase on the performance of the other phases. Experimental results based on a hybrid T-type converter are presented in Section 6 to validate the analytical and numerical results. Section 7 concludes the paper.

2. Topology-Based Miller Plateau Analysis

To illustrate the mechanism of false turn-on, an active T-type rectifier is considered in this study. The reason for choosing this converter topology is its acceptability in the industry as it has the best compromise between high power density and efficiency, as well as the possibility of reaching the pure sinusoidal supply current with a smaller input filter [36]. The topology of a single-phase active T-Type converter is shown in Figure 1. Switches Q_1 and Q_2 should maintain a high breakdown voltage that is equal to the DC link voltage ($2V_{DC}$) while the breakdown voltage cuts in half (V_{DC}) for the zero-level switches of Q_3 and Q_4. Therefore, SiC MOSFETs are used for Q_1 and Q_2 switches, while Q_3 and Q_4 are Si IGBT.

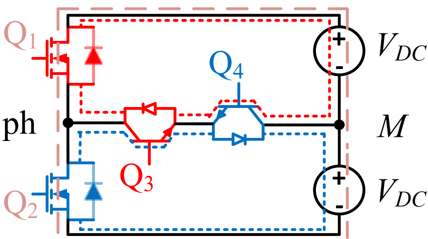


Figure 1. A schematic of a single-phase active T-Type converter.

The zero-voltage level is provided using two back-to-back IGBTs with the same source and different command gate signals. The T-type converter is generally composed of two half-bridges (see Figure 1). The upper side half-bridge loop (red color) includes complimentary switches Q_1 and Q_3 while the lower side half-bridge (blue color) includes Q_2 and Q_4 as the complimentary set of switches. The modulation algorithm depicted in Figure 2 shows that in the positive half cycle of the reference waveform (voltage or current depending on the application), the lower side switch of the leg (Q_2) is always off. Accordingly, during the switching of the upper half-bridge at the positive cycle, switch Q_4 is on. Thus, the current can be conducted in both directions through Q_4. The same situation is considered for the lower half-bridge. According to the control algorithm, switch Q_1 is off during the whole negative half cycle of the reference waveform. Hence, the Q_3 is always

on at this period and can conduct the bi-directional current through itself. Also, the dead time is defined at switching state changes.

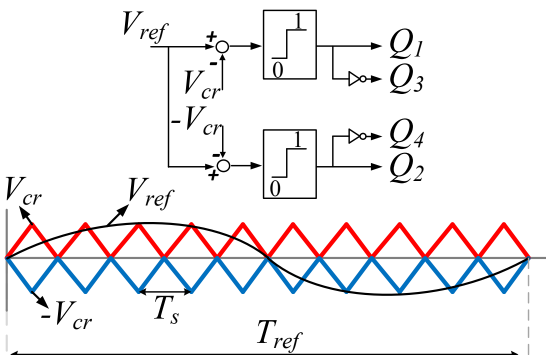


Figure 2. Switching modulation of T-Type.

As mentioned, to protect both half-bridges from shoot-through issues, the dead time is necessary to be considered for switching transient between Q_1 and Q_3, as well as switching states for Q_2 and Q_4. Nevertheless, each switch suffers from false turn-on occurrence after turning-on of the complimentary switch, which also causes unwanted shoot-through. In this paper, the Miller effect is investigated in three cases presented below:

(1) For the upper side half-bridge, where turning-on of SiC MOSFET (Q_1) affects false turn-on of Si IGBT (Q_3);
(2) For the lower side half-bridge, where turning-on of Si IGBT (Q_4) affects false turn-on of SiC MOSFET (Q_2);
(3) For leg switches, where turning-on of SiC MOSFET (Q_1) affects false turn-on of SiC MOSFET (Q_2).

Accordingly, for cases 1 and 2, the gate–source voltage oscillations of switches Q_3 and Q_2 are investigated during the transient turning-on of switches Q_1 and Q_4, respectively. In addition, for case 3, the gate–source voltage oscillations of switch Q_2 should be monitored during the transient turning-on of switch Q_1. During the transient, in all cases, the drain voltage variation of the target switch equals 0.5 V_{dc}. This is found by referring to the switching modulation of the T-type converter. Although the electric model and circuit equations of case 3 are the same as the others, this case is the most extreme one. The reason is that case 3 has fewer switches in the loop, which results in less loop resistance and a lower damping ratio. This means the oscillation amplitude and the possibility of false turning-on magnifies in case 3. In addition, the turn-on threshold voltage of SiC MOSFET is lower than IGBT, which leads case 3 to be more susceptible to a false turn-on. Therefore, as the worst one, case 3 was chosen to be investigated in this paper.

Switch Q_2 is supposed to be off in theory in the transient time of Q_1 turning on. However, the following analysis shows that the induced voltage across the gate–source capacitor of Switch Q_2 may even exceed the turn-on threshold voltage, which results in cross conduction. Repeating the problem in thousands of cycles will damage and even burn the switches. For demonstrative purposes, the parasitic capacitances of switches Q_2, Q_3, and Q_4 are illustrated in Figure 3. Just before a false turn-on occurs, Q_2 is in its off state while $V_{drv,2}$ is considered to be grounded. When Q_1 turns on, the drain terminal of Q_2 faces a high dv/dt, while the source of Q_2 is directly connected to the ground through a leakage inductance. High dv/dt at drain terminal of Q_2 leads to a current passing through gate–drain capacitance (C_{gd2}). The reason is that before Q_1 turns on, Q_3 and Q_4 conducted the current. Accordingly, the drain voltage was V_{dc} when Q_3 and Q_4 were conducting. After turning on Q_1, the drain voltage jumps to $2V_{dc}$, which results in current flow through Q_2 gate resistance, shown as R_{G2} in Figure 3. Exceeding gate resistance voltage from the turn-on threshold voltage of Q_2, this switch is pushed to cross conducting, mistakenly causing a significant switching loss. More detailed analysis of false turn-on in T-type

converters is still challenging in order to improve the reliable performance of the next generation ultra-high frequency converters which will use WBG switches.

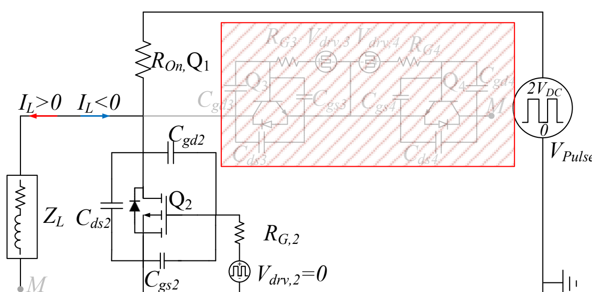


Figure 3. The equivalent circuit for Q_2 false turn-on demonstration considering parasitic capacitances.

3. Developed Model-Based Study

This paper aims to reveal the effective switch's parameters or PCB layout leakages on false turn-on and voltage oscillation characteristics across the drain–source of the switch. Here, this is carried out by assessing the dependency of the natural frequency, ω_n, and damping ratio, ζ, on the switch's intrinsic parameters (C_{ds}, C_{gs}, C_{gd}) and circuit leakage inductances. The simple and developed models considering all parasitics are analyzed mathematically in the following.

3.1. Simple Circuit Model

Based on the abovementioned, an abrupt turn-on of Q_1 results in high positive voltage derivative at the drain terminal of Q_2. Q_1 turn-on time depends on the turn-on gate resistance the switch's intrinsic capacitances. In addition, the gate–source voltage of Q_2 during turning-on of Q_1 is affected by the gate resistance and C_{gd} dv/dt, which is considered as induced current. The well-known first-order circuit at this transient time (Q_1 turn-on) is illustrated in Figure 4, to study parasitic negative effects on induced gate–source voltage amplitude. The transfer function of the mentioned model using the Laplace form is as follows:

$$\frac{V_{gs2}(s)}{V_{ds2}(s)} = \frac{sR_{G2}C_{gd2}}{1 + sR_{G2}\left(C_{gd2} + C_{gs2}\right)} \quad (1)$$

$V_{ds2}(s)$ and $V_{gs2}(s)$ are the drain–source voltage and gate–source voltage of switch Q_2, respectively. Variable s in Equation (1) can be replaced by $j\omega$ to achieve the frequency response function as:

$$\frac{V_{gs2}(j\omega)}{V_{ds2}(j\omega)} = \frac{j\omega R_{G2}C_{gd2}}{1 + j\omega R_{G2}\left(C_{gd2} + C_{gs2}\right)}. \quad (2)$$

In order to decrease false turn-on possibility, the absolute gain value of Equation (2) needs to be as low as possible. This guarantees V_{gs2} to be less than the turn-on threshold voltage of Q_2. Referring to Equation (2), it is obvious that false turn-on possibility may decrease by lower gate–drain capacitor, C_{gd2} while it increases by low gate–source capacitor (C_{gs2}) values. The experimental and analytical results in next sections will verify the findings here.

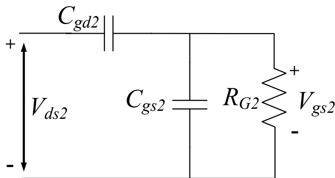


Figure 4. Simple circuit model of Q_2 in the OFF state.

It should be mentioned that the model illustrated in Figure 4 is not complete due to lack of drain–source capacitor, C_{ds2}, and also the circuit leakage inductances. The latter has a considerable effect on V_{ds} oscillation in some circuit topologies [43]. The following developed model is investigated in the circuit using SiC switches to comprehensively evaluate which condition is more prone to the occurrence of the false turn-on and voltage oscillation.

3.2. Higher Order False Turn-On Model Considering Parasitic Parameters

The C_{gd} dV/dt circuit shown in Figure 5 is used to analytically and experimentally investigation of SiC MOSFET's false turn-on in one leg. In theory and simulation, the ON and OFF states of Q_1 are modeled by a pulsating voltage source series to ON resistance whose value can be extracted from the switch datasheet document, in practice. The value of R_1 is adjusted during the analysis such that the in-mind dv/dt is applied to the drain terminal of Q_2. The gate terminal of the Q_2 is connected to the ground through a gate resistor, R_{G2}. The induced gate–source voltage (V_{gs2}) of Q_2 is studied by changing dv/dt at the drain terminal of Q_2. Using this technique, the maximum eligible dv/dt across the switch can be obtained in which the switch is still free of cross conduction.

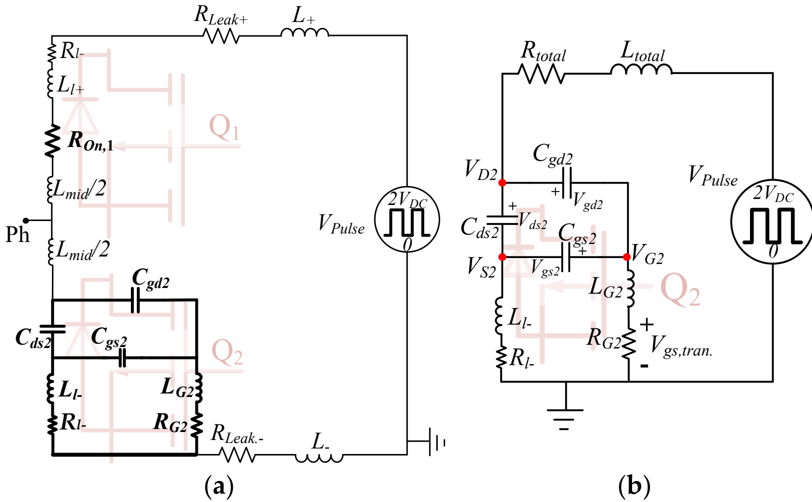


Figure 5. C_{gd} *dV/dt* test; (**a**) circuit model with all possible parasitic elements, (**b**) complete circuit model.

The circuit shown in Figure 5a is the complete model of the structure illustrated in Figure 3, which includes all the parasitic capacitors of the switch as a result of using DOL technology for the die switch planting process, as well as the parasitic inductance because of the single layer conducting track. Figure 5b illustrates a rearrangement of the elements in Figure 5a in which Q_2 is off. Now, the step responses of both V_{gs2} and V_{ds2} in terms of the input step voltage are derived. By applying KCL to nodes, the following equations can be extracted:

$$\frac{V_p - V_{D2}}{sL_{total} + R_{total}} = sV_{ds2}C_{ds2} + sV_{gd2}C_{gd2}, \tag{3}$$

$$sV_{gd2}C_{gd2} = V_{gs2}sC_{gs2} + \frac{V_{G2}}{sL_{G2} + R_{G2}}, \tag{4}$$

$$\frac{V_{S2}}{sL_{l-} + R_{l-}} = sV_{ds2}C_{ds2} + sV_{gs2}C_{gs2}, \tag{5}$$

$$\frac{V_{G2} - V_{GS,tran.}}{SL_{G2}} = \frac{V_{GS,tran.}}{R_{G2}}, \tag{6}$$

$$L_{total} = L_{l+} + L_{mid} + L_{+} + L_{-}, \tag{7}$$

$$R_{total} = R_{l+} + R_{mid} + R_{+} + R_{-}, \tag{8}$$

where $L_{l\pm}$, L_{mid}, and $L_{\pm}$ are the leakage inductances of the upper and lower side of the leg, leakage inductance at the middle of the leg between two switches and stray inductance of the conductor from DC link to the leg, respectively. The same index is also used for the parasitic resistances. The whole system parameters which are modeled in the simulations and used in analysis are depicted in Table 1.

Table 1. System parameters of the system model.

Parameter	Definition	Value	Parameter	Definition	Value
L_{+}	Upper side conductor leakage inductance	12.5 nH	L_{-}	Lower side conductor inductance	12.5 nH
R_{leak+}	Upper side conductor leakage resistance	12.5 mΩ	$R_{leak.-}$	Lower side conductor resistance	12.5 mΩ
L_{mid}	Leg inductance between the switches	5 nH	R_{mid}	Leg resistance between the switches	5 mΩ
L_{l+}	Leg inductance on top of the upper switch	5 nH	L_{l-}	Leg inductance under the lower switch	5 nH
R_{l+}	Leg resistance on top of the upper switch	5 mΩ	R_{l-}	Leg resistance under the lower switch	5 mΩ
L_{G2}	Gate on/off stray inductance	0.5 nH	$R_{G2,on}$	Gate ON-resistance	15.6 Ω
C_{gd2}	Gate–Drain capacitor for SiC	10 pF	C_{gs2}	Gate–Source capacitor for SiC	1300 pF
C_{ds2}	Drain–Source capacitor for SiC	50 pF	$R_{on,Q1}$	SiC MOSFET on resistance	75 mΩ

The values of parasitic capacitances are extracted from the datasheet of switches that are used in the experimental setup. Furthermore, the data regarding the leakage inductances is obtained through simulations of the entire PM using Ansys Q3D, employing the same size and material parameters, as depicted in Figure 6. This PM contains die switches for both T-Type converter and inverter.

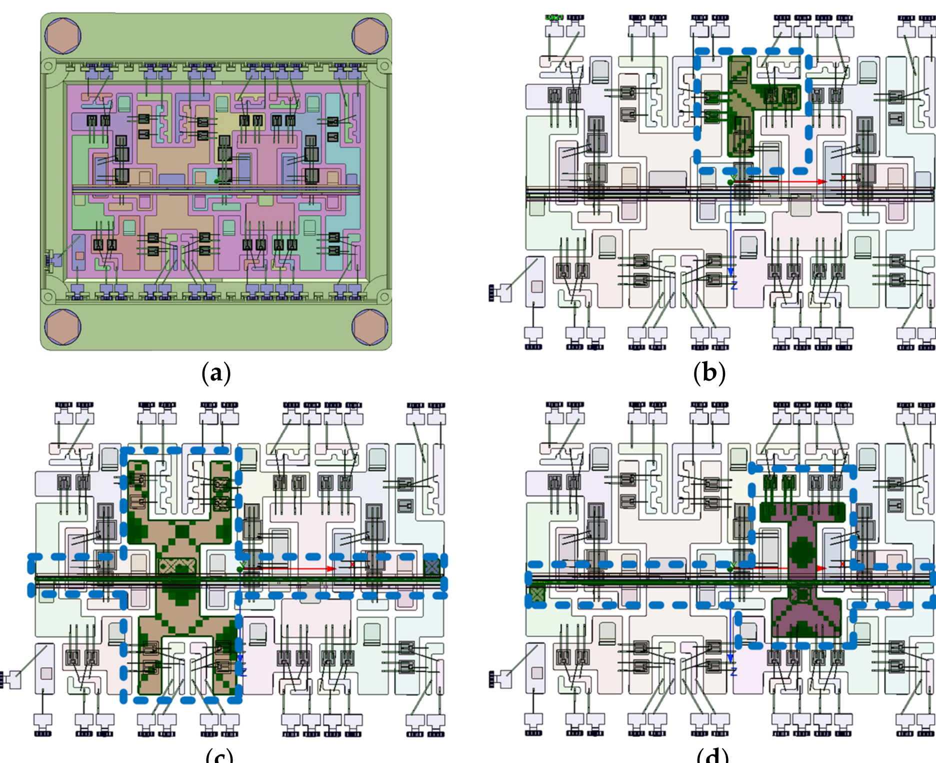


Figure 6. (**a**) PM simulated in Ansys Q3D, (**b**) middle track, (**c**) upper side (+) track, and (**d**) lower side (−) track.

Because of using Kelvin connection at source point of each die switch, the value of $Ll-$ is considered near zero in analysis. Based on Equations (3)–(6) and by considering V_p as the input step function, the step response of V_{ds2} and V_{gs2} is calculated. Then, the results are

plotted as shown in Figure 7a,b. It is noteworthy that the initial value of the step voltage is 400 V as IGBTs Q_3 and Q_4 conduct. In addition, the final value of Q_2 drain voltage (V_{D2}) is 800 V instantaneously after Q_1 turns on. Shown in Figure 7a, V_{ds} oscillates about 175 ns and then it reaches 800 V in steady state. Also, V_{gs} in Figure 7b jumps to approximately 2.5 V at transient time of false turn-on. Once after reaching the peak amplitude, V_{gs} falls below the threshold voltage for turn-on (v_{th} = 2.5 V). The results of Figure 7 are in a good agreement with the experimental results obtained in Section 6. The proposed model is also discussed with more details in the following section.

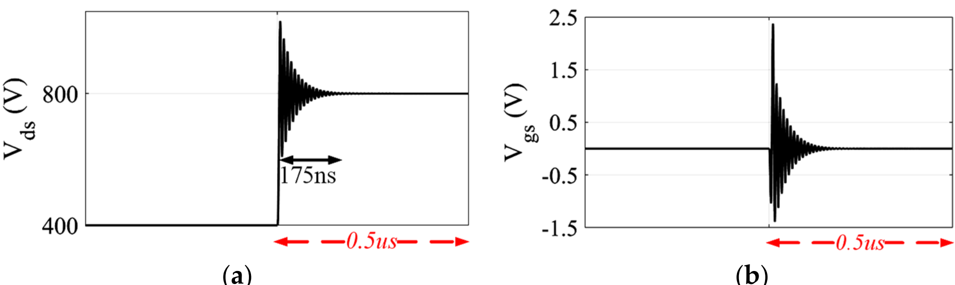


Figure 7. Step response of (**a**) V_{ds} across Q_2, and (**b**) V_{gs} of Q_2 during Q_1 turn-on.

4. Model Discussion

4.1. Sensitivity Analysis of ω_n and ζ

The general transfer function of V_{ds}, based on the proposed model and its corresponding Equations (3)–(8), can be obtained as follows

$$V_{ds}(s) = \frac{(s + z_1)(s + z_2)(s^2 + 2\alpha s + \beta)}{s(s + p_1)(s + p_2)(s^2 + 2\zeta\omega_n s + \omega_n^2)} \tag{9}$$

where z_1, z_2 and p_1, p_2 are the zeros and poles, respectively, and α and β are two constants in the transfer function. Also, in Equation (9), ω_n and ζ are the natural frequency and damping ratio, respectively, which determine the frequency of oscillations as well as the convergence speed of the system response. These two parameters are affected by the SiC MOSFET's parasitic components. To study the sensitivity of the natural frequency and damping ratio on the parasitic inductances and capacitances of the device, variation of each parasitic element is examined on Equation (9).

Figure 8 depicts the impact of the switch's parasitic capacitances on the damping ratio. Due to the sensitivity analysis, more focus has been carried out on the curve slope rather than its amplitude. Parameters of switch Q_2 have been considered in this study. In Figure 8, the slopes for C_{ds2} and C_{gd2} are negative up to certain values and will be increasingly positive beyond them. This means that increasing C_{gd2} and C_{ds2} first increases and then decreases the V_{ds2} oscillations. However, the slope for C_{gs2} is relatively constant, which shows that C_{gs2} has no considerable impact on damping ratio. To ensure the same curve trend for C_{gs2} due to the possibility of bifurcation, more values above the nominal C_{gs2} (1.3 nF) are considered in the plot. Nevertheless, the same result has been concluded, which shows negligible impact of C_{gs2} on damping ratio.

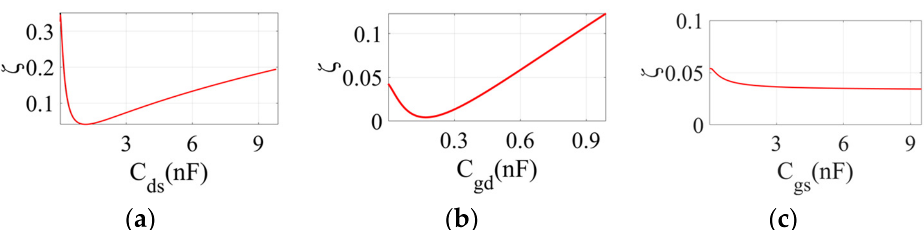


Figure 8. Damping ratio of ringing across the switch in terms of parasitic capacitor values; (**a**) C_{ds2}, (**b**) C_{gd2}, and (**c**) C_{gs2}.

On the other hand, referring to Figure 9, C_{ds2} and C_{gd2} have a sensible impact on the natural frequency. Among them, C_{gd2} is more effective. The negative slope in these two curves shows that the oscillation frequency of V_{ds2} across Q_2 will be reduced by increasing C_{ds2} and C_{gd2}. However, C_{gs2} has a little impact on the oscillation's frequency.

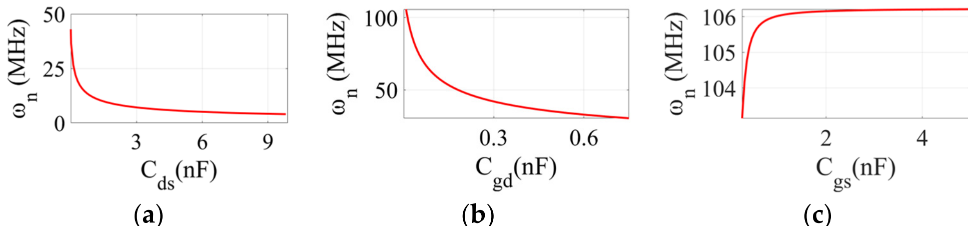


Figure 9. Natural frequency of oscillation across the switch in terms of parasitic capacitor values; (**a**) C_{ds2}, (**b**) C_{gd2}, and (**c**) C_{gs2}.

The result in Figure 10 clarifies these findings. In this figure, V_{ds2} is plotted for C_{gd2} = 2 nF which is higher than the one in nominal C_{gd2} (Figure 7a), as mentioned in Table 1. Comparing Figure 10 to Figure 7a, it can be seen that the settling time is less in Figure 10. This means bigger C_{gd2} leads to higher damping ratio with less oscillatory frequency. In addition, the peak–peak voltage oscillation ($V_{p\text{-}p}$) decreases to 250 V in Figure 10, while the value is 400 V in Figure 7a. Since the overshoot amplitude has an inverse relation with the damping ratio, this finding in Figure 10 is in good agreement with the findings extracted from Figures 8 and 9, which show that increasing C_{gd2} will result in an increment of the damping ratio and a decrement of the natural frequency.

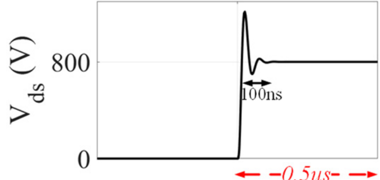


Figure 10. V_{ds} oscillation for C_{gd} = 2 nF.

The dependencies of the natural frequency and the damping ratio of V_{ds} on the parasitic inductors are presented in Figures 11 and 12, respectively. Figure 11 shows a decrease in the damping ratio when the major loop inductance, L_{total}, is increased. On the other hand, the increment of the source inductance, L_{l-}, is followed by a damping ratio increase. Based on this finding, source inductance may have a positive effect against false turn-on of switch in some cases. In return, the effect of gate inductance, L_G, on the damping ratio of V_{ds} can be neglected. Regarding Figure 12, it is obvious that the natural frequency of V_{ds} decreases by increasing L_{total} and L_{l-}. On the other hand, L_G has no significant effect on the natural frequency. Comparison of Figures 8 and 9 with Figures 11 and 12 demonstrates both natural frequency and damping ratio are more influenced by the parasitic capacitances, as the slope variations are bigger in Figures 8 and 9.

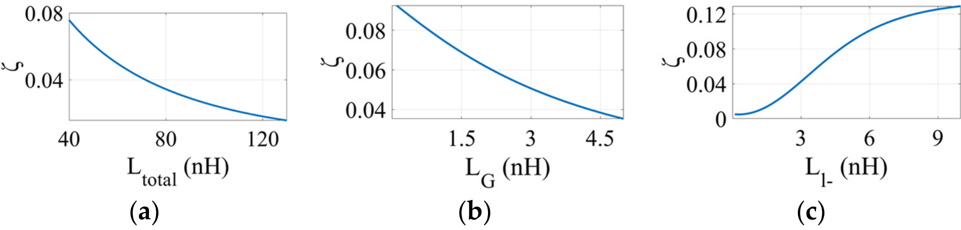


Figure 11. Damping ratio of ringing voltage across the switch in terms of the stray inductances in the circuit; (**a**) L_{total}, (**b**) L_G, and (**c**) L_{l-}.

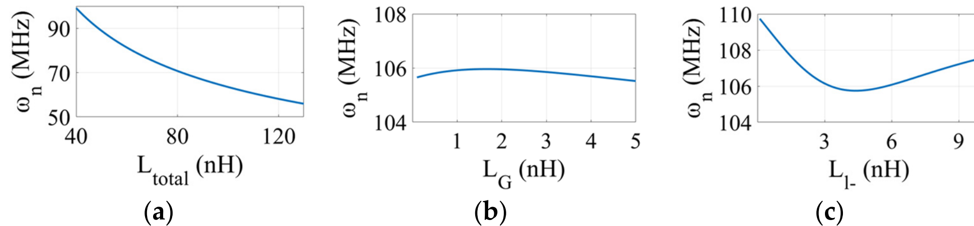


Figure 12. Natural frequency of oscillation across the switch (Drain–Source) in terms of the stray inductances in the circuit; (**a**) L_{total}, (**b**) L_G, and (**c**) L_{l-}.

4.2. Dependency of False Turn-On on Parasitics

In this part, the dependency of false turn-on due to the induced V_{gs} on the parasitic capacitances is analyzed. Both simulation and theoretical results are illustrated in Figure 13 in the form of the gate–source peak amplitude. As seen, there exists an appropriate agreement among them. In addition, Figure 13 verifies that during false turn-on, C_{gd} has a prominent impact on the induced gate–source voltage. In addition, during false turn-on, a roughly piecewise linear relationship exists between C_{gd} and the gate–source voltage. This observation agrees with the studies previously presented in Section 3. It should be mentioned that 10 pF is the nominal value of C_{gd}. Therefore, in this analysis, the nominal value is considered by extrapolation which is impractical for SiC. This analysis tries to provide the insight of how substantial the effect of C_{gd} could be even with a decreased value. Further analysis of Figure 13 determines the increased value of C_{gs} is followed by a decrement of the magnitude of the induced gate–source voltage during false turn-on. This observation again is in appropriate compliance with the studies previously presented in Section 3.

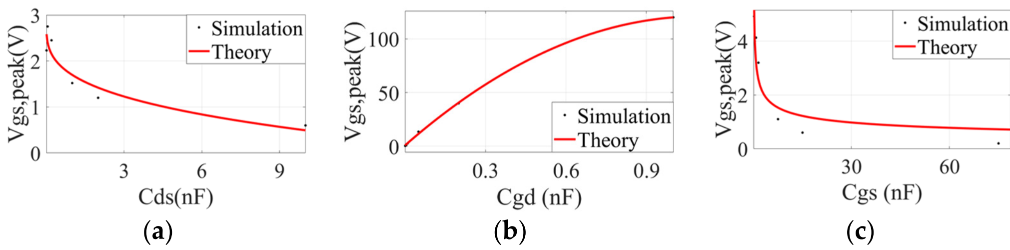


Figure 13. Effect of each parasitic capacitance of the switch on the induced gate–source voltage; (**a**) C_{ds}, (**b**) C_{gd}, and (**c**) C_{gs}.

V_{gs} waveform is analytically-drawn for the increased C_{gs} to 13 nF as shown in Figure 14. Comparing with Figure 7b, it is found that the peak value of V_{gs} is roughly 0.5 V, which is only 20% of peak voltage at nominal C_{gs} (1.3 nF). This finding can also be verified by referring to Figure 13c.

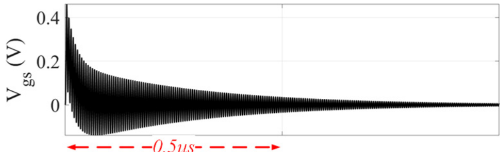


Figure 14. V_{gs} of the OFF switch in case that C_{gs} = 13 nF.

In a similar way, Figure 15 demonstrates the impact of C_{ds2} on V_{gs} for the increased C_{ds2} to 5 nF compared to nominal C_{ds2}, which is mentioned in Table 1. Figure 15 shows that increasing C_{ds2} will result in the decrement of the induced gate–source voltage. This could not manifest based on the response function of the simple model presented in Equation (2). The effect of C_{ds} for false turn-on is not as prominent as C_{gs}, but it is still required to be considered. It is considerable that increasing capacitance generally results in an increment of switching losses during the switches turn-off/on. Therefore, in high dv/dt circuits, the

values of C_{gs} and C_{ds} are required to be optimized to minimizing the total switching losses. Accordingly, their beneficial aspects during false turn-on are not completely offset by their parasitic effects during intended turn-off and turn-on. Experimental studies are presented in the next section to validate the reported analytical results.

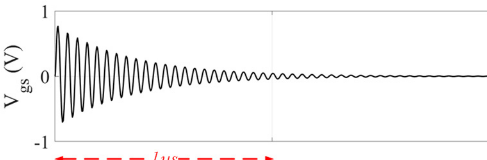


Figure 15. V_{gs} of the OFF switch in case that C_{ds} = 5 nF.

5. Model Extension to Three-Phase T-Type Converter

The single-phase converter had been investigated in previous sections. The same challenges are assumable for each phase of three-phases system which is shown in Figure 16. In addition, in inverter mode, the voltage of each phase ($V_{phX} = V_{phx} - V_M$) will be affected by the switching of two other phases. This issue is reflected in form of voltage oscillation across V_{phX}. At each time, the low-frequency reference voltage (V_{ref}) applying to one phase (leg 1, 2, or 3) is in opposite polarity to the others depending on the phase angle. Table 2 shows the sign of reference voltages of the three phases over the positive half cycle of phase 1. The same situation will occur for the negative half cycle.

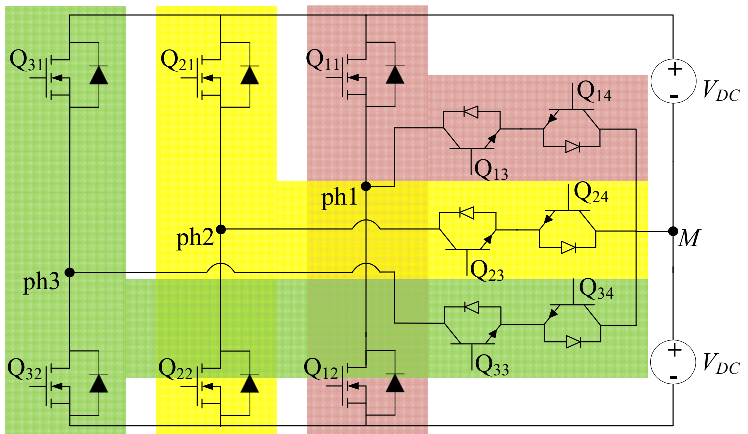


Figure 16. Three-phase T-Type converter.

Table 2. Polarity of reference voltage for each phase.

V_{ref} for:					
Phase 1/Sign		**Phase 2/Sign**		**Phase 3/Sign**	
θ_1 = 0–60°	+	120°–180°	+	240°–300°	-
θ_1 = 60°–120°	+	180°–240°	-	300°–360°	-
θ_1 = 120°–180°	+	240°–300°	-	0–60°	+

For 0° to 60° degrees of V_{ref} in phase 1 ($V_{ref,1}$), the effect of switching in legs 2 and 3 on V_{ph1} is investigated as a scenario. For simplification, ON and OFF state of the switch can be modeled by R_{on} and charged capacitor of C_{ds}, respectively. Accordingly, the circuit schematics before and after changes in the switching state of both legs 2 and 3 are shown in Figure 17. R_{on}, C_{ds}, R_{on}', and C_{ds}' illustrate MOSFET and IGBT ON and OFF state, respectively. Regarding Table 2, SiC MOSFET Q_{21} turns off and Si IGBT Q_{23} turns on for leg 2 only. In similar way, SiC MOSFET Q_{32} turns off while Si IGBT Q_{34} turns on in leg 3 only.

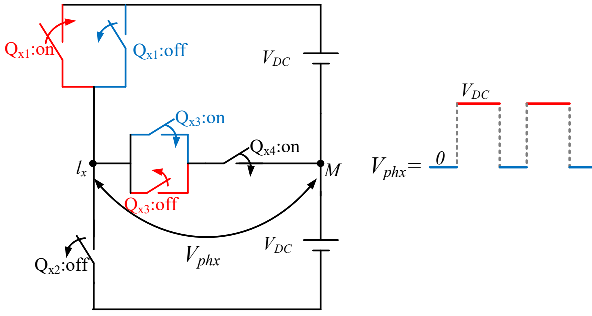


Figure 17. Switching state changes and the resulted phase voltage.

Like the circuit analysis in Section 3, Figure 5, a simplified circuit schematic by equating the switching state changes to pulse voltage across $V_{ph2,3}$ and midpoint (M) is shown in Figure 18 for $\theta_1 = 0°$. Here, the effect of switching state changes of leg 1 on V_{ph1} is not considered. The resulted voltage oscillation in this situation is obvious due to the leakage inductance of the route. Table 3 shows the amount of the parasitic components in Figure 18 and switches' parameters including C_{ds} and ON-resistance, which are employed for model simulation. It is noteworthy that the duty cycles of $V_{P,ph2}$ and $V_{P,ph3}$ depend on the exact phase degree of the related reference voltages, $V_{ref,2}$ and $V_{ref,3}$, which are 120° different in phase. As an example, for $\theta_1 = 0°$, 30° and 60°, the corresponding duty cycles of $V_{P,ph2}$ and $V_{P,ph3}$ are 0.86, 0.5, 0 and 0.86, 1, 0.86, respectively.

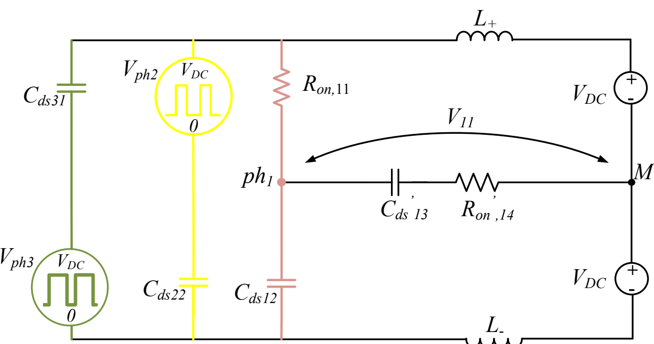


Figure 18. Simplified circuit considering switching state changes of legs 2 and 3 in form of pulse voltage.

Table 3. Parameters of the system presented in Figure 18.

Parameter	Definition	Value	Parameter	Definition	Value
L_+	Upper side conductor leakage inductance	40 nH	L_-	Conductor leakage inductance	40 nH
$R_{on,11}$	SiC MOSFET ON-resistance	75 mΩ	$R'_{on,14}$	Si IGBT ON-resistance	75 mΩ
C_{ds31}, C_{ds22}, C_{ds12}	SiC MOSFET drain–source capacity	550 pF	C'_{ds13}	Si IGBT drain–source capacity	55 pF

Figure 19 depicts the voltage oscillation of V_{ph1} with respect to switching state changes for two other phases (ph_2 and ph_3) when $\theta_1 = 0°$, 30°, and 60°. Based on the superposition principle, V_{ph1} contains both oscillations of each V_{ph2} and V_{ph3} which occur in different moments depending on θ_1. For better demonstration, the amount of θ_1 is kept constant for 6 high frequency cycles ($6T_s$). This is acceptable due to the slow changes of θ_1 comparing the switching speed.

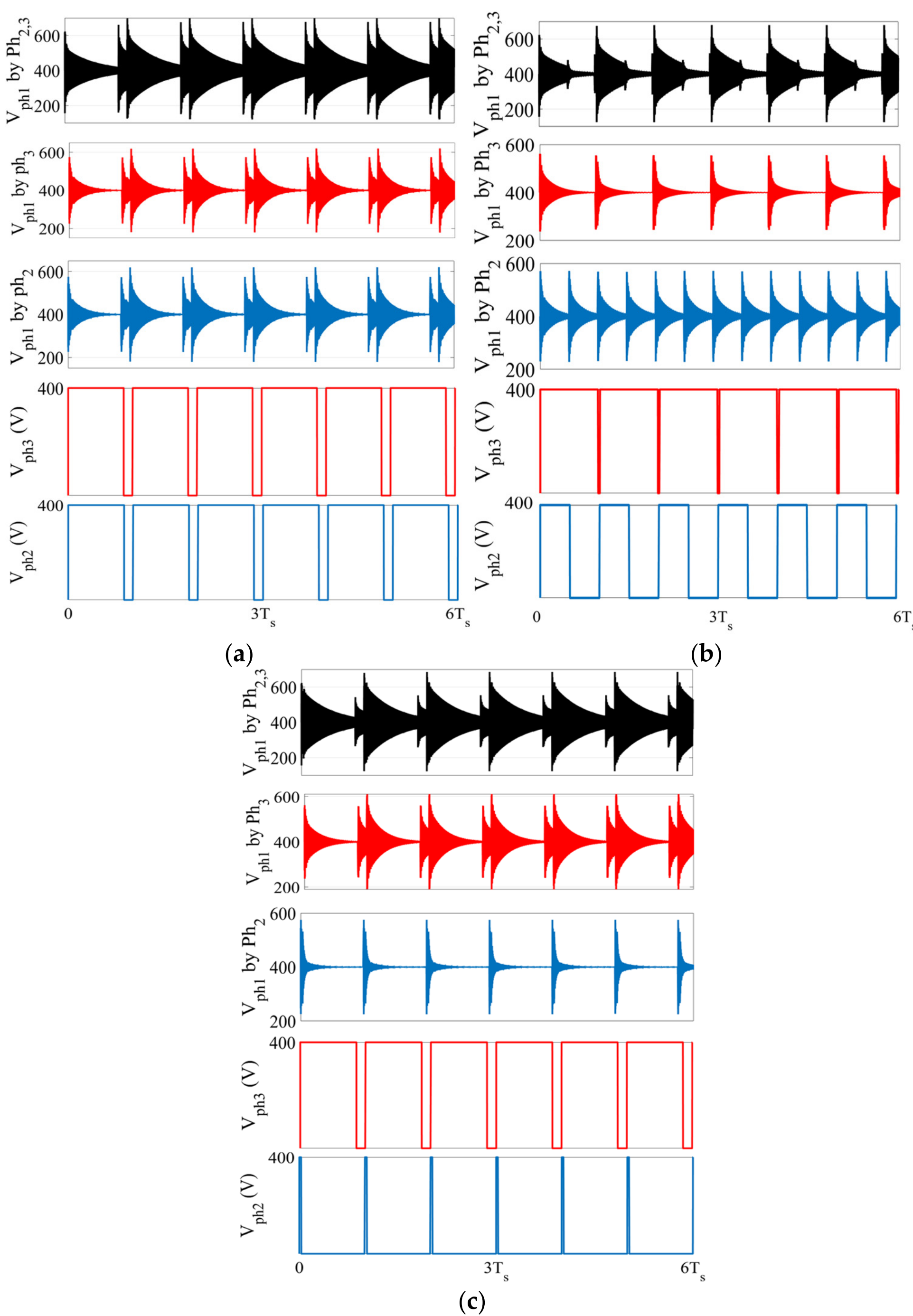


Figure 19. Voltage oscillation of V_{ph1} because of switching state changes for other phases (Ph_2 and Ph_3) for; (**a**) $\theta_1 = 0°$; (**b**) $\theta_1 = 30°$; and (**c**) $\theta_1 = 60°$.

For each amount of θ_1, the equivalent pulse voltage of phases 2 and 3 is illustrated, as well as the oscillation across phase 1 voltage (V_{ph1}) resulting by switching state changes in two other phases. The total results are also shown in black color which is the integration of two distinct oscillation. There is an appropriate agreement with the superposition principle which can be applied for such simplified linear circuit. It is obvious that by any change in the switching state of phases 2 and 3, V_{ph1} oscillates around V_{DC}. Without using a suitable filter at the output, this oscillation may be transferred to the load in stand-alone inverter mode, which is undesirable. Thus, this matter is taken into consideration in filter design for three-phase applications.

6. Experimental Evaluation

6.1. Double Pulse Setup Test

To authenticate the analytical and simulation-based investigations, the circuit depicted in Figure 5 underwent experimental scrutiny. This examination employed a SiC MOSFET for the legs and back-to-back Si IGBTs to attain a zero-voltage level, as illustrated in Figure 20. The three-phase T-Type converter utilized in this configuration served as the rectifier section of the entire Front-End converter, renowned for its high power density.

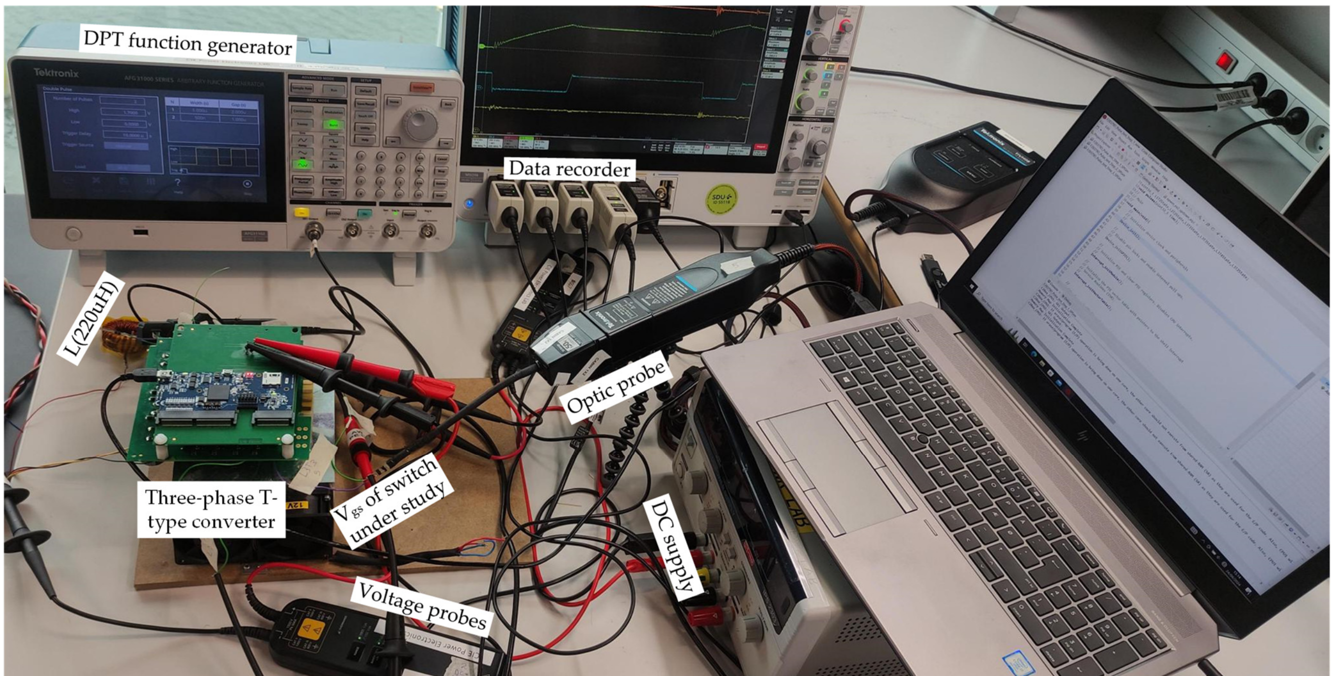


Figure 20. The experimental setup for result verification by DPT test.

For characterization, the Tektronix AFG 31000 double pulse generator (Tektronix company, Portland, OR, USA) was employed to generate two pulses with adjustable duty cycles based on the switch current rate. This facilitated the characterization of both the gate driving circuit and the under-test switch. The current behavior of inductor L during the double pulse test (DPT) is depicted in Figure 21, where the inductance current exhibited a ramp-like increase upon switch activation and decreased slightly during the off time due to the voltage drop across the freewheeling diode. Subsequently, detailed investigation of the obtained V_{gs} in DPT was conducted to verify the theoretical findings.

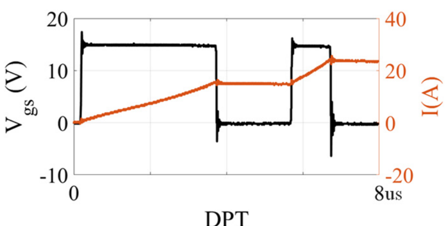


Figure 21. Current flow of the system under DPT test in practice.

Figure 22 considers all potential scenarios for false turn-on in the experimental testing circuits, with theoretical analysis and simulations focusing on case 3, regarded as the most critical scenario, wherein the false turn-on of switch Q_2 is investigated during the activation of switch Q_1.

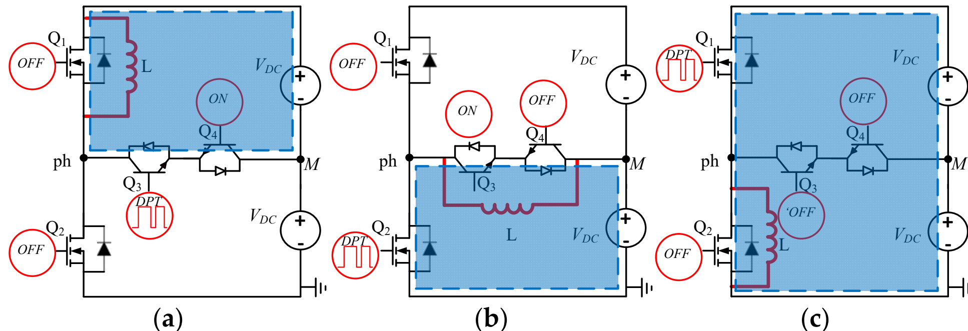


Figure 22. The equivalent circuit model under DPT test for (**a**) upper side half-bridge of T-type converter (case 1), (**b**) lower side half-bridge of T-type converter (case 2), and (**c**) T-type leg (case 3).

6.2. False Turn-On Evaluation

To address all three potential scenarios outlined previously, identical circuits were subjected to experimental testing. Figure 23 presents the experimental outcomes of the test system, featuring V_{DC} = 400 V and DPT inductance L = 220 uH. This figure depicts the gate–source voltage of the two switches with the highest likelihood of activation, alongside the gate–source and drain–source voltages of the switch undergoing the double pulse application. The results encompass all three previously introduced cases in Section 2. Consequently, switches Q_1 and Q_2 were observed in case 1, where switch Q_3 underwent DPT testing. Additionally, switches Q_1 and Q_4 were monitored in case 2, where the double pulse was applied to switch Q_2. Similarly, switches Q_1 and Q_3 were scrutinized in case 3, involving the application of the double pulse to the gate–source of switch Q_1.

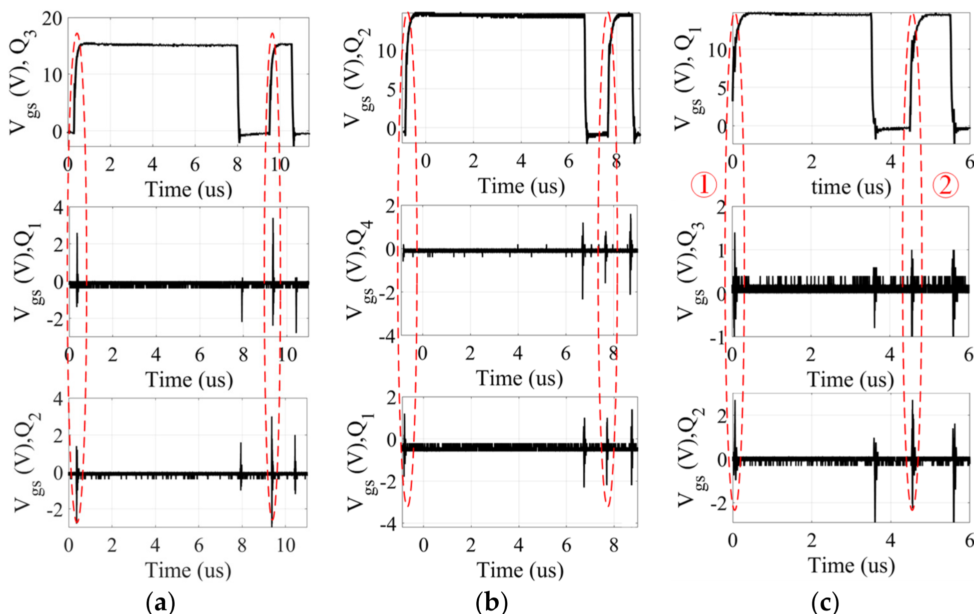
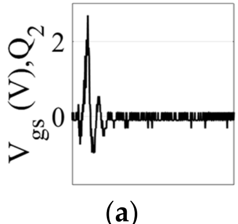


Figure 23. Induced gate–source voltage of switches with possibility of false turning on in DPT test; (**a**) case 1, (**b**) case 2, (**c**) case 3.

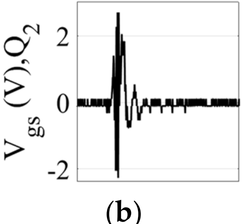
Across all three cases within the experimental setup (Figure 23a–c) and in case 3 of the analysis (Figure 7b), the peak value of the gate–source voltage was approximately 2.5 V. To facilitate better comparison, subsequent analysis exclusively concentrated on the experimental result of case 3.

Figure 24 provides a magnified perspective of the V_{gs} in Figure 23c, highlighting two turning-on transients (number 1: first turn-on; number 2: second turn-on) for clarity. Comparing the analytical/simulation model with experimental results reveals reasonable agreement. The peak value of the gate–source voltage in both experimental and ana-

lytical/simulation results is approximately 2.4 V. Notably, in the analytical model, the gate–source voltage reaches its first minimum value at 100 ns, whereas experimentally, this occurs slightly later, suggesting a slower experimental result attributed to larger circuit parasitics due to the new layout design. Nonetheless, the trends and shapes of the experimental waveforms reasonably align with the analytical/simulation results. It is worth noting that false turn-on during the falling edge of the applied gate–source pulses is less significant due to the deadtime between switching state changes, making monitoring of the rising edge of the pulses (indicated by dash loops) essential. In practical settings, induced gate–source voltage amplitude and voltage oscillation across switches are halved compared to DPT tests, as no inductance is placed in parallel to the switch, thus eliminating current conduction through the corresponding freewheeling diode during turning-off of the complementary switch. Consequently, the sensed step voltage across the switch in case 3 in real operation was V_{DC} (400 V) rather than $2V_{DC}$ (800 V), as depicted in Figure 7a.



(**a**)



(**b**)

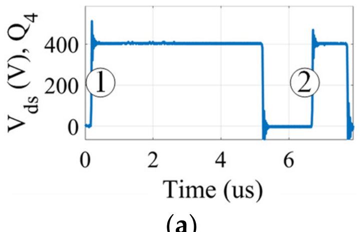
Figure 24. Enlarged view of the induced gate–source voltage of Q_2 in DPT test of case 3; (**a**) first turn-on of Q_1, (**b**) second turn-on of Q_1.

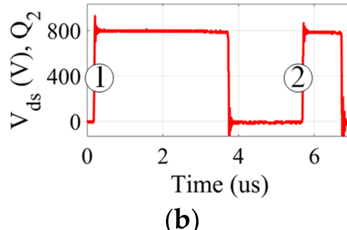
In all cases, it was observed that the damping ratio of the drain–source voltage was higher during the second turn-on. This phenomenon occurs because before the second turn-on, the freewheeling diode of the switch, operating in parallel with inductance L, conducts the circulating current. Consequently, this diode effectively clamps the phase voltage to $2V_{DC}$ in case 1, V_{DC} in case 2, and 0 V in case 3. Prior to the first turn-on, as no current flows through the freewheeling diode, the drain–source voltage cannot be clamped by it.

6.3. Voltage Stress Evaluation

In this subsection, we focus on cases 2 and 3, examining the corresponding circuits depicted in Figure 22b,c, respectively. Theoretical analysis is conducted specifically for case 3, investigating the drain–source voltage (V_{ds}) of SiC switch Q_2 during the activation of Q_1. To assess the impact of intrinsic capacitors, as depicted in Figures 8 and 9, another switch with different capacitances—C_{ds}, C_{gs}, and C_{gd}—compared to Q_2, requires investigation. Hence, case 2 was explored alongside case 3 to gather experimental results for Si switch Q_4, facilitating a comparison with the results of SiC switch Q_2. Notably, the differences in drain–source characteristics between Q_2 and Q_4 are primarily attributed to the intrinsic capacitors, as both switches received identical gating pulses with matching turn-on/off times and dv/dt rates. Subsequent analysis compared the results with analytical findings, focusing on C_{ds} as the sole varying parameter. Figure 25 illustrates the V_{gs} and V_{ds} of switches Q_2 and Q_4 in case 2, along with switches Q_1 and Q_2 in case 3, highlighting the V_{ds} at two rising edges of the gate–source pulses (indicated by dash loops) in Figure 26. Notably, V_{ds} overshoot for Q_2 in case 3 was 16% and 8% during the first and second rising edges, respectively, while these figures stood at 28% and 17% for Q_4 in case 2. This indicates a higher damping ratio of V_{ds} for Q_2, attributed to its smaller C_{ds} compared to Q_4. Such observations align well with analytical results, as showcased in Figure 8a, where an increase in C_{ds} up to 1.5 nF results in a decrease in damping ratio. Additionally, the natural frequency of V_{ds} oscillations remains similar for both switches, owing to the closely matched values of C_{gd}, which significantly influences ω_n. This correlation between experimental and analytical findings underscores the higher voltage overshoot during the first turn-on in both cases due to the absence of voltage clamping, a feature provided before

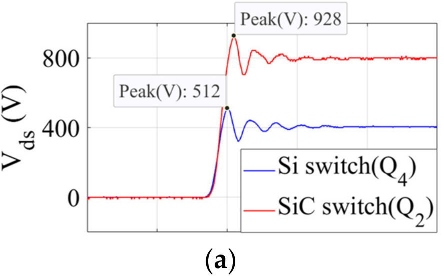
the second turn-on by the switch's body diode in parallel to the inductance, L. Overall, the observed overshoot amplitude and natural frequency in practice are generally lower than those predicted by theory, primarily due to anticipated parasitic effects associated with the PM layout and technology.

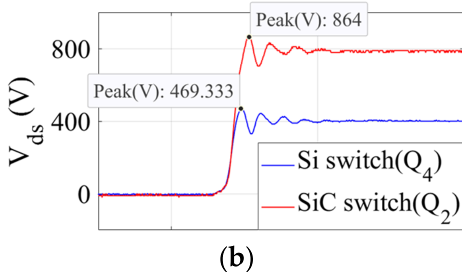




(**a**) (**b**)

Figure 25. (**a**) V_{ds} and V_{gs} of the switches in case 2, and (**b**) V_{ds} and V_{gs} of the switches in case 3.





(**a**) (**b**)

Figure 26. (**a**) V_{ds} across switches Q_2 and Q_4 for case 2 and 3 during first turning-on, and (**b**) V_{ds} across switches Q_2 and Q_4 for case 2 and 3 during second turning-on.

The analytical model exhibits a higher overshoot in the drain–source voltage compared to the experimental measurements, with the time needed to reach a steady state slightly prolonged in the experimental scenario. This suggests that the damping ratio in the experimental data surpasses that of the analytical model, while the natural frequency in the experiment was lower than predicted by the analytical model. This discrepancy is likely attributed to unaccounted-for experimental circuit parasitics in the analytical model.

6.4. Effects of dv/dt

Examining the effect of dv/dt involves altering the turn-on time of the switch, which is directly influenced by the turn-on gate resistance ($R_{G,on}$). By reducing $R_{G,on}$, an increase in dv/dt can be achieved. While previous plots were based on $R_{G,on}$ = 15.6 Ω, Figure 27 presents V_{ds} oscillation overshoot for varying $R_{G,on}$ values. Specifically, the V_{ds2} waveform for a new $R_{G,on}$ = 11.5 Ω was compared with $R_{G,on}$ = 15.6 Ω during the first and second Q_1 turn-on transients in case 3. It is evident that lower $R_{G,on}$ values result in higher voltage overshoot across the switch, indicating a correlation with increased dv/dt. Additionally, the overshoot amplitude is lower during the second turn-on transient for both turn-on gate resistance values due to this effect. Figure 28 illustrates the gate–source induced voltage for switch Q_2 in case 3 for $R_{G,on}$ = 15.6 Ω and $R_{G,on}$ = 11.5 Ω. Notably, decreasing turn-on gate resistance leads to an increase in induced V_{gs}, thereby escalating the risk of false turn-on with a higher voltage change rate. Consequently, the peak value of V_{gs} is 2.4 V for $R_{G,on}$ = 15.6 Ω, whereas it rises to 3.2 V for $R_{G,on}$ = 11.5 Ω, exceeding the safe range. This experiment aims to determine the maximum allowable dv/dt considering the induced voltage that might trigger false turn-on, ensuring it remains below the switch's turn-on threshold voltage. Finally, Figure 29 showcases the DPT test waveform in a comprehensive double pulse testing scenario with $R_{G,on}$ = 11.5 Ω.

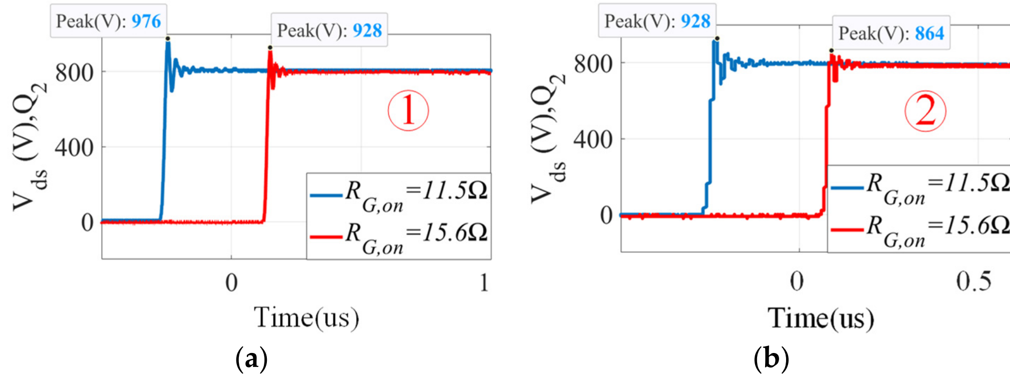


Figure 27. Comparison results of different voltage changes rate using different $R_{G,on}$; (**a**) first turn-on of switch $Q_1$and (**b**) second turn-on of switch Q_1.

Figure 28. Induced V_{gs} of Q_2 in case 3 for different $R_{G,on}$; (**a**) $R_{G,on}$ = 11.5 Ω and (**b**) $R_{G,on}$ = 15.6 Ω.

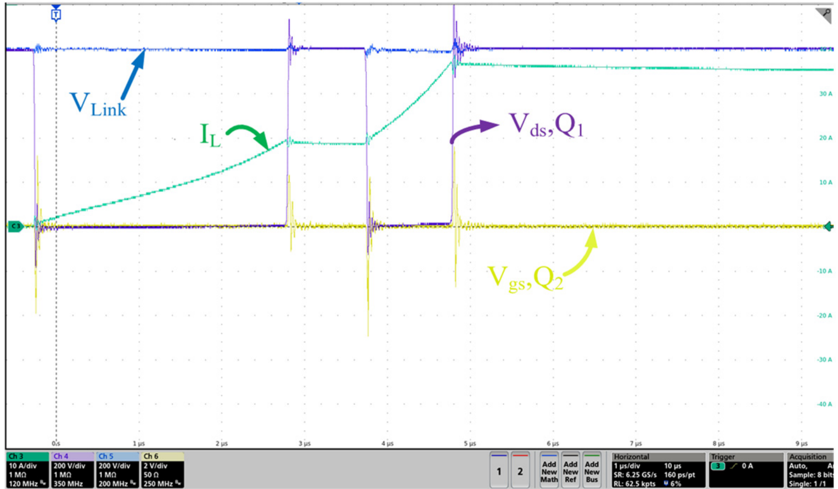


Figure 29. The overall key waveforms of DPT test with replacing R_G = 15.6 Ω by R_G = 11.5 Ω.

7. Conclusions

An analytical methodology for evaluating drain–source voltage oscillation and false turn-on issue in T-Type converter with hybrid structure (SiC MOSFET, Si IGBT) has been presented. In this method, the equivalent circuit of the converter with consideration of parasitic capacitances and inductances is used to derive a mathematical model of the converter. The voltage stress and the possibility of false turn-on depend on the overshoot and duration of oscillations, which are a function of the damping ratio and natural frequency. Sensitivity analysis based on the developed model is carried out to investigate the impact of parasitic parameters on the drain–source and gate–source voltages' damping ratio and natural frequency. The sensitivity analysis results show that the impact of parasitic capacitances on the voltage oscillations across both gate–source and drain–source is greater than the parasitic inductances. Furthermore, the most critical parameter affecting the possibility of false turn-on is the gain drain capacitance of the switch. The analytical results have

been validated quantitatively with the simulation and experimental data. Experimental results show that the voltage overshoot across the switch reduces with decreasing of the drain–source capacitance. Also, increasing dv/dt by using a smaller gate turn-on resistor leads to higher induced gate–source voltage, which increases the possibility of false turn-on. The presented method can be beneficial in designing further high-voltage power converters to operate in the safe region using wide band gap switches which are suitable in high-frequency applications.

Author Contributions: The individual contribution of the authors have been stated as follows: Conceptualization, A.B., M.S.G. and N.C.; methodology, A.B. and N.C.; software, A.B., N.C., S.B. and J.B.; validation, A.B. and M.S.G.; formal analysis, A.B.; investigation, A.B., N.C. and M.B.; resources, T.E., N.C., S.B. and J.B.; data curation, A.B. and T.E.; writing—original draft preparation, A.B. and M.S.G.; writing—review and editing, M.B. and M.S.G.; supervision, A.B. and T.E.; project administration, T.E.; funding acquisition, T.E. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by funds from the Energy Technology Development and Demonstration Program (EUDP), via the project with ref.: 64020-2075. Find further information on EUDP here: https://www.eudp.dk/en/om-eudp (accessed on 1 April 2024).

Data Availability Statement: The authors confirm that no new data have been created in this work.

Conflicts of Interest: Author Nicklas Christensen was employed by the company Danfoss Drives A/S. Author Stefan Behrendt was employed by the company Semikron Danfoss. Author Jesco Beyer was employed by the company FuE-Zentrum FH Kiel GmbH. The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

References

1. Bhattacharya, S.; Narwal, R.; Shah, S.S.; Baliga, B.J.; Agarwal, A.; Kanale, A.; Han, K.; Hopkins, D.C.; Cheng, T.-H. Power Conversion Systems Enabled by SiC BiDFET Device. *IEEE Power Electron. Mag.* **2023**, *10*, 39–43. [CrossRef]
2. Kumar, A.; Moradpour, M.; Losito, M.; Franke, W.-T.; Ramasamy, S.; Baccoli, R.; Gatto, G. Wide band gap devices and their application in power electronics. *Energies* **2022**, *15*, 9172. [CrossRef]
3. Yadlapalli, R.T.; Kotapati, A.; Kandipati, R.; Koritala, C.S. A review on energy efficient technologies for electric vehicle applications. *J. Energy Storage* **2022**, *50*, 104212. [CrossRef]
4. Mocevic, S.; Yu, J.; Fan, B.; Sun, K.; Xu, Y.; Stewart, J.; Rong, Y.; Song, H.; Mitrovic, V.; Yan, N. Design of a 10 kV SiC MOSFET-based high-density, high-efficiency, modular medium-voltage power converter. *IEnergy* **2022**, *1*, 100–113. [CrossRef]
5. Cha, K.-H.; Ju, C.-T.; Kim, R.-Y. Analysis and evaluation of WBG power device in high frequency induction heating application. *Energies* **2020**, *13*, 5351. [CrossRef]
6. Dini, P.; Ariaudo, G.; Botto, G.; Greca, F.L.; Saponara, S. Real-time electro-thermal modelling and predictive control design of resonant power converter in full electric vehicle applications. *IET Power Electron.* **2023**, *16*, 2045–2064. [CrossRef]
7. Dini, P.; Basso, G.; Saponara, S.; Romano, C. Real-time monitoring and ageing detection algorithm design with application on SiC-based automotive power drive system. *IET Power Electron.* **2024**. [CrossRef]
8. Verbrugge, B.; Rasool, H.; Hasan, M.M.; Chakraborty, S.; Geury, T.; El Baghdadi, M.; Hegazy, O. Reliability Assessment of SiC-Based Depot Charging Infrastructure with Smart and Bidirectional (V2X) Charging Strategies for Electric Buses. *Energies* **2022**, *16*, 153. [CrossRef]
9. Buffolo, M.; Favero, D.; Marcuzzi, A.; De Santi, C.; Meneghesso, G.; Zanoni, E.; Meneghini, M. Review and Outlook on GaN and SiC Power Devices: Industrial State-of-the-Art, Applications, and Perspectives. *IEEE Trans. Electron Devices* **2024**, *71*, 1344–1355. [CrossRef]
10. Rasool, H.; Verbrugge, B.; Zhaksylyk, A.; Tran, T.M.; El Baghdadi, M.; Geury, T.; Hegazy, O. Design optimization and electro-thermal modeling of an off-board charging system for electric bus applications. *IEEE Access* **2021**, *9*, 84501–84519. [CrossRef]
11. Dini, P.; Saponara, S. Electro-thermal model-based design of bidirectional on-board chargers in hybrid and full electric vehicles. *Electronics* **2021**, *11*, 112. [CrossRef]
12. Dini, P.; Saponara, S.; Chakraborty, S.; Hosseinabadi, F.; Hegazy, O. Experimental Characterization & Electro-Thermal Modeling of Double Side Cooled SiC MOSFETs for Accurate and Rapid Power Converter Simulations. *IEEE Access* **2023**, *11*, 79120–79143.
13. Tan, J.; Zhou, Z. An Optimized Switching Strategy Based on Gate Drivers with Variable Voltage to Improve the Switching Performance of SiC MOSFET Modules. *Energies* **2023**, *16*, 5984. [CrossRef]
14. Wei, S.; Wen, W. High-Frequency Oscillation of the Active-Bridge-Transformer-Based DC/DC Converter. *Energies* **2022**, *15*, 3311. [CrossRef]

15. Khanna, R.; Amrhein, A.; Stanchina, W.; Reed, G.; Mao, Z.-H. An analytical model for evaluating the influence of device parasitics on Cdv/dt induced false turn-on in SiC MOSFETs. In Proceedings of the 2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 17–21 March 2013.
16. Zhao, Q.; Stojcic, G. Characterization of Cdv/dt induced power loss in synchronous buck DC-DC converters. In Proceedings of the Nineteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2004. APEC'04, Anaheim, CA, USA, 22–26 February 2004.
17. Peters, D.; Aichinger, T.; Basler, T.; Rescher, G.; Puschkarsky, K.; Reisinger, H. Investigation of threshold voltage stability of SiC MOSFETs. In Proceedings of the 2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Chicago, IL, USA, 13–17 May 2018.
18. Li, R.; Zhu, Q.; Xie, M. A new analytical model for predicting *dv*/*dt*-induced low-side MOSFET false turn-ON in synchronous buck converters. *IEEE Trans. Power Electron.* **2018**, *34*, 5500–5512. [CrossRef]
19. Dalal, D.N.; Christensen, N.; Jørgensen, A.B.; Jørgensen, J.K.; Bęczkowski, S.; Munk-Nielsen, S.; Uhrenfeldt, C. Impact of power module parasitic capacitances on medium-voltage SiC MOSFETs switching transients. *IEEE J. Emerg. Sel. Top. Power Electron.* **2019**, *8*, 298–310. [CrossRef]
20. Liu, B.; Ren, R.; Jones, E.A.; Gui, H.; Zhang, Z.; Chen, R.; Wang, F.; Costinett, D. Effects of junction capacitances and commutation loops associated with line-frequency devices in three-level ac/dc converters. *IEEE Trans. Power Electron.* **2018**, *34*, 6155–6170. [CrossRef]
21. Xie, W.; Ji, S.; Zhao, Z.; Mo, X. SiC MOSFET Crosstalk Modelling with Suppression Considering Impacts of dv/dt and di/dt. In Proceedings of the 2023 11th International Conference on Power Electronics and ECCE Asia (ICPE 2023-ECCE Asia), Jeju Island, Republic of Korea, 22–25 May 2023.
22. Khanna, R.; Stanchina, W.; Reed, G. Effects of parasitic capacitances on gallium nitride heterostructure power transistors. In Proceedings of the 2012 IEEE Energy Conversion Congress and Exposition (ECCE), Raleigh, NC, USA, 15–20 September 2012.
23. Wei, S.; Zhao, Z.; Yuan, L.; Wen, W.; Chen, K. Voltage oscillation suppression for the high-frequency bus in modular-multiactive-bridge converter. *IEEE Trans. Power Electron.* **2021**, *36*, 9737–9742. [CrossRef]
24. HIZARCI, H.; KALAYCI, K.; Demirel, O.; Arifoğlu, U. Reducing electromagnetic interference in three-level T-type isolated bidirectional DC-DC converter using a snubber circuit. *Int. J. Appl. Math. Electron. Comput.* **2021**, *9*, 26–34. [CrossRef]
25. Zhang, M.; Ren, N.; Guo, Q.; Sheng, K. Understanding Turn-On Transients of SiC High-Power Modules: Drain-Source Voltage Plateau Characteristics. *Energies* **2020**, *13*, 3802. [CrossRef]
26. Qin, H.; Ma, C.; Wang, D.; Xie, H.; Zhu, Z.; Xu, K.; Wang, S. An overview of SiC MOSFET gate drivers. In Proceedings of the 2017 12th IEEE Conference on Industrial Electronics and Applications (ICIEA), Siem Reap, Cambodia, 18–20 June 2017.
27. Ma, C.-T.; Gu, Z.-H. Review on driving circuits for wide-bandgap semiconductor switching devices for mid-to high-power applications. *Micromachines* **2021**, *12*, 65. [CrossRef] [PubMed]
28. Gao, F.; Zhou, Q.; Wang, P.; Zhang, C. A gate driver of SiC MOSFET for suppressing the negative voltage spikes in a bridge circuit. *IEEE Trans. Power Electron.* **2017**, *33*, 2339–2353. [CrossRef]
29. Babaki, A.; Vaez-Zadeh, S.; Jahanpour-Dehkordi, M.; Zakerian, A. Wireless motor drives with a single inverter in primary side of power transfer systems. In Proceedings of the 2019 IEEE PELS Workshop on Emerging Technologies: Wireless Power Transfer (WoW), London, UK, 18–21 June 2019.
30. Okilly, A.H.; Baek, J. Design and Fabrication of an Isolated Two-Stage AC–DC Power Supply with a 99.50% PF and ZVS for High-Power Density Industrial Applications. *Electronics* **2022**, *11*, 1898. [CrossRef]
31. Liu, S.; Lin, H.; Wang, T. Comparative study of three different passive snubber circuits for SiC power MOSFETs. In Proceedings of the 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA, 17–21 March 2019.
32. Dzhunusbekov, E.; Orazbayev, S. A new passive lossless snubber. *IEEE Trans. Power Electron.* **2021**, *36*, 9263–9272. [CrossRef]
33. Behera, S.; Dash, S.K.; Sahu, M.K.; Sahu, I.; Parida, S. Design and Development of a New Soft-Switching Buck Converter. In Proceedings of the 2023 International Conference on Power Electronics and Energy (ICPEE), Bhubaneswar, India, 3–5 January 2023.
34. Kasasbeh, A.; Kelleci, B.; Ozturk, S.B.; Aksoz, A.; Hegazy, O. Sepic converter with an LC regenerative snubber for ev applications. *Energies* **2020**, *13*, 5765. [CrossRef]
35. Pastor, M.; Dudrik, J.; Michal, R. High-Frequency Soft-Switching DC-DC Converter with Simple Secondary Turn-Off Snubber. In Proceedings of the 2022 IEEE 20th International Power Electronics and Motion Control Conference (PEMC), Brasov, Romania, 25–28 September 2022.
36. Christensen, N. Demonstration of High Power Density kW Converters Utilizing Wide-Band Gap Devices. Ph.D. Thesis, Aalborg University, Aalborg, Denmark, 2019.
37. Mukherjee, S.; Ruiz, J.M.; Barbosa, P. A high power density wide range DC–DC converter for universal electric vehicle charging. *IEEE Trans. Power Electron.* **2022**, *38*, 1998–2012. [CrossRef]
38. Liu, H.; Wang, Y.; Wheeler, P.; Zhou, X.; Zhu, K. A voltage spike suppression strategy based on De-Re-coupling idea for the three-phase high-frequency isolated matrix-type inverter. *IEEE Trans. Power Electron.* **2022**, *37*, 9024–9034. [CrossRef]
39. Athwer, A.; Darwish, A. A Review on Modular Converter Topologies Based on WBG Semiconductor Devices in Wind Energy Conversion Systems. *Energies* **2023**, *16*, 5324. [CrossRef]

40. Bonyadi, R.; Alatise, O.; Jahdi, S.; Hu, J.; Gonzalez, J.A.O.; Ran, L.; Mawby, P.A. Compact electrothermal reliability modeling and experimental characterization of bipolar latchup in SiC and CoolMOS power MOSFETs. *IEEE Trans. Power Electron.* **2015**, *30*, 6978–6992. [CrossRef]
41. Heng, K.; Yang, X.; Wu, X.; Ye, J.; Liu, G. A temperature-dependent physical thermal network model including thermal boundary conditions for SiC MOSFET module. *IEEE Trans. Electron Devices* **2022**, *69*, 4444–4452. [CrossRef]
42. Dalal, D.N.; Zhao, H.; Jørgensen, J.K.; Christensen, N.; Jørgensen, A.B.; Bęczkowski, S.; Uhrenfeldt, C.; Munk-Nielsen, S. Demonstration of a 10 kV SiC MOSFET based medium voltage power stack. In Proceedings of the 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA, 15–19 March 2020.
43. Rodríguez, M.; Rodríguez, A.; Miaja, P.F.; Lamar, D.G.; Zúniga, J.S. An insight into the switching process of power MOSFETs: An improved analytical losses model. *IEEE Trans. Power Electron.* **2010**, *25*, 1626–1640. [CrossRef]

Disclaimer/Publisher's Note: The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.