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Sample Voltage Dead-Beat Control Based on Differentiative Voltage Prediction and Switching-Cycle Extension for DC-DC Converters

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Abstract: In this paper, a sample voltage dead-beat control based on differentiative voltage prediction (DVP) and switching-cycle extension (SCE) is presented to achieve optimal transient response for DC-DC converters under discontinuous conduction mode (DCM) operation. Firstly, to improve load transient response, a DVP method is proposed to estimate the load. With the estimated load, the controller realizes load current feedforward and thus improves the transient response with a wide load range. Secondly, an SCE strategy is proposed to enlarge the output current range and output voltage slew rate, both of which have limited value under conventional digital pulse width modulation (DPWM). When the output current reaches the limited value, the proposed strategy increases the switching cycle to enlarge the current range without losing DCM operation. Finally, combining DVP with SCE, the converter not only achieves optimal response in large signal transients, but also doubles the load range in DCM operation.

Keywords: DC-DC converters; dead-beat control; DCM operation; load estimation; transient response; switching-cycle extension

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1. Introduction

Transient response performance is widely studied as an important indicator of DC-DC converters, especially in processor and portable device applications. Also, the improvements in dynamic performance provide potential for reducing the size and weight of power stage filter components to increase circuit power density. Compared to voltage control, current control only has a single pole, providing greater bandwidth and faster response [1,2].

Due to the higher stability and faster response compared to linear compensation methods, nonlinear control has been widely studied and applied [3,4]. For example, sliding-mode control (SMC) guarantees stability and robustness against uncertainties in load, line, and other parameters [5–8]. Pulse train (PT) control and its extensions are well known for the inherent simplicity and fast transient response [9,10]. Nevertheless, both sliding-mode and pulse train controls have a variable switching frequency, which increases current and output voltage ripples.

In attempts to realize optimal control, a lot of constructive strategies have been proposed. Ripple-based control methods, including V^2 control [11,12] and enhanced V^2 control [13,14], are widely used in voltage regulator modules (VRMs). These methods realize load current feed-forward by measuring the difference between the inductor current and the load current based on the equivalent series resistance (ESR) of the capacitor. However, the need for large ESR results in more energy dissipation [15]. To optimize the response

time to load transients, time optimal control (TOC) has been proposed [16,17]. Based on the concept of capacitor charge balance, the TOC method saturates the duty cycle to either 100% or 0% during load transients. To suppress the transient voltage deviation, auxiliary inductor techniques have been proposed [18–20]. In these designs, transient voltage deviation is significantly reduced by applying small inductance in transients for greater current slope while using large inductance in steady state for less ripple. However, the aforementioned methods are usually limited to buck converters, which limits their application scenarios.

Another way to optimize dynamic performance is to use the dead-beat concept [21–23]. By applying current prediction and linear extrapolation, [24] achieves current dead-beat control with four cycles delay. In [25], predictive digital average current controls for three basic converters—buck, boost, and buck–boost—operated in continuous conduction mode (CCM) have been proposed. By predicting the duty cycle from the geometric relationship of the inductor current waveform, the estimated average current reaches the reference after two cycles without subharmonic oscillation.

The previously mentioned control methods are all operated in CCM for large current applications. In low-current applications, DCM is popular due to its ability to achieve soft switching, which has higher efficiency [26,27]. Also, a more compact inductor can be used in DCM, which provides greater power density with less cost and faster transient response. In [27], a charger balance average current (CBAC) control for DC-DC converters operating in DCM is proposed by using current estimation and capacitor charge balance methods. Furthermore, a dual current error compensation strategy is proposed to compensate current errors and eliminates the voltage steady state error caused by parasitic [28]. However, two essential issues that may degrade the transient performance should be noticed. The first one is the intrinsic delay induced by load estimation, which degrades the load transient response. Another issue lies in the saturation of DPWM, which constrains the maximum output current under DCM operation. This leads to limited voltage slew rate in large signal transient.

To address the two issues mentioned above, this paper proposes a sample voltage dead-beat control based on differentiative voltage prediction (DVP) and switching-cycle extension (SCE) for DC-DC converters operating in DCM. Before the switch turns off, the slope of the output voltage under the influence of load current is sampled through the differential circuit. Unlike load current estimation based on the capacitor charge balance of the previous cycle, the sampled voltage slopes reflect the load information of the present moment, eliminating the delay in load estimation. The DVP module then uses this voltage slope to predict the value of the output voltage after two cycles. By using capacitor charge balance, the average output current and the duty cycle required to bring this voltage to the reference value is obtained, which realizes a dead-beat control where the output voltage lags the reference value by two cycles. Furthermore, the SCE strategy solves the saturation problem by adaptively increasing the switching cycle in an acceptable range when a predicted duty cycle exceeds the DCM/CCM boundary. Combining DVP with SCE, the converter achieves dead-beat control with optimal transient response and wide load range in DCM.

This paper is organized as follows: Section 2 gives out the conventional CBAC control. In Section 3, the control scheme for the sample voltage dead-beat control based on DVP and SCE for boost converters is firstly presented and analyzed. Furthermore, overall control process and comparison of SSM between the proposed control and CBAC control are also given. In Section 4, the proposed method is extended to other basic converters, such as buck converters and buck–boost converters. In Sections 5 and 6, the effectiveness of the proposed controller is verified by simulations and experimental results. Finally, a brief conclusion is given in Section 7.

2. Conventional Charge Balance-Based Average Current Control

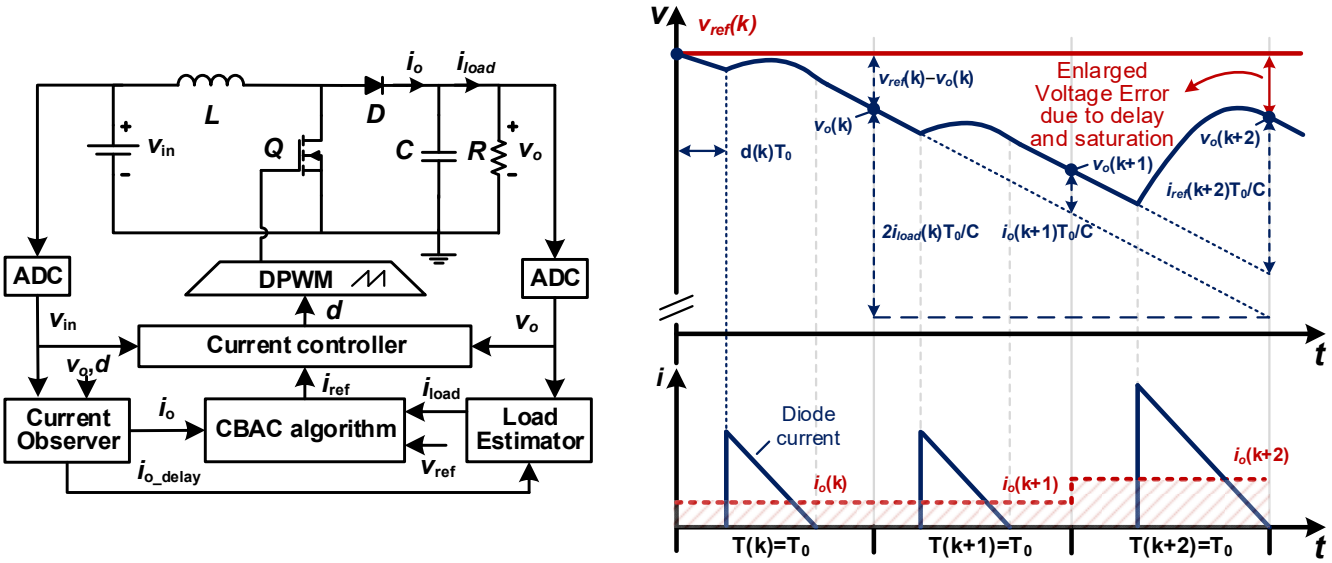
Controls based on the charge balance principle provide attractive alternatives to achieve optimal load/line transient response for DCM DC-DC converters. In the following,

the conventional CBAC control applied to a boost converter is introduced. Based on current observations, this approach generates a suitable duty cycle to regulate the output current that balances the output charge.

For DCM DC-DC converters, the inductor current reaches zero before the end of the switching cycle. Therefore, the average output current $i_o(k)$ during switching-cycle k is only determined by the period $T(k) = T_0$, the duty cycle $d(k)$, and the input/output voltage $v_{in}(k)$ and $v_o(k)$, respectively, of the present switching cycle so that the average output current $i_o(k)$ can be instantly regulated by DPWM signal, which facilitates CBAC control.

A typical CBAC control process for DCM boost converters is given in Figure 1a. According to the charge balance of output capacitor, the output voltage variation in switching cycle k is given by

$$v_o(k) - v_o(k-1) = \frac{T_0}{C}[i_o(k) - i_{\text{load}}(k)] \tag{1}$$



(**a**) (**b**)

Figure 1. (**a**) CBAC control scheme and (**b**) typical control process for DCM boost converter.

Therefore, the load current $i_{load}(k)$ of the switching cycle k is estimated by

$$i_{\text{load}}(k) = i_o(k) - \frac{C}{T_0}[v_o(k) - v_o(k-1)] \tag{2}$$

Furthermore, the voltage variation during the following two cycles is written as

$$\begin{aligned} \tfrac{C}{T_0}[v_o(k+2) - v_o(k)] &= i_o(k+2) + i_o(k+1) - i_{\text{load}}(k+2) - i_{\text{load}}(k+1) \\ &\approx i_o(k+2) + i_o(k+1) - 2i_{\text{load}}(k) \end{aligned} \tag{3}$$

The approximation is based on the assumption that load current remains constant within two switching cycles, i.e., $i_{load}(k+2) \approx i_{load}(k+1) \approx i_{load}(k)$. Substituting (1) into (2) gives

$$i_o(k+2) \approx \frac{C}{T_0}[v_o(k+2) - 3v_o(k) + 2v_o(k-1)] + 2i_o(k) - i_o(k+1) \tag{4}$$

In above equation, $v_o(k+2)$ and $i_o(k+2)$ indicate the output voltage and the required output current in switching cycle $(k+2)$, respectively. To bring the output voltage $v_o(k)$ to

the reference value $v_{ref}(k)$ after two cycles, substituting $v_o(k+2) = v_{ref}(k)$ and $i_o(k+2) = i_{ref}(k+2)$ into (4) gives the reference current as

$$i_{\mathrm{ref}}(k+2) \approx \frac{C}{T_0}[v_{\mathrm{ref}}(k) - 3v_o(k) + 2v_o(k-1)] + 2i_{\mathrm{o}}(k) - i_{\mathrm{o}}(k+1) \tag{5}$$

where $i_o(k)$ and $i_o(k+1)$ are obtained through current observer by

$$i_{\mathrm{o}}(k) = \frac{T_0[v_{\mathrm{in}}(k)d(k)]^2}{2L[v_o(k) - v_{\mathrm{in}}(k)]} \tag{6}$$

Furthermore, to produce the required $i_{ref}(k+2)$, an appropriate duty cycle $d(k+2)$ for the switching cycle $(k+2)$ is calculated by

$$\begin{aligned} d(k+2) &= \sqrt{\frac{2L[v_o(k+2) - v_{\mathrm{in}}(k+2)]i_{\mathrm{ref}}(k+2)}{T_0 v_{\mathrm{in}}^2(k+2)}} \\ &\approx \sqrt{\frac{2L\left[v_{ref}(k) - v_{\mathrm{in}}(k)\right]i_{\mathrm{ref}}(k+2)}{T_0 v_{\mathrm{in}}^2(k)}} \end{aligned} \tag{7}$$

and saturated within the interval

$$\left[0, \frac{v_{ref}(k) - v_{in}(k)}{v_{ref}(k)}\right] \tag{8}$$

where $\left[v_{ref}(k) - v_{in}(k)\right]/v_{ref}(k)$ is the CCM/DCM boundary of the boost converter. The approximation is made by the assumption that input voltage remains constant within two switching cycles, which means $v_{in}(k+2) \approx v_{in}(k+1) \approx v_{in}(k)$.

As indicated above, the CBAC algorithm calculates $i_{ref}(k+2)$ that regulates $v_o(k)$ to $v_{ref}(k)$ in two switching cycles. Although the expected performance is great, the practical performance will be degraded by the delay introduced by the load current estimation as indicated by (2). Another issue lies in the DPWM saturation, represented by (8), which limits the operation range and the output slew rate. As shown in Figure 1b, due to these two reasons, in practice, the output voltage does not reach the reference voltage value after two cycles, which will increase the transient time as well as increase the voltage deviation during transient.

3. Voltage Dead-Beat Control Based on Differentiative Voltage Prediction and Switching Cycle Extension

To address the aforementioned issues, a dead-beat controller based on differentiative voltage prediction and switching-cycle extension is proposed, which not only eliminates the load current estimation delay, but also enlarges the output slew rate for DCM DC-DC converters. The boost converter is used as a demonstration to show the concrete implementation of the proposed method in Section 3. Afterwards, the control method is extended to other basic topologies, the buck converter and the buck–boost converter, in Section 4.

A scheme of the proposed controller is given in Figure 2. By measuring the slope of the capacitor voltage under load current, the DVP predicts the output voltage v_p after two cycles without delay. With this approach, direct load information is then transformed to voltage decrement on output capacitor, and the dead-beat algorithm calculates $i_{ref}(k+2)$ to adjust this voltage to the reference value without load estimation delay.

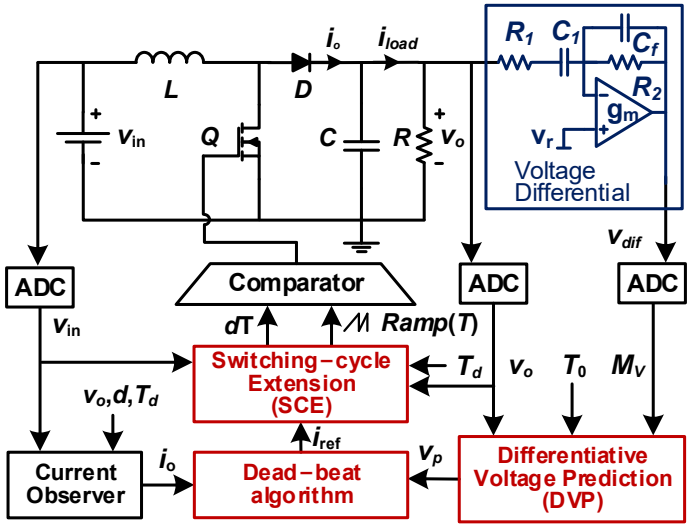


Figure 2. Scheme of dead-beat control based on DVP and SCE.

Furthermore, the SCE method is proposed to solve the duty cycle saturation problem caused by DPWM. When the calculated duty cycle reaches the upper limit of DCM operation, this strategy regulates the switching cycle in an acceptable range without losing DCM operation. A detailed control algorithm is described in the following section.

3.1. Dead-Beat Control Based on DVP

Unlike the CBAC, which estimates the average load current of the previous cycle through (2), the DVP uses a differential circuit to measure the effect of the load current on the slope of the voltage. The sampling time should be set slightly ahead of the next switch-off moment to allow sufficient stabilization time for the filtering results of the DVP module. In the experiment, the sampling moment is set at 300 ns before the MOSFET turns off, because the minimum throughput time of the ADC device LTC2314-14 (Analog Devices, Camas, WA, USA) is 222 ns. In practice, since the RC circuit time constant is much larger than the switching period, the voltage decrement is near linear, and the slope approximates $M_v \approx -v_o(k)/RC = -i_{load}(k)/C$. At the same time, since the load current is supplied entirely by the capacitor at the sampling moment of the differential output voltage, the presence of the capacitor ESR does not affect the sampling result. In a duration of two switching cycles, the voltage on the output capacitor is predicted as

$$\begin{aligned} v_p(k+2) =& v_o(k) - \frac{T(k+1)+T(k+2)}{C} i_{load}(k) \\ =& v_o(k) + [T(k+1)+T(k+2)]M_v \end{aligned} \tag{9}$$

where $T(k+1)$ and $T(k+2)$ represent the period of switching cycle $k+1$ and $k+2$, respectively. Note that if the SCE is not applied, the period per cycle is fixed to the default period T_0, which means $T(k+1) = T(k+2) = T_0$.

To achieve output sample voltage dead-beat control with two switching cycle delay, the average output current $i_o(k+2)$ should compensate the capacitor voltage from $v_p(k+2)$ to $v_{ref}(k)$, as shown in Figure 3. The required charge of the capacitor is expressed as

$$\begin{aligned} i_o(k+1)T(k+1) + i_{ref}T(k+2) &= C\left[v_{\mathrm{ref}}(k) - v_p(k+2)\right] \\ &= C\{v_{\mathrm{ref}}(k) - v_o(k) - M_v[T(k+1)+T(k+2)]\} \end{aligned} \tag{10}$$

where $i_o(k+1)$ is obtained through the current observer by

$$i_{\mathrm{o}}(k+1) \approx \frac{T(k+1)[v_{\mathrm{in}}(k)d(k+1)]^2}{2L\left[v_{ref}(k-1) - v_{\mathrm{in}}(k)\right]} \tag{11}$$

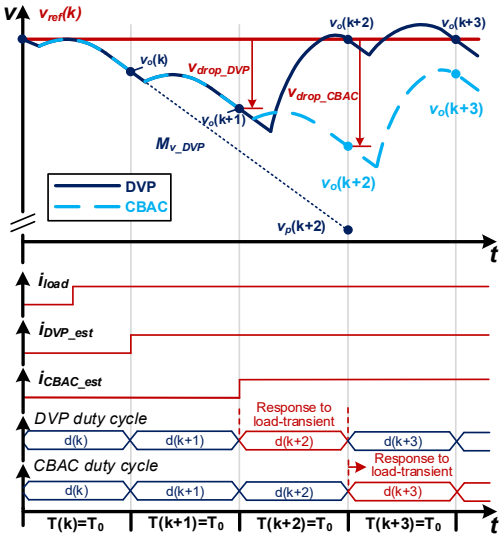


Figure 3. Load-response comparison of DVP-based dead-beat control (solid navy-blue line) with conventional CBAC control (dash light blue line) for DCM boost converter.

Therefore, the required reference current in switching cycle $k+2$ is derived as

$$i_{ref}(k+2) = \frac{C[v_{\text{ref}}(k) - v_o(k) - M_v T(k+1)] - i_o(k+1)T(k+1)}{T(k+2)} - CM_v \tag{12}$$

The duty ratio is calculated by

$$d(k+2) \approx \sqrt{\frac{2L\left[v_{ref}(k) - v_{\text{in}}(k)\right] i_{\text{ref}}(k+2)}{T(k+2)v_{\text{in}}^2(k)}} \tag{13}$$

and bounded the same way as (8).

The comparison of the load response of the proposed DVP-based bead-beat control (solid navy-blue line) with the conventional CBAC control (dashed light blue line) is given in Figure 3. A load change occurs during the interval of cycle k. The estimation of the load current through (2) in CBAC reflects the average effect over a cycle, and the estimated result is influenced by the moment of load change during the previous cycle. An extra cycle is needed to obtain real information about load changes; as shown in Figure 2, the CBAC detects this load change at the beginning moment of cycle k + 2. This delay in estimating the load current not only causes the response to be delayed by one cycle, but also introduces oscillations in the subsequent regulation, lengthening the load transient response time. In contrast, the DVP detects the slope of the output capacitor voltage by means of a differential circuit, which can reflect the changed load current without delay at the beginning moment of cycle k + 1 and complete the response to the load at cycle k + 2.

3.2. Dead-Beat Control Based on DVP and SCE

When the duty cycle calculated by (7) is within the CCM/DCM boundary of the boost converter, $v_o(k+2)$ tracks $v_{ref}(k)$ in two switching cycles. However, as shown by the dashed light blue line in Figure 4, this case turns invalid when the desired duty cycle is higher than $\left[v_{ref}(k) - v_{in}(k)\right]/v_{ref}(k)$, where the duty cycle saturation problem caused by DPWM constrains the reference tracking performance.

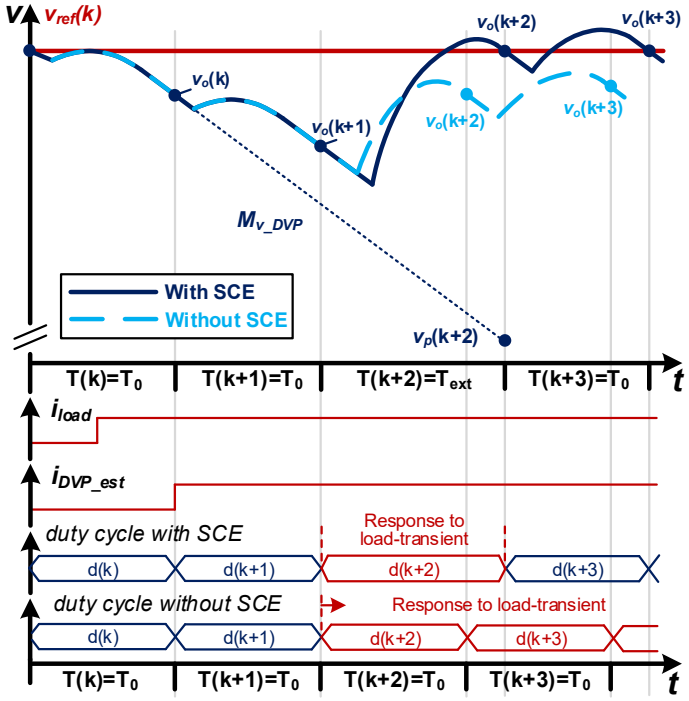


Figure 4. Voltage and current of the boost converter when DPWM saturation occurs "dash light blue line" without and "solid navy-blue line" with SCE.

To achieve output voltage dead-beat control over a wider range of conditions, the switching cycle could be extended to increase the maximum $i_o(k+2)$, as shown by the navy-blue line in Figure 4. With switching cycle $T(k+2)$, the maximum average output current of DCM boost is limited by

$$i_{\mathrm{o,max}}(k+2) \approx \frac{v_{in}^2(k)\left[v_{ref}(k) - v_{in}(k)\right]}{2Lv_{ref}^2(k)} T(k+2) \tag{14}$$

For the given input/output voltages, this value is in positive correlation to $T(k+2)$. Therefore, to generate an output current $i_{ref}(k+2)$ larger than $i_{o,\max}(k+2)$, the extended switching cycle is given by

$$T(k+2) = T_{ex} \approx \frac{2Lv_{ref}^2(k)}{v_{in}^2(k)\left[v_{ref}(k) - v_{\mathrm{in}}(k)\right]} i_{\mathrm{ref}}(k+2) \tag{15}$$

Note that the period $T(k+2)$ is not determined at the time of determining the reference current by (12). Using the extended period with the previously calculated reference current will introduce a prediction error. To address this problem, a substituting back method is used.

In (12), $i_{ref}(k+2)$ is inversely proportional to $T(k+2)$, while $T(k+2) = T_{ex}$ is proportional to $i_{ref}(k+2)$ in (15). Therefore, substituting the extended T_{ex} obtained from (15) back into (12) yields a proper $i_{ref}(k+2)$, which is smaller than the one calculated before, ensuring that it complies with the maximum current limit.

With this approach, the maximum output current is limited by the current limit of the MOSFET Q and is no longer limited by the DCM boundary, which improves both the operation range and the output voltage slew rate. For a design with a current limit of

$I_{\max}$ (the maximum peak current of MOSFET), the maximum output average current is calculated as

$$i_{o,\max}(k) = \frac{v_{in}(k)}{2v_o(k)} I_{\max} \tag{16}$$

Therefore, the output voltage slew rate with SCE is constrained by

$$-\frac{v_o(k)}{RC} \le \mathrm{SR}_{SCE} \le \frac{1}{C}\left[\frac{v_{in}(k)}{2v_o(k)} I_{\max} - \frac{v_o(k)}{R}\right] \tag{17}$$

while the output voltage slew rate without SCE is constrained by

$$-\frac{v_o(k)}{RC} \le \mathrm{SR} \le \frac{1}{C}\left[\frac{v_{in}^2(k)[v_o(k) - v_{in}(k)]}{2Lv_o{}^2(k)} T_0 - \frac{v_o(k)}{R}\right] \tag{18}$$

Obviously, the maximum slew rate under dead-beat control based on DVP and SCE is greatly increased by applying an extended period $T(k) = T_{ex}$. This improves the output voltage response in large signal transients, which is verified in the simulation and experiment parts.

3.3. Overall Control Process

Control process of the proposed strategy is given in Figure 5. At the beginning of each switching cycle, the controller receives sampled values of $v_{in}(k)$, $v_o(k)$, and M_v. Then, $i_o(k+1)$ and $v_p(k+2)$ are derived by the current observer and DVP module, respectively. The current reference $i_{ref,0}(k+2)$ with default period $T(k+2) = T_0$ is subsequently calculated by

$$i_{ref,0}(k+2) = \frac{C[v_{\mathrm{ref}}(k) - v_o(k) - M_v T(k+1)] - i_o(k+1)T(k+1)}{T_0} - CM_v \tag{19}$$

while the maximum average output current $i_{o,\max}(k+2)$ is obtained by (14).

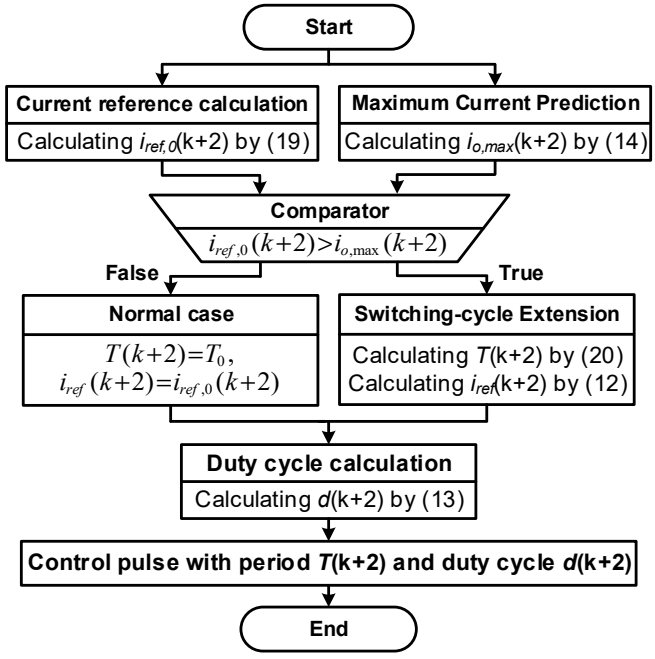


Figure 5. Control process of the proposed strategy for one switching cycle.

If $i_{ref,0}(k+2)$ is greater than $i_{o,\max}(k+2)$, the extended switching cycle is obtained as

$$T(k+2) = T_{ex} \approx \frac{2L{v_{ref}}^2(k)}{{v_{\text{in}}}^2(k)\left[v_{ref}(k) - v_{\text{in}}(k)\right]} i_{\text{ref},0}(k+2) \tag{20}$$

Substituting (20) back into (12), the required reference current $i_{ref}(k+2)$ in the case of applying cycle extension is derived. Then, the duty cycle for the next switching cycle is calculated by (13).

For the case where $i_{ref,0}(k+2)$ is not greater than $i_{o,\max}(k+2)$, the duty cycle will be derived by substituting $T(k+2) = T_0$ and $i_{ref}(k+2) = i_{ref,0}(k+2)$ into (13).

Finaly, a control pulse with period $T(k+2)$ and duty cycle $d(k+2)$ is generated to control the main switch of the boost convertor.

3.4. Small Signal Modeling

Closed-loop SSMs for boost converter under proposed dead-beat control and CBAC control are given in discrete-time domain in the following, which suits the analysis under digital control. The proposed dead-beat algorithm is based on (10), where $v_p(k+2)$ approximates $v_o(k)(1-2T_0/RC)$. The discrete-time equations are given by

$$\begin{cases} i_{\text{ref}} = \frac{C}{T}(v_{\text{ref}} - v_o + \frac{2T}{RC}v_o) - i_o z \\ v_o(1-z^{-1}) = \frac{T}{C}(i_o - i_{load}) \\ i_{load} = \frac{1+z^{-1}}{2}\frac{v_o}{R} \end{cases} \tag{21}$$

Differentiating these equations derives the linearized small signal model by

$$\begin{cases} \hat{i}_{\text{ref}} + \hat{i}_o z = \frac{C}{T}(\hat{v}_{\text{ref}} - \hat{v}_o + 2\frac{T}{RC}\hat{v}_o - 2\frac{v_o T}{R^2 C}\hat{R}) \\ (1-z^{-1})\frac{C}{T}\hat{v}_o + \frac{1+z^{-1}}{2}\left(\frac{\hat{v}_o}{R} - \frac{v_o}{R^2}\hat{R}\right) = \hat{i}_o \end{cases} \tag{22}$$

Since $\hat{i}_{\text{ref}} = \hat{i}_o z^2$ is ensured by the current controller, the closed-loop small signal model is given by

$$\begin{cases} \hat{v}_o = \Phi_{\text{v\_DVP}}(z)\hat{v}_{\text{ref}} + \Phi_{\text{R\_DVP}}(z)\hat{R} \\ \Phi_{\text{v\_DVP}}(z) = \frac{1}{z^2 + a(z^2+2z-3)/2} \\ \Phi_{\text{R\_DVP}}(z) = \frac{v_o}{R}\frac{a\left(z^2+2z-3\right)/2}{z^2+a(z^2+2z-3)/2} \end{cases} \tag{23}$$

where $a = T/RC$, $\Phi_{v\_DVP}(z)$ represents the closed-loop SSM from v_{ref} to v_o, and $\Phi_{R\_DVP}(z)$ represents the closed-loop SSM from load to v_o. Similarly, the closed-loop small signal model for converter under CBAC control is given by

$$\begin{cases} \hat{\text{v}}_{\text{o}} = \Phi_{\text{v\_CBAC}}(\text{z})\hat{\text{v}}_{\text{ref}} + \Phi_{\text{R\_CBAC}}(\text{z})\hat{\text{R}} \\ \Phi_{\text{vCBAC}}(\text{z}) = \frac{1}{z^2 + \text{a}\left(z^2+2z-1-2z^{-1}\right)/2} \\ \Phi_{\text{R\_CBAC}}(\text{z}) = \frac{\text{v}_o}{\text{R}}\frac{\text{a}\left(z^2+2z-1-2z^{-1}\right)/2}{z^2+\text{a}\left(z^2+2z-1-2z^{-1}\right)/2} \end{cases} \tag{24}$$

Since $RC \gg T$ is valid in most applications for DCM converters, $a \approx 0$ is always satisfied. Therefore, $\Phi_{v\_DVP}(z)$ and $\Phi_{v\_CBAC}(z)$ approximates z^{-2}, which achieves dead-beat output voltage control with two cycles delay under both controls. However, the basic CBAC control has a potential risk of DPWM saturation under large signal transients. Furthermore, for converters under CBAC control, $\Phi_{R\_CBAC}(z)$ indicates that v_o re-stabilizes in three switching cycles during load transients. Comparatively, for converters under proposed control, v_o re-stabilizes in a reduced duration of two switching cycles. The improved load transient response is verified by simulations and experiments.

3.5. Stability Analysis

Deviations in the model parameters can have an impact on the effectiveness of the control. The main parameters in the control are capacitance and inductance, where the deviation of capacitance only affects the speed of convergence of the system and does not have an effect on the stability. The main focus here is to analyze the effect of inductive bias on the system.

If there is an error $\Delta L = L_{real} - L$ in the inductance and an error $\varepsilon_k = v_{ref} - v_o(k)$ in the output voltage at k switching cycle, the control equation is expressed as follows

$$\frac{C}{T}\varepsilon_k = \hat{i}_o(k+1) + \hat{i}_o(k+2) - 2i_{load} \tag{25}$$

where $\hat{i}_o(k+1)$ and $\hat{i}_o(k+2)$ denote the current observation of the corresponding cycle. The new error at $k+2$ cycle can be expressed as

$$\frac{C}{T}\varepsilon_{k+2} = \frac{C}{T}\varepsilon_k - i_o(k+1) - i_o(k+2) + 2i_{load} \tag{26}$$

where $i_o(k+1)$ and $i_o(k+2)$ denote the actual current. The following relationship exists between the observed current and the real current

$$i_o(k+1) = \frac{L\left[v_{ref} - v_{\text{in}}\right]}{(L+\Delta L)\left[v_{ref} - v_{\text{in}} - \varepsilon_{k+1}\right]}\hat{i}_o(k+1) \tag{27}$$

Substituting (27) into (25) gives

$$\frac{C}{T}\varepsilon_k = \frac{(L+\Delta L)\left(v_{ref} - v_{\text{in}} - \varepsilon_{k+1}\right)}{L\left(v_{ref} - v_{\text{in}}\right)}i_o(k+1) + \frac{(L+\Delta L)\left(v_{ref} - v_{\text{in}} - \varepsilon_{k+2}\right)}{L\left(v_{ref} - v_{\text{in}}\right)}i_o(k+2) - 2i_{load} \tag{28}$$

Collating, eliminating higher order quantities, and substituting (26) yields

$$\left(1 + \frac{L+\Delta L}{L}\frac{T}{C}\frac{2i_{load}}{v_{ref} - v_{\text{in}}}\right)\varepsilon_{k+2} = \frac{\Delta L}{L}\frac{T}{C}2i_{load} + \frac{\Delta L}{L}(\varepsilon_k - \varepsilon_{k+2}) + \frac{L+\Delta L}{L}\frac{1}{v_{ref} - v_{\text{in}}}\frac{T}{C}i_{load}(\varepsilon_{k+2} - \varepsilon_{k+1}) \tag{29}$$

Analyzing the output voltage error in the z-domain yields

$$\varepsilon = \frac{\frac{\Delta L}{L}\frac{T}{C}2i_{load}}{\left\{\left(1 + \frac{L+\Delta L}{L}\frac{T}{C}\frac{2i_{load}}{v_{ref} - v_{\text{in}}}\right) + \frac{\Delta L}{L} - \frac{L+\Delta L}{L}\frac{1}{v_{ref} - v_{\text{in}}}\frac{T}{C}i_{load}\right\}z^2 + \frac{L+\Delta L}{L}\frac{1}{v_{ref} - v_{\text{in}}}\frac{T}{C}i_{load} \cdot z - \frac{\Delta L}{L}} \tag{30}$$

Plotting z-domain root trajectories using MATLAB R2020a is demonstrated in Figure 6.

By simulation analysis, the system is stable when $\frac{\Delta L}{L} > -0.5$, but there is a steady state error as follows

$$\varepsilon_0 = \frac{\frac{\Delta L}{L}\frac{T}{C}2i_{load}}{1 + \frac{L+\Delta L}{L}\frac{T}{C}\frac{2i_{load}}{v_{ref} - v_{\text{in}}}} \tag{31}$$

Generally, the inductance deviation of an inductor does not exceed 20%, so the stability of the system can be guaranteed. Substituting the design parameters of this experiment into the error expression yields

$$\varepsilon_0 = \begin{cases} -0.1071, \frac{\Delta L}{L} = -0.2 \\ 0.1062, \frac{\Delta L}{L} = 0.2 \end{cases} \tag{32}$$

Simulation results indicate that the steady state error is within acceptable limits.

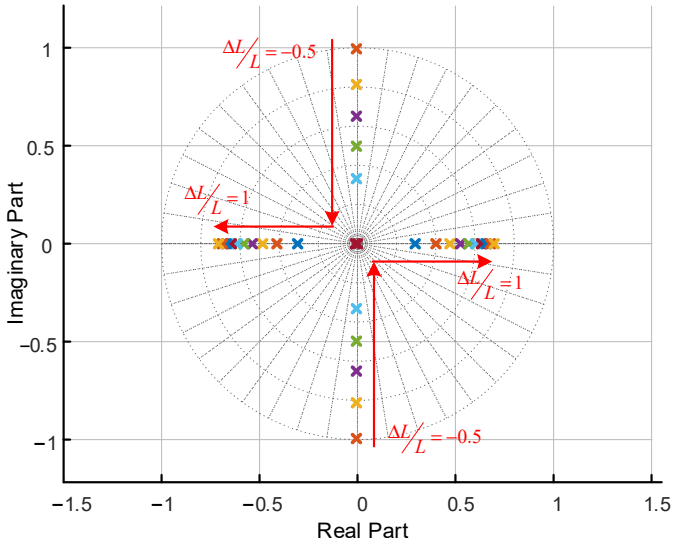


Figure 6. Plot of z-domain root trajectory of voltage error.

4. Extensions to Other Converters

In this section, the proposed control method is extended to other basic converters, i.e., the buck converter and the buck–boost converter. Different topologies bring about different relationships between $i_o(k)$, $T(k)$, and $d(k)$, which will affect output current observation, switching cycle extension, and duty cycle prediction, while the cycle-averaged capacitor charge balance relationship (12) remains constant. For an arbitrary converter, the control flow is the same as shown in Figure 5, except that the (11), (14), (20), and (13) are replaced with the formulas shown in Table 1, respectively.

Table 1. Control algorithm for basic converters.

Topology	Buck	Boost	Buck–Boost
$i_o(k+1)$	$\frac{d^2(k)\left[v_{in}(k)-v_{ref}(k-1)\right]^2 T(k)}{2Lv_{ref}(k-1)}$	$\frac{d^2(k)v_{in}^2(k)T(k)}{2L\left[v_{ref}(k-1)-v_{in}(k)\right]}$	$-\frac{d^2(k)v_{in}^2(k)T(k)}{2Lv_{ref}(k-1)}$
$i_{o,\max}(k+2)$	$\frac{\left[v_{in}(k)-v_{ref}(k)\right]^2 v_{ref}(k)T_0}{2Lv_{in}^2(k)}$	$\frac{v_{in}^2(k)\left[v_{ref}(k)-v_{in}(k)\right]T_0}{2Lv_{ref}^2(k)}$	$-\frac{v_{ref}(k)v_{in}^2(k)T_0}{2L\left[v_{in}(k)-v_{ref}(k)\right]^2}$
T_{ex}	$\frac{2Lv_{in}^2(k)i_{ref}(k+2)}{\left[v_{in}(k)-v_{ref}(k)\right]^2 v_{ref}(k)}$	$\frac{2Lv_{ref}^2(k)i_{ref}(k+2)}{v_{in}^2(k)\left[v_{ref}(k)-v_{in}(k)\right]}$	$-\frac{2L\left[v_{ref}(k)-v_{in}(k)\right]^2 i_{ref}(k+2)}{v_{ref}(k)v_{in}^2(k)}$
$d(k+2)$	$\sqrt{\frac{2Lv_{ref}(k)i_{ref}(k+2)}{\left[v_{in}(k)-v_{ref}(k)\right]^2 T(k+2)}}$	$\sqrt{\frac{2L\left[v_{ref}(k)-v_{in}(k)\right]i_{ref}(k+2)}{v_{in}^2(k)T(k+2)}}$	$\sqrt{\frac{-2Lv_{ref}(k)i_{ref}(k+2)}{v_{in}^2(k)T(k+2)}}$

5. Simulation Result

Simulations are carried out in MATLAB R2020a to verify the effectiveness of the proposed controller. The main specifications of the boost converter for simulations are the same as those for experiments, which are shown in Table 2, Section 5.

Table 2. Main specifications of boost converter.

$\mathbf{v_{in}}$	$\mathbf{v_o}$	L	C	R	$\mathbf{T_0}$	$\mathbf{I_{max}}$
24 V	48 V	22 µH	22 µF	100 Ω	12.5 µs	8 A

5.1. Magnitude–Frequency Responses of the Closed-Loop SSMs

Based on (23) and (24), frequency responses of the closed-loop SSMs are plotted in Figure 7. As shown in Figure 7a, both controls achieve similar closed-loop responses in reference voltage transients. Both magnitudes of $\Phi_{v\_DVP}(z)$ and $\Phi_{v\_CBAC}(z)$ are near unity

when $\omega < \pi/T$, which indicate a high bandwidth in reference to voltage tracking. As shown in Figure 7b, a magnitude of $\Phi_{R\_DVP}(z)$ is lower than that of $\Phi_{R\_CBAC}(z)$, while the phase of $\Phi_{R\_DVP}(z)$ is higher than that of $\Phi_{R\_CBAC}(z)$. These indicate that dead-beat control based on DVP reduces the delay and achieves better suppression to load disturbance.

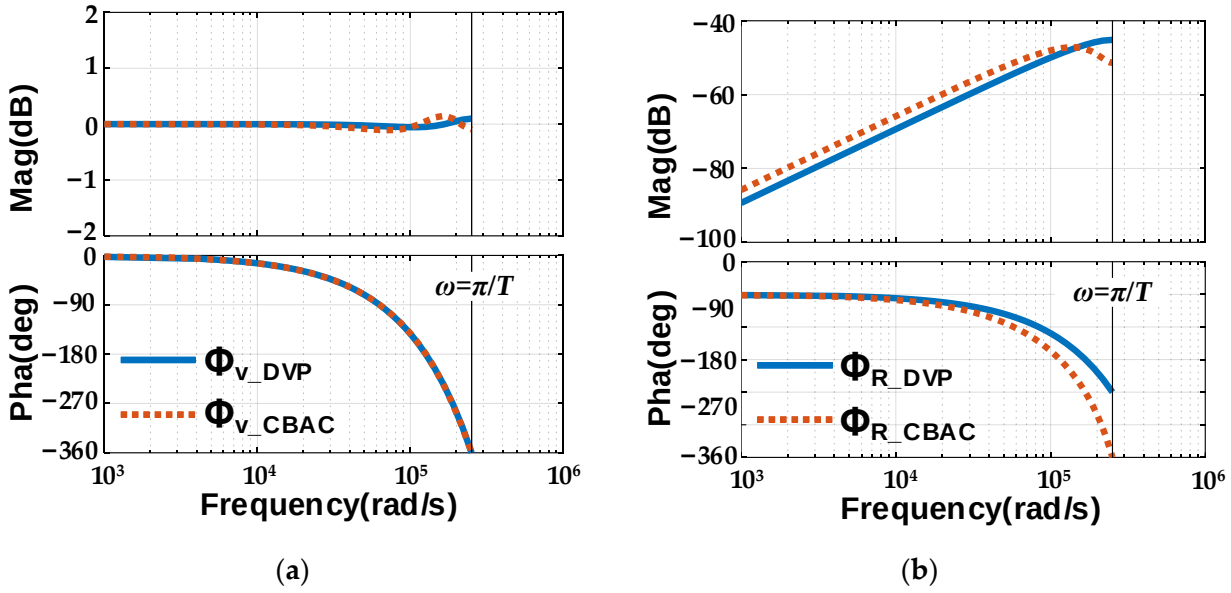


Figure 7. Frequency responses of the closed-loop SSMs (**a**) to reference voltage transients and (**b**) to load transient.

5.2. Maximum Average Output Current

With fixed switching cycle, the maximum average output current $i_{o,\max}$ under proposed control is limited by DPWM saturation. When SCE is implemented, $i_{o,\max}$ is determined by (16) where the limitation of $i_{o,\max}$ is the maximum current permitted by the circuit rather than the boundary of DCM/CCM. For proposed control with/without switching-cycle extension, variations of $i_{o,\max}$ with v_{in} and v_o are plotted in Figure 8. The result shows that $i_{o,\max}$ is effectively enlarged with SCE. When $v_{in} = 28$ V and $v_o = 40$ V, $i_{o,\max}$ with SCE reaches the maximum value of 2.8 A. Under the same input and output voltages, $i_{o,\max}$ without SCE reaches the maximum value of 1.67 A. Over the simulated input and output ranges, SCE improves $i_{o,\max}$ by an average of 30%.

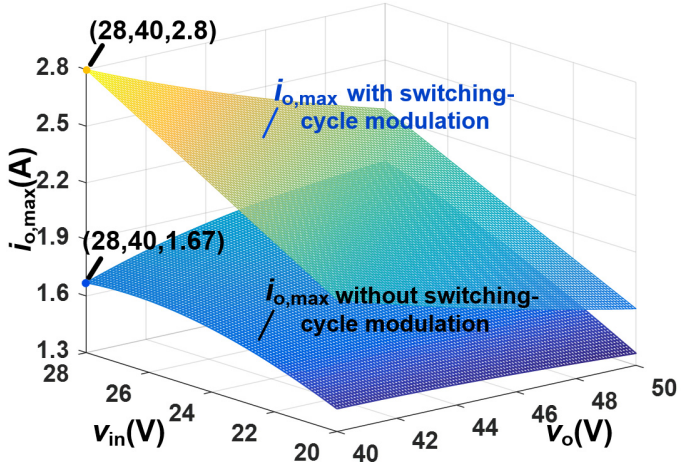


Figure 8. Maximum average output current with/without SCE.

Therefore, output current range is enlarged by the proposed controller, which will be verified by experiments of reference voltage tracking and load transient response.

5.3. Range of Output Voltage Slew Rate

According to (17) and (18), output voltage slew rate range under proposed control with/without SCE are plotted in Figure 9. The lower boundaries of both approaches are the same of $-v_o/RC$, since the minimum output current is zero. However, with SCE, the upper boundary is enlarged by an average of 70%.

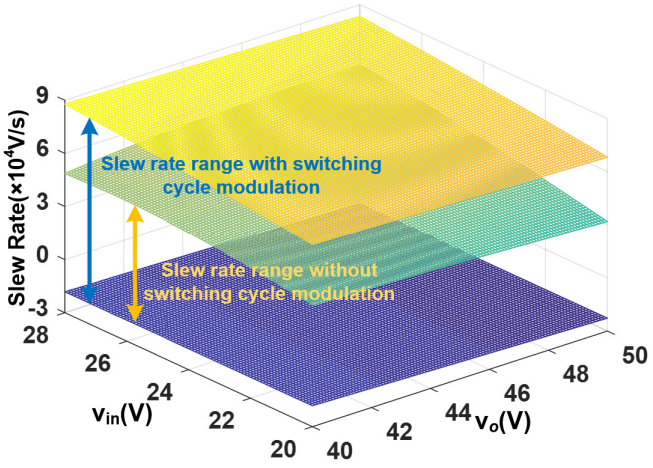


Figure 9. Output voltage slew rate range under the dead-beat control based on DVP control with/without SCE.

6. Experiments

An experimental prototype, as shown in Figure 10, is built to compare the transient performance under proportional-integral (PI) control, CBAC control, and the proposed control.

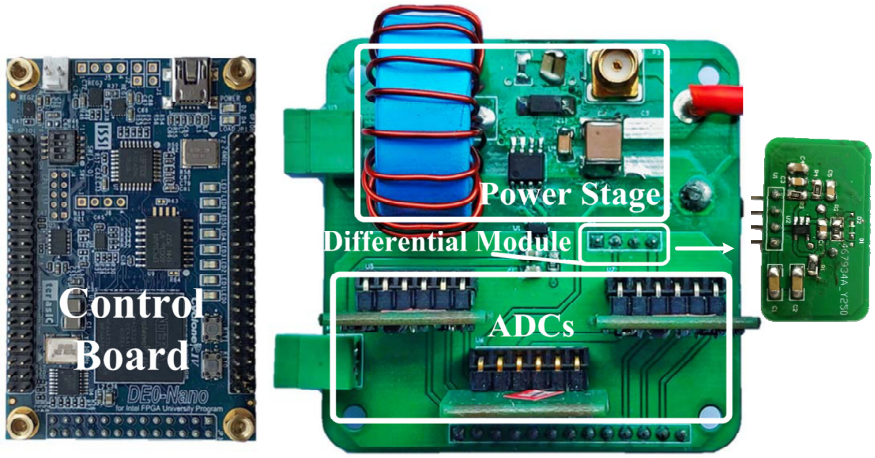


Figure 10. The experimental prototype.

Main specifications of the prototype are given in Table 2. An operational amplifier (opa354) with gain bandwidth (GBW) of 100 MHz is used to construct the differential circuit. Three ADC devices LTC2314-14, (Analog Devices, Camas, WA, USA) are used to convert the analog values to digital signals. Digital values of input/output voltages are received and processed by an FPGA (Cyclone IV) board, as shown in Figure 10. MOSFET FDS86540, (onsemi, Shenzhen, China) and diode NRVT-SA4100E, (onsemi, Shenzhen, China) are used as switching components in the main circuit. A 22 µF capacitor CKG57NX7S2A226M500JH, (TDK, Dongguan, China) and a 0.1 µF bypass capacitor are adopted as the output capacitors.

The core material of the inductor is NPH107060, (POCO, Shenzhen, China), which is suitable for operation frequency below 200 kHz. The setting of the switching period does not affect the control effect of the system due to the presence of the switching-cycle extension. The main tradeoffs in selecting the switching frequency are the power rating of the system, losses, and output voltage ripple. In this experiment, it is set to 80 kHz.

6.1. Differential Circuit

In Figure 2, a differential circuit is used to convert the output voltage to v_{diff}, where the effectiveness directly determines the stability of DVP. To improve the performance, the bandwidth of the differential circuit must be high enough with respect to the spectrum of the voltage ripple. To achieve a desired bandwidth, specific parameters of the differential circuit are given by $C_1 = 100$pF, $C_f = 12$pF, $R_1 = 5.6$ kΩ, and $R_2 = 100$ kΩ. The measured result is given in Figure 11, where v_{diff} highly matches the differential value of $-v_o$. At the sampling point of ADC, v_{diff} is relatively flat since v_o has a constant slope near this instant.

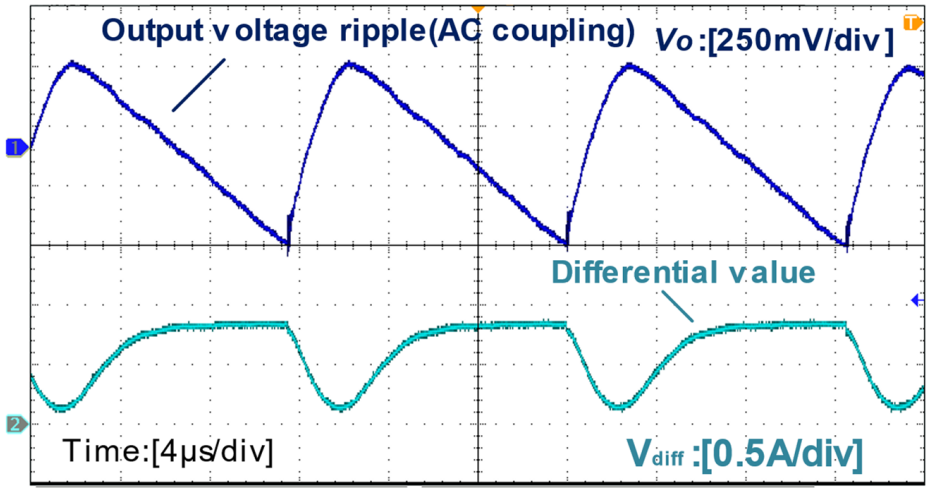


Figure 11. Output voltage ripple and the converted differential value.

6.2. Transient Performance

6.2.1. Transient Response to Load

To illustrate load transient performance of the proposed controller, transient voltages and currents are compared under PI, CBAC, and the proposed controls. As shown in Figure 12a, the output voltage under PI control re-stabilizes in 180 μs when R steps both from 100 Ω to 200 Ω and from 200 Ω to 100 Ω. For CBAC control in Figure 12b, v_o re-stabilizes in 70 μs with an overshoot of 1V when R steps from 100 Ω to 200 Ω, and re-stabilizes in 50 μs when R steps from 200 Ω to 100 Ω. For proposed control in Figure 12c, v_o re-stabilizes in 10 μs with little disturbance when the load steps from 100 Ω to 200 Ω and re-stabilizes in two switching cycles with 1 V undershoot when R steps from 200 Ω to 100 Ω. As indicated above, the proposed controller achieves excellent performance towards load transients, which not only shortens the response time, but also suppresses the overshoot or undershoot voltage.

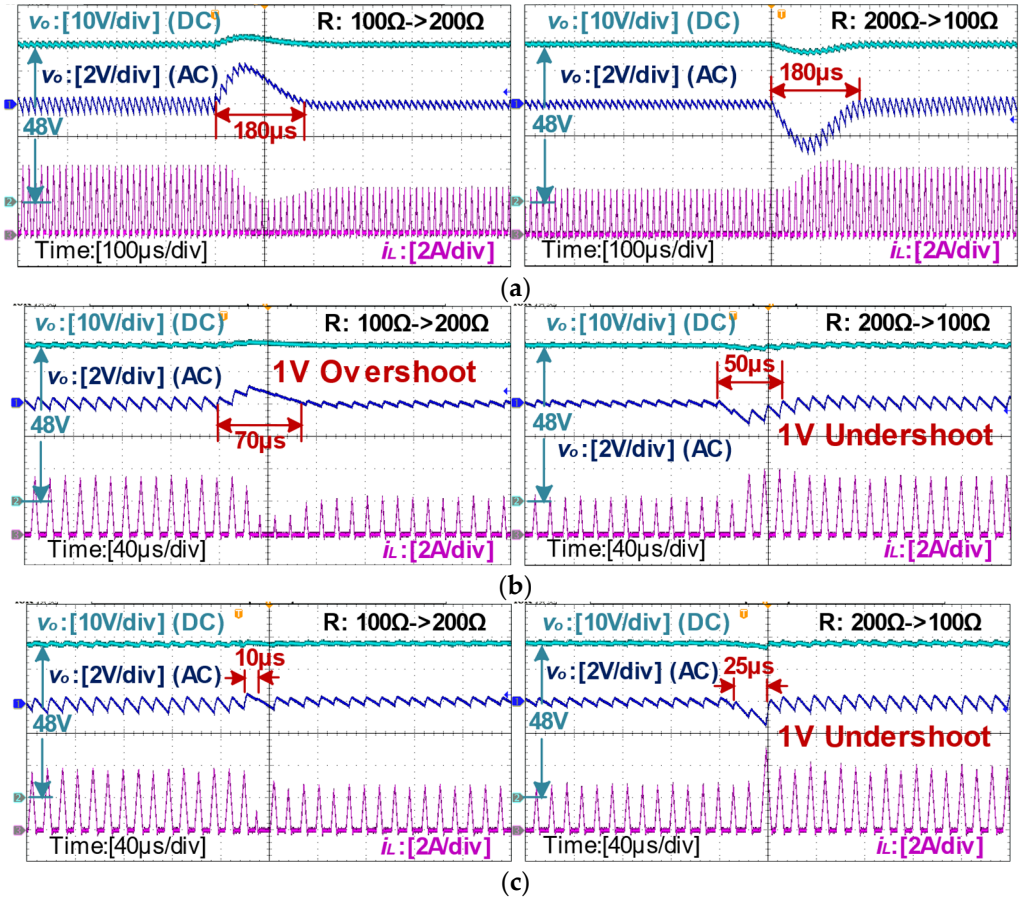


Figure 12. Transient voltages and currents when R steps from 100 Ω to 200 Ω and from 200 Ω to 100 Ω under (**a**) PI control, (**b**) CBAC control, and (**c**) dead-beat control based on DVP and SCE.

6.2.2. Transient Response to Line Voltage

To illustrate line voltage transient performance of the proposed controller, v_o and i_L are compared under PI, CBAC, and the proposed controls. As shown in Figure 13a, when vin steps from 19.2 V to 24 V, v_o re-stabilizes in 200 μs under PI control. When v_{in} steps from 24 V to 19.2 V, v_o re-stabilizes in 170 μs. As shown in Figure 13b, v_o re-stabilizes in 45 μs under CBAC control when v_{in} steps both from 19.2 V to 24 V and from 24 V to 19.2 V. Comparatively, as shown in Figure 13c, v_o re-stabilizes in 25 μs under proposed control when v_{in} steps both from 19.2 V to 24 V and from 24 V to 19.2 V. Furthermore, the voltage overshoot/undershoot is 1 V under CBAC control, and it is suppressed to 0.5 V under DVP control. As indicated above, the proposed controller achieves better transient response towards line voltage variations with shorter response time and lower overshoot/undershoot.

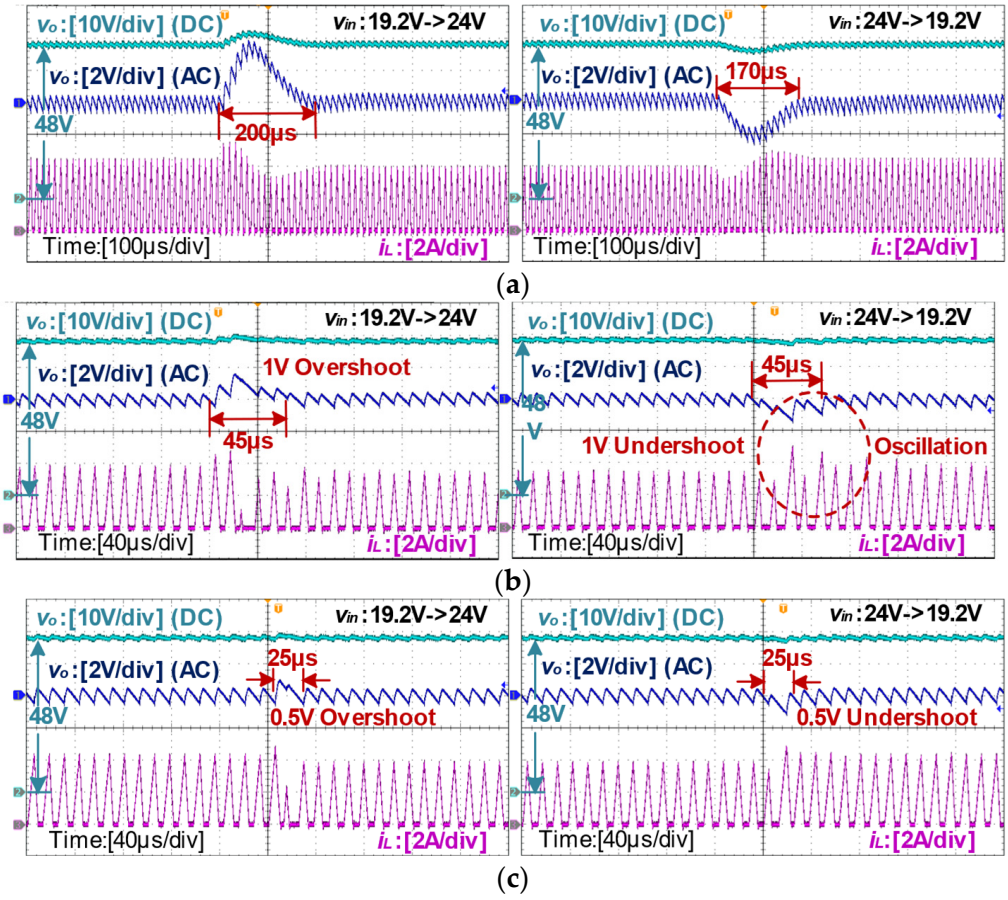


Figure 13. Transient voltages and currents when vin steps by 20% under (**a**) PI control, (**b**) CBAC control, and (**c**) dead-beat control based on DVP and SCE.

6.2.3. Reference Voltage Tracking

To illustrate reference voltage tracking performance of the proposed controller, v_o and i_L are compared under PI, CBAC, and the proposed controls. For a converter with PI controller, v_o tracks v_{ref} in 160 µs when v_{ref} steps from 48 V to 52 V, and in 180 µs when v_{ref} steps from 52 V to 48 V, as shown in Figure 14a. For CBAC control in Figure 14b, v_o tracks v_{ref} in 60 µs when v_{ref} steps from 48 V to 52 V and in 40 µs when v_{ref} steps from 52 V to 48 V. Furthermore, due to load estimation error and additional control delay, some oscillation occurs in both transients. As a comparison, v_o under proposed control tracks v_{ref} in 40 µs in both transients, as shown in Figure 14c. As indicated above, for reference voltage tracking, the proposed control achieves better transient response than PI and CBAC controls.

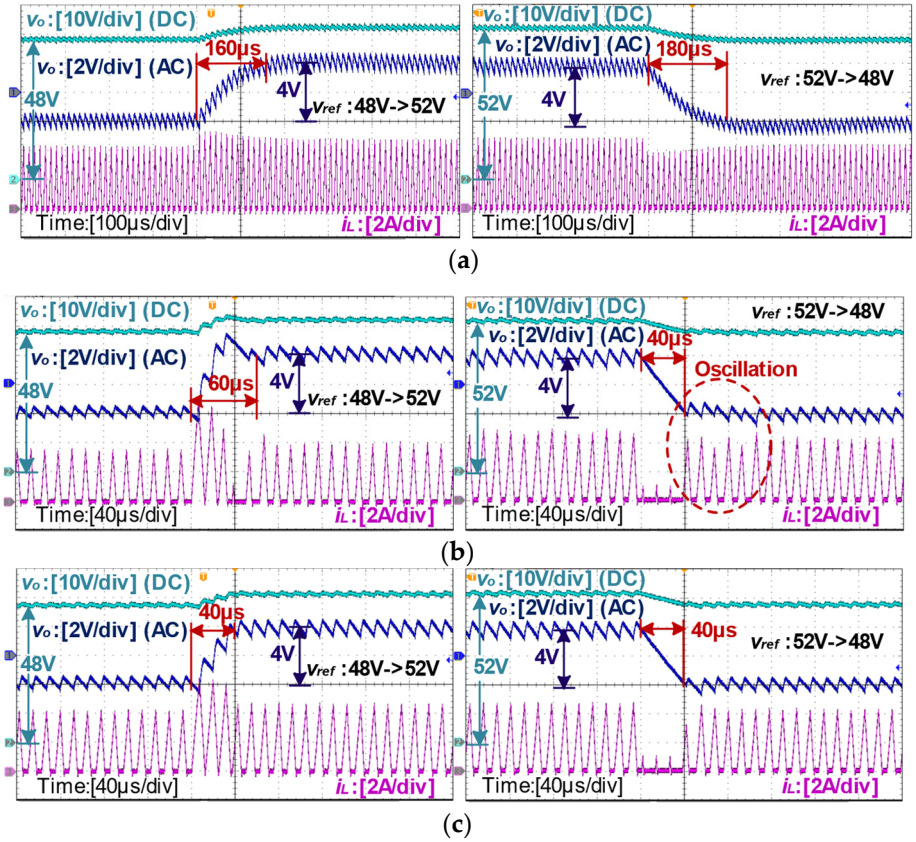


Figure 14. Transient voltages and currents when v_{in} steps by 4 V under (**a**) PI control, (**b**) CBAC control, and (**c**) dead-beat control based on DVP and SCE.

6.3. Large Signal Transients

Since DPWM saturation usually does not occur in small signal transients, large signal transient experiments are given in the followings to illustrate the effectiveness of the proposed switching-cycle extension strategy.

Transient voltage and current when R steps from 250 Ω to 60 Ω are given in Figure 15. As shown in Figure 15a, v_o re-stabilizes in 40 μs without switching-cycle extension. With switching-cycle extension, it re-stabilizes in 25 μs, as shown in Figure 15b. Furthermore, the first extended switching cycle during transient is 16 μs with switching-cycle extension while it remains 12.5 μs without switching-cycle extension.

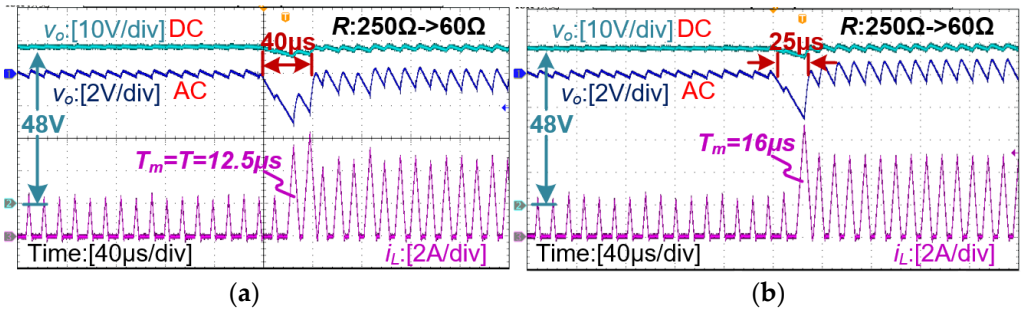
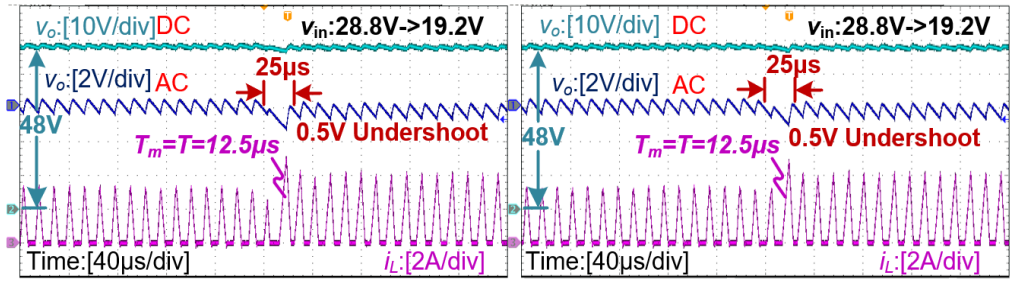


Figure 15. Transient voltages and currents when R steps from 250 Ω to 60 Ω under proposed control (**a**) without SCE and (**b**) with SCE.

Transient voltages and currents when v_{in} steps from 28.8 V to 19.2 V are given in Figure 16. When the input voltage drops, there is a small steady-state error in the output voltage due to parasitic resistance in the circuit. This steady-state error can be eliminated

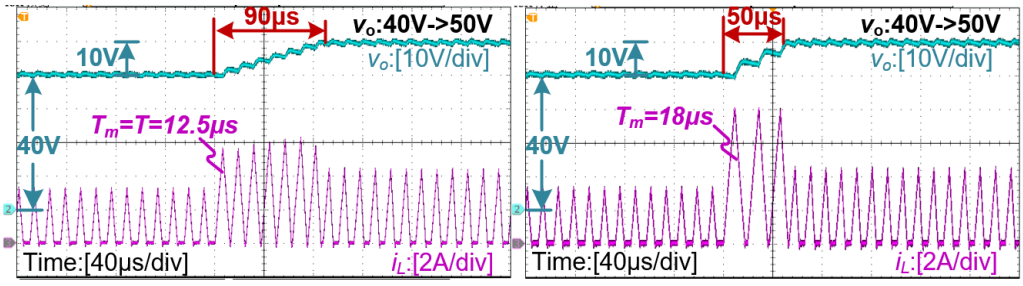
by a more accurate system model that takes into account the parasitic parameters, but this increases the arithmetic complexity. Since this steady-state error is within the allowable range, as a compromise, the complex parasitic parameter model is not used. For proposed control with/without switching-cycle extension, both output voltages re-stabilize in 25 µs. The achieved performance is similar, since DPWM saturation does not occur during the tested line voltage transients. The results also indicate that the proposed control can effectively suppress the line voltage disturbance.



(**a**) (**b**)

Figure 16. Transient voltages and currents when v_{in} steps from 28.8 V to 19.2 V under proposed control (**a**) without SCE and (**b**) with SCE.

Transient voltages and currents when v_{ref} steps from 40 V to 50 V are given in Figure 17. Without switching-cycle extension, v_o tracks v_{ref} in 90 µs. As a comparison, v_o tracks v_{ref} in 50 µs with switching-cycle extension. Furthermore, the first switching cycle during transient is 18 µs with switching-cycle extension, whereas it remains 12.5 µs without switching-cycle extension.



(**a**) (**b**)

Figure 17. Transient voltages and currents when v_{ref} steps form 40 V to 50 V under proposed control (**a**) without SCE and (**b**) with SCE.

In conclusion, dead-beat control based on DVP with switching-cycle extension improves the large signal transient when DPWM saturation occurs.

7. Conclusions

In this paper, optimal transient response for DCM DC-DC converters is achieved by voltage dead-beat control based on differentiative voltage prediction and switching-cycle extension. Through differentiative voltage prediction, the load estimation delay is effectively reduced, which improves the bandwidth and the output response in load transient. Furthermore, switching-cycle extension is implemented to enlarge the output voltage slew rate and operation range, which further improves large signal transients. Combining DVP with SCE, both line/load transient and reference tracking performances are optimized with shorter response time and smaller overshoot/undershoot. Effectiveness of the proposed controller is proved by closed-loop SSMs and verified by experimental results.

Author Contributions: Conceptualization, Q.L.; methodology, Q.L. and D.Z.; software, Q.L.; validation, Q.L.; formal analysis, Q.L.; investigation, Q.L. and L.Z.; resources, Q.L. and W.Z.; data curation, Q.L.; writing—original draft preparation, Q.L.; writing—review and editing, Q.L.; visualization, Q.L.; supervision, Q.L.; project administration, R.M., Q.Z. and Q.T.; funding acquisition, Q.T. All authors have read and agreed to the published version of the manuscript.

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