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Design of a 200 W Flying Capacitor Multilevel Flyback Converter

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Abstract: This directive proposes an efficiency optimization process in which the flying capacitor multilevel flyback converter (FCMFC) will be designed for the highest efficiency based on component selection, the number of flying capacitor stages, with isolation. The application of interest is a front-end voltage-boosting converter that is part of a solar microinverter. The converter will need high gain and high efficiency over a large range due to the variable input voltage supplied by the output of a solar panel. The electrical specifications are 40 V to 400 V conversion for a 200 W load; however, the input voltage and load power are subject to variability.

Keywords: flying capacitors; multilevel conversion; optimization; system efficiency

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1. Introduction

Multilevel inverters started to be explored in the 1980s with the neutral-point-clamped topology [1], began to be explored in the early 1990s for induction motor drives by both ABB [2] and Robicon [3], and was used for static var utility applications as well [4]. The most common inverter topologies include the neutral point clamped, cascaded H-bridge, and flying capacitor (FC) designs [5], but they have mainly found their applications in high voltage, high power grid applications.

In 2014, Google offered a global competition called the Little Box Challenge where teams set out to design a 2 kW-rated inverter and had to have an efficiency greater than 95% and fit within a 40 cubic inch containment. As a result, teams started to scale these multilevel topologies traditionally used in high power applications to meet these specifications. Design teams chose the modular multilevel topology [6], and the FC began to penetrate the literature more prominently through the team's effort showcased in [7]. Observing [7–9], the authors designed FC articles with 7-, 9-, and 13-level architectures for inverter applications. Others have designed significantly higher-power topologies using the FC architecture [10], using silicon carbide MOSFETs, and proposed protection schemes in [11]. In this work, the team explores the utilization of FC in an isolated DC-to-DC topology, optimizes the number of FC output stages, and designs and tests the topology for higher power levels but nowhere near the levels for a grid-connected system.

The flying capacitor multilevel flyback converter (FCMFC) operation is well-documented in [12] with one of its most notable features tied to its voltage conversion ratio, $M(D)$, listed as (1), where n is the transformer turns ratio, N-1 is the capacitor stages, D is the duty cycle, V is the output voltage, and V_{in} is the input voltage.

$$M(D) = \frac{V}{V_{in}} = \frac{n(N-1)D}{1-D} \tag{1}$$

As explained in [12], the operation of the FCMFC is shown in Figure 1. Note that this is the simplest FCMFC with N = 3 voltage levels (2 capacitors: 1 flying capacitor and 1 output). With S MOSFET ON, the magnetizing inductance of the double wound inductor will charge for DT_s shown in the top left of Figure 1, where T_s is the switching period (or

the inverse of the switching frequency f_s). During this stage in the sequence, secondary conduction through the body diode of the FETs is prevented by the addition of diode D_3. In the next stage, S MOSFET turns OFF and S_2 turns ON with S_1 OFF as shown in the top right of Figure 1. Here, the inductor solely charges the flying capacitor C_1 through D_1, S_2, and D_3. The next state in the sequence is the same as the first that was earlier described and shown in the top left of Figure 1. Finally, the output stage is shown in the bottom right of Figure 1 where S and S_2 are OFF and S_1 is ON. It is important to note that the current is flowing through the negative end of C_1 and through D_2 into the output capacitance and then back through D_3. The energy of the output capacitor is boosted by the inductor and flying capacitor leading to a multiplication effect with higher gains described by (1). For comparison purposes, a traditional flyback converter is shown in the bottom left of Figure 1 (or when $N = 2$).

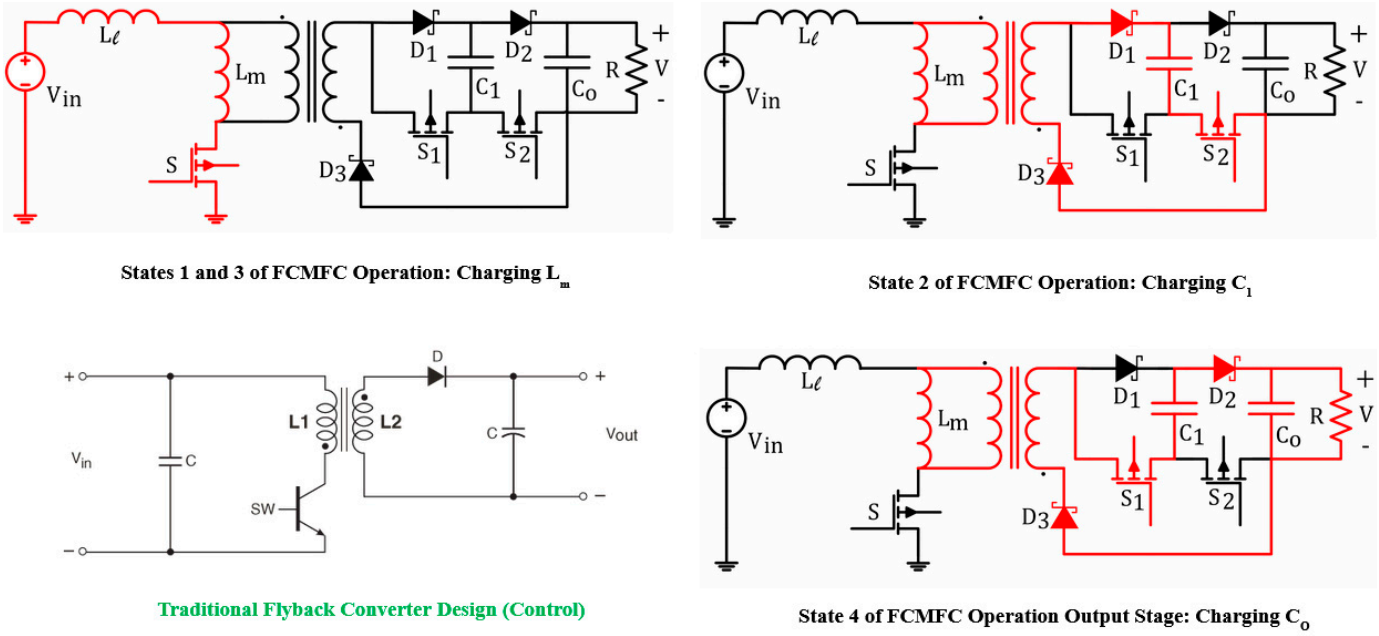

Figure 1. States of the FCMFC [12].

In [13], the authors expanded on these findings with a holistic and accurate efficiency model of the converter. The models can now be used to optimize the FCMFC designs for the number of flying capacitors. As was seen in previous work, there are significant improvements that are seen using this multilevel topology. However, there is a diminishing return where the added conduction losses of higher-level converters (more flying capacitors) start to degrade the overall efficiency. This work proposes an efficiency optimization process in which the FCMFC will be designed for the highest efficiency based on component selection and number of flying capacitors. The application of interest is a front-end voltage-boosting converter that is part of a solar microinverter. The converter will need high gain and also high efficiency over a large gain range due to the variable input voltage supplied by the output of the solar panel. The electrical specifications are 40 V to 400 V conversion for a 200 W load; however, the input voltage and load power are subject to variability.

Optimization for power converters can take on many forms. Single or multi-objective problems can be solved. For example, efficiency itself can be optimized as a single objective, but this design will likely not be as power dense if power density were the design objective. This leads to a multi-objective optimization problem where tradeoffs can be made between efficiency and power density. This work focuses on the single objective problem of efficiency to prove the electrical capabilities of the proposed converter. Power density objective optimization could be performed beyond this work in order to shrink the converter down for commercial use. Techniques from all forms of optimization are useful, however, in the formulation of this work.

A multidimensional optimization of efficiency, output capacitor current ripple, and core temperature rise of boost and flyback converters was performed in [14]. Many variables were chosen before performing the optimization, such as input and output voltage and load power requirement, whereas some papers leave the optimization more open-ended. The optimizations were performed in many dimensions for varying switching frequency and magnetic core turns, n. Certain values were varied, and then, efficiency was optimized at those various points generating 3D surfaces, which could be analyzed for the optimization of relationships. The authors also discuss weighting functions as to what matters more in some cases, cost or efficiency. Another point made was that optimization is not always possible. Sometimes, like in this case with discrete converter levels (N), the optimal choice would be unrealizable, such as zero or infinity, and in these cases, the variables will need to be constrained in order to find a realizable result for the optimization. Again, optimizing two things is not always possible because one will be in contention with the other.

One work detailed an optimization process for a boost converter that was powered with fuel cells for portable military applications [15]. The metrics of optimization are efficiency, switching frequency, capacitance, ON resistance of FETs, current density, and inductor ripple. These values were found at which point the mass would be minimum, and then, the plots were made as a function of mission duration. The paper has useful equations to predict switching and conduction losses for transistors and diodes. It also discusses how to estimate loss components, like the gate charge, from the data sheet. Other optimizations have been performed for the basic converter structures and for varying objectives tied to efficiency [16,17].

In recent literature, authors have proposed optimization routines for power electronic rectifier systems [18]. The team was concerned about system parameter impacts on the efficiency limits. The team was also one of the first to conceptualize multi-objective requirements tied to both power density and efficiency. Generally, the optimization loop routines will calculate magnetic and semiconductor losses based upon electrical parameter setpoints (currents, voltages, and flux density) and drive the losses to a minimum by making modifications to converter setpoints for frequencies, inductor volumes, etc. The authors applied the same optimization routines to phase-shift converters and parallel resonant converters for telecom power supplies [19].

In the last few decades, the use of genetic algorithms has grown in optimizing a power electronic system as opposed to an individual component. Here, each design is represented by a gene string, where a gene string represents the set of electrical components that define one possible converter design (switch, magnetic core, and capacitor). Further details are elaborated on in [6]. Other groups who have designed power converters with flying capacitors have chosen to use Monte Carlo approaches because of the wide design optimization space [8].

Specific to the flyback design and base topology of the FCMFC, the authors developed a routine that utilized a bank of core sizes, materials, diodes, MOSFETs, and operating points (similar to all cited work in this article) and utilized an objective function based upon a ratio between the minimum loss and output power as a function of the electrical design parameters (turns ratio, primary side turns, MOSFET selection), operating point, and switching frequency [20].

Similar techniques as those presented in [20] were adopted because the team desired a relatively simple routine that would utilize their detailed loss model capable of representing the main loss mechanisms over a wide range of operating points [2] and an objective function that allows for minimization of the power loss weighted over a range of operating points. Similar to all routines mentioned and cited, the team also wanted to utilize a bank of semiconductor devices that were readily available and utilized by the authors in previous designs and would serve as constraints in the optimization routine. The critical question for this work is to not optimize the overall power electronic system but optimizing the number stages of the FCMFC and seeing the impact of these stages on system loss.

2. Materials and Methods

Previous work in [12] has shown that the higher order, N, of a FCMFC converter, the lower the voltage stress and, thus, the required rating of semiconductor devices. In the prototype to be developed, this was not taken advantage of because robust design and reliability were paramount to verify the novel converter's functionality. Now that the converter has been proven to operate in a stable matter with open loop control, a component selection mechanism will be used in the optimization process. The key is that lower voltage rating devices have inherently lower on-resistance and will thus experience lower conduction losses and make the converter more efficient. With a higher N, the more the voltage is reduced that each stage must withstand.

Power Converter Optimization and Component Selection

The optimization process for a voltage-boosting converter is outlined in Figure 2, where minimal power loss is the objective. This converter is designed to serve as the front end of a microinverter, boosting the photovoltaic panel output to adequate levels for inversion into AC power. The components selected for this routine will constrain the problem, as well as the electrical operating points shown in Table 1. The input voltage will vary based on solar shading, as well as the output power depending on load demand. The switching frequency is a free variable of the optimization within its given constraint boundary. The output voltage is fixed at 400 V with a 5% ripple value.

Table 1. Electrical specifications.

Input Voltage (V_g)	Output Power (P_{out})	Switching Frequency (f_s)	Output Voltage	Voltage Ripple
20–40 V	100–200 W	100–600 kHz	400 V	5%

Given the (N) value and operating ranges defined in Table 1, the estimated voltage ratings of the components are used to select commercially available MOSFETs, capacitors, and diodes. The data sheet information for each component is now fed into the optimizer routine so it can perform the outermost loop of the routine, which is the number of converters levels (N) that equates to the number of flying capacitors ($N - 1$). Q_{in} and Q_{out} are defined as the input and output MOSFET gate charge values provided from their respective data sheets. The frequency range considered is 100–600 kHz and is treated as a continuous variable in the routine. This outermost loop runs the entire optimization routine for each potential (N) level FMCFC. The next inner loop sets the operating point (V_g and P_{out}) and then sweeps to find which frequency results in the least amount of power loss. This loop is running all possible operating scenarios based on solar irradiance varying the input voltage from 20 V to 40 V. The routine now has multiple optimal frequencies of operation for each potential quiescent operating point. These values are then fed into the objective function that assigns a weight value (<1) to each operating point. The objective function is now a minimized compilation of the various operating points. The routine continues for all N values specified and will result in one design that is the most efficient.

In summary, this design routine considers the various operating points required by the boost converter. Considering the stress reduction explained herein, each (N) level design is able to utilize components of lower voltage ratings in their operation. The datasheet information for these components is entered into the routine so that it can optimize singular (N) level design overall operating points where each operating point will have an optimal frequency associated with it. Considering that the converter will have some tendency to vary how often it operates on certain points based on solar irradiance, there is a weighting coefficient tied to each operating point in the objective function. This weighting was applied equally to all nine operating points, which are derived with equal steps from 20–40 V input voltage and 100–200 W output power. The routine will calculate and find the most efficient design and the associate converter level (N). Now, the optimal converter can be built and

tested over the operating range with an optimal switching frequency for each quiescent point. For a deeper elaborate treatment, see [21] for the Matlab code that programmed the algorithm in Figure 2.

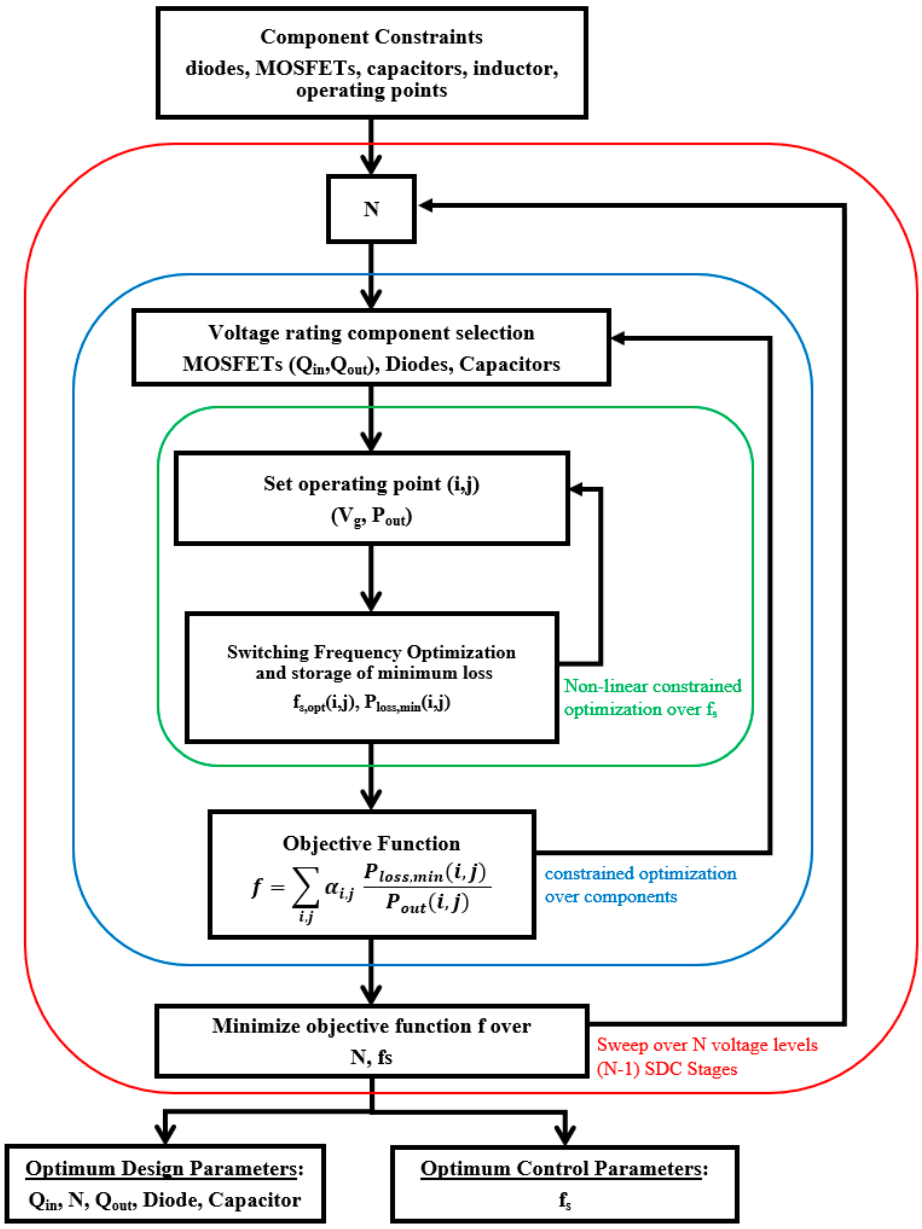

Figure 2. Multilevel design process.

Converter levels were limited to N = 2–7. This includes the flyback converter for comparison to the FCMFC topology. Given the supply chain constraints brought about by the COVID-19 pandemic, the component selection process was limited by availability. Semiconductor components were chosen with a 65% voltage derating factor and 55% current derating factor. Table 2 show the component ratings required for each of the considered converters in this study. These tables were calculated using the steady-state operation equations provided in [12] and the operating specifications in Table 1.

The MOSFET package size was constrained to a TO-263 surface mount package and diodes were constrained to a TO-252 surface mount package. Higher N level devices require lower blocking voltages, which also opens up for higher available drain currents leading to even lower ON resistances. This in turn will have a significant efficiency benefit for FCMFC over the flyback converter. In addition, when discussing the added components,

this does not add significant loss because of the conduction time for each component. For example, the flyback suffers the worst diode loss (~40%) even though it only has 1 diode. This is because of the significant voltage that the diode must block. The FCMFC converters do have more diodes, but each diode conducts for a fraction of time less than the flyback converter and thus does not double or triple diode losses. This will have the added benefit of reliability because FCMFC components are under less stress and power loss, thus operating at lower temperatures, making them last longer than a flyback converter. *iQ* is calculated steady-state input current, *iQ* Rating is the rated max current of the semiconductor, V_{block} *Q* is the calculated max voltage across the semiconductor while Q_{min} *Rating* is the rated blocking voltage in Table 2.

Table 2. Primary FET (left) and Secondary FETS and diodes (right).

Primary FET						Secondary FETs								
N	V_{in} [V]	*iQ* [A]	*iQ* Rating [A]	V_{block} *Q* [V]	Q_{min} Rating [V]	*N*	V_{out} [V]	I_{out} [A]	R_{out} [Ω]	P_{max} [W]	V_{block} [V]	V_{min} Rating [V]	I_{sec} Peak [A]	I_{min} Rating [A]
2	40	13	23	280	431	2	400	0.5	800	200	400	615	7.8	14.2
3	40	13	23	160	246	3	400	0.5	800	200	200	308	7.8	14
4	40	13	23	120	185	4	400	0.5	800	200	133	205	7.8	14
5	40	13	23	100	154	5	400	0.5	800	200	100	154	7.8	14
6	40	13	23	88	135	6	400	0.5	800	200	80	123	7.8	14
7	40	13	23	80	123	7	400	0.5	800	200	67	103	7.8	14

These data were then used to search Digi-Key and Mouser online catalogues to find MOSFETs with the lowest ON-resistance and diodes with the lowest forward power dissipation. The components chosen are shown for primary FETs, secondary FETs, and secondary diodes and are shown in Table 3, Table 4, and Table 5, respectively.

Table 3. Primary FET Available Options.

	Required Ratings		Digi-Key	Component Ratings		
N	*iQ* Rating [A]	*Q* Rating [V]	Part Number	R_{max} [mΩ]	Volts	Amps
2	20–30	431	AOB29S50L	150.0	500	29
3	20–30	246	IPB407N30NATMA1	40.7	300	44
4	20–30	185	IXTA94N20X4	10.6	200	94
5	20–30	154	FDB075N15A	7.5	150	130
6	20–30	135	FDB075N15A	7.5	150	130
7	20–30	123	FDB075N15A	7.5	150	130

Table 4. Secondary FET available options.

	Required Ratings		Digi-Key	Component Ratings		
N	qd Rating [V]	iq Rating [A]	Part Number	R_{max} [mΩ]	Volts	Amps
2	615	14–20	-	-	-	-
3	308	14–20	IPB407N30NATMA1	40.7	300	44
4	205	14–20	IXTA94N20X4	10.6	200	94
5	154	14–20	FDB075N15A	7.5	150	130
6	123	14–20	FDB075N15A	7.5	150	130
7	103	14–20	AUIRLS4030	4.3	100	180

Table 5. Secondary diode available options.

	Required Ratings		Digi-Key	Data
N	**qd Rating [V]**	**iq Rating [A]**	**Part Number**	P_{loss} **Curve**
2	615	14–20	VS-15EWX06FNTR-M3	yes
3	308	14–20	RFN10BM3SFHTL	yes
4	205	14–20	DSA15IM200UC-TRL	yes
5	154	14–20	SBR20M150D1Q-13	yes
6	123	14–20	V20PWM12HM3/I	yes
7	103	14–20	V20PW10-M3/I	yes

All diodes selected have forward dissipation curves that are interpolated using Microsoft Excel 2016 as shown in Figure 3 for the N4 converter diodes. These data are used with the curve fit function that produces a second-order equation. This equation is then used within a Matlab 2022a script to interpolate the diode forward dissipation loss for all given operating points.

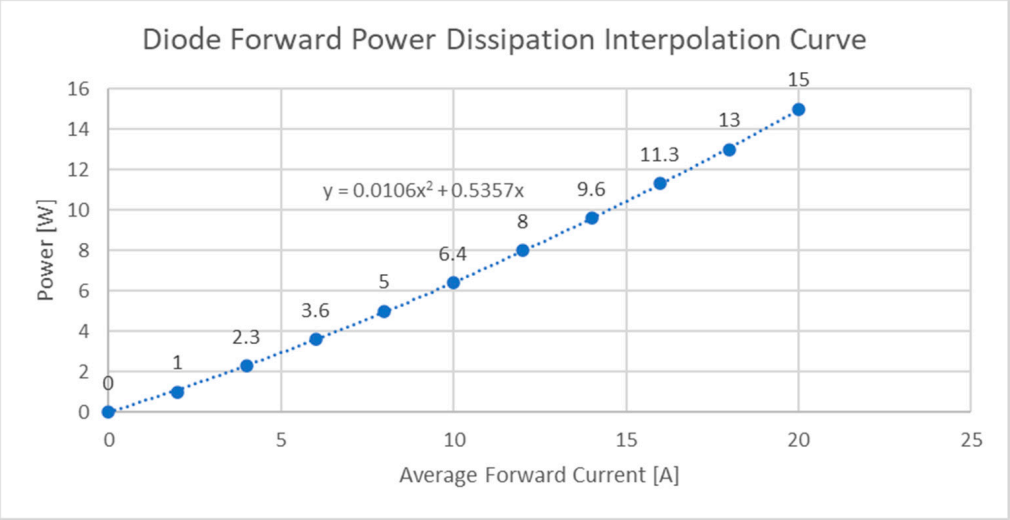

Figure 3. Diode forward power dissipation interpolation curve.

3. Results

The optimization routine outlined in Figure 2 was programmed in Matlab. The code is included as a .m file found in [21]. The electrical operating specifications are set as per Table 1. Next, all the necessary data for components are set using arrays for each operating variable. This includes the transformers, capacitors, and the various MOSFETs and diodes that can be used given each converter's operating limits.

Point plots are shown for the comparison of each converter's power loss at the three operating points shown in Figure 4 (P = 200 W | V_{in} = 40 V; P = 100 W | V_{in} = 20 V; P = 66.7 W | V_{in} = 13.33 V). The flyback converter, N2, has the highest losses associated with all three operating points while the N4 FCMFC is the lowest. The N6 converter has a similar loss profile to N4, but, due to the added complexity of two additional switching stages, this converter is not optimal. Notice that going from N6 to N7, the power losses begin to increase partly because of the added stage but also due to the diminishing return of the voltage-distribution benefit associated with multilevel converters. For these design criteria and available components, the optimal converter is with N = 4.

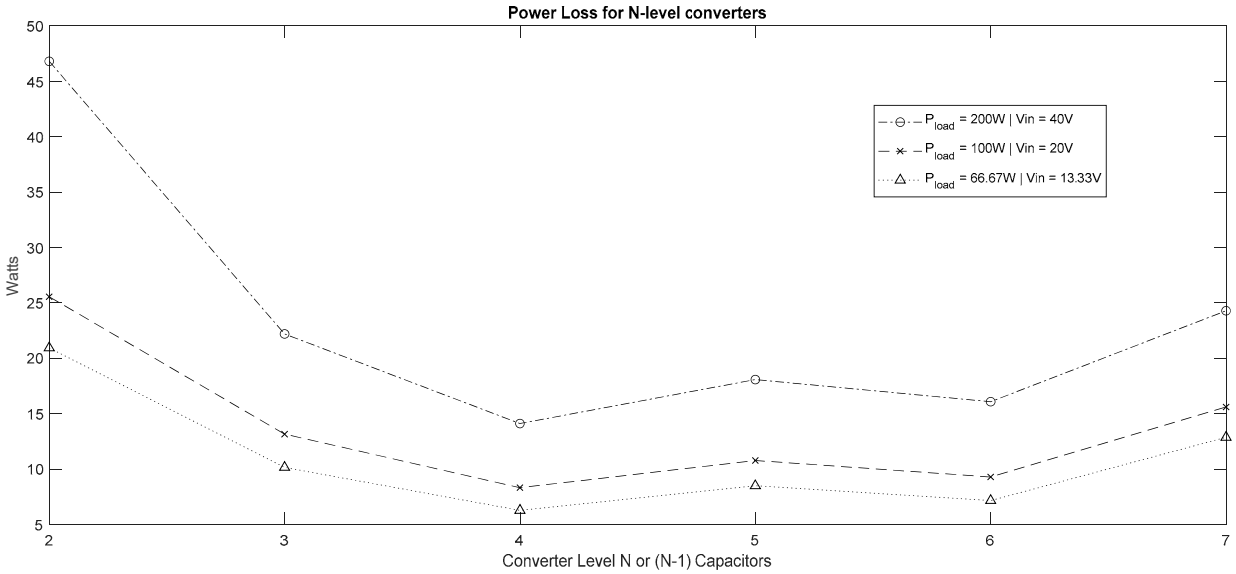

Figure 4. Power loss curve (P = 200 W | V_{in} = 40 V; P = 100 W | V_{in} = 20 V; P = 66.7 W | V_{in} = 13.33 V).

3.1. Power Loss Breakdown Comparison

It is important to understand the power loss mechanisms for these converters and how they influence the optimal design. For each point in Figure 4, the associated power loss breakdown is shown in a pie chart in this section. Six different converters at three different operating points leads to 18 separate loss breakdowns, Figures 5–7. The charts are interleaved so that each operating point can be compared easily amongst the converters. The pie charts are a percentage breakdown of the power loss for a particular converter at a particular operating point; with this, it is important to understand that the percent values in each chart are portions of a different number each time. Trending in this case will be discussed accordingly. For example, the diode loss percentage increases from 29% to 34% but as a portion of a smaller total power loss. This means that diode losses for the N2 case make up a smaller portion of total loss, but when compared to the N3, the diode losses are much higher. Both the portion of a loss component and its absolute power loss are important in this section when describing the trends in the design process results. Also note that the flyback converter does not have the secondary FETs, gate drivers, and isolated power associated with the FCMFC converters. The optimal designs are chosen to have the lowest total loss, which means that each individual component loss is not minimized in every case, which can have an effect on trends. For a thorough treatment in calculating the losses for the FCMFC, readers are encouraged to review [13].

Operating Point 200 W | 40 V_{in}. Efficiencies for this power point start at 81% for the N2 flyback and increase up to 93.4% for N4 and then trend down slowly to 89% for the N7. Diode losses are reduced from N2 to N7 even with the addition of multiple diodes for the multilevel converters. The primary reason for this is the reduction in reverse recovery loss due to lower reverse voltage on the diodes. Capacitor ESR is insignificant (<1%) and consistent for all converters. The input primary FET power loss is significantly reduced for FCMFCs, going from 44% for N2 down to 11% for N7, indicating the reduction in voltage stress on that component. The secondary FETs result in a power loss that is increasing for higher level converters. Starting at 10% for the N3 converter and increasing to 43% of the loss for the N7 converter, the secondary FET loss increases because of the increase in FETs present that must handle the secondary current. The diminishing return effect is seen in this instance. As the converter level increases, the voltage-distribution benefit is counteracted by the sheer increase in power processing components and conductive loss through them, and thus, the most efficient converter is not the highest level considered. Core loss ranges between 10 and 20% of the total loss for all converters. Core loss is driven by the peak flux density and switching frequency. FCMFC converters have lower duty cycles and result

in lower peak flux but have varying minimum switching frequencies, and thus, no trend occurs across converters for core loss in percent terms. In absolute terms, the FCMFCs experience lower core loss, which will be discussed in the coming sections. Primary FET gate drive loss is similar for all converters as expected. Secondary FET gate drive increases for higher-level converters that have more FETs, which is expected but also not a significant loss mechanism. The multilevel converters have isolated power components that have a similar trend due to the current they supply to the gate drivers. Winding loss is below 1% for all converters and should be similar because of the same average current processed by the transformer. Zener leakage is a significant loss component shown to vary amongst the converters in percent terms. The Zener snubber circuit protection level is different for each converter based on the FET protection required due to transformer reflection voltage. The snubbers required from N2–N7 are 336 V, 192 V, 144 V, 120 V, and 105.6 V respectively. A higher clamping voltage means less current let-through and thus lower power loss, but the voltage reflected by the secondary of the transformer is also critical, and in the case of FCMFCs, that voltage is reduced two, three, four, etc., times for each level added. This allows for ample protection of the lower rated FET in the FCMFC converters without any increase in snubber power loss. In fact, the FCMFCs will experience a decrease in snubber power loss as a result of this.

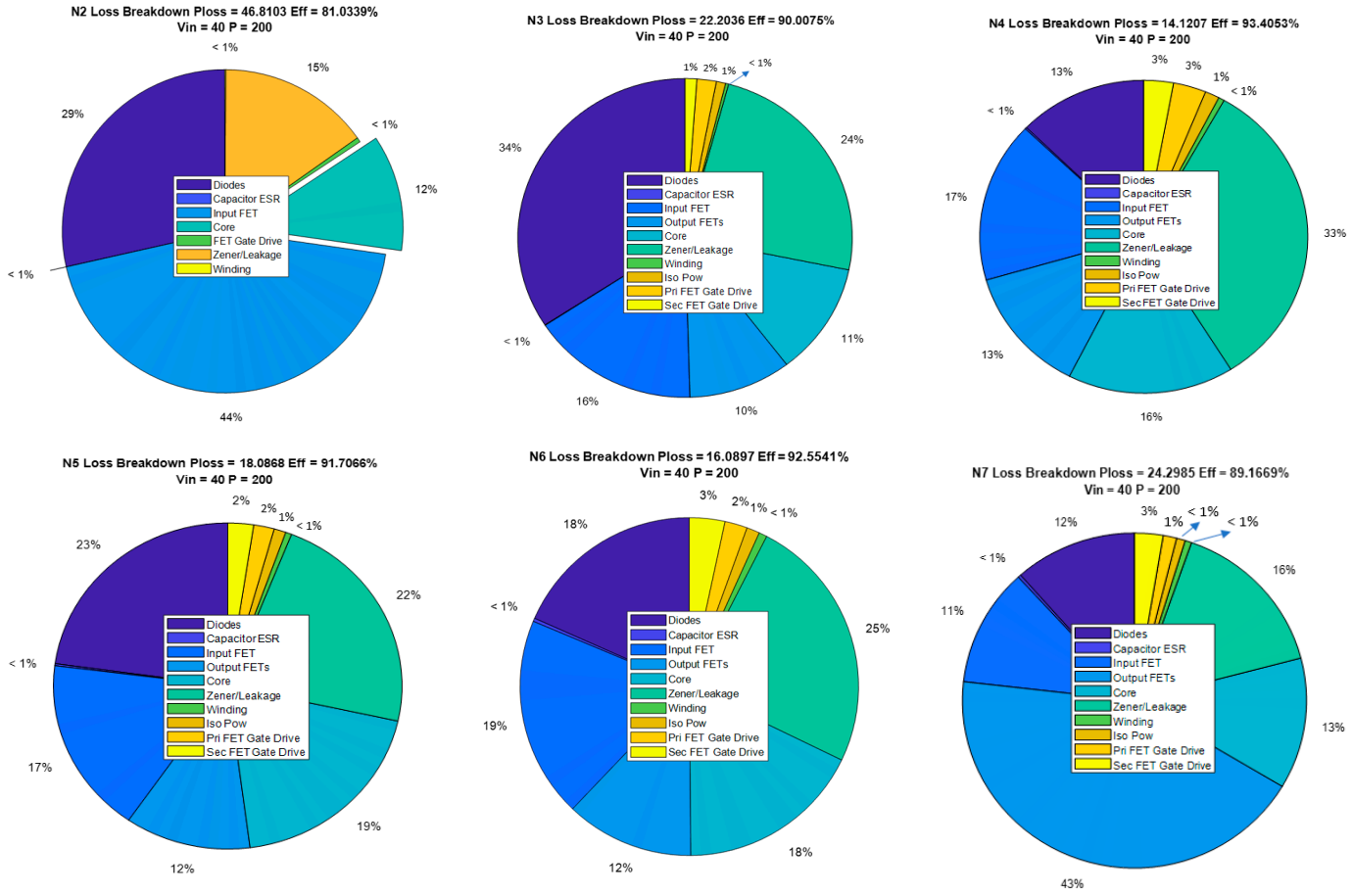

Figure 5. Power loss per component for P = 200 W | V_{in} = 40 V for N = 2 through N = 7.

Operating Point 100 W | 20 V_{in}. For the second operating point, the power processing is lower, but the voltage gain is higher. The same trends are seen for the 200 W 40 Vin operating point as for this operating point of 100 W 20 Vin shown in Figure 6. Because the power level is lower, the total power losses are lower, and the smaller fixed power losses (gate drive and isolated power) start to make up a larger percent of the total power loss.

Operating Point 66.67 W | 13.33 V_{in}. For the third operating point, the power processing is even lower, and the voltage gain is even higher. The same trends are seen for the 200 W 40 Vin operating point as for this operating point of 66.67 W 13.33 Vin shown in Figure 7. Because the power level is even lower, the total power losses are lower and the smaller fixed power losses (gate drive and isolated power) start to make up an even larger percent of the total power loss. Notice also that the diode loss percentages are falling as they are primarily a function of current.

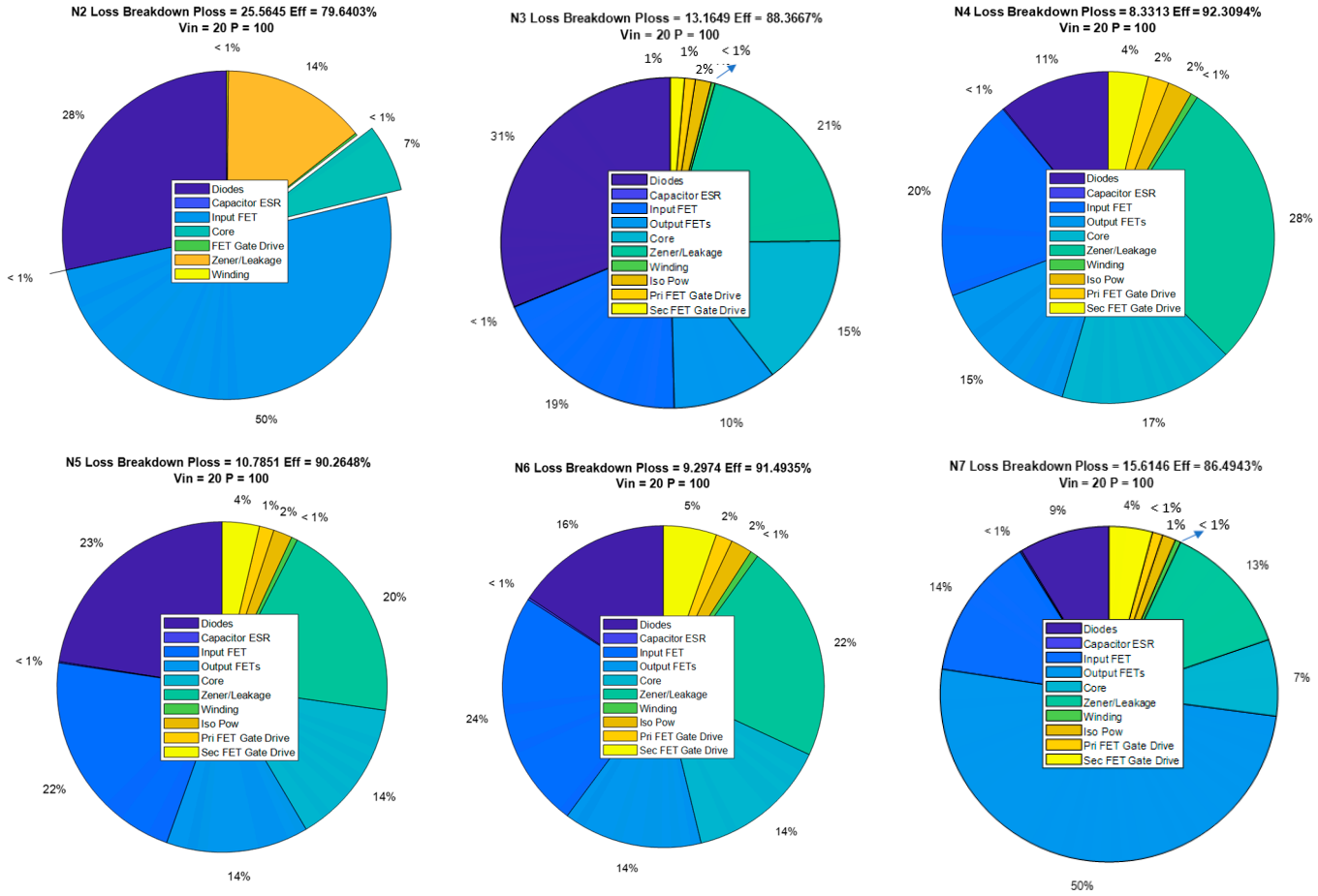

Figure 6. Power loss per component for P = 100 W | V_{in} = 20 V for N = 2 through N = 7.

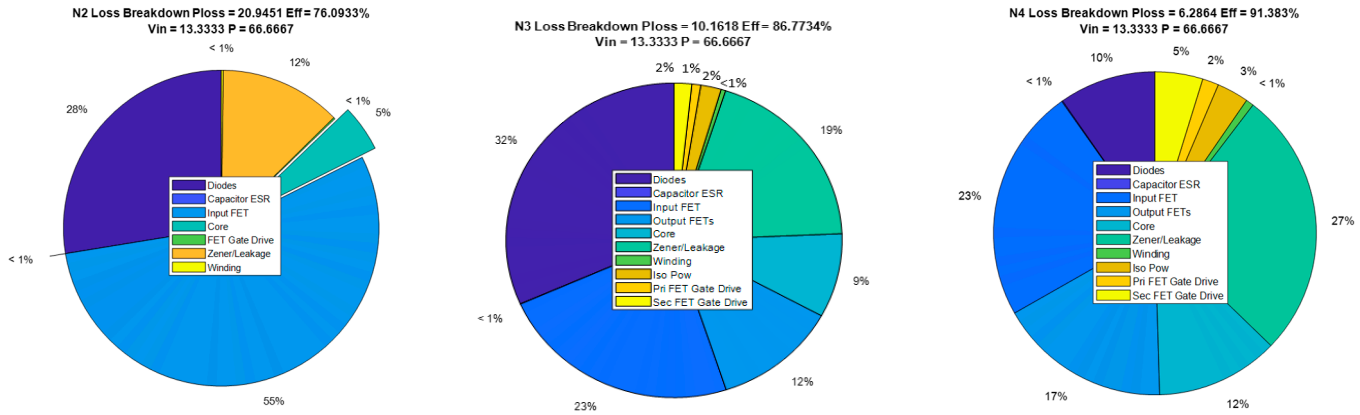

Figure 7. *Cont.*

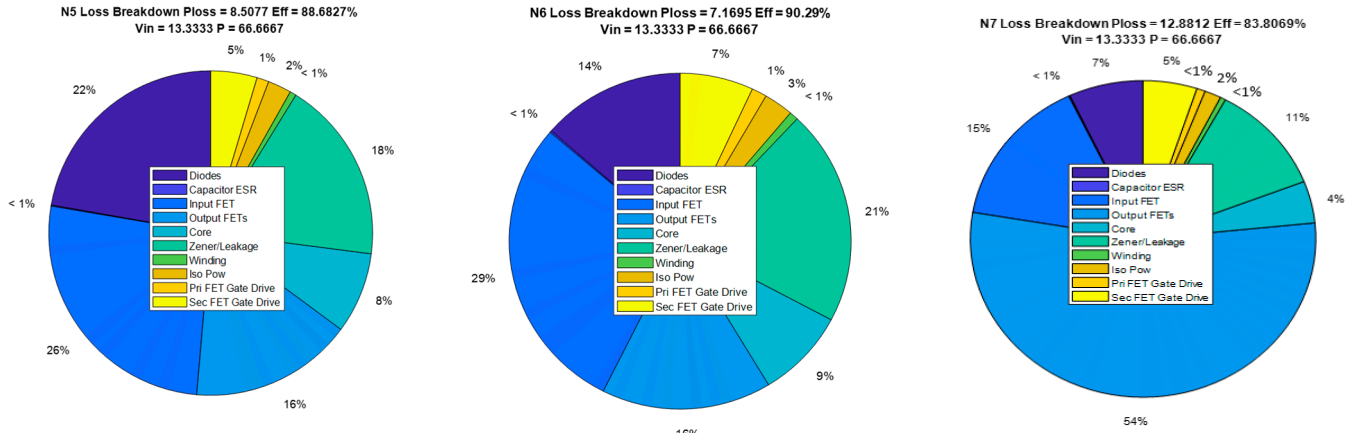

Figure 7. Power loss per component for P = 66.67 W | V_{in} = 13.33 V for N = 2 through N = 7.

3.2. Power Loss Comparison in Absolute Terms

This section summarizes the power-loss mechanisms for the six converters in three separate tables corresponding to the three operating points. Trends are important here to compare the multilevel structures to the flyback (N2). In Table 6 and highlighted in yellow is the diode power loss for the flyback and the lowest-level FCMFC. It would be expected that a converter with more diodes would suffer from a higher diode loss. In the case of FCMFC, the power is distributed so that more diodes can operate in an overall more efficient manner and thus cut the power loss almost in half. The trend continues for higher-level FCMFCs that have even lower losses.

Table 6. Operating point (200 W | 40 V_{in}) in absolute loss value comparison (Watts).

Converter	Diodes	Cap ESR	Input FET	Output FETs	Core Loss	Zener Snubber	Winding Loss	Isolated Power	Pri FET Gate Drive	Sec FET Gate Drive	Total [W]
N2	13.36	0.004	20.69	-	5.43	7.06	0.05	-	0.22	-	46.81
N3	7.59	0.012	3.60	2.20	2.53	5.34	0.06	0.20	0.42	0.25	22.20
N4	1.79	0.023	2.34	1.84	2.32	4.65	0.08	0.20	0.46	0.41	14.11
N5	4.12	0.036	3.14	2.11	3.53	4.07	0.10	0.20	0.35	0.43	18.09
N6	2.96	0.050	3.09	1.97	2.85	3.96	0.12	0.20	0.35	0.54	16.09
N7	2.80	0.067	2.77	10.5	3.07	3.77	0.15	0.20	0.31	0.65	24.23

Highlighted in red is the primary FET power loss that is significantly reduced from 20.69 W to 3.60 W with the addition of a single flying capacitor stage. This is a reduction of 83% and did not require complex auxiliary sensing and a control circuit that is required for zero-voltage switching schemes. Highlighted in blue is the loss for the secondary output FETs that are significant but do not add more loss than what is saved in the diodes and input FET as previously discussed, justifying their addition. Core loss in green is shown to be reduced in all FCMFC converters compared to the flyback converter. Similar trends are seen in Tables 7 and 8 for the 100 W and 66.67 W operating points, respectively.

Table 7. Operating point (100 W | 20 V_{in}) in absolute loss value comparison (Watts).

Converter	Diodes	Cap ESR	Input FET	Output FETs	Core Loss	Zener Snubber	Winding Loss	Isolated Power	Pri FET Gate Drive	Sec FET Gate Drive	Total [W]
N2	7.26	0.002	12.88	-	1.70	3.62	0.04	-	0.05	-	25.55
N3	4.12	0.005	2.50	1.31	1.96	2.70	0.05	0.20	0.13	0.18	13.15
N4	0.90	0.010	1.64	1.24	1.42	2.37	0.06	0.20	0.17	0.32	8.33
N5	2.43	0.014	2.36	1.51	1.54	2.13	0.06	0.20	0.15	0.39	10.78
N6	1.46	0.020	2.22	1.30	1.33	2.04	0.07	0.20	0.15	0.50	9.29
N7	1.36	0.025	2.15	7.85	1.15	1.99	0.08	0.20	0.15	0.65	15.60

Table 8. Operating point (66.67 W | 13.33 V_{in}) in absolute loss value comparison (Watts).

Converter	Diodes	Cap ESR	Input FET	Output FETs	Core Loss	Zener Snubber	Winding Loss	Isolated Power	Pri FET Gate Drive	Sec FET Gate Drive	Total [W]
N2	5.77	0.001	11.5	-	1.00	2.61	0.04	-	0.04	-	20.96
N3	3.21	0.003	2.38	1.22	0.87	1.97	0.05	0.20	0.09	0.17	10.16
N4	0.61	0.006	1.47	1.08	0.77	1.69	0.05	0.20	0.10	0.30	6.28
N5	1.89	0.009	2.24	1.38	0.69	1.55	0.05	0.20	0.10	0.39	8.50
N6	0.97	0.012	2.07	1.15	0.62	1.49	0.06	0.20	0.10	0.50	7.17
N7	0.90	0.015	1.96	7.00	0.55	1.44	0.07	0.20	0.10	0.65	12.89

3.3. Operating Parameters of Final Design

Each of the optimal designs from the previous section has an associated duty cycle and switching frequency of operation associated with it. That information is shown in Table 9 and will help further explain the power loss trends seen for flyback to multilevel converters.

Table 9. Operating parameters for final designs.

	200 W 40 V_{in}		100 W 20 V_{in}		66.67 W 13.33 V_{in}	
Converter	**Duty**	**Freq [Hz]**	**Duty**	**Freq [Hz]**	**Duty**	**Freq [Hz]**
N2	0.86	207,387	0.93	117,470	0.95	100,000
N3	0.75	160,070	0.86	103,324	0.90	100,000
N4	0.67	147,943	0.80	109,799	0.86	100,000
N5	0.60	112,270	0.75	100,000	0.82	100,000
N6	0.55	112,316	0.71	100,000	0.79	100,000
N7	0.50	100,000	0.67	100,000	0.75	100,000

From the previous section, it was apparent that the FCMFC greatly reduced the power loss associated with the primary FET. Table 9 shows that the N2 converter is switching at a higher frequency compared to the FCMFC converters. This is partially the reason for its higher loss, but also the voltage stress it handles is much higher due to the flybacks operation. These frequencies listed are shown for the converter operating as efficiently as possible for a given operating point so there are tradeoffs between loss mechanisms that lead to these duty cycle and switching frequency values. Note that the duty cycles of operation for the higher-level converters are lower, another reason for higher efficiencies in these converters.

The results listed in the previous Tables 6 and 9 show that N4 is the most efficient of the six converters considered. N4 values are highlighted in gray to emphasize this being the converter of choice. The N4 is at the cross-over point of benefit and trade-offs for the loss mechanisms and less complex to implement than the N6, which is a close second in terms of efficiency. These results are heavily dependent on the devices available and operating parameters of the converter.

3.4. Hardware Design and Prototype

The component list for the final design is shown in Table 10. Semiconductors from the previous design process are included, as well as the flying capacitors that are chosen for lowest ESR. The auxiliary component is also shown and has been tested in previous design to work for multilevel operation.

Table 10. 200 W component list.

Component	Brand	Part Number
Planar Transformer	Coilcraft	NA5871-AL 42 µH, 3:5
Flying Capacitors	KYOCERA AVX WIMA	2220CC105KAZ2A—1 µF DCP4I051006GD2KSSD—10 µF 600 V
MOSFETs	IXYS	IXTA94N20X4 200 V, 94 A
Diodes	IXYS	DSA15IM200UC-TRL 100 V, 15 A
Bootstrap Diode	Nexperia	PMEG10010ELR 100 V, 1 A, 50 Apk, 3.7 ns
Zener Diodes	Micro Commercial Co	3SMAJ5952B-TP 130 V 3 W
Heat Sink	Ohmite	BGAH150-125E
Gate Driver	Texas Instruments	UCC27512
Isolated Gate Driver	Texas Instruments	UCC21220A
Isolated Power	Analog Devices	LTM8067
Controller	Texas Instruments	C2000 F28335

The input voltage is now varying from 20 V to 40 V, and an auxiliary input power circuit was designed for 5 V to drive primary side gate driver chip logic. Another LTM8067 power circuit was designed to provide an isolated 12 V driving voltage for the FET gate drivers. Five Zener diodes were used in parallel to provide ample current handling at all operating points.

A four-layer board was required to make appropriate circuit routing without interference. Caution was taken to keep the gate driving and logic chips away from higher voltage and current areas that could cause electromagnetic interference with the gate signals. Figure 8 shows the prototype of the N4 design. The final board measures in at 325 × 172 mm.

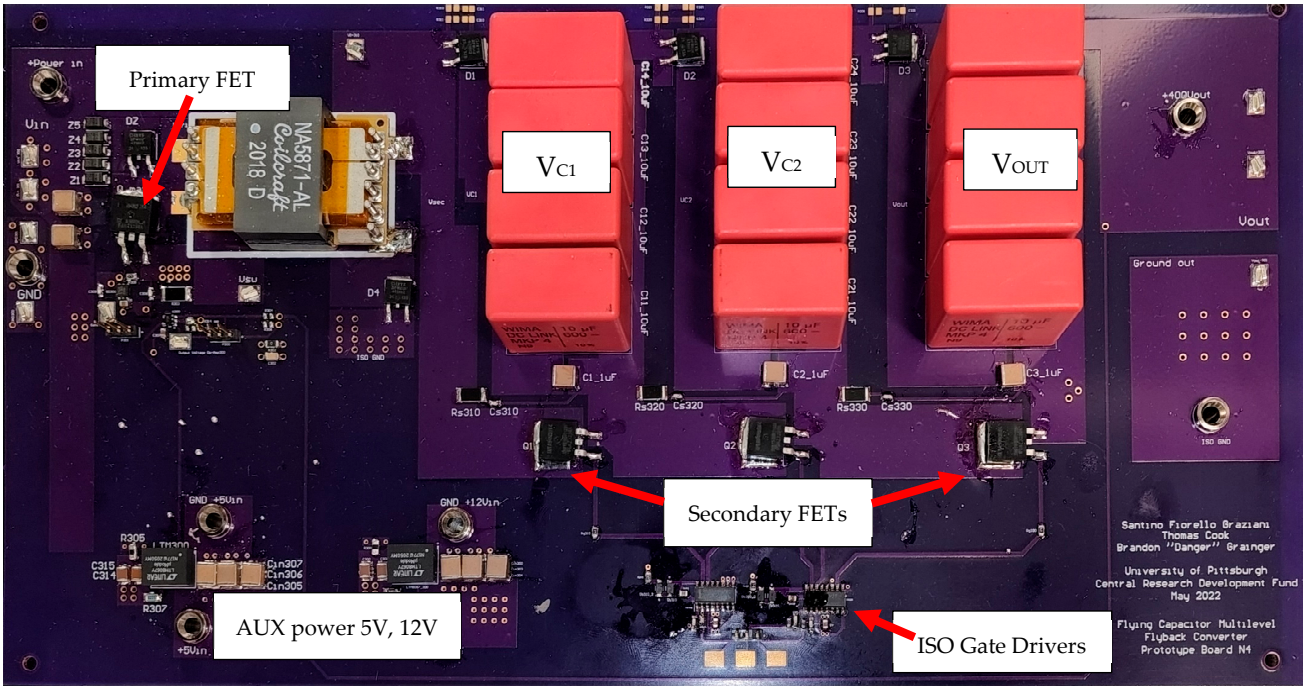

Figure 8. N4 Prototype board.

The power converter was tested using a Magna-Power DC power supply (SL500-5.2/208+LXI) and a Sorenson programmable DC load (SLH-300-18-1800). Scope captures were taken using a Yokogawa DL850E. Voltage and current measurements were taken using Fluke 87 multimeters. The hardware testing setup is shown in Figure 9 with equipment outlined.

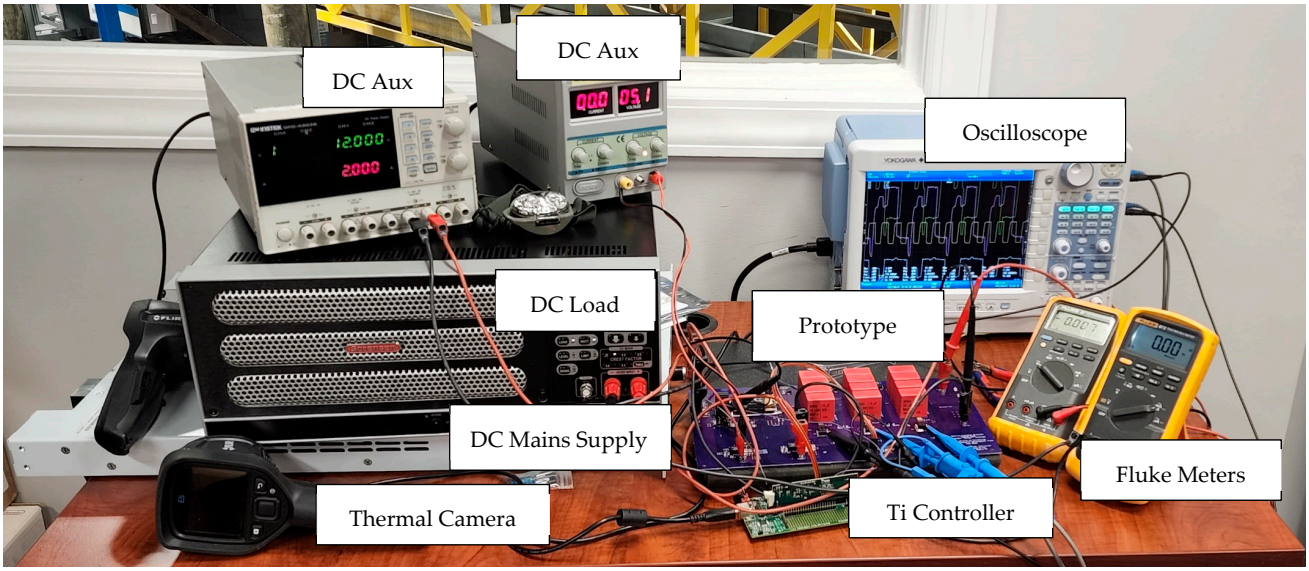

Figure 9. Hardware testing setup.

3.5. Prototype Results

The converter was tested for voltage output capability at a light load (~25–50 mA). Output voltages are shown in Table 11. The voltage across the flying capacitors is also shown in this table to verify that natural voltage balance occurs. Each operating point achieves the 400 V desired voltage and has a natural voltage balance across flying capacitors. This balance is key to maintaining the reduced blocking voltage across the semiconductors chosen for the FCMFC.

Table 11. Voltage gain and balance testing.

Operating Point	Voltage [V]	V_{C2} [V]	V_{C1} [V]
13.33 Vin	417.2	275.2	138.1
20.00 Vin	595	401.5	200.3
40.00 Vin	612	409.7	204.1

Gate drive signals are shown for 150 kHz and 500 kHz in Figure 10, respectively. In both figures, from top to bottom, the gate signals correspond to the following: the primary FET (yellow), the first flying capacitor FET (cyan), the second flying capacitor FET (pink), and the output capacitor FET (green). The converter was loaded in both cases, and the gate drive signals are properly synchronized and phase-shifted. Synchronization is critical to stable operation and the voltage balance of the flying capacitors. This ensures that each stage is charged for an equal amount of time by the inductor and capacitor stage. In both cases, the duty cycle is 85%, which corresponds to the yellow gate drive signal for the primary FET. This sets the pace for the converter, and the secondary flying capacitor stages follow suit. Notice the secondary FETs have a fixed 60% duty cycle, which is necessary to ensure that the secondary FETs are in position when the primary FET turns OFF and supplies current to the secondary side. The secondary switches change during the ON stage of the primary FET when current is not being supplied to the secondary by the transformer. Phase shifting

and synchronization makes the three secondary gate drive signals 120° consistently. The secondary FET states determine the charging stage of the flying capacitors.

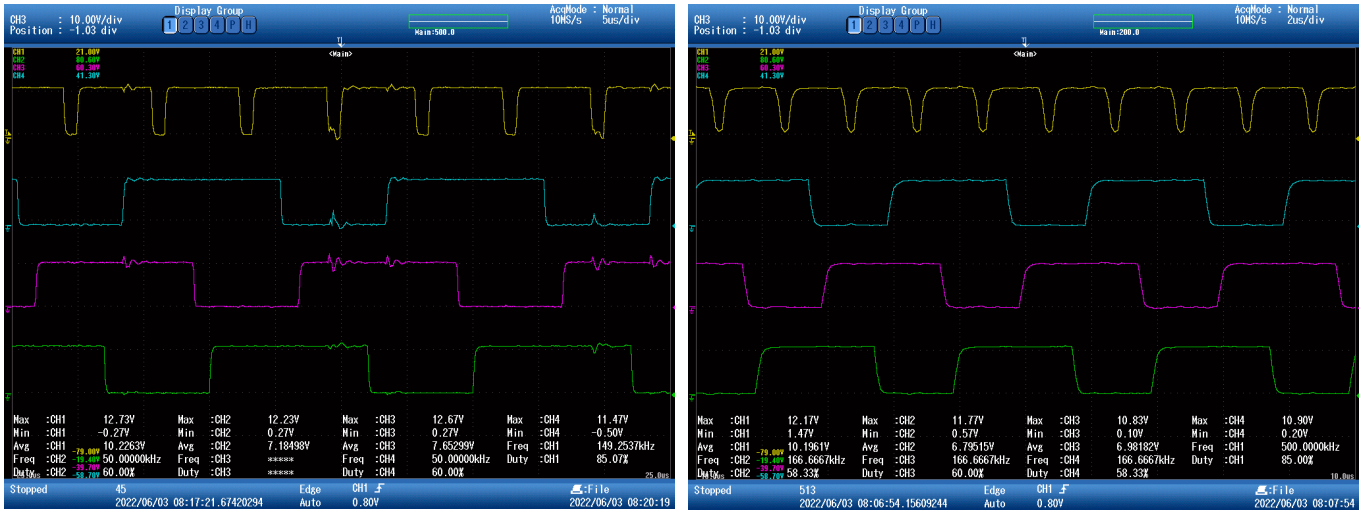

Figure 10. 150 kHz (**left**) and 500 kHz (**right**) gate driver signal PWM under load.

The primary FET snubber operation was verified and is shown in the scope capture of Figure 11. The yellow waveform on the top is the voltage across the switch node of the primary FET to the ground. The secondary PWM gate drive signals are also shown in this capture for a timing comparison. The voltage spikes occur when the primary FET turns OFF and there is a voltage rise due to the inductor energy of the transformer's leakage inductance. This energy is re-routed back into the power supply using the Zener snubber circuit and prevents a harmful voltage rise across the primary FET. The snubber circuit is operating as expected, and the primary FET is protected for rated operating parameters.

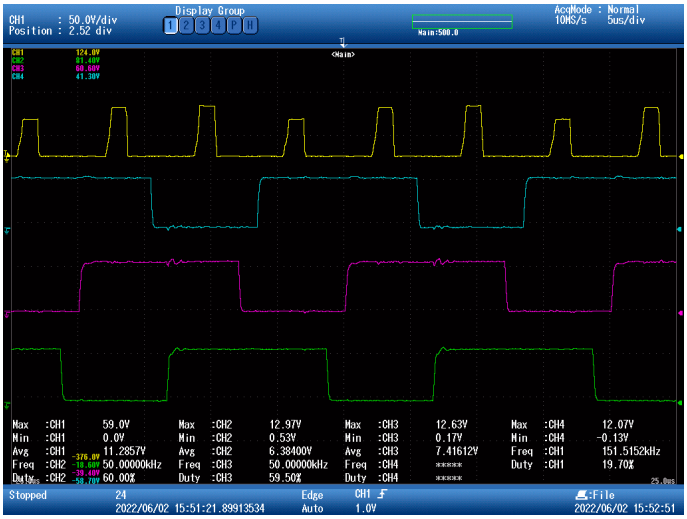

Figure 11. Snubber circuit operation.

Table 12 shows the stable testing results that were acquired. This table is not indicative of the converters peak capabilities but what was able to be recorded given DC supply instability and current limitations. Testing was performed at a 65% duty cycle with varying input and secondary gate driving voltages in an attempt to reach peak power outputs (67–200 W). Peak efficiency of 84.1% was achieved at a 10 W output with a 48.8% efficiency achieved at the highest recorded 29.21 W output.

Table 12. Testing results.

D	V_{in} [V]	I_{in} [A]	P_{in} [W]	V_{out} [V]	I_{out} [A]	P_{out} [W]	Efficiency	V_{gd} [V]
65%	20	3	60.0	250	0.08	20.00	33.3%	12
65%	15.5	0.773	12.0	180	0.056	10.08	84.1%	12
65%	20.1	0.674	13.5	241	0.045	10.85	80.1%	10
65%	30.8	0.409	12.6	150	0.061	9.15	72.6%	5.1
65%	30.8	0.4	12.32	143	0.061	8.723	70.8%	4.5
65%	41.2	0.593	24.4316	219	0.06	13.14	53.8%	4.5
65%	19.89	3.01	59.8689	230	0.127	29.21	48.8%	10

4. Conclusions

The efforts herein present the flying capacitor multilevel flyback converter to the power electronics field. Multilevel conversion as a sub-field has yet to explore the flyback converter for this topology prior to this work and related publications. A new choice is available now for a power electronics designer to consider when designing a power converter for a new application. This converter, while studied for solar voltage boosting, has capabilities for multilevel inversion electric vehicle charging amongst many others.

Flyback converters are one of the most commonly used for small consumer electronics. This work has extended the capability of the basic flyback converter by modifying it for multilevel operation. The FCMFC improves upon the voltage gain and efficiency of the flyback converter. The addition of flying capacitors allows a designer to use an existing off-the-shelf flyback transformer and extend its power and voltage range. This has the potential to save significant time in the design process. It also makes the industrial adoption of this converter more attractive.

The FCMFC as a standalone converter is relevant in the space on its own and not as a modified and improved flyback converter. It performs at levels equal to or greater than advanced prototypes in the power electronics academic space. The converter also provides electrical isolation, which makes it attractive for certain power applications that require circuit protection. This work has shown that the FCMFC exhibits natural balancing, which is key for the use of semiconductors with lower voltage ratings. The converter was able to support 600 V output operation using 200 V MOSFETs without failing due to the voltage balancing.

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