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A High-Quality and Space-Efficient Design for Memristor Emulation

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Abstract: The paper presents a new design for a compact memristor emulator that uses a single active component and a grounded capacitor. This design incorporates a current backward transconductance amplifier as the active element, enabling the emulation of both grounded and floating memristors in incremental and decremental modes. The paper provides an in-depth analysis of the circuit, covering ideal, non-ideal, and parasitic factors. The theoretical performance of the memristor emulator is confirmed through post-layout simulations with 180 nm generic process design kit (gpdk) technology, demonstrating its capability to operate at low voltages (±1 V) with minimal power consumption. Additionally, the emulator shows strong performance under variations in process, voltage, and temperature (PVT) and functions effectively at a frequency of 2 MHz. Experimental validation using commercially available integrated circuits further supports the proposed design.

Keywords: analog circuit; memristor simulator; CBTA; grounded/floating structure; memristor emulator

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1. Introduction

Since the inception of the memristor [1,2], there has been a notable surge in its integration into analog signal processing. This increase has driven a growing interest in pioneering memristor-based designs, leading to significant advances in signal processing. Particularly noteworthy is the significant headway in utilizing memristors as emulators, revolutionizing fundamental design approaches. Numerous emulator designs leveraging memristors have emerged, boasting remarkable enhancements in circuit simplicity, operational frequency, real-time performance, power efficiency, and other crucial aspects.

With the substantial growth in designs centered on memristor emulators (Mes), there is now a plethora of these Mes documented in the literature, providing designers with a great deal of versatility [3–32]. Some reported designs exclusively utilize passive components for realization [3–5]. It is noteworthy that the first notable work on passive ME is documented in [3]. Conversely, designs outlined in [6–32] rely on active building block(s). Researchers have also shown interest in further realizing higher-order memelements like meminductors and memcapacitors [33–35]. This study identifies, summarizes, and compares the most pertinent works on memristors, delineating proposed ideas based on numerous key performance attributes of significant importance.

The ME circuits outlined In various references [6–9,12,13,16–18,23,24] rely on analog multipliers for their design, resulting in increased circuit complexity and power consumption. However, the proposed ME circuit offers a solution by eliminating the need for an analog multiplier, thereby simplifying the overall circuitry. Furthermore, compared to existing Mes in [6–10,13,15–19,21–24,26–28,31,32], the proposed ME circuit has a higher operational frequency. Unlike previous ME designs documented in [6–13,15–19,21,23,24,26,27,29–32], which often incorporate two or more passive components and are not resistorless, the proposed ME circuit achieves a streamlined design by utilizing only a single capacitor and offers resistorless design. Additionally, while prior ME circuits [6–21,23,24,26,27,29,30,32] exclusively focus on either grounded or floating structures, this work introduces both

grounded and floating ME configurations. Furthermore, while the ME circuits in [8,10,19,32] typically achieve either decremental or incremental functionality, the proposed ME circuit offers the unique capability to realize both decremental and incremental characteristics within the same circuit structure, eliminating the need for additional switches.

The above classifications highlight the limitations of existing circuits. To address these issues, this study introduces an innovative memristor emulator with MOS-C realization only, aiming to achieve diverse functions. The proposed design makes use of a single current backward transconductance amplifier (CBTA) and a grounded capacitor only, leading to a simpler configuration. The grounded and floating memristors can be realized in both incremental and decremental configurations with the proposed design. The study includes a comprehensive examination of ideal and non-ideal scenarios to emphasize the real-time performance of the suggested ME. Performance validation under variations in process, voltage, and temperature is carried out through Monte Carlo analysis. Furthermore, experimental verifications have been incorporated.

2. CBTA Symbol and CMOS Realization

The active element CBTA is a versatile element featuring a combination of a dual-output second-generation current conveyor and a transconductance amplifier [36]. The use of a transconductance amplifier in any active element introduces an electronic tunability feature, allowing for precise control of circuit parameters [37–39]. A symbolic representation of the CBTA is illustrated in Figure 1a, while its CMOS implementation is depicted in Figure 1b. The terminal attributes of CBTA are defined as given below.

$$I_Z = g_m(V_P - V_N),\ I_{ZC} = g_m(V_P - V_N),\ V_W = V_Z,\ I_P = -I_W,\ I_N = I_W \tag{1}$$

where, I_Z, I_{ZC}, I_P, I_N and I_W are the currents at Z, Z_C, P, N and W terminals, respectively; V_P, V_N, V_Z and V_W are the voltages at P, N, Z and W terminals, respectively, and g_m is the transconductance of CBTA. The transconductance (g_m) of the CBTA in (1) is expressed as shown below:

$$g_m = K(V_B - V_{SS} - V_{TH}) \tag{2}$$

where $K = \frac{\mu_n C_{OX}}{\sqrt{2}}\left(\frac{W}{L}\right)_{Mi}$ (i = 23, 24, 27) and $\left(\frac{W}{L}\right)_{M23} = \left(\frac{W}{L}\right)_{M24} = \left(\frac{W}{L}\right)_{M27}$; μ_n and C_{OX} are the mobility of electron and gate oxide capacitance per unit area. In (2), V_B, V_{SS}, and V_{TH} are the bias voltage of the CBTA, the negative supply voltage, and the threshold voltage of the MOS transistor, respectively. It is observed from (2) that the transconductance (g_m) can be adjusted through the bias voltage, V_B.

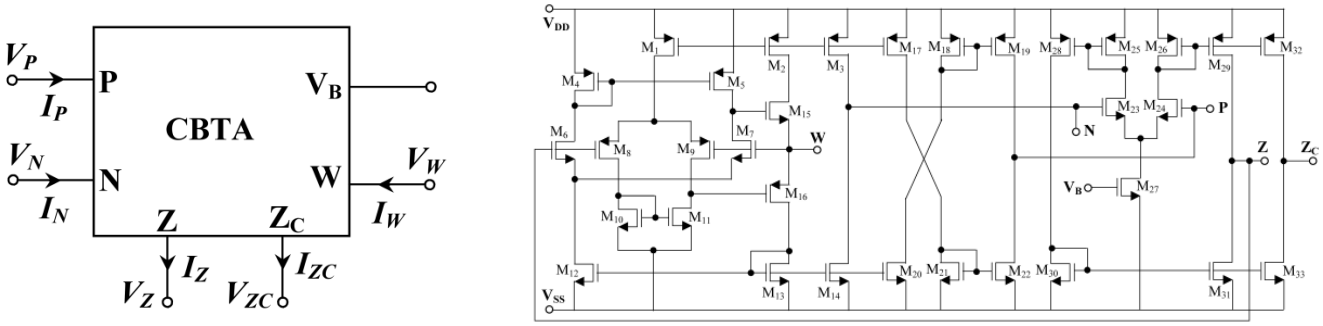


Figure 1. (**a**) CBTA symbol; (**b**) CMOS implementation of CBTA [36].

The CBTA's terminal attributes are described as follows by considering non-idealities.

$$I_Z = \gamma_1 g_m(V_P - V_N),\ I_{ZC} = \gamma_2 g_m(V_P - V_N),\ V_W = \beta V_Z,\ I_P = -\alpha_1 I_W,\ I_N = \alpha_2 I_W \tag{3}$$

where γ_1 and γ_2 are transconductance inaccuracies, β is the non-ideal voltage transfer gain and α is the non-ideal current transfer gain.

A parasitic model of the CBTA is depicted in Figure 2. In the CBTA, the terminals P, N, Z, and Z_C are high impedance terminals and terminal W is a low impedance terminal. The high-impedance terminals exhibit a parallel combination of an internal resistor and capacitor such that $Z_i = R_i//(1/sC_i)$ (where $I = P$, N, Z and Z_C). A small series resistance R_W appears at terminal W.

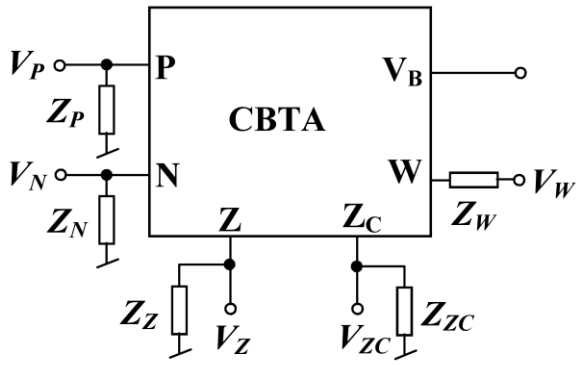


Figure 2. Parasitic model of CBTA.

3. Proposed Memristor Emulator Using CBTA

The proposed design of an memristor emulator using a single CBTA is depicted in Figure 3. The proposed design realizes a floating memristor emulator which can work both as incremental and decremental memristor emulator. The input voltage signal applied between terminals P and N, as shown in Figure 3, realizes a decremental memristor emulator. If the polarity of input signal is changed then it realizes an incremental memristor emulator. Additionally, by grounding terminal N, the proposed design works as a decremental grounded memristor emulator and by grounding terminal P, the proposed design works as incremental grounded memristor emulator.

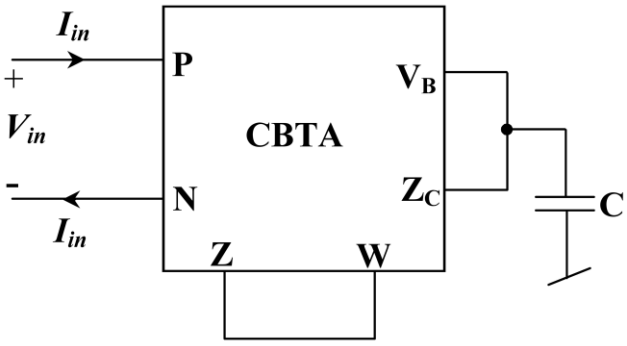


Figure 3. Proposed decremental/incremental memristor emulator.

As per the terminal relationships of the CBTA, the input voltage is transferred to the capacitor in terms of current and develops a voltage as given below.

$$V_C = V_B = \frac{g_m \phi_{in}}{C}; \text{ where } \phi_{in} = \int V_{in} dt \tag{4}$$

After putting the expression of V_B in (2), the transconductance (g_m) is expressed as given below.

$$g_m = \frac{-K(V_{SS} + V_{TH})}{1 - K\frac{\phi_{in}}{C}} \tag{5}$$

The expression for the memristance of the suggested memristor emulator circuit is given below.

$$M(\phi_{in}) = \frac{V_{in}}{I_{in}} = -\frac{1}{g_m} = \underbrace{\frac{1}{K(V_{SS}+V_{TH})}}_{fixed\ part} \mp \underbrace{\frac{\phi_{in}}{C(V_{SS}+V_{TH})}}_{variable\ part} \tag{6}$$

In (6), the fixed part is linear time invariant and variable part is a function of input flux and capacitor. If terminal P is more positive than terminal N, the proposed emulator realizes a decremental memristor. On the other hand, if terminal N is more positive than terminal P, the proposed emulator realizes an incremental memristor. Thus, the proposed emulator has the capability to operate both as decremental and incremental memristor without the need for a switch. If we assume the input signal to be a sinusoidal waveform such that $V_{in} = V_m \sin(\omega t)$, the memristance can be formulated as follows.

$$M(\phi_{in}) = \underbrace{\frac{1}{K(V_{SS}+V_{TH})}}_{fixed\ part} \mp \underbrace{\frac{V_m cos(\omega t - \pi)}{\omega C(V_{SS}+V_{TH})}}_{variable\ part} \tag{7}$$

It is observed from (7) that the variable part of a memristance depends on the operating frequency, input voltage, negative supply, and capacitor. The minimum operating frequency of the proposed emulator for which the memristance is always positive can be found by using (7) and the formula is given as follows.

$$f_{min} > \frac{KV_m}{2\pi C} \tag{8}$$

4. Non-Ideal Study of Memristor Emulator

Figure 4 illustrates the non-ideal model of the suggested memristor emulator. Both the non-idealities and parasitic of the CBTA are taken consideration in Figure 4. The voltage V_B is now given as follows.

$$V_B \cong \frac{\gamma_2 g_m \phi_{in}}{C'} \tag{9}$$

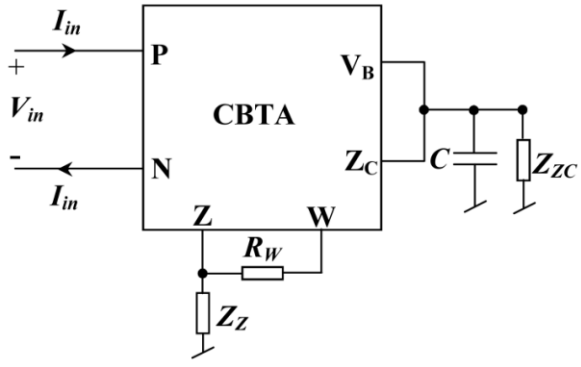


Figure 4. Non-ideal model of the proposed memristor emulator.

The transconductance (g_m) is modified as given below.

$$g_m \cong \frac{-K(V_{SS}+V_{TH})}{1-\frac{K\gamma_2\phi_{in}}{C'}} \tag{10}$$

The memristance is modified as given below.

$$M(\phi_{in}) \cong \frac{1}{\alpha_1\alpha_2\gamma_1}\left(1+\frac{R_W}{Z_Z}\right)\left[\frac{1}{K(V_{SS}+V_{TH})} \mp \frac{\gamma_2\phi_{in}}{C'(V_{SS}+V_{TH})}\right] \tag{11}$$

It is observed from (11) that the non-ideal gains and parasitic of the CBTA affect the memristance. The non-ideal gains are impactful at very high frequencies but approach unity at lower frequencies. Consequently, the impact of these non-ideal gains can be disregarded at lower frequencies. Additionally, selecting an appropriate capacitor such that $C >> C_{ZC}$ helps minimize the effects of the parasitic.

5. Simulation Results

The simulations were carried out using Cadence Virtuoso tool with 180 nm gpdk technology and ±1 V power supplies. The MOSFET's aspect ratios are given in Table 1. Figure 5 shows the CBTA's layout measuring 46 µm × 25.5 µm in area. To layout the CMOS structure of a CBTA, large transistors are segmented into multiple fingers. To ensure consistent matching among MOS transistors, all the transistors are positioned close together and aligned in the same direction, and the layout is kept as compact as possible. A grounded decremental ME is simulated first using C = 30 pF. The input voltage signal is applied to terminal P while terminal N is grounded. Figure 6 displays the transient responses of the suggested ME for an input voltage of 80 mV at frequencies of 200 kHz and 500 kHz. The observed current value is 32.5 µA. It is observed from Figure 6 that the non-linearity of the current signal is higher at 200 kHz frequency as compared to 500 kHz frequency. The pinch characteristics of the proposed ME at different frequencies (100, 200 and 500 kHz) are shown in Figure 7a. It is observed from Figure 7a that the non-linearity of the proposed ME decreases with the increase in frequency. Thus, the proposed ME functions as a linear resistor at higher frequencies. The pinch characteristics for constant product of frequency, f and capacitor, C are shown in Figure 7b. In Figure 7b, for different values of f and C providing the same product $f \times C$, the pinch characteristics remain almost similar.

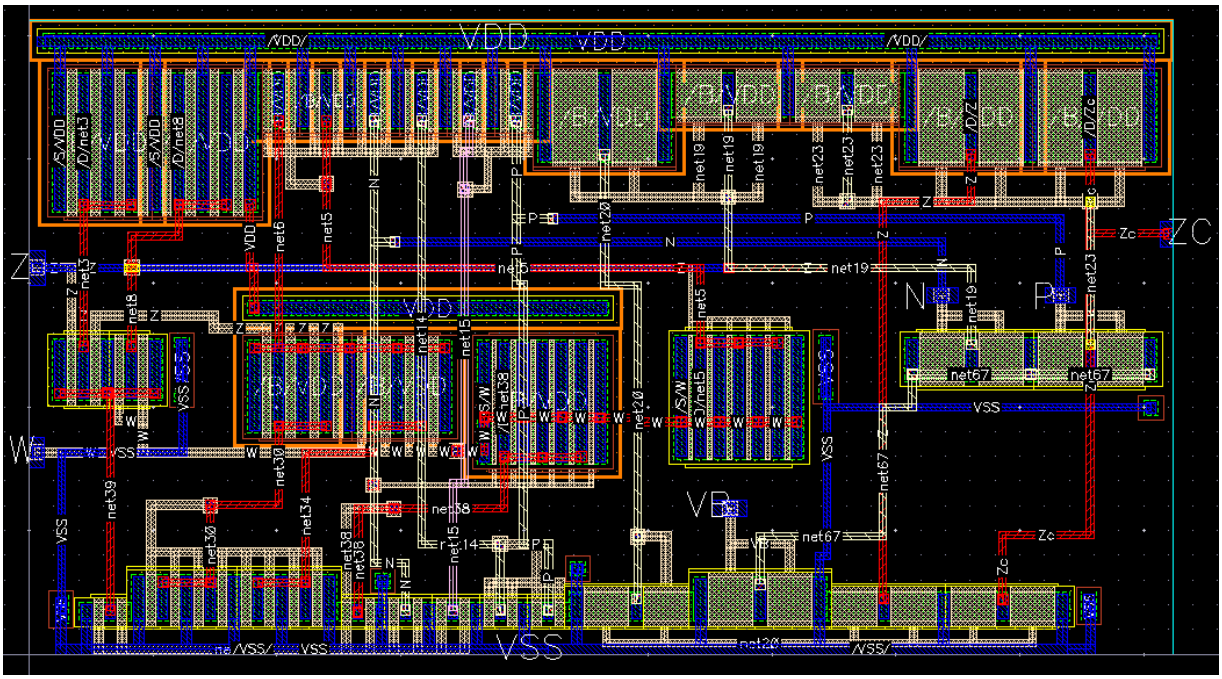


Figure 5. Layout of CBTA.

To check the stability of the proposed ME, its performance against the PVT variations is also examined. Monte Carlo sampling (MCS) results for MOS transistors' mismatch and process variations are examined through 100 multiple runs using a random sampling method. Figure 8 illustrates the MCS results for the histogram of frequency of the observed current signal for MOS transistors' mismatch and process variation when a voltage of 200 kHz frequency is applied at the input. The average value of the frequency in Figure 8a is 199.7 kHz, while in Figure 8b, it is 199 kHz. Thus, Figure 8 confirms that the proposed

ME demonstrates the robust performance against mismatch and process variation. The pinch characteristics of the proposed ME against temperature and supply voltage variations are shown in Figure 9. In Figure 9a, the pinch characteristics are shown at three different temperatures, i.e., 25, 50, and 75 °C. In Figure 9b, the pinch characteristics are shown at three different supply voltages, i.e., ±1, ±1.1, and ±1.2 V. It can be seen in Figure 9 that the pinch characteristic is not adversely affected by temperature and supply voltage variations. The proposed ME is also tested at higher frequencies by selecting a capacitor with a lower value, i.e., C = 5 pF. Figure 10 shows the pinch characteristics of the proposed ME at 1, 1.5 and 2 MHz frequencies. The proposed ME works well up to 2 MHz frequency and a decrement in the non-linearity is also observed with the increase in frequency.

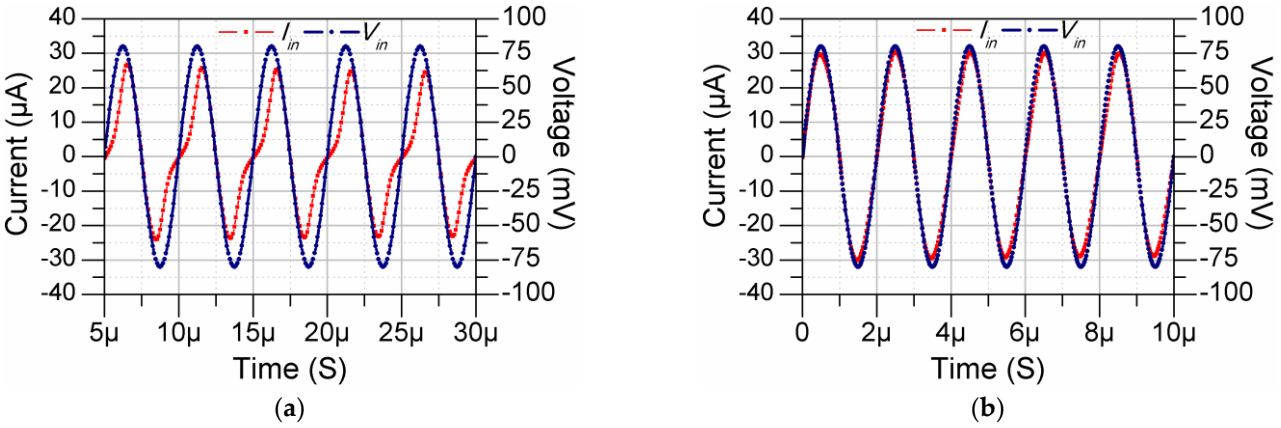


Figure 6. Transient responses for input voltage and current at (**a**) 200 kHz and (**b**) 500 kHz.

Table 1. Aspect ratios of MOS transistors.

MOSFET	W/L
M_1–M_3, M_{17}–M_{19}	4.5 μm/0.36 μm
M_4, M_5	22.5 μm/0.36 μm
M_6, M_7	5 μm/0.36 μm
M_8, M_9	15 μm/0.36 μm
M_{10}, M_{11}	7.5 μm/0.36 μm
M_{12}–M_{14}, M_{20}–M_{22}	1.5 μm/0.36 μm
M_{15}, M_{16}	30 μm/0.18 μm
M_{23}–M_{27}	3.6 μm/1.8 μm
M_{28}, M_{29}, M_{32}	7.2 μm/1.8 μm
M_{30}, M_{31},M_{33}	2.4 μm/1.8 μm

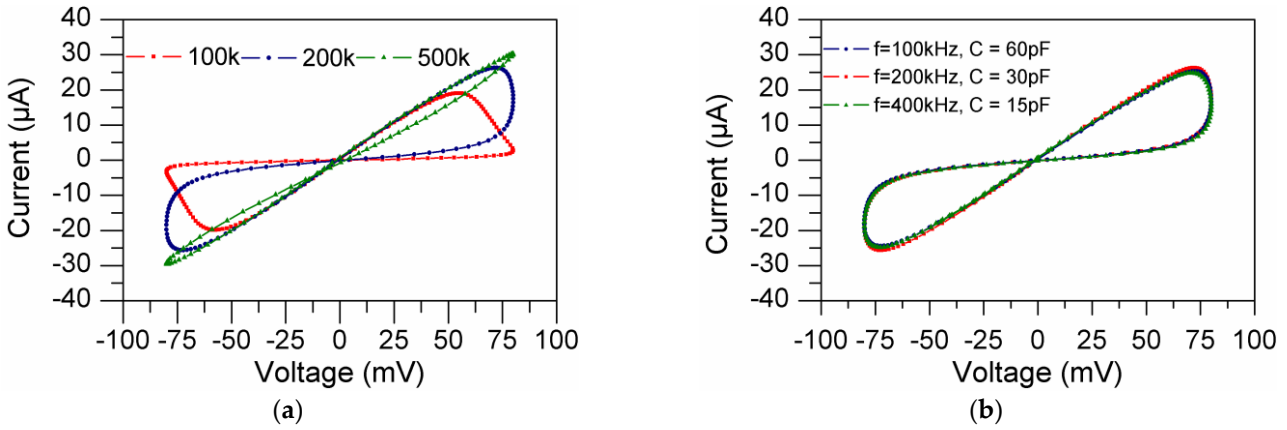


Figure 7. Pinch characteristics of the proposed decremental memristor (**a**) at different frequencies and (**b**) for a constant product of f and C.

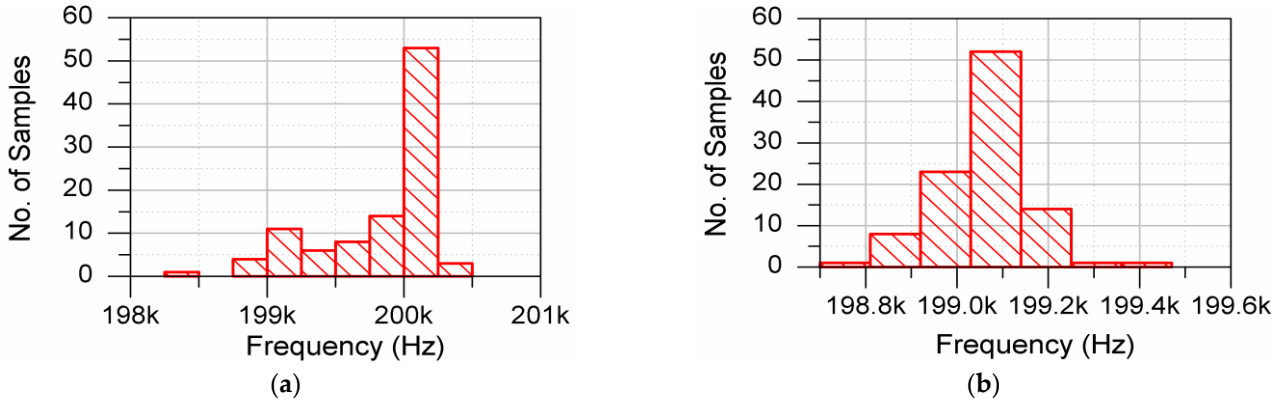


Figure 8. MCS results for frequency variations of input current signal for (**a**) MOS transistors' mismatch and (**b**) the process variation.

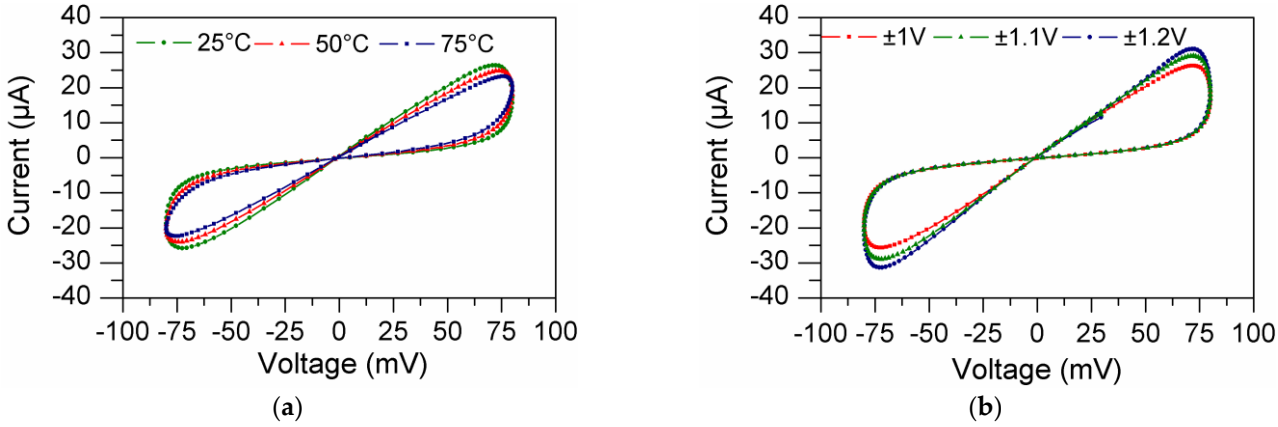


Figure 9. Pinch characteristics at different (**a**) temperatures and (**b**) supply voltages.

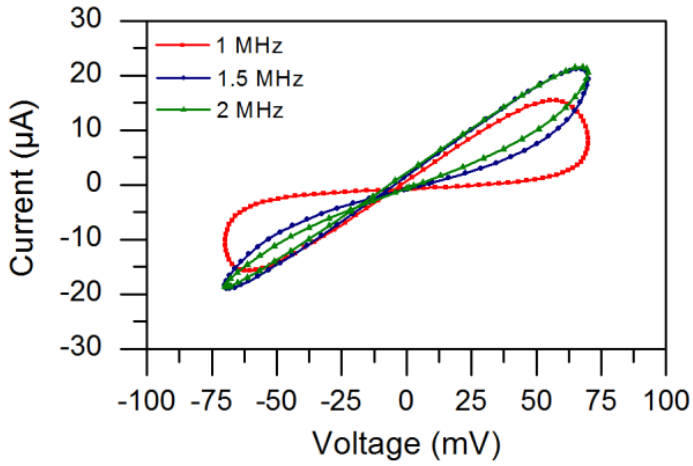
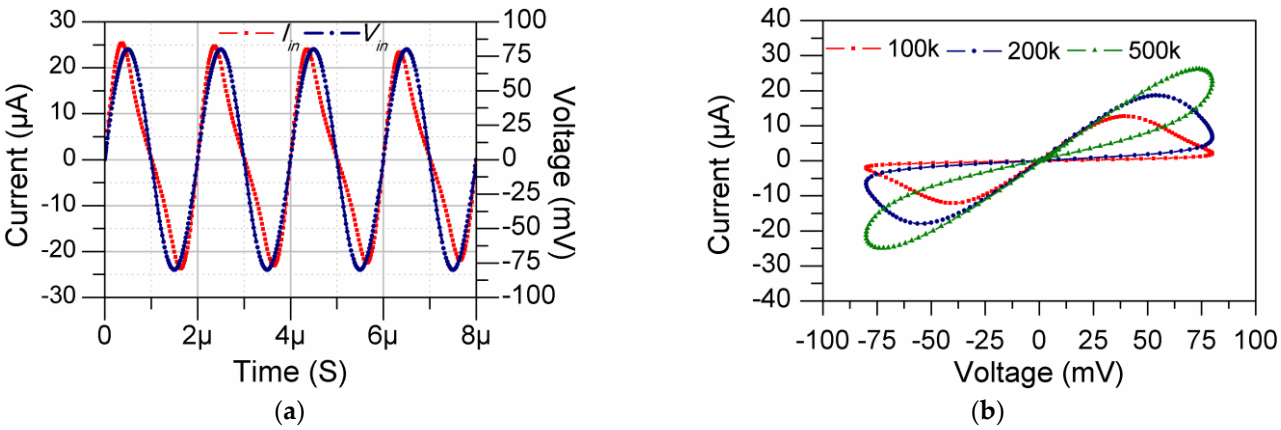


Figure 10. Pinch characteristics at different higher frequencies for *C* = 5 pF.

The time domain responses of input voltage and observed current of the suggested incremental ME for an input voltage of 80 mV at 500 kHz frequency are shown in Figure 11a. Figure 11b shows the pinch characteristics of incremental ME at different frequencies (100, 200, and 500 kHz). Figure 11b confirms that the non-linearity of the proposed incremental ME decreases with the increase in frequency. The volatile nature of the proposed incremental ME is tested by applying a voltage pulse of 80 mV with a pulse width of 200 ns and a time period of 500 ns, as depicted in Figure 12. A decrement in the amplitude of memristor

current can be seen within each pulse. Thus, memristance increases in the subsequent pulses. Memristance, however, does not alter during the pulse intervals.



(**a**) (**b**)

Figure 11. Simulation results of incremental memristor (**a**) transient responses for input voltage and current at 500 kHz. (**b**) Pinch characteristics at different frequencies.

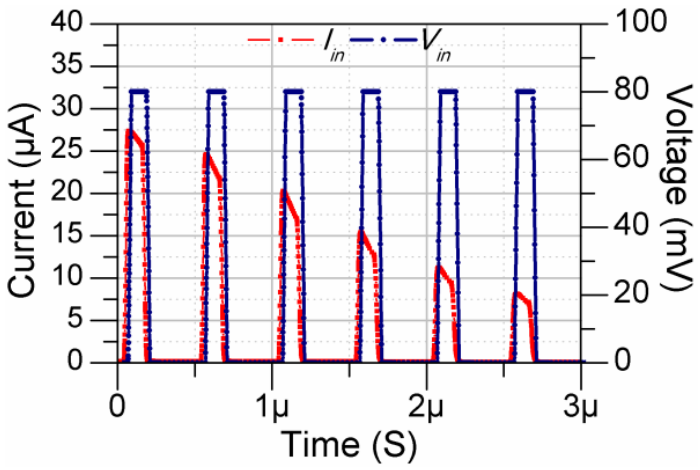


Figure 12. Transient responses for input voltage and current which confirm the volatility.

6. Experimental Verification and Comparison

The practical implementation of a CBTA which is used to realize the proposed decremental ME is shown in Figure 13. One IC for the current feedback amplifier (AD844) and two ICs for the operational transconductance amplifier (LM13700) are used to implement a prototype of CBTA. Figure 14 illustrates the experimental setup, showcasing the breadboard arrangement for mounting ICs, along with the DC power supply, function generator, and digital storage oscilloscope (DSO) used in the laboratory. The input voltage signal is generated using the RIGOL DG822 function generator and a DSO RIGOL DS1104 is used to observe the input and output waveforms. A DC power supply of ±10 V was used for the experimental results. An additional AD844 IC along with a load resistor of 1 kΩ were used to measure the memristor current, as detailed in reference [40]. A 1 V peak-to-peak amplitude sinusoidal waveform was used as an input voltage signal. The pinched characteristics of the proposed ME obtained for different frequencies (1, 10 and 50 kHz) are shown in Figure 15. The pinch characteristic is more non-linear at lower frequencies and non-linearity decreases with the increase in frequency.

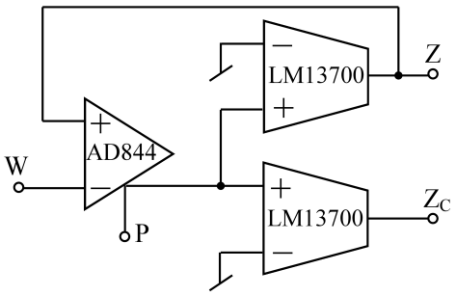


Figure 13. Experimental realization of CBTA used to realize the grounded ME.

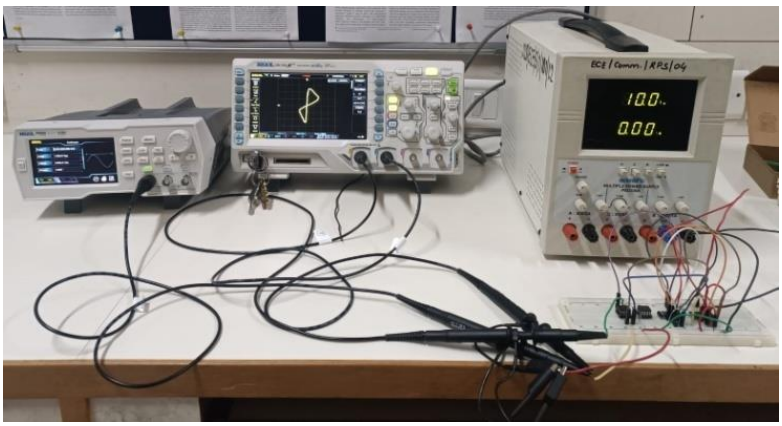


Figure 14. Experimental setup.

(**a**)

(**b**)

(**c**)

Figure 15. Pinch characteristics at different temperatures: (**a**) 1 kHz, (**b**) 10 kHz, (**c**) 50 kHz.

A comparison between the proposed memristor emulator structure and the most pertinent previous research works [6–32] is given in Table 2. The ME structures reported in [22,25,28,31] are similar to the proposed ME structure as they allow for the emulation of both grounded and floating memristors in both incremental and decremental modes. The ME structures in [22,25] use two different kind of active elements and the ME in [31] uses a higher count of passive components thus these ME structures suffer from increased circuit's complexity. The proposed ME uses the minimum number of active and passive components. Additionally, the operating frequencies of the circuits in [22,25,28,31] are less than the proposed one. Moreover, the practicality of the MEs reported in [22,25,28,31] is not examined via experimental results. It is further observed from Table 2 that the proposed emulator offers the following simultaneous features: a compact and simpler structure, the use of a minimal number of active and passive components, easy integration as it utilizes only grounded capacitor, a resistorless structure, the availability of both incremental and decremental configurations without using any additional switches, the availability of both floating and grounded type ME structures, a good operational frequency, and low operating power supplies. The proposed ME is validated using post-layout simulations and experimental results as well. These features are not simultaneously available in previous works.

Table 2. A comparison between the proposed ME and the most pertinent previous research.

Ref.	Count of Active Components	Passive Components/Count	All Grounded Passive Components	Incremental/ Decremental	Floating (F)/Grounded (G) Structure	Supply Voltages (V)	Operational Frequency	Sim/Exp Results
6	1 DDCC, 1 Multiplier	R/2, C/1	No	Both	F	±1.5	1 MHz	Sim
7	5 OPAMP, 1 Multiplier, 10 MOSFET	R/8, C/1	No	Both	F	±5	800 Hz	Both
8	4 AD844, 1 AD633, 1 OPAMP	R/8, C/1	No	Decremental	F	±15	120 Hz	Exp
9	4 AD844, 1 AD633	R/5, C/1	No	Both	F	±10	20.2 kHz	Both
10	4 CFOA, 2 D	R/4, C/4	No	Incremental	F	NA	6 kHz	Exp
11	1 CCII, 1 OTA	R/1, C/1	Yes	Both	G	±1.2	26.3 MHz	Both
12	1 VDTA, 1 Multiplier	R/2, C/1	Yes	Both	F	±0.9	2 MHz	Both
13	4 CCII, 1 Multiplier	R/3, C/1	No	Both	F	±10	40 kHz	Both
14	1 VDCC, 2 MOSFET	C/1	Yes	Both	G	±0.9	2 MHz	Both
15	3 CFOA (AD844), 1 D	R/4, C/2	No	Both	G	NA	700 Hz	Exp
16	1 AD844, 1 Multiplier (AD633)	R/1, C/1	No	Both	G	±10	860 kHz	Both
17	1 MO-OTA, 1 Multiplier	R/1, C/1	Yes	Both	G	±1.25	5 kHz	Both
18	1 CBTA,1 Multiplier	R/2, C/1	No	Both	G	±0.9	460 kHz	Sim
19	2 CFOA, 1 OTA	R/3, C/2	Yes	Decremental	G	±12	600 Hz	Exp
20	1 VDTA	MOS-C/1	Yes	Both	G	±0.9	50 MHz	Both
21	1 DVCCTA	R/3, C/1	No	Both	G	±1.25	1 MHz	Sim
22	1 CDBA, 1 OTA	C/1	Yes	Both	Both	±0.9	1 MHz	Sim
23	2 OTA, 1 Multiplier	R/1, C/1	Yes	Both	F	±1.5	180 kHz	Both
24	2 CCII, 1 Multiplier, 1 Buffer	R/3, C/1	No	Both	G	±10	100 kHz	Both
25	1 CDTA, 1 OTA	C/1	Yes	Both	Both	±0.9	2 MHz	Sim
26	2 VDTA	R/1, C/1	Yes	Both	F	±0.9	1.5 MHz	Sim
27	1 OTA, 1 DVCC	R/1, C/1	Yes	Both	G	±1.2	1 MHz	Sim
28	1 FB-VDBA	C/1	Yes	Both	Both	±0.9	1 MHz	Sim
29	1 DVCC, 1 OTA	R/1, C/1	Yes	Both	G	±0.9	30 MHz	Both
30	1 VDIBA, 1 OTA, 2 MOS	R/1, C/1	Yes	Both	F	±1	8 MHz	Both

Table 2. *Cont.*

Ref.	Count of Active Components	Passive Compo-nents/Count	All Grounded Passive Components	Incremental/ Decremental	Floating (F)/Grounded (G) Structure	Supply Voltages (V)	Operational Frequency	Sim/Exp Results
31	1 OPAMP, 1 MOSFET	R/5, C/1	No	Both	Both	±1.5	20 kHz	Both
32	1 VDCC, 1 OTA	R/2, C/1	Yes	Incremental	G	---	1 MHz	Both
This work	**1 CBTA**	**C/1**	**Yes**	**Both**	**Both**	**±1**	**2 MHz**	**Both**

Abbreviations: DDCC: differential difference current conveyor; OPAMP: operational amplifier; CCII: second-generation current conveyor; CFOA: current feedback operational amplifier; OTA: operational transconductance amplifier; VDTA: voltage differencing transconductance amplifier; VDCC: voltage differencing current conveyor; MO-OTA: multi-output operational transconductance amplifier; CBTA: current backward transconductance amplifier; DVCCTA: differential voltage current conveyor transconductance amplifier; CDBA: current differencing buffered amplifier; CDTA: current differencing transconductance amplifier; DVCC: differential voltage current conveyor; VDIBA: voltage differencing inverted buffered amplifier C: capacitor; R: resistor; D: diode; NA: not available; Sim: simulation; Exp: experimental.

7. Conclusions

In conclusion, this paper introduces a novel and compact memristor emulator structure, utilizing a single active element specifically employing a current backward transconductance amplifier and a grounded capacitor. This configuration enables the emulation of both grounded and floating memristors in both incremental and decremental configurations. The study provides a comprehensive analysis of the circuit, addressing ideal, non-ideal, and parasitic effects. The theoretical aspects are successfully validated through post-layout simulations using 180 nm gpdk technology, demonstrating the effectiveness of the proposed ME. The layout of the CBTA active block used has an area of 1.173 nm^2 only. Noteworthy features include its compact structure with low voltage (±1 V) and low power consumption, making it a promising solution. The emulator exhibits robust performance against process, voltage, and temperature (PVT) variations, and it operates efficiently up to a 2 MHz frequency. Our experimental results using commercially available ICs further confirm the practicality of the solution.

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