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System-Level Implementation of a Parallel-Path Hybrid Switched-Capacitor Amplifier with an Embedded Successive Approximation Register for IoT Applications

Javad Bagheri Asli *, Alireza Saberkari and Atila Alvandpour

Department of Electrical Engineering, Linköping University, 58 183 Linköping, Sweden; alireza.saberkari@liu.se (A.S.); atila.alvandpour@liu.se (A.A.)
* Correspondence: javad.bagheri.asli@liu.se

Abstract: A system-level implementation of a parallel-path hybrid switched-capacitor amplifier is presented in this paper. The proposed parallel-path amplifier incorporates a gain and slew rate-boosting switching path in parallel with an embedded assisted SAR path, aiming for IoT applications. As an alternative concept to the conventional analog topologies, the proposed amplifier combines nonlinear and linear paths to provide coarse and fine amplifications. In the coarse amplification, a high current is provided through a switching path for a fraction of time, which improves the slew rate and open-loop DC gain without adding significant static current. Moreover, high accuracy is achieved through the embedded assisted SAR path, which provides a resolution of $1/2^N$. In addition, each extra bit of the embedded SAR path improves the total open-loop DC gain by 6 dB. The theory of operation is performed to study how the switching and assisted SAR paths can enhance the amplifier's settling error. In addition, an existence trade-off between the coarse amplification error and the capacitive digital-to-analog converter's number of bits is investigated. The theory and system-level simulation show that the gain and slewing restrictions of the conventional topologies, especially in advanced CMOS technology, can be handled much easier by this parallel combination, where the switching path and assisted SAR path combination provides a high slewing capability and high DC open-loop gain.

Keywords: parallel-path amplifier; switched-capacitor amplifier; hybrid amplifier

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1. Introduction

Nowadays, Internet-of-Thing (IoT) applications are widely used in different areas of life such as smart home automation, energy harvesting devices, edge computing, wearable devices, etc. In IoT applications, the captured data are processed by local processors and (or) by sending them to a central system through a wired or wireless interface. In these systems, analog-to-digital converters (ADCs) as a key block, play a significant role in the analog-front-end (AFE). The ADCs are responsible for converting analog signals obtained by the sensors to digital signals that can be analyzed and processed in local and central processors [1–3]. It means that physical attributes, e.g., temperature, light, motion, heart rate, etc., are monitored by sensors of IoT devices and then ADCs, as the essential bridge, convert sensors' analog outputs into digital data to enable the analysis of this captured information.

For different IoT applications, a spectrum of requirements is engendered on ADCs in terms of power consumption, accuracy, sampling rate, size, etc., which makes a specific type of ADC, e.g., successive approximation register (SAR), pipelined SAR, pipeline, or delta-sigma modulator ($\Delta\Sigma$) ADCs, to fulfil the prerequisites of the applications. Among them, pipeline SAR, pipeline, and $\Delta\Sigma$ ADCs are commonly utilized topologies for a wide range of continuous-time analog signal processing applications. However, these types of ADCs are dependent on switched-capacitor (SC) amplifiers/integrators that have become

a design bottleneck for ADC designers due to the voltage headroom and intrinsic gain limitations in advanced CMOS technologies. This imposes significant challenges to obtain a large open-loop gain and high output swing, required to reach a high signal-to-noise-and-distortion ratio (SNDR). As a result, the need for a replacement for conventional SC amplifiers is serious. Several solutions have been proposed to overcome these challenges. A open-loop amplifier is one alternative [4], which can achieve a high bandwidth apart from the unity-gain-bandwidth (UGB) restriction of closed-loop amplifiers. However, linearity and stability issues may still exist, which make the amplifier sensitive to transient voltage variations and integrated noise. Comparator-based and zero-crossing-based amplifiers [5–8] provide efficient and fast amplification. However, overshoots, settling errors, and offset issues may become troublesome. The correlated level shifting (CLS) technique [9,10] through a two-step amplification improves the opamp gain by a factor of two. However, due to the low intrinsic gain of the opamp in the scaled CMOS process, this gain improvement may not be sufficient. A digital amplifier [11] improves the opamp gain by its embedded asynchronous SAR in a two-step amplification. However, the optimization of the number of bits in the SAR capacitive digital-to-analog converter (CDAC) is highly dependent on the linear amplifier UGB and slew rate in the first step of amplification. An adaptively biased amplifier with two nested positive and negative feedback loops has been proposed in [12] for slew rate and GBW enhancement. However, the embedded voltage followers limit the signal swing range, which can cause slew rate limitation. In addition, slew rate enhancement techniques are provided in [13] for reducing the slewing time by providing dynamic output current. However, the used auxiliary analog amplifier is always enabled, which may cause higher static current and noise performance. Ultimately, ring amplifiers [14,15] are efficient amplifiers with a simple structure. However, in scaled CMOS technology and by aggravated inverter intrinsic gain, achieving high gain may become challenging.

In this paper, a parallel-path hybrid (PPH) amplifier has been proposed, in which a charge-based slew rate and gain-boosting switching path and an embedded SAR path are working in parallel, Figure 1a. The switching path provides a high nonlinear open-loop gain and a high slewing capability, while high accuracy is achieved by the assisted SAR path. The system level of the proposed PPH amplifier is implemented in Cadence Virtuoso, using standard Verilog-A blocks and ideal logic gates. The paper is organized as follows. Section 2 discusses the theory of the proposed PPH amplifier. Details of the system-level implementation are described in Section 3. Section 4 shows the simulation results of an SC amplifier exploiting the proposed PPH amplifier. Finally, the conclusion is given in Section 5.

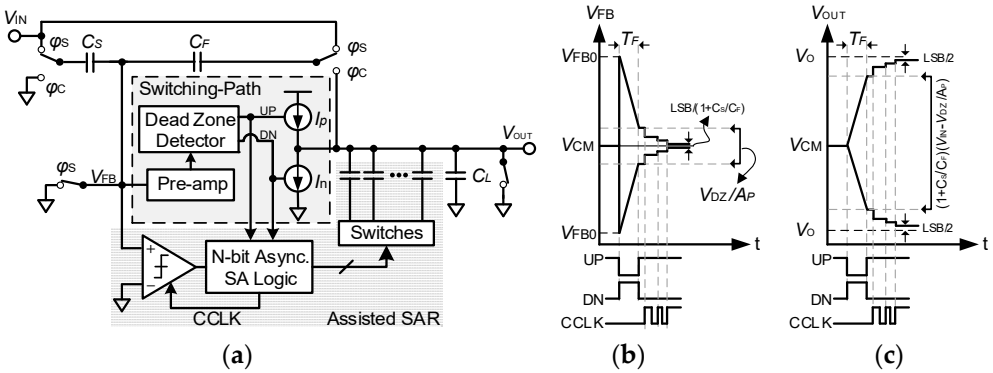

Figure 1. Proposed parallel-path amplifier (**a**) block diagram. Waveforms (**b**) V_{FB} and (**c**) V_{OUT} in the amplification phase.

2. Theory of Operation

SC amplifiers require sufficient high open-loop DC gain (A) to mitigate imperfection of the virtual ground in the feedback node and final voltage settling error in the output node, which is a challenge in the advanced CMOS technology because of the low intrinsic

DC gain and limited voltage headroom of transistors. For the amplifier shown in Figure 1a, the closed-loop voltage gain and the amplification error due to the finite open-loop DC gain of the amplifier can be expressed as Equations (1) and (2), respectively [16].

$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{C_S}{C_F}\right)\left(\frac{T}{1+T}\right) \tag{1}$$

$$V_{error} = V_{OUT} - V_{OUT_{ideal}} = \left(1 + \frac{C_S}{C_F}\right)\frac{T}{1+T} - \left(1 + \frac{C_S}{C_F}\right) = \frac{1}{1+T} \overset{T \gg 1}{\rightarrow} V_{error} \approx \frac{1}{T} \tag{2}$$

where T is $AC_F/(C_F + C_S)$ and V_{error} is the settling error (accuracy of amplification). According to Equation (2), the open-loop DC gain of the amplifier has a reverse relation with a prerequisite settling error, i.e., an $A > 66$ dB is required for a 10-bit resolution with a closed-loop gain of 2, which is challenging to achieve in advanced CMOS technologies. In the proposed PPH amplifier, the switching and assisted SAR paths boost the total open-loop DC gain of the amplifier to ($A_{\text{ff}} + A_{\text{sar}}$) in the amplification mode (Figure 1b), where A_{ff} and A_{sar} are the effective open-loop DC gain of the switching and assisted SAR paths, respectively. This relaxes the gain requirement of each path individually.

The main concept of the proposed PPH amplifier's switching path is shown in Figure 1a, i.e., working as a nonlinear coarse amplifier and aiming to reduce V_{error} to the $(1 + C_S/C_F)V_{DZ}$ at the start of the conversion mode (φ_C), where V_{DZ} is defined as the hysteresis voltage level of the dead-zone detector, and it is a portion of the feedback node voltage (V_{FB}) and common mode voltage (V_{CM}) difference. For coarse amplification, the dead-zone detector generates *UP* and *DN* control signals in a way that V_{FB} and output voltage (V_{OUT}) move from their initial values and reach V_{DZ}/A_P and $(1 + C_S/C_F)(V_{IN} - V_{DZ}/A_P)$, respectively, (Figure 1b,c), where A_P is the gain of the pre-amp, with sinking (sourcing) current I_n (I_p) from (to) output nodes to discharge (charge) C_L, thus yielding an open-loop gain of [17]:

$$A_{ff} \approx A_{CMP} I_{CS} R_{CS} \tag{3}$$

where A_{CMP} is the effective gain of the pre-amp and hysteresis detector (in V^{-1}), I_{CS} represents the current sources, and R_{CS} is the output resistance of the current sources. The error gain through the switching path at the end of coarse amplification (T_F), Figure 1c can be expressed as:

$$V_{error-ff} = V_{OUT} - V_{OUT|@T_F} = \left(1 + \frac{C_S}{C_F}\right)V_{IN} - \left(1 + \frac{C_S}{C_F}\right)\left(V_{IN} - \frac{V_{DZ}}{A_P}\right)$$

$$V_{error-ff} \approx (1 + C_S/C_F)(V_{DZ}/A_P) \tag{4}$$

By reaching V_{error} to $V_{\text{error\_ff}}$, the switching path is deactivated, and the assisted SAR path will be activated. The initial amplification part performed by the switching path has been sampled on the CDAC's capacitors, which are in parallel with C_L (Figure 1a). Accordingly, the assisted SAR path provides binary step voltages at the output node to decrease the settling error from $V_{\text{error-ff}}$ to V_{LSB}, given by Equation (5), as the fine amplification process (Figure 1b,c). The LSB voltage, V_{LSB}, of the SAR-assisted path can be halved by increasing the resolution of CDAC by 1-bit, which means the provided open-loop DC gain of the assisted SAR path is increased by 6 dB for an additional bit of CDAC. The total DC open-loop gain of the proposed PPH amplifier can be calculated as Equation (6) [18].

$$V_{error-sar} = V_{LSB} = \frac{V_{FS}}{2^N} \;\&\; V_{FS|@T_F} = V_{error-ff} \rightarrow V_{LSB} = \frac{(1 + C_S/C_F)(V_{DZ}/A_P)}{2^N} \tag{5}$$

$$A_{ff} + A_{sar} \approx 20log(A_{CMP} I_{CS} R_{CS}) + 6 \times N \tag{6}$$

where N is the CDAC resolution. Equations (5) and (6) imply that the DC open-loop gain of the PPH amplifier, and hence the closed-loop amplification accuracy, can be configured

easier by dynamic parameters of the switching path, e.g., I_{CS}, A_{CMP}, R_{CS}, and number of bits of CDAC, N, compared to intrinsic gain challenges of conventional amplifiers. Furthermore, because each path works intermittently, they do not need to be on all the time and they are active only for a portion of the amplification period, meaning that this approach does not increase the power consumption dramatically.

3. System-Level Implementation of the Proposed PPH Amplifier

3.1. Switching Path

Figure 2a shows the PPH-based SC amplifier, where the switching path consists of a pre-amplifier, a dead-zone detector, and current sources. The dead-zone detector is implemented using a pre-charged level shifter and chains of inverters. The input voltage is sampled on both C_S and C_F capacitors in the sampling mode (φ_S) and then C_F is flipped to be connected to the output node at the start of the conversion mode (φ_C). During the coarse amplification, Figure 2b, the feedback voltage, V_{FB}, is amplified by the pre-amplifier (A_P), and then V_X is level shifted by the pre-charged capacitors C_1 and C_2 to generate three-state control signals for *UP* and *DN* as Equation (7), by comparing the level-shifted V_X and common mode voltage (V_{CM}) through the inverter chains.

$$\begin{cases} state\ I & UP = 0\ \&\ DN = 1 & V_X > V_H \\ state\ II & UP = 0\ \&\ DN = 0 & V_L < V_X < V_H \\ state\ III & UP = 1\ \&\ DN = 0 & V_X < V_L \end{cases} \tag{7}$$

where $V_H - V_L = V_{DZ}$. The generated control signals are fed to the current sources (I_p and I_n) to enable sinking (sourcing) current from (to) the load. Based on Equation (7), the current sources are activated outside of the dead-zone region ($V_L < V_{DZ} < V_H$) to reduce the error and deactivated as the error falls in the dead-zone region, and then the assisted SAR path is enabled to take care of the rest of amplification.

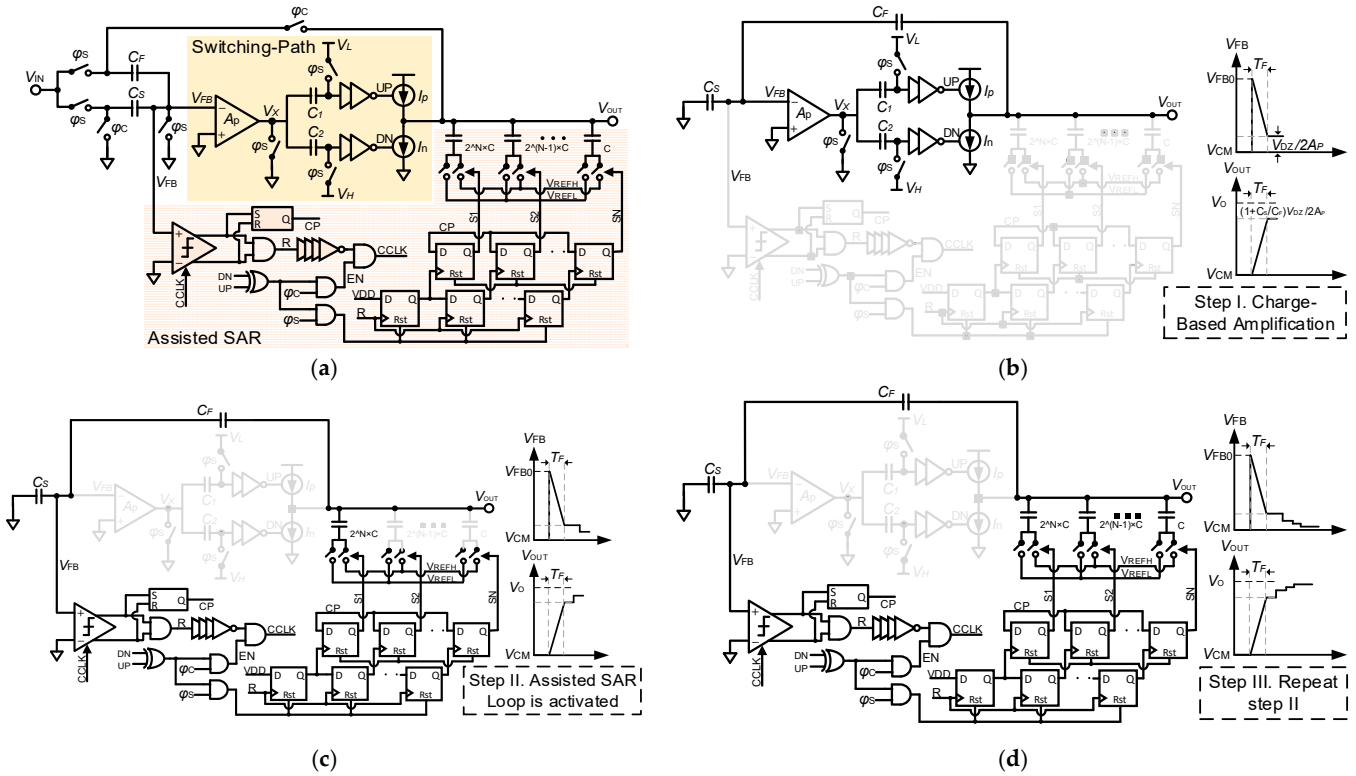

Figure 2. (**a**) Proposed PPH-based SC amplifier. (**b**) Coarse amplification with switching path. (**c**,**d**) Steps of fine amplification by SAR-assisted path.

3.2. Embedded Asynchronous Assisted SAR Path

In Figure 2, implementation of the embedded assisted SAR path is shown, which consists of a comparator, an asynchronous SAR logic (clock generation loop and SAR logic), and a CDAC. By finalizing the coarse amplification (described in Section 3.1) and reducing the V_{FB} in the dead-zone region, V_{DZ}, the switching path's current sources are deactivated (*state II* in Equation (7)) (Figure 2c) and the clock generation loop of the asynchronous SAR logic is enabled, i.e., the *EN* signal becomes high. The clock signals for the comparator (*CCLK*) and SAR logic (*R*) are generated by the clock generation loop of the asynchronous SAR logic. The *CCLK* is fed to the comparator to perform the quantization and generate the *CP* signal. Depending on the *CP* signal, in each cycle of the clock signal *R*, the statuses of CDAC switches (S_1, S_2, …, S_N) are defined by the D-flip flop (D-FF) outputs, i.e., either connected to V_{REFH} or V_{REFL}. Then, CDAC provides the binary step voltage at the output node, which reduces the settling error to V_{LSB} through the rest of the amplification period, Figure 2b,c.

Based on Equation (5), V_{DZ} and the number of CDAC capacitors define the possible V_{LSB} that is achievable at the end of the fine amplification process. It is required for the SAR logic cycles to be completed within the amplification mode, meaning that the generated asynchronous *CCLK* includes at least *N* cycles that all CDAC capacitors can be involved in the error reduction process of the embedded SAR path. The effective time allocated to perform fine amplification by the embedded assisted SAR path is derived as Equation (8).

$$N \times t_{SAR\_logic} = T_C - T_F = T_C - (C_{CDAC} + C_L)\frac{(1 + C_S/C_F)(V_{in} - V_{DZ}/A_P)}{I_{CS}} \quad (8)$$

where t_{sar_logic} is the time for a single SAR cycle, T_C is the amplification time, T_F is the switching path activation time, and V_{in} is the input signal amplitude. Additionally, the comparator needs to perform the quantization by following the *CCLK*, which has a frequency of N/T_F. It depends on how the amplification time is divided between the switching and SAR-assisted paths. By increasing the size of the current sources (higher slew rate), the time allocated to the switching path decreases, and more time will be left for the assisted SAR path, making *CCLK* more relaxed. It should be noticed that since the switching path current sources are active for a fraction of time, increasing the slew rate does not increase the power consumption dramatically.

4. Results and Discussions

In this section, simulation results for the PPH-based SC amplifier are explored. Figure 3 shows V_{FB}, *UP* and *DN*, and φ_C waveforms for different V_{IN}, V_{DZ}, and slew rates (*SRs*) of the switching path, while the assisted SAR path is deactivated (only the switching path is performing). Depending on the input voltage amplitude V_{IN}, the defined V_{DZ}, and the provided slew rate by current sources, the activating time of the switching path is different, as shown in Figure 3a–c. Figure 3a shows the performance of the switching path when V_{DZ} and the slew rate are set to 20 mV and 1 V/ms, respectively, while V_{in} amplitude changes from 100 mV to 400 mV. It shows that for higher amplitudes, the *UP*&*DN* control signals are required to keep the switching path active for a longer period to reduce the V_{FB} error from its initial value to V_{DZ}. Figure 2b shows that higher V_{DZ} will result in more settling error left for the SAR-assisted path to handle. Additionally, Figure 2c shows the effect of the slew rate on the performance of the switching path, where a higher slew rate makes the reduction in the initial V_{FB} error faster and, subsequently, makes the coarse amplification time shorter. The switching path relaxes the strict gain bandwidth and slewing restrictions of the conventional SC amplifier, and also its switching concept makes the design much easier than the conventional analog topologies.

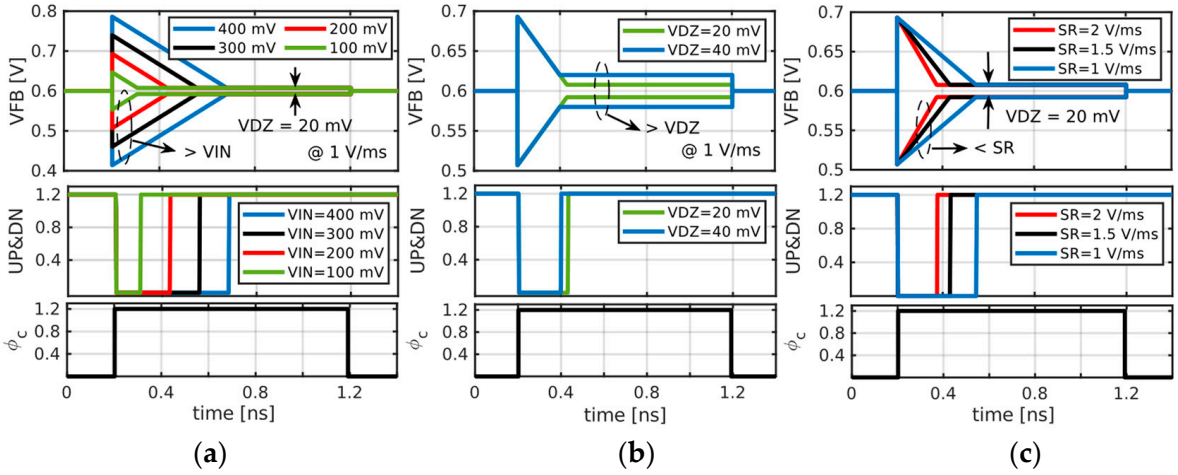

Figure 3. Waveforms of V_{FB}, *UP* and *DN* control signals, and conversion phase's clock when the switching path is operating for different: (**a**) V_{IN}, (**b**) V_{DZ}, and (**c**) slewing rates.

The performance of the assisted SAR path is explored in Figure 4, by illustrating the V_{FB} error and *CCLK* signals for different V_{DZ} and CDAC's number of bits. Figure 4a shows the V_{FB} error for different V_{DZ} with a 4-bit CDAC and a 1.5 V/ms slew rate, where V_{DZ} defines the errors left for the assisted SAR path, larger V_{DZ} results in a larger error being left in a fixed 4-bit CDAC, i.e., $V_{DZ}/2^4$. Figure 4b,c show the V_{FB} error for V_{DZ} = 20 mV and a 1.5 V/ms slew rate, and two different CDAC's number of bits, 4 and 5 bits, respectively. As is shown, adding an extra bit yields a half V_{LSB}, from 1.25 mV to 0.625 mV, while an extra SAR cycle is needed due to an additional bit. In addition, since C_{CDAC} is doubled, the coarse amplification takes around $\times 2$ more time.

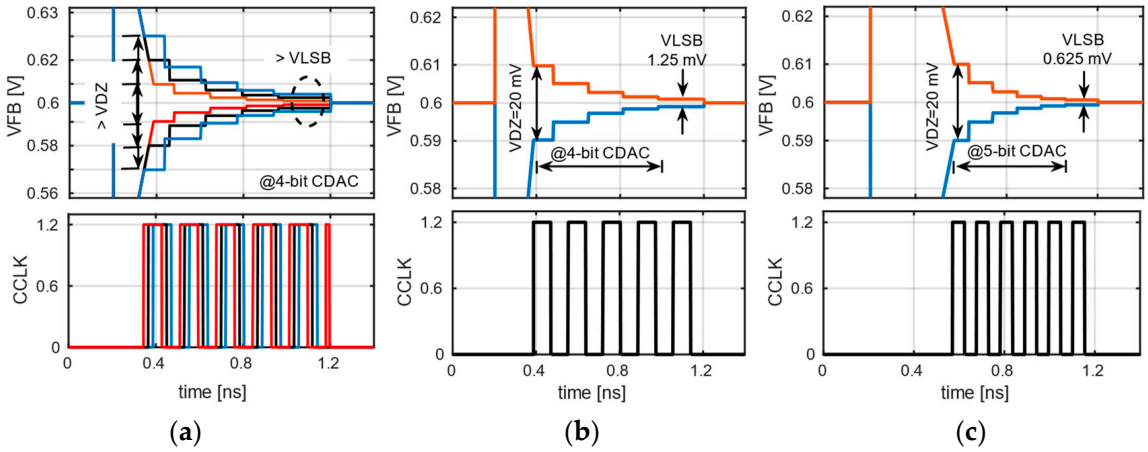

Figure 4. V_{FB} and *CCLK* signals for (**a**) different V_{DZ}, (**b**) 4-bit CDAC with V_{DZ} = 20 mV, and (**c**) 5-bit CDAC with V_{DZ} = 20 mV.

Figure 5a shows the step response of the PPH amplifier with a 2 V/ms slew rate for 4-bit and 5-bit CDACs. For the amplification time of 1 ns, in the case of a 4-bit CDAC, it takes 0.3 ns to reach the dead-zone voltage of 20 mV, while it takes almost double that in a 5-bit CDAC, around 0.6 ns. Then, the assisted SAR starts to perform with 4 and 5 step voltages and reduces the error to around 1 mV and 0.5 mV, respectively. The V_{FB} error versus the input voltage for 4-bit and 5-bit CDACs is shown in Figure 5b, where the error is kept to less than 1.25 mV and 0.625 mV for a range of input voltages between 300 mV and 900 mV.

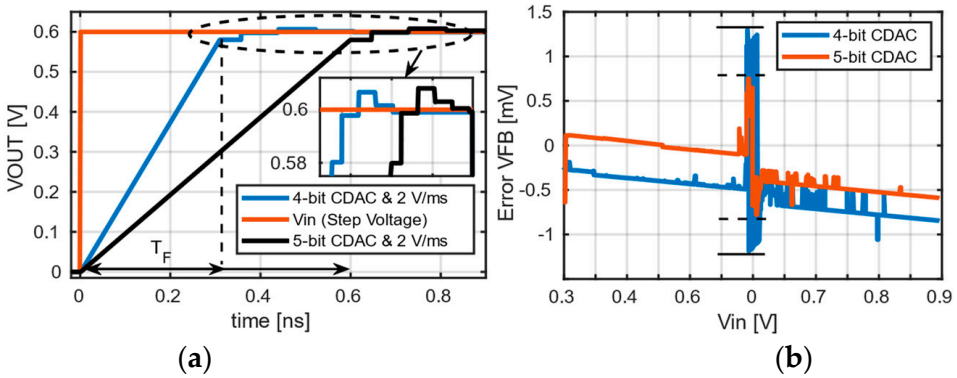

Figure 5. (**a**) Step response and (**b**) V_{FB} error versus input voltage, for 4-bit and 5-bit CDACs, and with 2 V/ms slew rate.

5. Conclusions

A switched-capacitor parallel-path hybrid amplifier is presented in this work, which consists of a gain and slew rate-boosting switching path in parallel with an embedded assisted SAR path. The proposed amplifier boosts the slew rate significantly through the provided large dynamic current sources of its switching path, which is activated for a fraction of amplification time for coarse amplification. Moreover, fine amplification to reach high accuracy is aimed to be performed through an embedded assisted SAR path, handling a small error which is left after coarse amplification to reach an accuracy of $1/2^N$. In addition, the switching path provides a high nonlinear open-loop gain that improves the total open-loop DC gain. Furthermore, an additional bit of the CDAC in the embedded SAR path increases the open-loop gain by 6 dB and halves the settling error. The potential limitation could be the trade-off between the voltage sensitivity of the switching path and the CDAC's number of bits. A smaller V_{DZ} in the switching path means there is a lower gain error left for the SAR-assisted path to handle, which means a lower number of bits for CDAC is required. Then, the SAR-assisted path implementation will be more relaxed in terms of operation frequency. The theory and simulation show that the conventional gain and slewing restrictions of the traditional topologies, especially in advanced CMOS technologies, can be handled much easier by this proposed combination.

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Abbreviations

SC: switched capacitor, ADC: analog-to-digital-converter, CDAC: capacitive digital-to-analog-converter, PPH: parallel-path amplifier, Opamp: operational amplifier, D-FF: D-flip flop, SAR: successive approximation register, UGB: unity-gain-bandwidth, AFE: analog-front-end.

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