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A Low-Power, High-Resolution Analog Front-End Circuit for Carbon-Based SWIR Photodetector

Yuyan Zhang [1], Zhifeng Chen [2], Wenli Liao [2], Weirong Xi [2], Chengying Chen [2,*] and Jianhua Jiang [1,*]

[1] School of Electronics, Peking University, Beijing 100871, China; yuyanzhang@stu.pku.edu.cn
[2] School of Opto-Electronic and Communication Engineering, Xiamen University of Technology, Xiamen 361024, China
* Correspondence: chenchengying@xmut.edu.cn (C.C.); jhjiang@pku.edu.cn (J.J.)

Abstract: Carbon nanotube field-effect transistors (CNT-FETs) have shown great promise in infrared image detection due to their high mobility, low cost, and compatibility with silicon-based technologies. This paper presents the design and simulation of a column-level analog front-end (AFE) circuit tailored for carbon-based short-wave infrared (SWIR) photodetectors. The AFE integrates a Capacitor Trans-impedance Amplifier (CTIA) for current-to-voltage conversion, coupled with Correlated Double Sampling (CDS) for noise reduction and operational amplifier offset suppression. A 10-bit/125 kHz Successive Approximation analog-to-digital converter (SAR ADC) completes the signal processing chain, achieving rail-to-rail input/output with minimized component count. Fabricated using 0.18 µm CMOS technology, the AFE demonstrates a high signal-to-noise ratio (SNR) of 59.27 dB and an Effective Number of Bits (ENOB) of 9.35, with a detectable current range from 500 pA to 100.5 nA and a total power consumption of 7.5 mW. These results confirm the suitability of the proposed AFE for high-precision, low-power SWIR detection systems, with potential applications in medical imaging, night vision, and autonomous driving systems.

Keywords: carbon nanotube field effect transistors; photodetector; successive approximation register analog-to-digital converter; capacitor trans-impedance amplifier; correlated double sampling

Citation: Zhang, Y.; Chen, Z.; Liao, W.; Xi, W.; Chen, C.; Jiang, J. A Low-Power, High-Resolution Analog Front-End Circuit for Carbon-Based SWIR Photodetector. *Electronics* **2024**, *13*, 3708. https://doi.org/10.3390/electronics13183708

Academic Editor: Sergio Busquets-Monge

Received: 6 September 2024
Revised: 11 September 2024
Accepted: 16 September 2024
Published: 18 September 2024

1. Introduction

The increasing demand for high-performance infrared imaging technologies, particularly in applications such as medical diagnostics, night vision systems, and autonomous vehicle navigation [1–5], has driven significant advancements in short-wave infrared (SWIR) photodetectors. These uncooled SWIR detectors are favored for their low power consumption, compact form factor, and ability to operate without cooling mechanisms, making them suitable for portable and embedded systems. However, traditional silicon-based photodetectors often struggle with low optical absorption efficiency and limited integration capabilities with mainstream electronics, which hampers their sensitivity and overall performance in SWIR applications. In the burgeoning field of optoelectronics, an extensive array of materials have been explored for their light interaction and detection capabilities. Notably, the studies presented in [6,7] delve into the intricate details of Type-II superlattices and the innovative 1D p-Te/2D n-Bi_2Te_3 heterojunction, respectively, showcasing advancements in material for improving the efficiency and sensitivity of photodetectors. However, among the many channel materials, carbon nanotube field-effect transistors (CNT-FETs) exhibit high carrier mobility, excellent electrical conductivity, and compatibility with existing silicon technology, enabling the development of high-performance, low-cost SWIR photodetectors [8]. Moreover, the unique properties of carbon nanotubes, such as their ultra-thin structure and ability to operate at low voltages, provide a pathway to achieve higher sensitivity and detectivity in photodetector arrays [9–11].

Recent studies have shown that CNT-FETs can achieve low dark current and high detectivity (5.6×10^{13} Jones under 1300 nm), making them suitable for high-performance

SWIR photodetectors. However, most existing AFE circuits fail to meet the current detection requirements of carbon-based SWIR photodetectors. Prior research has primarily focused on readout circuits. For instance, there has been research on the CNT infrared detector with a CTIA as an input-level circuit, which used a low-pass filter to eliminate high-frequency noise, disregarding the impact of low-frequency noise on the system's SNR [12]. Further, some AFEs are optimized for small current ranges, limiting their applicability in broader detection scenarios. Sun et al. [13] proposed a readout system based on carbon nanotube infrared detectors using a CTIA as the input level, which can detect currents as low as 0.11 pA. In 2022, Li et al. proposed a BDI injection-level input circuit with a maximum measurement range of only 100 pA, far below the upper current limit of the existing detector [14]. Designing AFEs necessitates a large-bandwidth analog circuit module [15]. Some reasonable compromises among the various parameters become the main difficulty found in the design of an AFE circuit.

This paper addresses these challenges by proposing an AFE circuit designed specifically for CNT-FET photodetectors. The AFE integrates a CTIA for low-noise current-to-voltage conversion, a CDS circuit for noise reduction and offset suppression, and a 10-bit/125 kHz SAR ADC for efficient signal digitization. The proposed design is implemented in 0.18 μm CMOS technology, and its performance is validated through post-simulation results, demonstrating significant improvements in the SNR, linearity, and power efficiency over existing designs. The contributions of this work include a wider detection range, enhanced signal integrity, and lower power consumption, making it a viable solution for advanced SWIR imaging systems.

2. Analog Front End Circuit Design

2.1. CNT-FET Structure and Integration

Figure 1a illustrates the detailed structure of the CNT-FET photodetector, highlighting its integration with the AFE circuit. The proposed AFE circuit integrates a CNT-FET photodetector as the primary sensing element due to its high sensitivity and compatibility with silicon-based processes. The CNT-FET photodetector is capable of converting optical signals into current signals. Figure 1b presents the CNT-FET photodetector. The photodetector array utilizes CNT-FETs due to their ability to achieve a low dark current and high detectivity across a wide wavelength range. The response performance of the CNT-FET photodetector, including dark current detectivity and detection range, is critical for its application in SWIR imaging. This CNT-FET photodetector was provided by Zhou [8]. The dark current of the CNT-FET was measured to be approximately 1.25×10^{-13} $Hz^{-1/2}$ at a frequency of 1 Hz and the detection range of this photodetector spans from 900 nm to 1700 nm. This range is determined by the absorption characteristics of the PbS CQDs. The CNT-FETs are fabricated with a PIN structure using lead sulfide (PbS) quantum dots and zinc oxide (ZnO), which serve as the gate material for the transistor. The PbS quantum dots efficiently absorb infrared light and generate electron–hole pairs, creating a photovoltage at the heterojunction. This photo-induced voltage modulates the gate of the CNT-FET, which is then amplified and converted into a photocurrent. However, the initial current signal is inherently weak and susceptible to various noises and interferences, rendering it unsuitable for direct digital processing. In this context, the AFE is crucial. Its primary function is to receive the analog signals from the sensor array, convert them into a digital-friendly format, and perform essential signal conditioning and enhancement. As shown in Figure 1c, the AFE designed in this paper comprises several critical components: a ROIC, CDS, and an ADC. The input stage of the ROIC employs a CTIA integrator, which ensures low input impedance and minimal noise. The CDS circuit incorporates an offset suppression structure, effectively eliminating signal noise and suppressing the offset voltage of the OPA. For the ADC, the design utilizes a 10 bit/125 KHz SAR ADC, which meets the requirements for high precision and low power consumption.

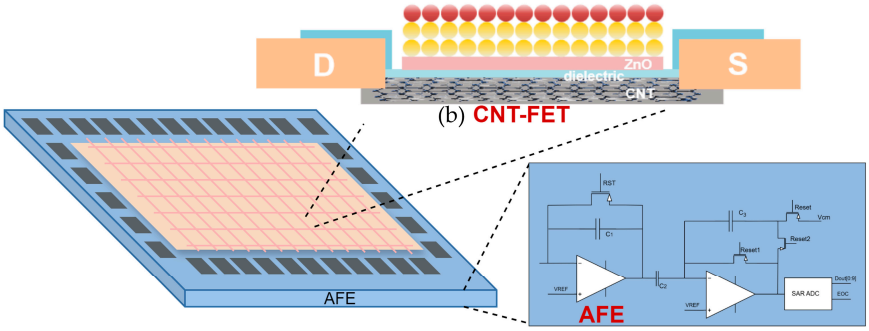


Figure 1. Structure of the CNT-FET photodetector and AFE system. (**a**) structure of CNT-FET photodetector and AFE (**b**) structure of the CNT-FET and (**c**) diagram of AFE.

2.2. AFE Components and Their Roles

The AFE's primary function is to interface with the CNT-FET-based photodetector array, converting the weak analog signals into digital data while minimizing noise and ensuring high precision. The CTIA, CDS, and SAR ADC components each play a critical role in this process:

- CTIA: The CTIA stage converts the photocurrent from the CNT-FETs into a voltage signal with minimal noise.
- CDS: The CDS circuit further reduces noise by eliminating fixed-pattern noise (FPN) and suppressing the offset voltage, critical for maintaining signal integrity.
- SAR ADC: Finally, the SAR ADC digitizes the analog signals with high resolution, ensuring that the output data accurately represent the original photodetector signal.

2.2.1. Capacitor Trans-Impedance Amplifier (CTIA) Design

The Capacitor Trans-impedance Amplifier (CTIA) input stage offers significant advantages, including low input impedance and minimal read noise. The CTIA is the first stage in the AFE and plays a crucial role in converting the photocurrent from the SWIR photodetector into a voltage signal suitable for further processing. The basic CTIA circuit is illustrated in Figure 2. The CTIA design employs a feedback loop with a capacitor (C_f) and an operational amplifier (OPA) configured to operate in two distinct phases. During the first phase (reset phase), the feedback capacitor is discharged, and the OPA operates in a voltage follower configuration, ensuring that the initial voltage across the capacitor is zero. In the second phase (integration phase), the reset switch is turned off, allowing the input photocurrent (I_{in}) to charge the feedback capacitor. The resulting voltage across the capacitor (V_{out}) is directly proportional to the integrated input current over time, as governed by the following equation:

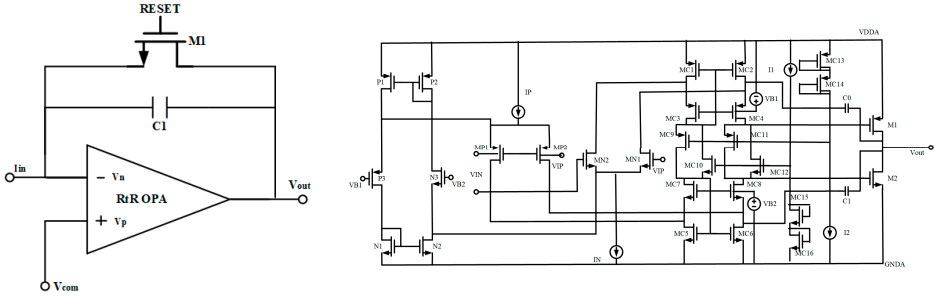
$$V_{\mathrm{int}(t)} = V_{\mathrm{int}(t_0)} + \frac{1}{C_f}\int_{t_0}^{t} Iin(t)dt \quad (1)$$

where $V_{int(t)}$ is the initial voltage, Iin is the photocurrent or dark current, and C_f is the feedback capacitance.

One of the primary challenges in designing the CTIA is minimizing the noise introduced by the OPA and other circuit components. The noise performance of the CTIA is critically dependent on the open-loop gain of the OPA, as higher gains help reduce the voltage deviation at the output terminal, thereby improving the accuracy of the integration process. The CTIA also employs a negative feedback mechanism to stabilize the output voltage and minimize deviations caused by the inherent offset voltages of the OPA. This is particularly important in maintaining linearity and accuracy in the presence of varying input currents. The voltage deviation at the output terminal of the OPA can be expressed as follows:

$$\Delta V_{\text{out}} = -A \times \Delta V_{in} = -A \times \frac{\int Iin(t)dt}{C_1(1+A)} = \frac{\int Iin(t)dt}{C_1}(1 - \frac{1}{A}) \tag{2}$$

where t is the integration time.



(**a**) (**b**)

Figure 2. (**a**) Diagram of CTIA and (**b**) schematic of RtR OPA.

2.2.2. Correlated Double Sampling (CDS) Circuit Design

Following the CTIA stage, the output signal is processed by the CDS circuit. CDS is integral to reducing the fixed-pattern noise (FPN) [16] and suppressing the offset voltage introduced by the OPA, which are common issues in large-scale detector arrays. CDS operates by sampling the output signal at two closely spaced time intervals, effectively canceling out any noise that is temporally correlated.

The CDS circuit is designed with a high-gain OPA to enhance noise suppression capabilities, as shown in Figure 3. The circuit operates by first sampling the signal when the OPA is in its reset state (initial sampling), and then sampling again after the CTIA has integrated the photocurrent (final sampling). The difference between these two sampled values represents the desired signal with most of the noise components canceled out. The ideal output value VOUT can be calculated as follows:

$$\begin{aligned} Q_1 = Q_2 &= (V_{\text{com}} - V_{\text{os}} - V_{\text{int}})C_1 + (V_{com} - V_{\text{os}} - V_{com})C_2 \\ &= (V_{com} - V_{\text{os}} - V_{RST})C_1 + (V_{com} - V_{\text{os}} - V_{OUT})C_2 \end{aligned} \tag{3}$$

$$V_{OUT} = V_{\text{com}} + \frac{C_1}{C_2}(V_{\text{int}} - V_{RST}) \tag{4}$$

where V_{com} is the common-mode voltage of the OPA, V_{int} is the final integrated voltage output, V_{RST} is the reset voltage, and V_{os} is the offset voltage. The Q_1 and Q_2 are the sampling charge quantity.

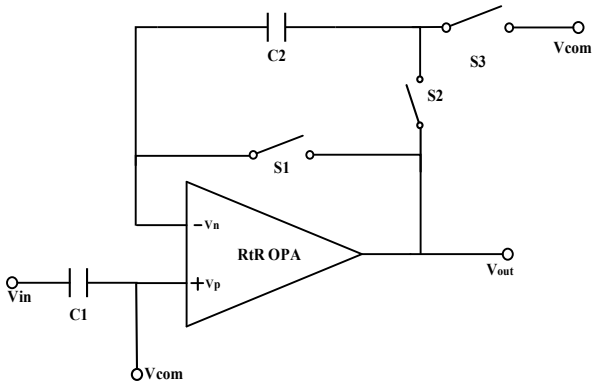


Figure 3. CDS circuit structure.

However, the effectiveness of the CDS in noise reduction depends on the gain of the OPA and the timing accuracy of the sampling process. High-gain OPAs are used to ensure

that the offset voltage is minimized, while precise timing control is necessary to ensure that the noise components are effectively canceled. The final output value V_{OUT} can be calculated as follows:

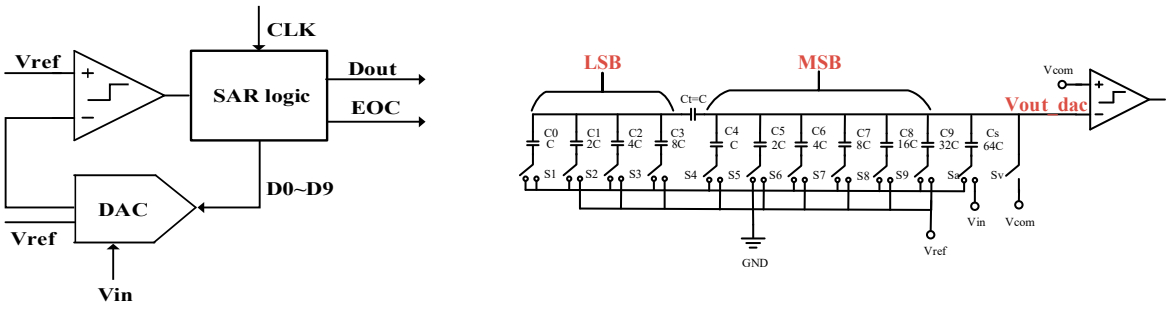
$$V_{OUT} = \frac{1}{\frac{A+1}{A} + \frac{1}{A}\frac{C_1}{C_2}}[(\frac{1}{A+1}\frac{C_1}{C_2} + 1 + \frac{1}{A+1})V_{\text{ref}} + (\frac{1}{A+1}\frac{C_1}{C_2} + \frac{1}{A+1})V_{OS} + \frac{C_1}{C_2}(V_{sig} - V_{RST})] \quad (5)$$

where A represents the open-loop gain of the OPA. Additionally, the CDS circuit also functions as an S & H circuit, which stabilizes the final output voltage before it is passed to the ADC for digitization. This dual functionality reduces the need for additional circuitry, contributing to the overall compactness and efficiency of the AFE design.

2.2.3. Successive Approximation Register (SAR) ADC Design

The final stage of the AFE is the SAR ADC, which digitizes the analog signal from the CDS circuit [17–19]. The SAR ADC is chosen for its ability to provide high-resolution conversion with moderate speed and low power consumption, making it ideal for targeted SWIR photodetector applications [20,21].

The SAR ADC in the proposed AFE circuit employs a charge redistribution DAC and a comparator to perform the analog-to-digital conversion. Figure 4a demonstrates the SAR logic that controls the operation, using a binary search algorithm to approximate the input voltage and convert it into a corresponding digital code. The conversion process begins with the input voltage being sampled and held by the S & H circuit, ensuring a stable input during the conversion. During the conversion phase, the SAR logic executes a binary search algorithm to determine the digital code corresponding to V_{in}. The DAC output is then compared with the sampled input voltage. If V_{in} is greater than ½ V_{ref}, the comparator outputs '1'; otherwise, it outputs '0'. At the same time, the SAR logic accordingly adjusts the subsequent bits. This process is iterated for each bit, from the most significant bit (MSB) to the least significant bit (LSB), until the final digital code is determined.



(**a**) (**b**)

Figure 4. (**a**) Block diagram of single-end SAR ADC operation and (**b**) structure of the modified piecewise DAC.

To optimize the SAR ADC for low power consumption and high resolution, several design strategies were employed. First, the DAC architecture uses a segmented approach with a single-capacitor sampling structure, which significantly reduces the number of capacitors and the overall chip area. This design choice not only minimizes power consumption but also enhances the conversion speed by reducing the settling time of the DAC [22].

The proposed DAC architecture is depicted in Figure 4b. In this DAC design, the segmented capacitor C_t serves as a unit capacitor, and the sampling capacitor C_s is 64 C, resulting in a total equivalent capacitance of 128 C. The operation is divided into three steps: sampling, holding, and charge redistribution. During the sampling phase, switches Sx (x = 0–9) are connected to GND, and the SAR logic provides control signals b0 to b9. Switches Sa and Sv are on, connecting the bottom plate of C_s to V_{in} and the top plate is

determined by V_{com}. In the holding phase, Sa and Sv are off, maintaining the charge on C_s. The DAC output voltage (V_{out}_dac) is given by

$$V_{\text{out\_}dac} = \frac{Q}{C} = \frac{64C(V_{com} - V_{in}) + V_{com}(15C//1C + 63C)}{15C//1C + 127C} = \frac{-1024}{2047}V_{in} + V_{com} \quad (6)$$

During the charge redistribution phase, the SAR logic sets b9 = 1, connecting the bottom plate of the highest-order capacitor C9 to the reference voltage V_{ref}. If V_{in} is greater than 1/2 V_{ref}, the comparator output is '1', and b9 remains '1'; otherwise, it outputs '0'. This process is repeated until all bits are determined. This results in the final DAC output voltage:

$$V_{OUT\_}dac = \frac{-1024}{2047}(-V_{in} + V_{\text{ref}} \times \sum_{i=0}^{9} \frac{bi}{2^{10-i}}) + V_{com} \quad (7)$$

The comparator within the SAR ADC is another critical component that affects both power consumption and resolution. A three-stage preamplifier and latch structure with cascaded offset calibration using Input Offset Storage (IOS) and Output Offset Storage (OOS) techniques are employed [20], as shown in Figure 5. To improve calibration accuracy, OOS technology is used in the first-stage preamplifier, while IOS is employed in the latter stages to prevent calibration errors caused by coupling capacitor saturation. During the offset calibration phase, switch S1 is off, and S2 is on, connecting the positive and negative inputs of the first preamplifier to the common-mode voltage (V_{com}). At the same time, switches Sx (x = 3–6) are off, storing the output offset voltage of the first preamplifier in C1 and C2. The second and third preamplifier offset voltages are stored in C_x (x = 1–4). In the comparison phase, S1 is on, and Sx (x = 2–6) are off. The comparator then compares V_{com} with V_{in}, canceling most offset during the process.

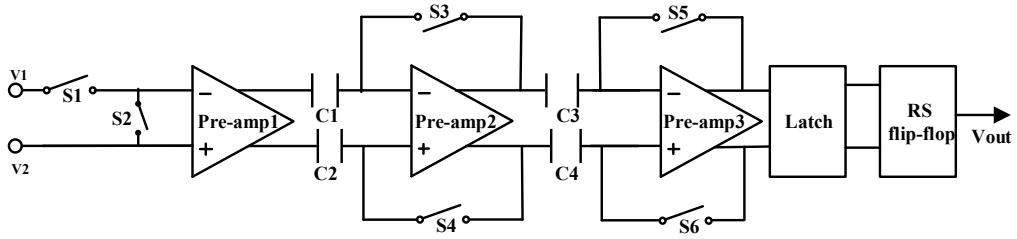


Figure 5. Schematic diagram of the comparator.

The SAR logic and timing control are essential to ensure that the ADC operates efficiently and accurately. The structure and timing diagram for the SAR ADC, as shown in Figure 6, illustrates the sequence of operations for sampling, holding, and binary searching. The timing control ensures that each bit of the digital code is determined in a well-defined sequence, with minimal latency between steps.

During a conversion cycle, EN remains high for four clock cycles. In the first and second clock cycles, the DAC samples the analog input signal, while in the third and fourth clock cycles, the DAC holds the signal. When EN is high, registers F0 to F9 are cleared, and D0 to D9 outputs are set to 0. Conversion starts when EN goes low, and on the rising edge of CLK, the most significant bit D9 is set to 1. When the second rising edge of CLK arrives, the D8 is set to 1. If VCOMP is 1 then K9 is 1, and D9 remains as 1; otherwise, D9 is 0. After 11 low-EN clock cycles, DAC redistribution ends, D0–D9 are set, and EOC goes high. In the 12th low-EN cycle, the tri-state gate opens, outputting a 10-bit code B0–B9, completing a cycle.

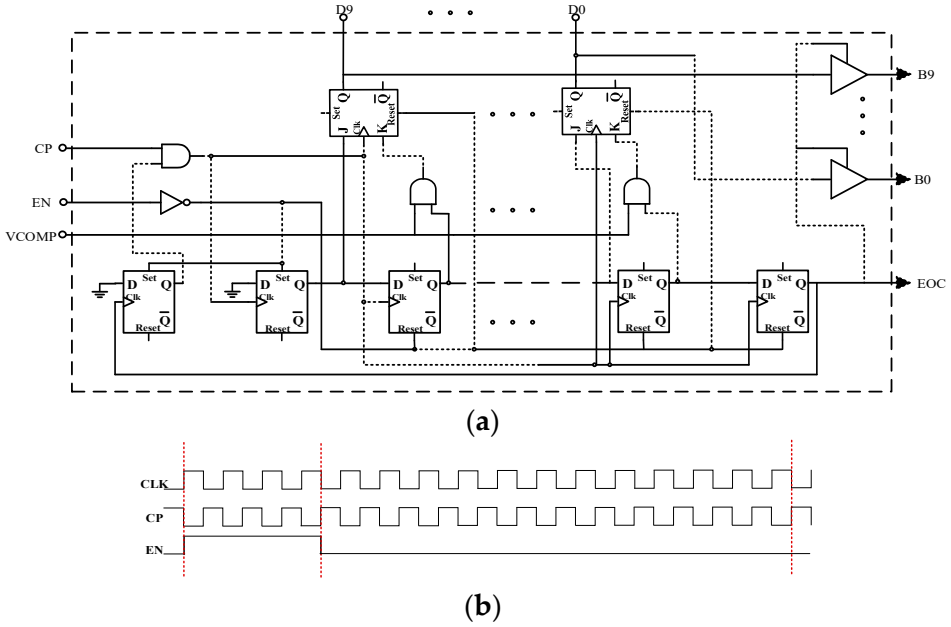


Figure 6. SAR logic. (**a**) SAR logic circuit; (**b**) timing of CLK, CP, and EN.

3. Simulation Result and Discussion

Cadence allows for accurate modeling of analog circuits in CMOS technology and provides detailed post-layout simulation capabilities. The circuit was designed and simulated by using Cadence Virtuoso IC 6.1.7. The AFE was implemented using 0.18 µm 1P7M CMOS technology, operating at a supply voltage of 3.3 V. As depicted in Figure 7, the chip area measures 1475 µm × 1410 µm.

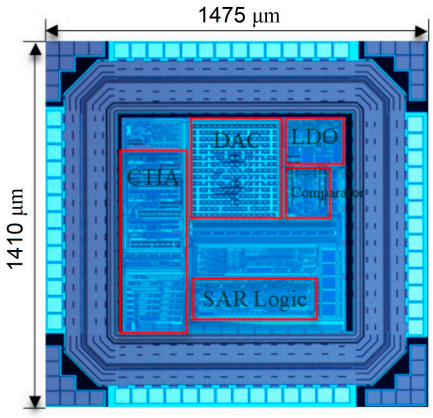
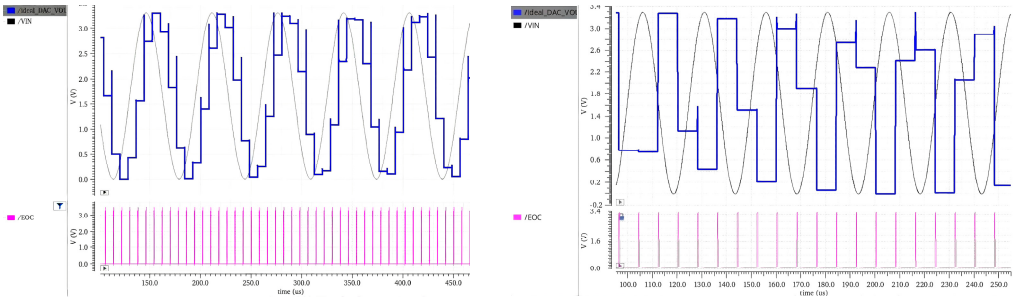


Figure 7. Layout view of the AFE.

Figure 8 presents the comparison between the ideal DAC output and the AFE's response to input sine wave signals at frequencies of 15 KHz and 40 KHz. The simulation results demonstrate that the output signal code B0 to B9 from the AFE accurately represent the input sine wave signals, verify the functionality of the SAR ADC.

To evaluate the performance under different input currents, we tested the AFE with input currents of 10 nA. The output waveforms of the integrator, CDS, and SAR ADC are illustrated in Figure 9. The results indicate that the CDS effectively stabilizes the integrator's final voltage output, and the SAR ADC accurately quantizes the CDS output. Upon receiving the EOC signal, the final quantization result is held for one operating cycle before the next EOC.



(**a**) (**b**)

Figure 8. Comparison to ideal DAC output in 15 kHz and 40 kHz: (**a**) input sine wave signal at 15 kHz; (**b**) input sine wave signal at 40 kHz.

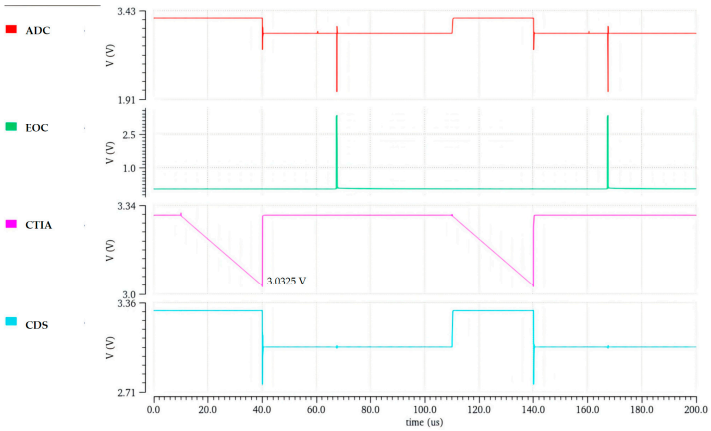


Figure 9. The simulation output waveform.

Figure 10 presents the FFT result, which was conducted with 2048 sampling points and an input sine wave frequency of 15 kHz. The proposed AFE circuit achieves an SNR of 59.27 dB. This high SNR is primarily due to the optimized CTIA and CDS circuits, which effectively minimize thermal, flicker, and quantization noise. And the proposed AFE achieves an ENOB of 9.35 bits. This high ENOB is made possible by the 10-bit SAR ADC architecture, which was optimized to minimize the effects of quantization noise and thermal fluctuations. The slight reduction from the full 10-bit resolution to the effective 9.35 bits is due to the noise from the analog front-end components, including the CTIA and DAC. The SINAD of the AFE is measured to be 58.07 dB, which indicates that the system effectively suppresses harmonic distortion. This was achieved by optimizing the feedback loop in the CTIA to reduce non-linearities and employing a well-balanced DAC in the SAR ADC to minimize distortive elements.

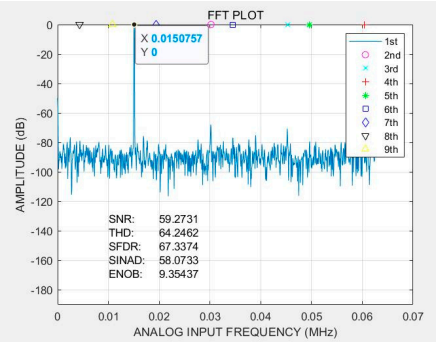


Figure 10. FFT result with the input signal frequency of 15 KHz.

The frequency spectrum of the AFE output under different input signal frequencies is shown in Figure 11a–c. By processing the simulation results and performing Fast Fourier Transform (FFT) analysis, we observed that the output frequency spectrum corresponds accurately to the input frequencies. Simulations were conducted with 512 sampling points and an input sine wave frequency of 15 kHz. Additionally, to ensure the robustness of the AFE design, simulations were performed under different process corners, including typical (tt), fast (ff), and slow (ss) corners. The results, presented in Figure 11d–f, confirm that the AFE maintains stable performance across varying process conditions, with minimal deviation in output frequency and signal integrity. This robustness is crucial for ensuring consistent performance in mass production and varying environmental conditions.

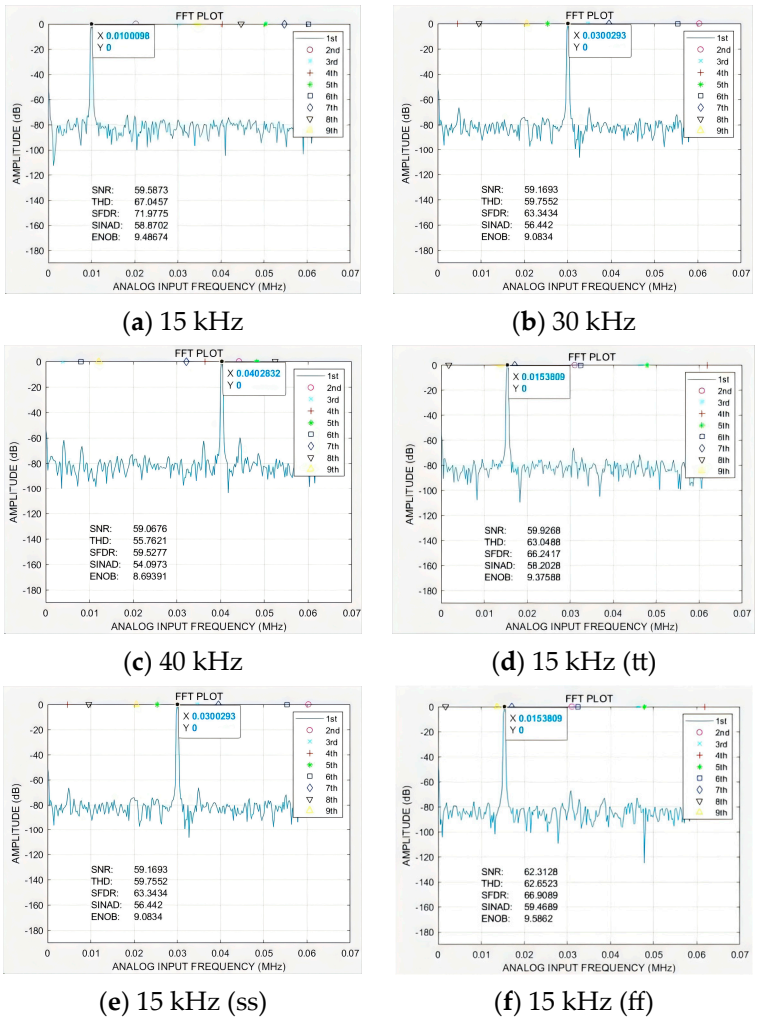


Figure 11. The FFT results at different input signal frequencies and corners: (**a**) input signal frequencies at 10 KHz; (**b**) input signal frequencies at 30 KHz; (**c**) input signal frequencies at 40 KHz; (**d**) input signal frequencies at 15 KHz and corner of tt; (**e**) input signal frequencies at 15 KHz and corner of ss; and (**f**) input signal frequencies at 15 KHz and corner of ff.

To evaluate the performance of the proposed AFE circuit for carbon-based SWIR photodetectors, a comparison was conducted with several recent works in the field. The comparison focuses on key parameters such as detectable current range, SNR, ENOB, power consumption, voltage swing, linearity, and pixel array size. Table 1 provides a summary of the performance metrics of the proposed AFE and those reported in other studies. The proposed AFE demonstrates several key advantages over existing designs. It achieves a larger voltage swing compared to refs. [23,24], while operating under the same power supply conditions, which enhances the dynamic range and overall performance.

Although ref. [14] exhibits good linearity, its detection range and output voltage swing are relatively limited. In contrast, our AFE not only maintains high linearity but also supports a broader detection range and larger output voltage swing, making it more versatile for various applications. The AFEs in refs. [13,14,24–26] employing a CTIA were primarily designed for either small current ranges or high dynamic current scenarios. Our design extends the current detection range from 500 pA to 100.5 nA, accommodating a wider array of signal conditions without compromising performance. Furthermore, the proposed AFE achieves an impressive readout linearity of 99.92%, surpassing the linearity metrics of most prior works. This high linearity ensures accurate signal processing and enhances the reliability of the sensor data. Overall, the proposed AFE outperforms existing designs in key performance metrics such as voltage swing, linearity, and current range compatibility. However, while the proposed AFE demonstrates superior performance in many aspects, it is important to acknowledge certain trade-offs. For instance, achieving a wide detection range and high linearity may come at the expense of increased design complexity and layout area.

Table 1. Comparison with recent AFEs.

Parameter	[13]	[14]	[23]	[25]	[24]	[26]	This Work
Technology (nm)	350	180	350	180	180	180	180
Array Format	128 × 128	640 × 512	1280 × 1024	NA	32 × 32	4 × 4	8 × 8
Pixel Input	DI.CTIA	BDI	DI	CTIA	SFD/CTIA	CTIA	CTIA
Voltage Swing	2 V	0.98	3.2 V	2 V	NA	/	2.8 V
Detectable current range	0.11 pA–50 nA	fA–100 pA	0–3.1 nA	470 nA–5 uA	15 pA–3 nA	2 pA–10 nA	500 pA–100.5 nA
Linearity	>99%	99.95%	97.76%	99%	NA	99.5%	99.92%
Consumption	<50 mw	57.5 mW	/	60 uW/pixel	2.8 uW/pixel	800 nW	7.5 mW

4. Conclusions

In this paper, we have presented the design and simulation of a low-power, high-resolution AFE circuit tailored for carbon-based SWIR photodetectors. Implemented using 0.18 μm 1P7M CMOS technology, the proposed AFE integrates a CTIA, a CDS circuit, and a 10-bit/125 kHz SAR ADC, achieving a high SNR of 59.27 dB and an ENOB of 9.35. The circuit supports a wide detectable current range from 500 pA to 100.5 nA with a total power consumption of 7.5 mW, making it suitable for high-precision, low-power SWIR photodetector applications. The simulation results confirm that the AFE effectively addresses the challenges associated with processing weak photocurrents from SWIR photodetectors, providing stable and accurate signal conversion even under varying conditions. The enhanced detection range, high linearity, and low power consumption are key advantages that set this design apart from existing solutions, making it a strong candidate for integration into advanced infrared imaging systems. Future research will focus on further optimizing the power consumption of the AFE circuit and extending its detectable current range to accommodate even lower signal levels. Additionally, exploring the integration of the AFE with other emerging materials and sensor technologies could open new avenues for high-performance, low-cost SWIR imaging solutions. Further experimental validation and real-world testing will also be essential to transition this design from simulation to practical application.

Author Contributions: Conceptualization, Y.Z. and Z.C.; software simulation and parameter optimization, Y.Z. and W.L.; data processing, W.X. and W.L.; writing—original draft preparation, W.X. and Z.C.; writing—review and editing, Y.Z. and C.C.; supervision, J.J. and C.C. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by Natural Science Foundation of Fujian Province (No. 2023 H0052) and major science and technology projects of Xiamen (No. 3502Z20221022).

Data Availability Statement: All the data are reported/cited in the paper.

Conflicts of Interest: The authors declare no conflicts of interest.

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