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Diagnosis of DC-DC Converter Semiconductor Faults Based on the Second-Order Derivative of the Converter Input Current

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Abstract: The deployment of DC microgrids presents an excellent opportunity to enhance energy efficiency in buildings. Among other components, DC-DC converters play a crucial role in ensuring the interface between the microgrid and its energy generation, storage, and consumption components. However, the reliability of these energy conversion solutions remains somewhat limited. Adopting strategies for accurate monitoring and diagnostics of the DC-DC converter topologies that best suit each equipment's constraints is, therefore, of critical relevance. Solutions available in the literature concerning fault diagnostics on DC-DC converters do not consider the application of such converters in the household and tertiary sector environments and associated constraints—cost effectiveness, robustness against parameter uncertainty of the converter model, and obviation of the need for historical data. On this basis, this paper presents a simple and effective fault diagnostic strategy, based on a time-domain analysis of the second-order derivative of the converter input current. Its implementation is straightforward and can be integrated into the pre-installed converter control unit. The unique features of the fault diagnostic algorithm show good results for a broad range of operating points, along with insensitivity against load transients and supply voltage fluctuations.

Keywords: DC microgrids; DC-DC power conversion; fault diagnostics; fault location; semiconductor faults

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1. Introduction

Recent technological developments have promoted significant changes in the energy systems used in homes and offices. These systems consist of electrical equipment, with several end-uses, that can be framed in three major categories: energy microgeneration systems, loads, and energy storage systems.

Technologies for distributed energy generation, usually consisting of photovoltaic cells, wind turbines, cogeneration systems, or fuel cells, take advantage of some renewable energy sources of energy. Most of these technologies operate in DC, or involve, at a certain point, a power conversion process with a DC voltage bus.

Concurrently, the electricity consumption associated with the set of DC-compatible loads has increased significantly. Electricity consumption related to small appliances (TVs, mobile phones, laptops, etc.), where most state-of-the-art DC-powered products are framed, in conjunction with heating, lighting and variable-speed DC-compatible appliances (refrigerators, freezers, washing machines, dishwashers, etc.), represent the prevailing end-uses of electricity within the domestic context in Europe [1]. The broad adoption of the electric vehicle shall further leverage the energy consumption made by DC-compatible devices in the household and tertiary sectors.

In this framework, the shift towards a paradigm where the broad adoption of DC microgrids is a reality becomes increasingly compelling. Hence, connecting microgeneration plants, loads, and energy storage systems into a common DC bus presents a major opportunity to significantly improve energy efficiency in buildings, reduce reliance on fossil fuels, and lower electricity costs.

Given the key role of DC-DC converters within DC microgrids, the successful deployment of this novel energy distribution paradigm is strongly conditioned by the availability of efficient and reliable DC-DC converters. State-of-the-art fault tolerant DC-DC converters are too expensive and complex for household applications, making the migration to DC microgrids prohibitively costly. Cheaper and robust fault tolerant DC-DC converters are required for such purpose. This concern becomes particularly relevant in case of DC-DC converters responsible for interfacing microgeneration or energy storage systems with the microgrid itself. Bidirectional DC-DC converters are increasingly requested for charging energy storage devices and electric vehicles (EVs). Within the context of DC microgrids, the ability to absorb or inject power into the grid is a particularly appreciated feature, providing peak shaving and additional system inertia.

As any other power electronics converter, DC-DC converters are often exposed to stressful operating conditions, which may lead to faults, in extreme cases. Semiconductor faults, considered of particular relevance because of their impact on the converter operation, can be categorised as short-circuit (SC) or open-circuit (OC) faults. SC faults evolve very fast and are extremely damaging. Typically, SC faults arise from defective gate drivers or control circuits, or from an increase in temperature caused by overcurrent or overvoltage on the semiconductors. To prevent catastrophic damage to the entire system, hardware protection circuits such as circuit breakers, relays, or fuses are implemented, leading to subsequent OC faults. This is the main reason why research in this field mainly focuses on diagnosing OC faults rather than SC faults.

Several OC fault diagnostic methods, applied to different DC-DC converters topologies, have been studied in the literature [2]. Semiconductor fault diagnosis may either be accomplished through signal processing approaches, model-based approaches, or artificial intelligence methods [3,4]. The most recurring signal-processing-based fault diagnostic methods include the comparison of the PWM duty cycle with the inductor current slope [5], time-domain analysis of the DC-link current derivative sign [6], adoption of a state machine for evaluating the inductor current and gating signal [7], time-domain analysis of the current amplitude [8], evaluation of the reference current error [9], comparison of the inductor current samples taken during the rising and falling edges [10], analysis of the input current integral [11], estimation of the Fourier series coefficients [12], analysis of the input current slope [13,14], analysis of the current inflexion points [15], sampling of the input and output current at the peak/valley point of the carrier [16], monitoring of the capacitors voltage [17,18], detection of the sub-module output voltage [19], monitoring of the magnetic near-field [20], monitoring of the interleaved converter output voltage [21,22], evaluation of the magnetic components voltage waveforms [23], diode voltage evaluation [24,25], analysis of the switching frequency harmonic [26], modality analysis [27], vector analysis [28], or slope analysis of the phase currents [29]. These approaches enable effective diagnostics in a broad range of DC-DC converter topologies, including, among others, conventional buck and boost converters [30,31], multiport bidirectional converters [32,33], dual active-bridge converters [34] and triple active-bridge converters [35]. The limitation in effectiveness for certain DC-DC converter topologies, the significant number of measurements required to accomplish fault diagnostics, the risk of misdiagnosis, or the extended time to diagnostics are some of the main bottlenecks associated to state-of-the-art fault diagnostic approaches based on signal processing.

The emergence of sophisticated DSPs triggered the development of model-based approaches. State-space observers [36,37], Luenberger observers [38,39], sliding mode observers [40], immersion and invariant observers [41], parameter identification [42,43], inductor current emulation [44,45], or digital twins [46], are among the most common model-based fault diagnostic approaches adopted in DC-DC converters. The derivation of such converter models may be particularly challenging in converters with a significant number of components, making the implementation of such approaches challenging. Moreover, real-time emulation of the converter response requires significant computational effort.

More recently, approaches based on artificial intelligence were proposed to detect parametric fault characteristics, using neural networks [47,48], machine learning [49], transfer learning [50], or contrastive learning [51]. The large datasets and requirement of prior training make artificial intelligence approaches hard to implement without compromising cost-effectiveness.

To address these concerns, this paper proposes an OC fault diagnostic algorithm for DC-DC converters, but particularly tailored for interleaved converters. Unlike most fault diagnostic algorithms that focus on analysing diagnostic variables during the on-state or off-state periods of converter switches, the proposed algorithm focuses on the converter's response during the transition between switch states. The behaviour of the second-order derivative of the converter low-side current reflects, in almost all instances, the behaviour of a single converter phase. The application of the second-order derivative to the converter input current successfully isolates the components of the second-order derivative related to each converter phase, allowing to assess, for each moment, the influence that each converter phase plays into the second-order derivative of the converter current. Thanks to the features of the proposed method, the resiliency of the fault diagnostic process and, most of all, of the fault identification action, becomes greatly improved.

A thorough analytical description of the fault diagnostic algorithm first proposed in [15] is presented in the paper. Also, additional simulation and experimental results confirm the effectiveness of the algorithm.

This paper is organised as follows. Section 2 describes the operational principles of a three-phase non-isolated bidirectional interleaved DC-DC converter under normal and faulty conditions. The proposed OC fault diagnostic strategy is explained in Section 3. Simulation results are presented and analysed in Section 4, while experimental data are provided and evaluated in Section 5. Lastly, concluding remarks are given in Section 6.

2. Converter Operation

2.1. Operation under Healthy Condition

Figure 1 depicts the three-phase non-isolated bidirectional interleaved DC-DC converter, used in this study.

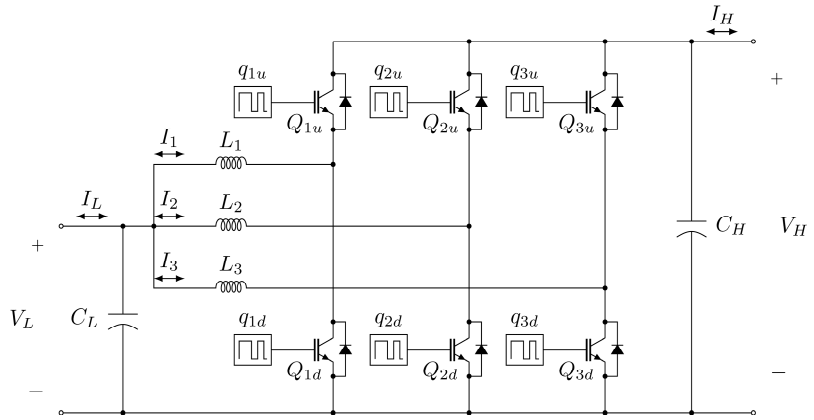

Figure 1. Three-phase non-isolated bidirectional interleaved DC-DC converter.

The low-voltage side current I_L comprises the sum of each phase current:

$$I_L = I_1 + I_2 + I_3. \tag{1}$$

The identical nature of all the converter phases confer a reasonable balance between them, just impaired by small deviations of phase inductances or parasitic resistances [52]. The introduction of a perturbation in one or more of the converter phases $I_{1\ldots3}$ will be reflected in the low-voltage side current I_L. Considering that I_L is commonly acquired by

the converter controller, for both control and safety purposes, the evolution of this signal in the time-domain can be tracked, to detect abnormal behaviour of any converter phase.

The following analysis focuses on the converter operation under boost mode, i.e., with power flow taking place from the low-side to the high-side. Identical analysis is applicable to the converter operation in buck mode. An analysis will be performed for just one converter phase, due to the identical nature of the remaining phases. When a gating signal is applied on the power switch Q_{1d}, the voltage across inductor L_1 equals the low voltage V_L. The current crossing the switch Q_{1d} is equal to the current on inductor L_1. Therefore, the first-order derivative of the inductor current dI_1/dt will be defined as:

$$\frac{dI_1}{dt} = \frac{V_L}{L_1}. \tag{2}$$

Hence, the slope of the current crossing inductor L_1 is constant and positive, and the current increases linearly while Q_{1d} is conducting. Consequently, the second-order derivative of the inductor current d^2I_1/dt^2 during this period will be null:

$$\frac{d^2I_1}{dt^2} = 0. \tag{3}$$

Meanwhile, when the gating signal is removed from the power switch Q_{1d}, no current flows across it. The voltage across the inductor L_1, given by the difference between the low voltage V_L and the high voltage V_H, is negative, as V_H is higher than V_L. Therefore, the first-order derivative of the current flowing through the inductor L_1 is given by

$$\frac{dI_1}{dt} = \frac{V_L - V_H}{L_1}. \tag{4}$$

This means that the current crossing the inductor L_1 decreases linearly after the switch Q_{1d} turn-off. Consequently, the first-order derivative dI_1/dt is constant and negative immediately after the switch Q_{1d} turn-off. This means that the second-order derivative of the inductor current d^2I_1/dt^2 is also null when Q_{1d} is off:

$$\frac{d^2I_1}{dt^2} = 0. \tag{5}$$

According to (3) and (5), d^2I_1/dt^2 equals to zero during the on- and off-states of the power switch Q_{1d}. However, such statement is no longer valid for the transition between the on- and off-states (and vice-versa) of the power switch Q_{1d}. During the transition between switch states, there is a variation in time on the absolute value of dI_1/dt, that can be expressed as a linear function.

For the turn-off transition, dI_1/dt can be expressed as:

$$\frac{dI_1}{dt} = -\frac{V_H}{L_1 t_{\text{on}\to\text{off}}} t + \frac{V_L t_{\text{on}\to\text{off}} + V_H t_i}{L_1 t_{\text{on}\to\text{off}}} \tag{6}$$

where t denotes the time variable, $t_{\text{on}\to\text{off}}$ refers to the turn-off transition period, and t_i denotes the instant at which the transition begins. Based on (6), the second-order derivative d^2I_1/dt^2, observed during the turn-off transient of switch Q_{1d}, is negative and given by:

$$\frac{d^2I_1}{dt^2} = -\frac{V_H}{L_1 t_{\text{on}\to\text{off}}}. \tag{7}$$

On the other hand, for the turn-on transition, dI_1/dt can be expressed as follows:

$$\frac{dI_1}{dt} = \frac{V_H}{L_1 t_{\text{off}\to\text{on}}} t + \frac{(V_L - V_H) t_{\text{off}\to\text{on}} - V_H t_i}{L_1 t_{\text{off}\to\text{on}}} \tag{8}$$

where t denotes the time variable, $t_{\text{off}\to\text{on}}$ refers to the turn-on transition period, and t_i denotes the instant at which the transition begins. Based on (9), the second-order derivative d^2I_1/dt^2, observed during the turn-on transient of switch Q_{1d}, is positive and defined as:

$$\frac{d^2I_1}{dt^2} = \frac{V_H}{L_1 t_{\text{off}\to\text{on}}}. \tag{9}$$

Two additional conditions must be considered in case that the converter operates in discontinuous conduction mode (DCM), as the phase current increases from zero during the turn-on instant. At the same time, the phase current extinguishes before the beginning of the next switching period. Considering DCM conditions, the first-order derivative dI_1/dt, observed during the turn-on transient of switch Q_{1d}, is given by:

$$\frac{dI_1}{dt} = \frac{V_L}{L_1 t_{0\to\text{on}}} t - \frac{V_L t_i}{L_1 t_{0\to\text{on}}} \tag{10}$$

where t denotes the time variable, $t_{0\to\text{on}}$ refers to the turn-on transition period, and t_i denotes the instant at which the transition begins. Hence, the second-order derivative d^2I_1/dt^2, observed during the turn-on transient of switch Q_{1d}, is positive and defined as:

$$\frac{d^2I_1}{dt^2} = \frac{V_L}{L_1 t_{0\to\text{on}}}. \tag{11}$$

On the other hand, the first-order derivative dI_1/dt, observed during the extinction of the phase current, is given by:

$$\frac{dI_1}{dt} = \frac{V_H - V_L}{L_1 t_{\text{off}\to 0}} t + \frac{(V_L - V_H)(t_i + t_{\text{off}\to 0})}{L_1 t_{\text{off}\to 0}} \tag{12}$$

where t denotes the time variable, $t_{\text{off}\to 0}$ refers to the current extinction transient period, and t_i denotes the instant at which the transition begins. Hence, the second-order derivative d^2I_1/dt^2, observed during the extinction of the phase current, is given by:

$$\frac{d^2I_1}{dt^2} = \frac{V_H - V_L}{L_1 t_{\text{off}\to 0}}. \tag{13}$$

Please note that constants $t_{\text{on}\to\text{off}}$, $t_{\text{off}\to\text{on}}$, $t_{0\to\text{on}}$ and $t_{\text{off}\to 0}$ mostly depend on the switching characteristics of the semiconductor devices, meaning that such parameters can usually be retrieved from the device datasheet.

From the above theoretical analysis, it is concluded that the relevant increment in the magnitude of d^2I_1/dt^2 allows to clearly identify the effective transition between states of the power switch Q_{1d}. Figure 2 provides a generic representation of the phase current and the corresponding first- and second-order derivatives, considering the two conduction modes: DCM and continuous conduction mode (CCM).

From Figure 2, it is shown that d^2I_1/dt^2 clearly reflects the switching events taking place in phase 1. Particularly prominent and distinguishable increments in the magnitude of d^2I_1/dt^2 are verified during the commutation of the power switch associated to that phase.

Since the low-voltage side current results from the sum of the three phase currents—see (1), the same is valid for the second-order derivative:

$$\frac{d^2I_L}{dt^2} = \frac{d^2I_1}{dt^2} + \frac{d^2I_2}{dt^2} + \frac{d^2I_3}{dt^2}. \tag{14}$$

As demonstrated in Figure 3, the second-order derivative of the low-voltage side current (d^2I_L/dt^2) clearly reflects all the switching events taking place in the converter, either in DCM or CCM.

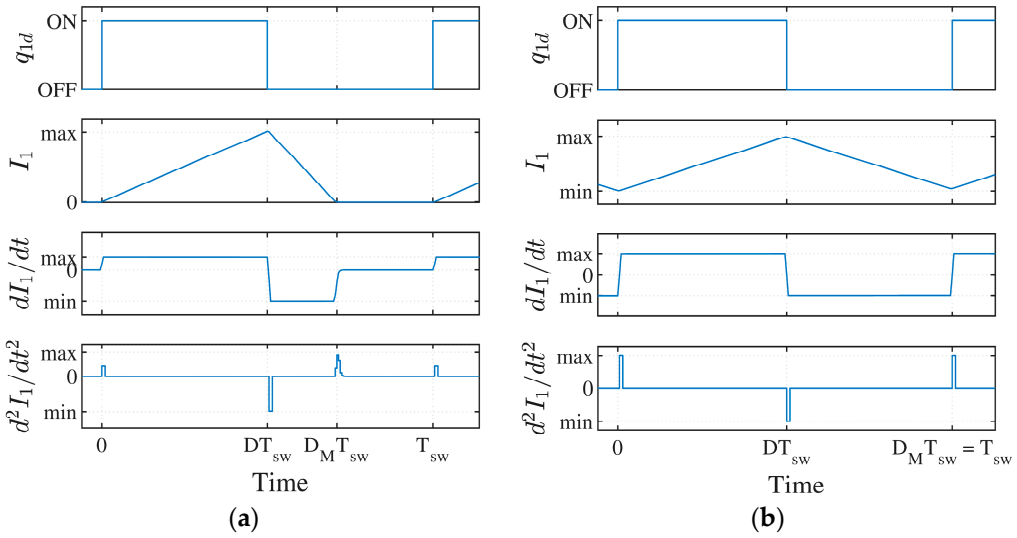

Figure 2. Phase 1 control pulse q_{1d}, phase 1 inductor current I_1, first- and second-order derivatives of phase 1 inductor current (dI_1/dt and d^2I_1/dt^2, respectively), considering the following conduction modes: (**a**) DCM; (**b**) CCM.

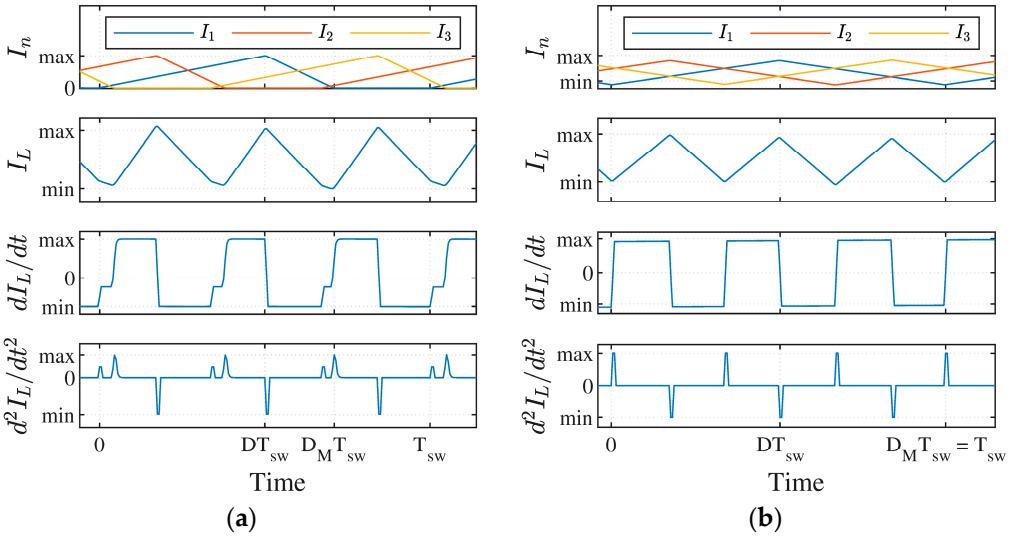

Figure 3. Individual phase currents $I_{1...3}$, low-voltage side current I_L, first- and second-order derivatives of current I_L (dI_L/dt and d^2I_L/dt^2, respectively), considering the following conduction modes: (**a**) DCM; (**b**) CCM.

2.2. Operation under Faulty Condition

After an open-circuit (OC) fault in a power switch, no current flows through it. If the fault occurs while the power switch Q_{1d} was on, a quick transition from the on-state to the off-state will occur, and the absolute value of the second-order derivative d^2I_1/dt^2 will decrease substantially right after the OC fault:

$$\frac{d^2I_1}{dt^2} = -\frac{V_H}{L_1 t_{on \to off}}. \tag{15}$$

On the other hand, the increment of d^2I_1/dt^2, expected right after a state transition on the gating signal applied to the faulty power switch Q_{1d}, will not take place because of the likely extinction of the phase current. Therefore, d^2I_1/dt^2 will be characterised as follows:

$$\frac{d^2 I_1}{dt^2} = 0. \tag{16}$$

Figure 4 shows the most important variables of the converter, during an OC fault episode. An OC fault is introduced in power switch Q_{1d} at around half of $D \cdot T_{sw}$. After that moment, solid lines depict the effective evolution of the variables, whereas dashed lines represent the behaviour that would be verified for healthy operation.

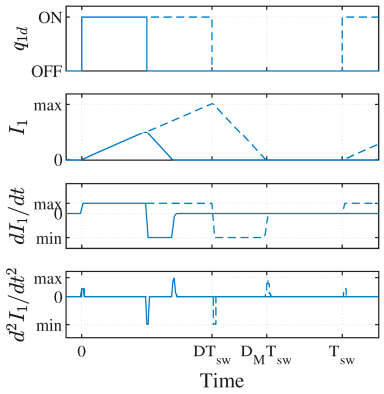

Figure 4. Phase 1 control pulse q_{1d}, phase 1 inductor current I_1, first- and second-order derivatives of phase 1 inductor current (dI_1/dt and d^2I_1/dt^2, respectively), observed in the presence of an OC fault in IGBT Q_{1d}.

2.3. Comparison between Healthy and Faulty Condition

Considering the ideal model of the interleaved converter, the voltage gain of the converter is expressed as follows:

$$\frac{V_H}{V_L} = \frac{D_M}{D_M - D} \tag{17}$$

where D_M denotes the period of non-zero inductor current and D denotes the switching duty cycle.

Assuming equal components in all the converter phases, it is possible to derive the general expressions of d^2I_L/dt^2, for each state transition taking place.

For ease of analysis, the following assumptions are taken:

(1) Considering the converter steady-state condition, it is possible to assume that variables D and D_M do not suffer significant oscillations along one switching period and, consequently, these variables remain constant.
(2) D_M is always equal or higher than D. In practice, this means that condition $D_M - D$ is always positive.
(3) The turn-on and turn-off periods are assumed to be identical, resulting in the following conditions:

$$t_{0\to on} \approx t_{off\to 0} \approx t_{off\to on} \approx t_{on\to off} = t_t \tag{18}$$

Based on the aforementioned assumptions, the information of second-order derivative d^2I_L/dt^2, assessed during the transition between switch states, provides useful information about the converter condition.

Table 1 compares the second-order derivative d^2I_L/dt^2 in the case of healthy and faulty operation, when the converter operates in boost mode. The fault condition being considered consist of an open-circuit fault in IGBT Q_{1d}.

It is worth noting that the analysis of d^2I_L/dt^2, presented in Table 1, is carried out exclusively during the state transitions observed in the command signal q_{1d}. The same analysis is valid for any of the three converter phases.

Table 1. Second-order derivative of the low-voltage side current I_L (steady state)—boost mode.

D	D_M	q_{1d} State Transition	d^2I_L/dt^2, Healthy	d^2I_L/dt^2, Faulty
$0 < D < \frac{1}{3}$	$D_M = \frac{1}{3}$ $D_M = \frac{2}{3}$	OFF → ON	$\frac{V_H}{Lt_t} > 0$	$\frac{V_H - V_L}{Lt_t} > 0$
		ON → OFF	$-\frac{V_H}{Lt_t} < 0$	0
	$D_M = 1$ (BCM and CCM)	OFF → ON	$\frac{V_H}{Lt_t} > 0$	0
		ON → OFF	$-\frac{V_H}{Lt_t} < 0$	0
	$0 < D_M < \frac{1}{3}$ $\frac{1}{3} < D_M < \frac{2}{3}$ $\frac{2}{3} < D_M < 1$	OFF → ON	$\frac{V_L}{Lt_t} > 0$	0
		ON → OFF	$-\frac{V_H}{Lt_t} < 0$	0
	$D_M = \frac{1}{3} + D$ $D_M = \frac{2}{3} + D$	OFF → ON	$\frac{V_L}{Lt_t} > 0$	0
		ON → OFF	$-\frac{V_L}{Lt_t} < 0$	$\frac{V_H - V_L}{Lt_t} > 0$
$D = \frac{1}{3}$	$D_M = \frac{2}{3}$	OFF → ON	0	$-\frac{V_L}{Lt_t} < 0$
		ON → OFF	0	$\frac{V_H}{Lt_t} > 0$
	$D_M = 1$ (BCM and CCM)	OFF → ON	0	$-\frac{V_H}{Lt_t} < 0$
		ON → OFF	0	$\frac{V_L}{Lt_t} > 0$
	$\frac{1}{3} < D_M < \frac{2}{3}$ $\frac{2}{3} < D_M < 1$	OFF → ON	$\frac{V_L - V_H}{Lt_t} < 0$	$-\frac{V_H}{Lt_t} < 0$
		ON → OFF	$\frac{V_L - V_H}{Lt_t} < 0$	$\frac{V_L}{Lt_t} > 0$
$\frac{1}{3} < D < \frac{2}{3}$	$D_M = \frac{2}{3}$	OFF → ON	$\frac{V_H}{Lt_t} > 0$	$\frac{V_H - V_L}{Lt_t} > 0$
		ON → OFF	$-\frac{V_H}{Lt_t} < 0$	0
	$D_M = 1$ (BCM and CCM)	OFF → ON	$\frac{V_H}{Lt_t} > 0$	0
		ON → OFF	$-\frac{V_H}{Lt_t} < 0$	0
	$\frac{1}{3} < D_M < \frac{2}{3}$ $\frac{2}{3} < D_M < 1$	OFF → ON	$\frac{V_L}{Lt_t} > 0$	0
		ON → OFF	$-\frac{V_H}{Lt_t} < 0$	0
	$D_M = \frac{1}{3} + D$	OFF → ON	$\frac{V_L}{Lt_t} > 0$	0
		ON → OFF	$-\frac{V_L}{Lt_t} < 0$	$\frac{V_H - V_L}{Lt_t} > 0$
$D = \frac{2}{3}$	$D_M = 1$ (BCM and CCM)	OFF → ON	0	$-\frac{V_H}{Lt_t} < 0$
		ON → OFF	0	$\frac{V_H}{Lt_t} > 0$
	$\frac{2}{3} < D_M < 1$	OFF → ON	$\frac{V_L - V_H}{Lt_t} < 0$	$-\frac{V_H}{Lt_t} < 0$
		ON → OFF	$\frac{V_L - V_H}{Lt_t} < 0$	$\frac{V_L}{Lt_t} > 0$
$\frac{2}{3} < D < 1$	$D_M = 1$ (BCM and CCM)	OFF → ON	$\frac{V_H}{Lt_t} > 0$	0
		ON → OFF	$-\frac{V_H}{Lt_t} < 0$	0
	$\frac{2}{3} < D_M < 1$	OFF → ON	$\frac{V_L}{Lt_t} > 0$	0
		ON → OFF	$-\frac{V_H}{Lt_t} < 0$	0

An evaluation of the results provided in Table 1 allows us to draw the following conclusions:

- For the intervals where D is variable (i.e., $0 < D < 1/3$, $1/3 < D < 2/3$, and $2/3 < D < 1$), d^2I_L/dt^2 approaches to zero for at least one state transition, when an OC fault occurs;
- When D is either equal to $1/3$ or $2/3$, d^2I_L/dt^2 is positive for the ON → OFF transition; under healthy state, d^2I_L/dt^2 is either null or negative.

Given the architecture of the DC-DC converter, both boost and buck modes are feasible. For buck mode, in particular, current I_L becomes negative, thus impacting the estimated values of d^2I_L/dt^2. Table 2 compares the second-order derivative d^2I_L/dt^2 in the case of healthy and faulty operation, when the converter operates in buck mode. The fault condition being considered consist of an open-circuit fault in IGBT Q_{1u}.

Table 2. Second-order derivative of the low-voltage side current I_L (steady state)—buck mode.

D	D_M	q_{1u} State Transition	d^2I_L/dt^2, Healthy	d^2I_L/dt^2, Faulty
$0 < D < \frac{1}{3}$	$D_M = \frac{1}{3}$ $D_M = \frac{2}{3}$	OFF → ON	$-\frac{V_H}{Lt_t} < 0$	$-\frac{V_L}{Lt_t} > 0$
		ON → OFF	$\frac{V_H}{Lt_t} > 0$	0
	$D_M = 1$ (BCM and CCM)	OFF → ON	$-\frac{V_H}{Lt_t} < 0$	0
		ON → OFF	$\frac{V_H}{Lt_t} > 0$	0
	$0 < D_M < \frac{1}{3}$ $\frac{1}{3} < D_M < \frac{2}{3}$ $\frac{2}{3} < D_M < 1$	OFF → ON	$\frac{V_L - V_H}{Lt_t} < 0$	0
		ON → OFF	$\frac{V_H}{Lt_t} > 0$	0
	$D_M = \frac{1}{3} + D$ $D_M = \frac{2}{3} + D$	OFF → ON	$\frac{V_L - V_H}{Lt_t} < 0$	0
		ON → OFF	$\frac{V_H - V_L}{Lt_t} > 0$	$-\frac{V_L}{Lt_t} < 0$
$D = \frac{1}{3}$	$D_M = \frac{2}{3}$	OFF → ON	0	$\frac{V_H - V_L}{Lt_t} > 0$
		ON → OFF	0	$-\frac{V_H}{Lt_t} < 0$
	$D_M = 1$ (BCM and CCM)	OFF → ON	0	$\frac{V_H}{Lt_t} > 0$
		ON → OFF	0	$-\frac{V_H}{Lt_t} < 0$
	$\frac{1}{3} < D_M < \frac{2}{3}$ $\frac{2}{3} < D_M < 1$	OFF → ON	$\frac{V_L}{Lt_t} > 0$	$\frac{V_H}{Lt_t} > 0$
		ON → OFF	$\frac{V_L}{Lt_t} > 0$	$\frac{V_L - V_H}{Lt_t} < 0$
$\frac{1}{3} < D < \frac{2}{3}$	$D_M = \frac{2}{3}$	OFF → ON	$-\frac{V_H}{Lt_t} < 0$	$-\frac{V_L}{Lt_t} > 0$
		ON → OFF	$\frac{V_H}{Lt_t} > 0$	0
	$D_M = 1$ (BCM and CCM)	OFF → ON	$-\frac{V_H}{Lt_t} < 0$	0
		ON → OFF	$\frac{V_H}{Lt_t} > 0$	0
	$\frac{1}{3} < D_M < \frac{2}{3}$ $\frac{2}{3} < D_M < 1$	OFF → ON	$\frac{V_L - V_H}{Lt_t} < 0$	0
		ON → OFF	$\frac{V_H}{Lt_t} > 0$	0
	$D_M = \frac{1}{3} + D$	OFF → ON	$\frac{V_L - V_H}{Lt_t} < 0$	0
		ON → OFF	$\frac{V_H - V_L}{Lt_t} > 0$	$-\frac{V_L}{Lt_t} < 0$
$D = \frac{2}{3}$	$D_M = 1$ (BCM and CCM)	OFF → ON	0	$\frac{V_H}{Lt_t} > 0$
		ON → OFF	0	$-\frac{V_H}{Lt_t} < 0$
	$\frac{2}{3} < D_M < 1$	OFF → ON	$\frac{V_H}{Lt_t} > 0$	$\frac{V_H}{Lt_t} > 0$
		ON → OFF	$\frac{V_H}{Lt_t} > 0$	$\frac{V_L - V_H}{Lt_t} < 0$
$\frac{2}{3} < D < 1$	$D_M = 1$ (BCM and CCM)	OFF → ON	$-\frac{V_H}{Lt_t} < 0$	0
		ON → OFF	$\frac{V_H}{Lt_t} > 0$	0
	$\frac{2}{3} < D_M < 1$	OFF → ON	$\frac{V_L - V_H}{Lt_t} < 0$	0
		ON → OFF	$\frac{V_H}{Lt_t} > 0$	0

An evaluation of the results provided in Table 2 allows us to draw the following conclusions:

- For the intervals where D is variable (i.e., $0 < D < 1/3$, $1/3 < D < 2/3$, and $2/3 < D < 1$), d^2I_L/dt^2 is null for at least one state transition; these conditions are identical to those observed for the boost mode;
- When D is either equal to $1/3$ or $2/3$, d^2I_L/dt^2 is negative for the ON $\rightarrow$ OFF transition; under healthy state, d^2I_L/dt^2 is either null or positive; these conditions are complementary to those observed for the boost mode.

As confirmed in Tables 1 and 2, the analysis of d^2I_L/dt^2 provides useful information about the condition of the converter semiconductors. The following section provides an explanation of the procedures taken to implement the proposed fault diagnostic strategy.

3. Proposed Fault Diagnostics Algorithm

As mentioned in Section 2, the converter left-side current I_L is used for fault diagnostic purposes, as the effects of possible faults, in any of the converter phases, end up reflected in the low-voltage side current I_L. Previous literature has also focused on the evaluation of I_L and its evolution over time, resorting to strategies like slope analysis [5,13,14]. It is relevant to note that the proposed fault diagnostic method assures an important advantage over the diagnostic tools based on slope analysis, especially the tools applied to interleaved DC-DC converters. Considering that the diagnostic variable (input current) comprises the sum of multiple non-zero phase currents, with distinctive rising and falling slew rates overlapped in time, it is generally stated that the implementation of a diagnostic tool based on the slope analysis of the input current requires a complex and detailed analysis of many distinctive operating conditions. The adoption of a diagnostic tool based on the second-order derivative greatly simplifies the developed analysis. The overlap on time of phase current with distinctive slew rates does not impact the second-order derivative. Instead, the second-order derivative only extracts relevant information from the diagnostic variable during the switches transient states, observed as a result of the switching action.

The action of the proposed fault diagnostic solution lies on the evaluation of the magnitude of d^2I_L/dt^2, in well-defined periods. Naturally, the computation of d^2I_L/dt^2 involves significant processing effort. To simplify the computation process, while allowing the integration of the strategy in a DSP, d^2I_L/dt^2 is estimated through the Euler backward approximation method, resulting in:

$$\frac{d^2I_L}{dt^2} \approx \ddot{I}_L = \frac{I_L(t_2) - 2I_L(t_1) + I_L(t_0)}{\Delta t^2} \tag{19}$$

with $\Delta t = t_2 - t_0$.

The instants $t_{0\ldots2}$ are established resorting to the gating signals applied to the converter. Figure 5 illustrates the positions of these three instants, when analysing the gating signal q_{1d}, associated to IGBT Q_{1d}.

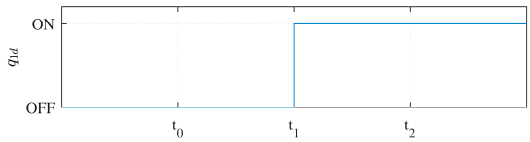

Figure 5. Identification of the instants for sampling the current I_L.

Since the response of the physical system is affected by delays, delay compensation is introduced. The compensation aims to account for the delay observed between the considered gating signals and the effective beginning/ending of the conduction/blocking of the semiconductors. Such compensation is considered through careful selection of the period between instants $t_{0\ldots2}$.

To identify the faulty semiconductor, the gating signals, available in the converter controller, are used along with the information of the d^2I_L/dt^2 to locate the faulty semiconductor. Figure 6 depicts a schematic representation of the entire fault diagnostics algorithm.

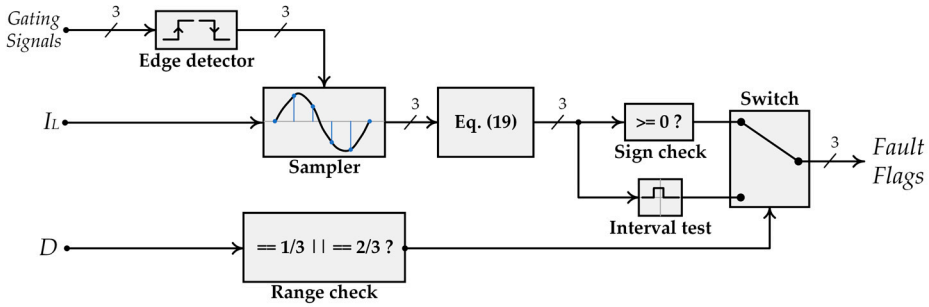

Figure 6. Schematic representation of the proposed fault diagnostics algorithm.

4. Simulation Results

To verify the effectiveness of the fault diagnostic algorithm proposed in this paper, simulations were carried out using MATLAB/Simulink™ R2023a software. The converter controller is based on a dual-loop PI controller. The converter operates using an asynchronous switching pattern, which implies that only IGBTs Q_{1d}, Q_{2d} and Q_{3d} are operated when the converter is in boost mode, whereas only IGBTs Q_{1u}, Q_{2u} and Q_{3u} are operated when the converter is in buck mode. This system is based on a real laboratory implementation of a non-isolated bidirectional interleaved DC-DC converter.

The main parameters used in this simulation are summarised in Table 3.

Table 3. System parameters.

Left-side voltage (V_L)	48 V
Right-side voltage (V_H)	{70, 90} V
Inductance (L_i)	{4, 10} mH
Output capacitance (C_H)	680 µF
Load resistance (R_L)	{50, 100} Ω
Switching frequency (f_{sw})	{2.5, 5} kHz
Simulation sampling time (T_s)	5 µs

The following results, which concern the converter operation in boost mode, aim to confirm the feasibility of the proposed approach in multiple operating conditions, namely in the presence of various levels of duty cycle D, conduction modes (expressed through parameter D_M), and switching frequencies f_{sw}, as well as transient state conditions.

Figure 7 depicts the evolution, in time, of the most relevant DC-DC converter and fault diagnostic variables, when the converter operates in DCM.

The converter operates in the region $0 < D < 1/3$, at a switching frequency f_{sw} of 2.5 kHz. The load resistance is 100 Ω, the phase inductance is 4 mH, and the converter output voltage V_H is 70 V.

The OC fault condition, which takes place at t = 2.00036 s, translates into a noticeable unbalance in the current I_L—see Figure 7b.

Referring to Figure 7c,d, which represent the second-order derivatives computed at the falling and rising edges of the gating signals, it is stated that both indicators provide accurate information about the faulty phase. Nonetheless, it is observed that faulty phase is identified quicker when evaluating the falling edges. Indeed, it is noticeable that the fault indicator computed resorting to information sampled at the falling edges (see Figure 7d) responds faster than the fault indicator computed resorting to information sampled at the rising edges (see Figure 7c). Therefore, the three diagnostic variables $\left(\ddot{I}_{L_1} \ldots \ddot{I}_{L_3}\right)$ presented in the following analyses are computed around the turn-off instants of each

converter phase. The diagnostic variable related to phase 1 of the converter (denoted as $\ddot{I}_{L_1}$ in Figure 7c,d) provides relevant information about the condition of switch Q_{1d}. Under healthy condition, $\ddot{I}_{L_1}$ oscillates around -2×10^8; after the fault, $\ddot{I}_{L_1}$ suddenly approaches zero, allowing an effective fault signaling at $t = 2.0008$ s. On the other hand, the evolution of the fault indicators related to phases 2 and 3 remains steady and unaffected by the fault. Such behaviour suggests the robustness of the approach against false positives.

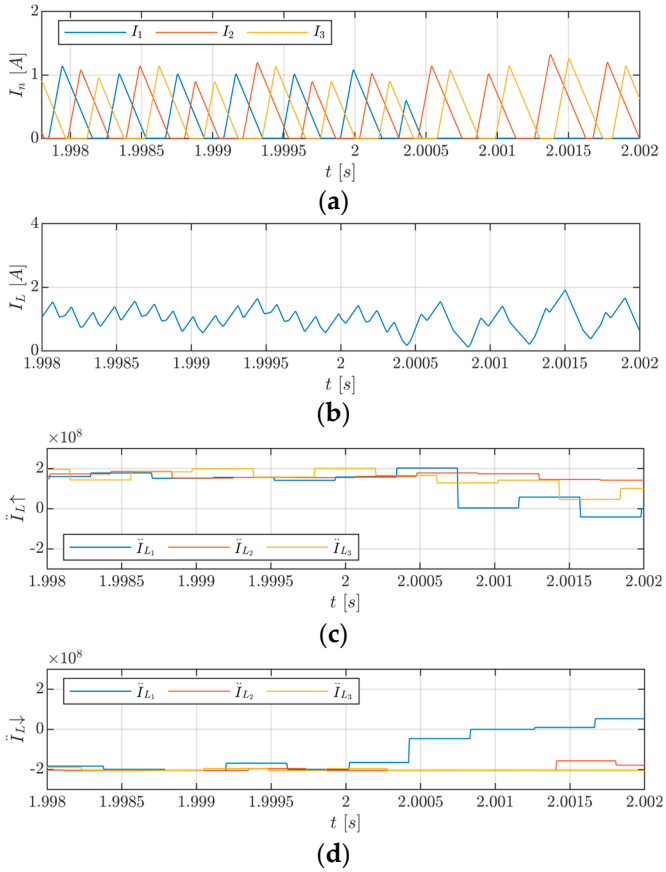

Figure 7. Evolution of the most relevant converter variables when an OC fault occurs in power switch Q_{1d}, at $t = 2.00036$ s: (**a**) phase currents $I_{1\ldots3}$; (**b**) low-voltage side current I_L; (**c**) second-order derivatives $I_{L1\ldots3}$, computed at the rising edges of the gating signals; (**d**) second-order derivatives $I_{L1\ldots3}$, computed at the falling edges of the gating signals.

Figure 8 evaluates the performance of the proposed approach for steady state condition, when the duty cycle D increases.

The converter operates in the region $1/3 < D < 2/3$, at a switching frequency f_{sw} of 2.5 kHz. The load resistance is 100 Ω, the phase inductance is 4 mH and the converter output voltage V_H is 90 V.

Because of the increment in the duty cycle D, the ripple content of the current I_L is greatly reduced, as seen in Figure 8b. This means that the effective diagnostic action may also reveal more demanding. As stated in Figure 8c, all three fault diagnostic indicators remain negative for healthy condition. After the OC fault in IGBT Q_{1d}, which takes place at $t = 2.00036$ s, $\ddot{I}_{L_1}$ suddenly increases to 3×10^8, allowing an effective fault signaling at $t = 2.00049$ s. The fault is diagnosed within 130 µs, representing 32.5% of the switching period. The evolution of the three fault diagnostic variables suggests the feasibility of the proposed solution.

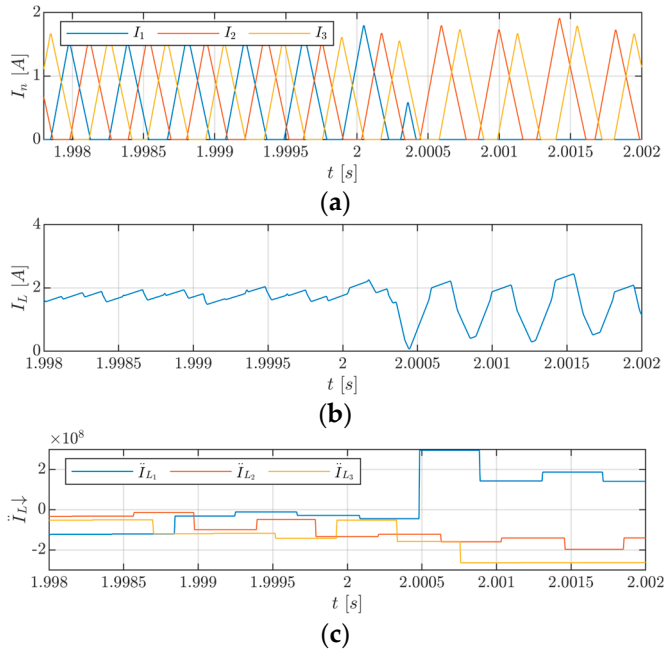

Figure 8. Evolution of the most relevant converter variables when OC fault occurs in power switch Q_{1d}, at t = 2.00036 s: (**a**) phase currents $I_{1\ldots3}$; (**b**) low-voltage side current I_L; (**c**) second-order derivatives $I_{L1\ldots3}$, computed at the falling edges of the gating signals.

The good indicators of the algorithm are extended to scenarios where either boundary conduction mode (BCM) or continuous conduction mode (CCM) are observed—see Figure 9a.

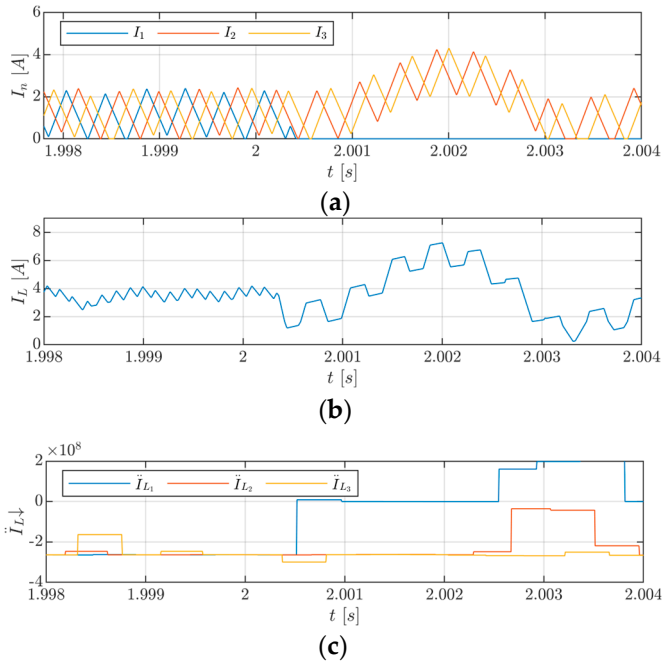

Figure 9. Evolution of the most relevant converter variables when OC fault occurs in power switch Q_{1d}, at t = 2.00036 s: (**a**) phase currents $I_{1\ldots3}$; (**b**) low-voltage side current I_L; (**c**) second-order derivatives $I_{L1\ldots3}$, computed at the falling edges of the gating signals.

The converter operates in the region $1/3 < D < 2/3$, at a switching frequency f_{sw} of 2.5 kHz. The load resistance is 50 Ω, the phase inductance is 4 mH and the converter output voltage V_H is 90 V.

As stated in Figure 9c, all three fault diagnostic indicators have fairly constant negative values during healthy condition. After the OC fault in IGBT Q_{1d}, which takes place at $t = 2.00036$ s, $\ddot{I}_{L_1}$ becomes positive, allowing an effective fault signaling at $t = 2.00052$ s. The fault is diagnosed within 160 µs, representing 40% of the switching period.

The tests also involved an evaluation of the method at higher switching frequency. The results of the evaluation are presented in Figure 10.

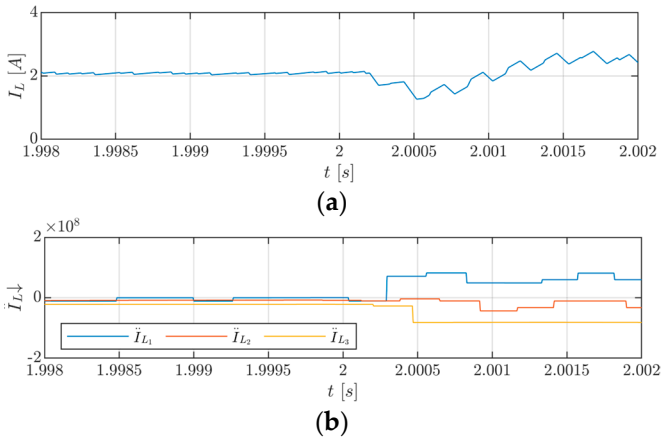

Figure 10. Evolution of the most relevant converter variables when OC fault occurs in power switch Q_{1d}, at $t = 2.00021$ s: (**a**) low-voltage side current I_L; (**b**) second-order derivatives $I_{L1\ldots3}$, computed at the falling edges of the gating signals.

The converter operates in the region $0 < D < 1/3$, at a switching frequency f_{sw} of 5 kHz. The load resistance is 100 Ω, the phase inductance is 10 mH and the converter output voltage V_H is 70 V.

The increment in the switching frequency f_{sw}, allied to the increment of the phase inductance, contribute to the smooth pattern of the current I_L during healthy converter condition—see Figure 10b. Because of this, all three fault diagnostic indicators remain negative, but close to zero when the converter is healthy. After the OC fault in IGBT Q_{1d}, which takes place at $t = 2.00021$ s, $\ddot{I}_{L_1}$ suddenly increases to 0.7×10^8, allowing an effective fault signaling at $t = 2.00030$ s. The fault is diagnosed within 90 µs.

To confirm the effectiveness under transient-state conditions, both step load change and OC fault conditions were tested in a single scenario, whose results are provided in Figure 11. In this scenario, the load resistance is changed from 100 Ω to 50 Ω, creating a load transient at the instant $t = 2.5$ s. Later, at $t = 6.0003$ s, an OC fault occurs at IGBT Q_{1d}.

The converter operates in the region $1/3 < D < 2/3$, at a switching frequency f_{sw} of 2.5 kHz. The phase inductance is 10 mH and the converter output voltage V_H is 80 V. The effect of the load transient is noticed in current I_L, thanks to the increment of the current—see Figure 11a.

Referring to Figure 11b, where the three fault diagnostic variables are represented, it is noted that both load transient and OC fault impact the evolution of the diagnostic variables. Still, the differences in the evolution of these parameters are clear. While all three variables remain negative during the load transient event, the same is not observed during the OC fault event. After the OC fault in IGBT Q_{1d}, which takes place at $t = 6.00030$ s, $\ddot{I}_{L_1}$ suddenly increases to 3.1×10^7, allowing an effective fault signaling at $t = 6.00045$ s. The fault is diagnosed within 150 µs.

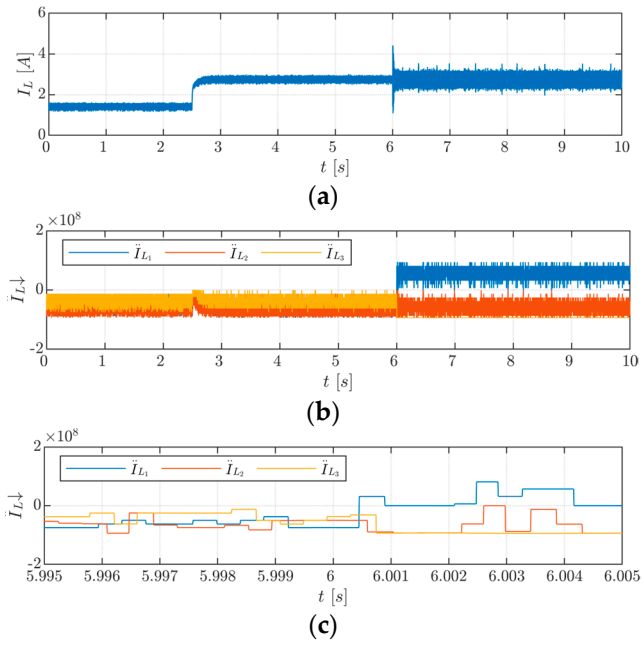

Figure 11. Evolution of the most relevant converter variables when OC fault occurs in power switch Q_{1d}, at t = 6.0003 s: (**a**) low-voltage side current I_L; (**b**) second-order derivatives $I_{L1\ldots3}$, computed at the falling edges of the gating signals; (**c**) zoomed view of the second-order derivatives $I_{L1\ldots3}$ around the OC fault instant.

5. Experimental Results

To confirm the accuracy of the simulation model and of the obtained simulation results, experimental tests were conducted on a laboratory prototype of the bidirectional interleaved DC-DC converter. The parameters of the experimental setup are the same as those reported in Table 3, which were also considered in simulation environment.

Figure 12 provides a schematic representation of the experimental setup used to test the converter operation and verify the effectiveness of the proposed fault diagnostics algorithm.

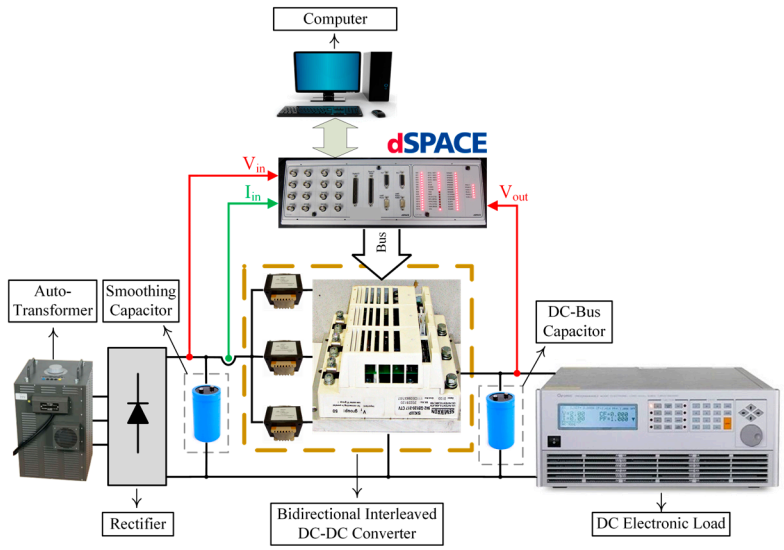

Figure 12. Schematic of the experimental assembly.

The following results address the operating conditions which have been evaluated in simulation context, i.e., steady- and transient-state conditions.

Figure 13 evaluates the performance of the proposed approach for steady-state conditions, when the converter operates in DCM.

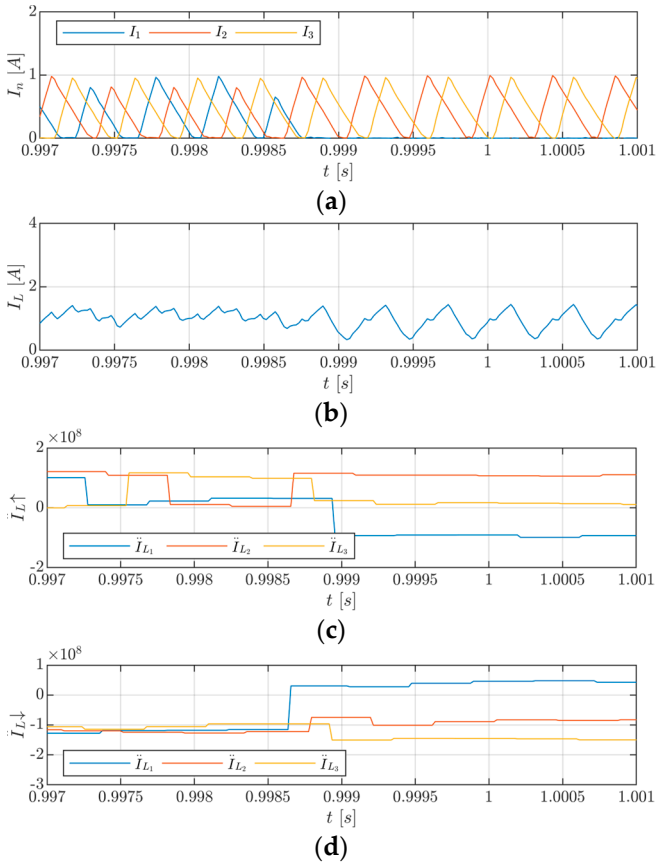

Figure 13. Evolution of the most relevant converter variables when an OC fault occurs in power switch Q_{1d}, at t = 0.99857 s: (**a**) phase currents $I_{1\ldots3}$; (**b**) low-voltage side current I_L; (**c**) second-order derivatives $I_{L1\ldots3}$, computed at the falling edges of the gating signals; (**d**) second-order derivatives $I_{L1\ldots3}$, computed at the rising edges of the gating signals.

The converter operates in the region $0 < D < 1/3$, at a switching frequency f_{sw} of 2.5 kHz. The load resistance is 100 Ω, the phase inductance is 4 mH and the converter output voltage V_H is 70 V.

The condition of discontinuous conduction is clear in Figure 13a, where the phase currents momentarily reach 0 A. Likewise, Figure 13b reveals the unbalance introduced in the sum of the phase currents, introduced after the OC fault in IGBT Q_{1d}.

The diagnostic variable related to phase 1 of the converter (denoted as $\ddot{I}_{L_1}$ in Figure 13c,d) provides relevant information about the condition of switch Q_{1d}. Under healthy condition, $\ddot{I}_{L_1}$ is -1.15×10^8; after the fault, $\ddot{I}_{L_1}$ becomes positive but nearing 0. This evolution, which aligns with the theoretical formulation provided in Table 1 for the specific combination of D and D_M, allows to diagnose the fault within 80 µs, at t = 0.99865 s. Also referring to the indicators related to phases 2 and 3, it is noted that their evolution remains steady, even after the fault. This suggests the robustness of the approach against false positives.

To verify the effectiveness of the approach when the duty cycle D increases, Figure 14 evaluates the performance of the proposed approach for steady state conditions, when the converter operates in DCM.

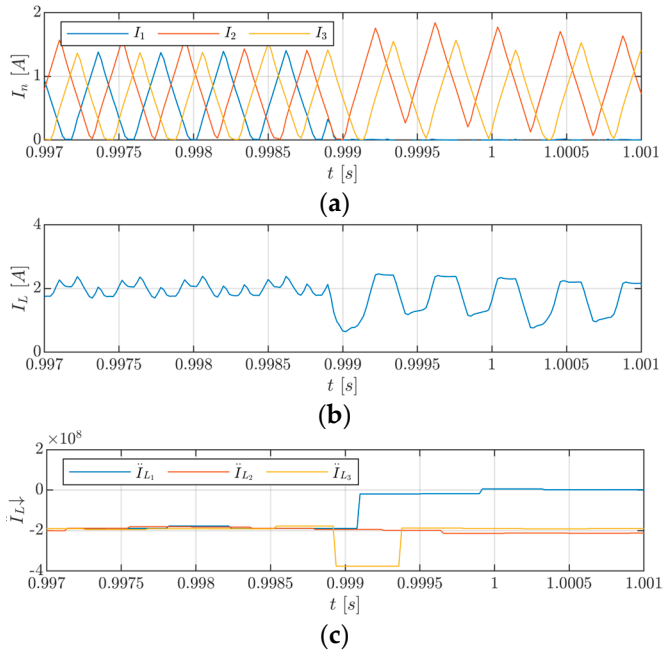

Figure 14. Evolution of the most relevant converter variables when OC fault occurs in power switch Q_{1d}, at t = 0.99890 s: (**a**) phase currents $I_{1\ldots3}$; (**b**) low-voltage side current I_L; (**c**) second-order derivatives $I_{L1\ldots3}$, computed at the falling edges of the gating signals.

The converter operates in the region $1/3 < D < 2/3$, at a switching frequency f_{sw} of 2.5 kHz. The load resistance is 100 Ω, the phase inductance is 4 mH and the converter output voltage V_H is 90 V.

Even though D_M approaches to the unitary value, the condition of discontinuous conduction is maintained in this scenario—see Figure 14a.

The diagnostic variable related to phase 1 of the converter (denoted as $\ddot{I}_{L_1}$ in Figure 14c) provides relevant information about the condition of switch Q_{1d}. Under healthy condition, all three diagnostic variables remain close to -2×10^8; after the fault, $\ddot{I}_{L_1}$ remains negative but nearing 0. This evolution in the diagnostic variable allows to diagnose the fault within 200 µs, at t = 0.99910 s.

To verify the effectiveness of the approach when the converter operates in CCM, Figure 15 evaluates the performance of the proposed approach for steady state conditions.

The converter operates in the region $1/3 < D < 2/3$, at a switching frequency f_{sw} of 2.5 kHz. The load resistance is 50 Ω, the phase inductance is 4 mH and the converter output voltage V_H is 90 V. In this scenario, continuous conduction mode is accomplished—see Figure 15a. The unbalance verified in the phase currents results from the asymmetry between phases and from the lack of a dedicated current balancing mechanism, which is not considered in this study. Given the non-ideal behaviour of the physical converter, associated to the presence of noise on the measurement of current I_L, the unbalance between phases or other non-idealities, will translate into minor deviations of diagnostic variables from the theoretical values, tabulated in Table 1.

Like in the previous scenarios, the diagnostic variable related to phase 1 of the converter (denoted as $\ddot{I}_{L_1}$ in Figure 15c) provides relevant information about the condition of switch Q_{1d}. Under healthy condition, all three diagnostic variables remain close to -2×10^8; after the fault, $\ddot{I}_{L_1}$ remains negative but nearing 0. This evolution in the diagnostic variable allows to diagnose the fault within 200 µs, at t = 0.99890 s.

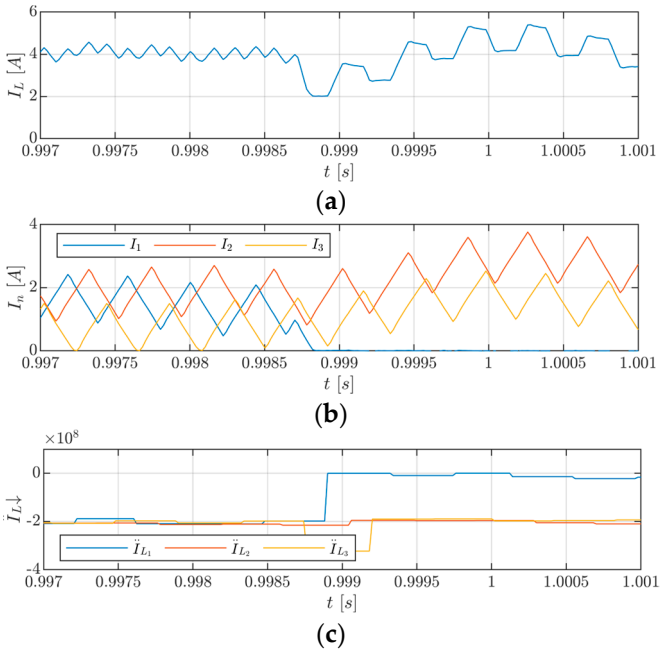

Figure 15. Evolution of the most relevant converter variables when OC fault occurs in power switch Q_{1d}, at t = 0.99870 s: (**a**) phase currents $I_{1\ldots3}$; (**b**) low-voltage side current I_L; (**c**) second-order derivatives $I_{L1\ldots3}$, computed at the falling edges of the gating signals.

The proposed approach also reveals effective when the switching frequency increases, as confirmed in Figure 16.

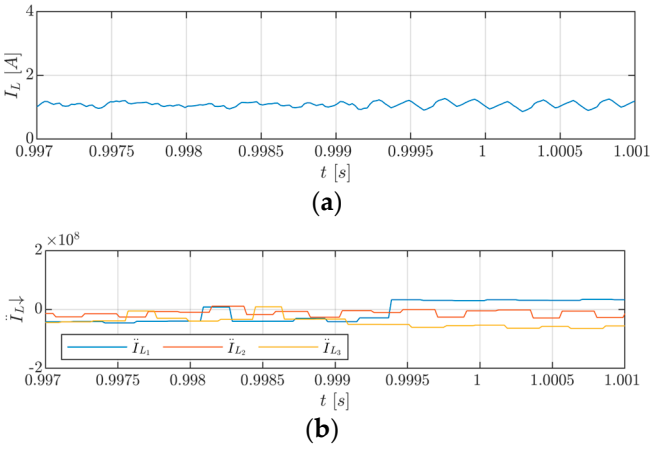

Figure 16. Evolution of the most relevant converter variables when OC fault occurs in power switch Q_{1d}, at t = 0.99911 s: (**a**) low-voltage side current I_L; (**b**) second-order derivatives $I_{L1\ldots3}$, computed at the falling edges of the gating signals.

The converter operates in the region $0 < D < 1/3$, at a switching frequency f_{sw} of 5 kHz. The load resistance is 100 Ω, the phase inductance is 10 mH and the converter output voltage V_H is 70 V. The effect of the higher switching frequency is noticed in current I_L, thanks to the lower ripple amplitude and higher ripple frequency—see Figure 16a.

Like in the previous scenarios, the diagnostic variable related to phase 1 of the converter effectively flags the OC fault at switch Q_{1d}. After the fault, $\ddot{I}_{L_1}$ becomes positive, standing out from the other two variables. This evolution in the diagnostic variable allows to diagnose the fault within 280 µs, at t = 0.99939 s.

To confirm the effectiveness under transient state condition, both step load change and OC fault conditions are tested in a single scenario, whose results are provided in Figure 17.

In this scenario, the load resistance is changed from 100 Ω to 50 Ω, creating a load transient at the instant t = 2.5 s. Later, at t = 5.99401 s, an OC fault occurs at IGBT Q_{1d}.

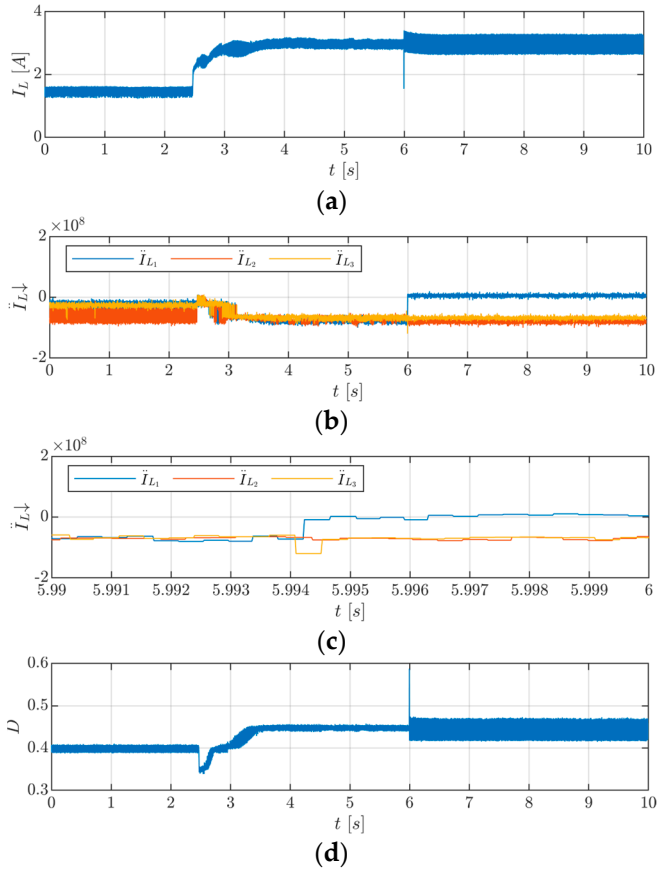

Figure 17. Evolution of the most relevant converter variables when OC fault occurs in power switch Q_{1d}, at t = 5.99461 s: (**a**) low-voltage side current I_L; (**b**) second-order derivatives $I_{L1\ldots3}$, computed at the falling edges of the gating signals; (**c**) zoomed view of the second-order derivatives $I_{L1\ldots3}$ around the OC fault instant; (**d**) duty cycle D.

The converter operates in the region $1/3 < D < 2/3$, at a switching frequency f_{sw} of 2.5 kHz. The phase inductance is 10 mH and the converter output voltage V_H is 80 V. The effect of the load transient is noticed in current I_L, thanks to the increment of the current—see Figure 17a.

Referring to Figure 17b, it is noted that all three diagnostic variables approach to zero, because of the load transient condition. This behaviour does not compromise the effectiveness of the solution, since the sign of the diagnostic variables remains negative. Indeed, when looking at the evolution of the duty cycle D, shown in Figure 17d, it is noted that this parameter approaches 1/3. Under such circumstance, the proposed fault diagnostic approach applies the exception that allows to fulfil the conditions expressed in Table 1 for cases where D approaches 1/3 and 2/3. Accordingly, no fault diagnostic flags are triggered.

Referring to Figure 17c, it is observed that $\ddot{I}_{L_1}$ becomes positive, standing out from the other two fault diagnostic variables, at t = 5.99425 s.

Comparison with the State of the Art

Table 4 compiles information considered useful in evaluating the performance of the fault diagnostic algorithms available in the literature, particularly those intended for DC-DC converters. It is worth noting that the performance metrics shown in Table 4 solely take into consideration the data provided by the authors in their corresponding communications.

Table 4. Comparative analysis of the fault diagnostic strategies available in the literature.

Ref.	Target Converter Topologies	Diagnostic Variable	f_{sw} (1)	T_s (2)	t_{d_max} (3)	t_{d_max}/T_s (4)
[17]	DC-DC converters for PV applications	PV variables	5 kHz	50 µs	250 ms	5000
[6]	Interleaved boost converter	Input current derivative sign	1 kHz	25 µs, 50 µs	2 T_{sw} (5) (2 ms)	40
[44,45]	Non-isolated DC-DC converters	Inductor current emulation	{10, 20} kHz	10 µs	T_{sw} (100 µs, 50 µs)	5
[37]	Switching power converters	State estimation	10 to 20 kHz	100 µs	10 ms	100
[43]	Interleaved boost converters	Parameter identification	10 kHz	10 µs	T_{sw} (100 µs)	10
[13]	Interleaved boost converters	Input current slope	{1, 3, 5} kHz	20 µs	2 T_{sw} (400 µs)	20
[11]	Interleaved boost converters	Input current sampling	20 kHz	16.7 µs	2 T_{sw} (100 µs)	6
[24,25]	Non-isolated DC-DC converters	Diode voltage monitoring	50 kHz	-	T_{sw} (20 µs)	-
[39]	Boost converters	Luenberger observer	10 kHz	10 µs	T_{sw} (100 µs)	10
[36]	Interleaved buck converters	State observer	25 kHz	0.67 µs	2 T_{sw} (80 µs)	119.4
[41]	IPOS boost converters	I&I observer for input voltage	25 kHz	20 µs	2 T_{sw} (80 µs)	4
[46]	Four-switch buck-boost converter	Digital twin	50 kHz	2 µs	201 T_{sw} (4.03 ms)	2015
Proposed	Bidirectional interleaved converters	Second-order current derivative	{2.5, 5} kHz	20 µs	T_{sw} (200 µs)	10

Nomenclature: (1) f_{sw}—switching frequency; (2) T_s—fault signatures sampling time; (3) t_{d_max}—maximum fault diagnostic time; (4) t_{d_max}/T_s—lowest ratio between maximum fault diagnostic time and sampling time; (5) T_{sw}—switching period ($T_{sw} = 1/f_{sw}$).

As stated in Table 4, the proposed diagnostic strategy provides remarkable capabilities to diagnose faults in a short period of time, while requesting a small computational effort. When compared to the state-of-the-art fault diagnostic strategies, the proposed diagnostic strategy reaches one of the lowest ratios between the maximum fault diagnostic time and sampling time. Such performance lies on the fact that the proposed fault diagnostic algorithm resorts to simple manipulation of the converter variables and their values, without requiring complex mathematical computations or emulation of the converter model.

6. Conclusions

The adoption of DC-DC converters is becoming increasingly important. Historically, DC-DC converters were mainly dedicated to industrial applications. However, these converters may become part of office equipment and home appliances soon, due to the increasing interest in DC microgrids for residential and offices buildings. In this context, ensuring high reliability and availability of power conversion solutions is of utmost importance. Therefore, significant attention should be paid to fault diagnostics in DC-DC power converters.

This paper presented a new fault diagnostic strategy capable of effectively diagnosing OC faults in the power switches of a multiphase non-isolated DC-DC converter. An approximation of the second-order derivative is applied to the converter input current, aiming to obtain fault signatures suitable to diagnose faults in any of the converter phases. Since the method synchronises the instants for sampling the converter input current with the gating signals, the risk of false fault alarms is obviated for the entire operating range of the converter. In addition, the synchronisation feature applied to the sampling operation promotes the effective diagnosis for converters with a high number of phases. The simplicity of the method also enables its transposition to many other DC-DC converter topologies.

Another advantage of the proposed approach is its ease of integration with existing control units. Because the proposed method only requires variables typically available as inputs or outputs of the control system (converter input current I_L, duty cycle D and gating signals), it can be implemented without altering the control architecture or extracting internal variables of the controller.

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