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# SEPIC-Boost-Based Unidirectional PFC Rectifier with Wide Output Voltage Range

**Hong Cheng, Xin Li *, Cong Wang, Zhihao Zhao, Yucheng Shen and Wei Yuan**

School of Mechanical and Electrical Engineering, China University of Mining and Technology-Beijing, Beijing 100080, China; chengh@cumtb.edu.cn (H.C.); wangc@cumtb.edu.cn (C.W.); bqt1900403012@student.cumtb.edu.cn (Z.Z.); sqt2200403054@student.cumtb.edu.cn (Y.S.); yuanwei@student.cumtb.edu.cn (W.Y.)

* Correspondence: liliana@student.cumtb.edu.cn; Tel.: +86-189-0964-6971

**Abstract:** A novel unidirectional hybrid PFC rectifier topology based on SEPIC and boost converters is proposed, which is applicable to various industrial applications such as electric vehicle charging stations, variable speed AC drives, and energy storage systems. Compared to other rectifiers, the proposed SEPIC-boost-based rectifier exhibits continuous current on the AC side, lower voltage stress on the active switches, a wider range of DC output voltage, no auxiliary DC-DC converters, and a high step-up static voltage gain operating with low input voltage and a low step-up static gain for the high-input-voltage operation. These traits allow the SEPIC-boost-based rectifier to utilize smaller input-side harmonic filtering inductors and adopt active switches with lower voltage ratings, resulting in reduced conduction losses. Additionally, the proposed rectifier features power factor correction and high boost/buck voltage-gain capabilities, simplifying control for electric vehicle charging and expanding its range of applications. In this paper, the operating principle of the novel topology is presented first, and then the mathematical model of the proposed rectifier is built. Based on this, the comparison between the proposed topology and conventional boost and SEPIC converters is given. Furthermore, the control strategy, including the high-power-factor control and the balancing control to the DC capacitor voltages, is discussed. Finally, to validate the accuracy of the proposed rectifier's theoretical research, a 500-W SEPIC-boost rectifier system has been constructed in the laboratory, generating a 200/120 $V_{dc}$ output voltage from a 155 $V_{pk}$/50 Hz power source.

**Keywords:** hybrid PFC rectifier; step-up and step-down functions; high power factor; balancing control of DC capacitor voltages



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## 1. Introduction

With the growing utilization of power electronic equipment, active power factor correction (PFC) has become indispensable for various power supplies and renewable energy systems available in the market today. This is particularly evident in various power supplies and renewable energy systems available today, including photovoltaic systems, fuel cell stacks, energy storage systems, and electric vehicle charging stations [1–8]. For power supplies with certain power rating, a front-end PFC converter is essential to provide a higher power factor (PF) and reduce the total harmonic distortion (THD) to meet the harmonic current and PF requirements, such as IEC61000-3-2 [9].

Boost-type converters are widely used as active PFC rectifiers in conventional rectifiers due to their simple structure, low cost, and excellent performance in terms of efficiency and power factor. However, as the required voltage gain becomes higher, conventional boost converters that change their step-up gain by adjusting the duty cycle are no longer suitable. This is because high voltage gain will result in a duty cycle close to 1, leading to high losses including switching losses and diode reverse recovery losses. Additionally, the voltage stress of active switches is comparatively large under the higher output voltage

occasions; in this case, the conventional boost converter no longer satisfies the above demand. Therefore, in practice, the voltage gain is commonly limited to lower than 5.

To overcome these limitations and achieve higher voltage gain, several enhanced boosting solutions have been proposed, including isolation transformers, switched capacitors, coupled inductors, and cascaded converters. However, isolation transformers, while capable of achieving step-up and step-down functions, have drawbacks such as significant weight, volume, and cost, making their design complex and expensive [10]. Switched capacitors offer advantages in terms of high-power density and the use of only power switches and clamped capacitors. Nonetheless, they suffer from high-current transients, which can reduce both power density and efficiency, limiting their application in some cases. Moreover, as the output voltage increases, the number of switched-capacitor stages also increases, requiring additional clamped capacitors, diodes, and current snubbers [11,12]. In recent years, coupled inductor-based have been good alternatives for high-voltage-gain converters in medium-power applications. The voltage gain is determined by the turn ratio of the coupled inductor. However, the inherent leakage inductance of coupled inductors can result in high voltage stress on the switches, leading to reduced system efficiency [13,14]. Considering the drawbacks mentioned above, cascaded boost converters have become an attractive choice, offering advantages such as high gain, simple structure, and low voltage stress [15–17]. By connecting two or more basic boost converters in cascade, a larger voltage gain can be achieved while reducing the voltage stress and switching losses. Nonetheless, the cascade boost converter will cause the energy to be processed multiple times, which reduces the system efficiency.

However, in certain specialized scenarios, there is a need for a wider range for the output voltage of the rectifier. These scenarios include specific power sources such as mining power supplies and adjustable DC power supplies, as well as electric vehicle charging stations, centralized battery charging stations, and energy storage systems [18,19]. Furthermore, there are countries with poor power quality, characterized by weak grid infrastructure and significant voltage fluctuations. In such cases, an active step-up and step-down PFC converter capable of accommodating a wide input voltage range is required [20]. Consequently, these industrial applications demand a continuously adjustable output voltage over a wide range to enable high step-up static gain operation at low input voltage and low step-up static gain operation at high input voltages. However, traditional cascaded boost PFC converters no longer meet these requirements, as their DC-link bus voltage must be higher than the maximum input peak voltage to ensure proper rectifier operation.

To overcome these challenges, much research has been conducted and several typical topologies have been presented in a number of technical studies. On the other hand, buck-type PFC rectifiers offer the possibility of voltage step-down. However, they lack a pure sinusoidal input current due to the appearance of the dead zones within the waveform when the instantaneous input voltage is below the output DC voltage [21]. Consequently, buck PFC rectifiers often exhibit limited PF and high current distortion, making it difficult to comply with current harmonic requirements, particularly in lighting applications [22]. Furthermore, a modified SEPIC converter was proposed in [23] to achieve low-switch-voltage operation and high static gain at low line voltages. However, in order to reduce active switch voltage stress, this modified structure is unable to operate with an output voltage lower than the input voltage, thereby limiting the adjustable range of the output voltage. The authors of [24] proposed a voltage-double high-power factor SEPIC rectifier for higher output voltage applications, which causes reduced voltage stress on the semiconductors for the same output voltage level or supplies double the gain of the output voltage with the same voltage stress. However, this kind of converter cannot achieve low step-up static gain at higher input voltage application, which is not applied to wide input voltage occasions. Meanwhile, the static gain of a SEPIC rectifier is lower than that of a boost converter under boost conditions, and the voltage stress of active switches is higher than that of dual boost converters.

To address the aforementioned issues, this paper proposes a novel unidirectional hybrid rectifier based on SEPIC and boost converters, which is utilized to obtain a high step-up static voltage gain operating with low input voltage and a low step-up static gain for the high-input-voltage operation. The objective of the hybrid PFC rectifier is to combine the advantages of the boost converter and SEPIC converter to achieve a wide range of continuously adjustable output voltage and in particular to further improve their performance at low input voltage.

The structure of this paper is as follows. Section 2 presents the basic principles of the proposed rectifier, including the topology configuration, the steady-state mathematical model, and the comparison of step-up and step-down functions. On this basis, double closed loop control strategy is presented, with emphasis on the DC capacitor voltage control and the high power factor control in Section 3. Simulation and experimental results are provided in Section 4 to verify the validity of the proposed topology and theoretical findings. Finally, the conclusions are summarized in Section 5.

## 2. Analysis of the Operating Principles of the Novel Topology

### *2.1. Configuration of the Novel Topology*

Figure 1 shows the proposed novel unidirectional hybrid single-phase rectifier topology, in which $S_i$ and $D_i$ ($i$ = 1, 2) are active switches and fast recovery diodes, respectively. Each of the active switches $S_i$ can operate in two states: "on" corresponds to the "1" state, while "off" corresponds to the "0" state, and $d_1$ and $d_2$ are the duty cycles of $S_1$ and $S_2$, so two active switches with different states will have a total of four operating modes from (0, 0) to (1, 1). $v_{o1}$, $v_{o2}$ and $v_b$ denote the voltages of capacitors $C_{o1}$, $C_{o2}$ and $C_b$, respectively; $v_o$, $v_s$ and $v_i$ represent the DC-link voltage, the power supply voltage and the AC input voltage of the diode rectifier, respectively. $i_{L1}$ and $i_{L2}$ denote the currents of inductors $L_1$ and $L_2$, and $R_1$ and $R_2$ are the equivalent resistance of load. It should be noted that in Figure 1, $v_o$, $v_{o1}$, $v_{o2}$, $v_s$, $v_i$, $v_b$, and $i_{L1}$ are all the average variables in one switching cycle, which are defined by:

$$x = \langle x(t) \rangle_{T_S} = \frac{1}{T_S} \int_0^{T_s} x(t)dt, x = v \text{ or } i \tag{1}$$

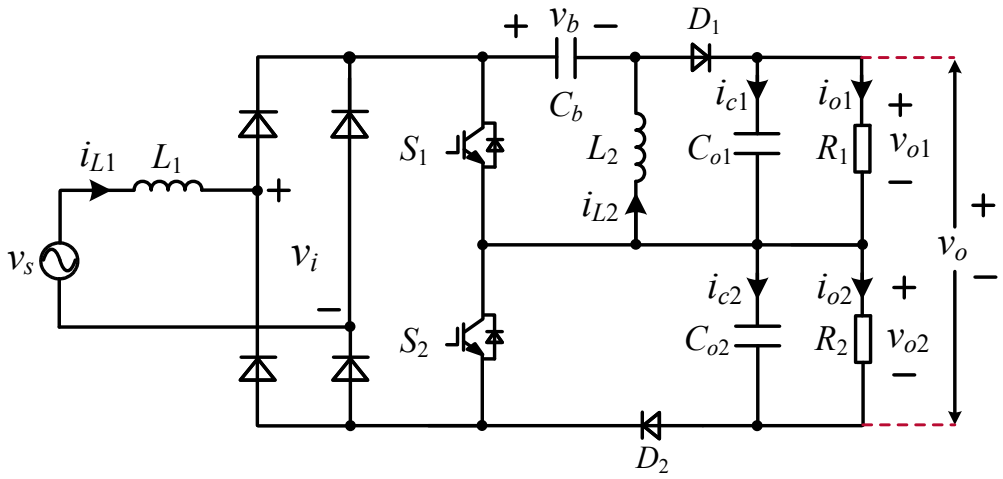



**Figure 1.** The proposed unidirectional hybrid single-phase rectifier topology.

To simplify the analysis, only the positive half period of the input current $i_{L1}$ will be taken as an example to carry out the following discussion. Assuming that the circuit shown in Figure 1 is operating in continuous conduction mode (CCM), all the operating modes and corresponding current flowing paths are shown in Figure 2, and relevant electrical waveforms are showcased in Figure 3.

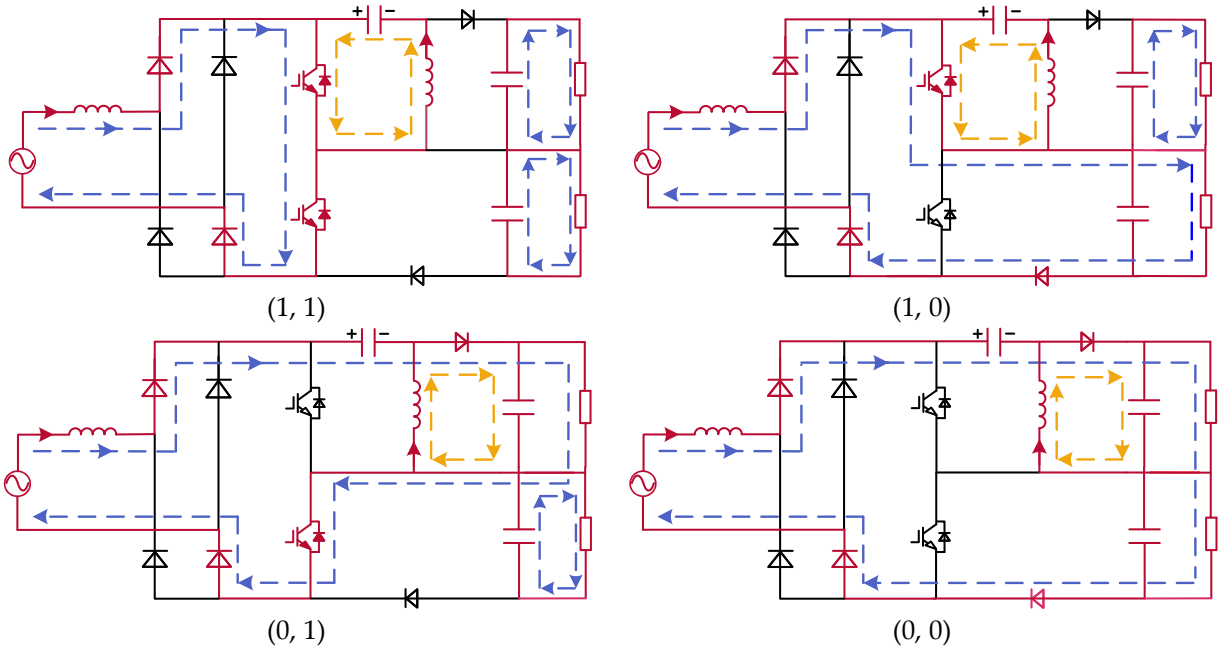



**Figure 2.** All the operating modes and the corresponding current flowing paths of the rectifier.

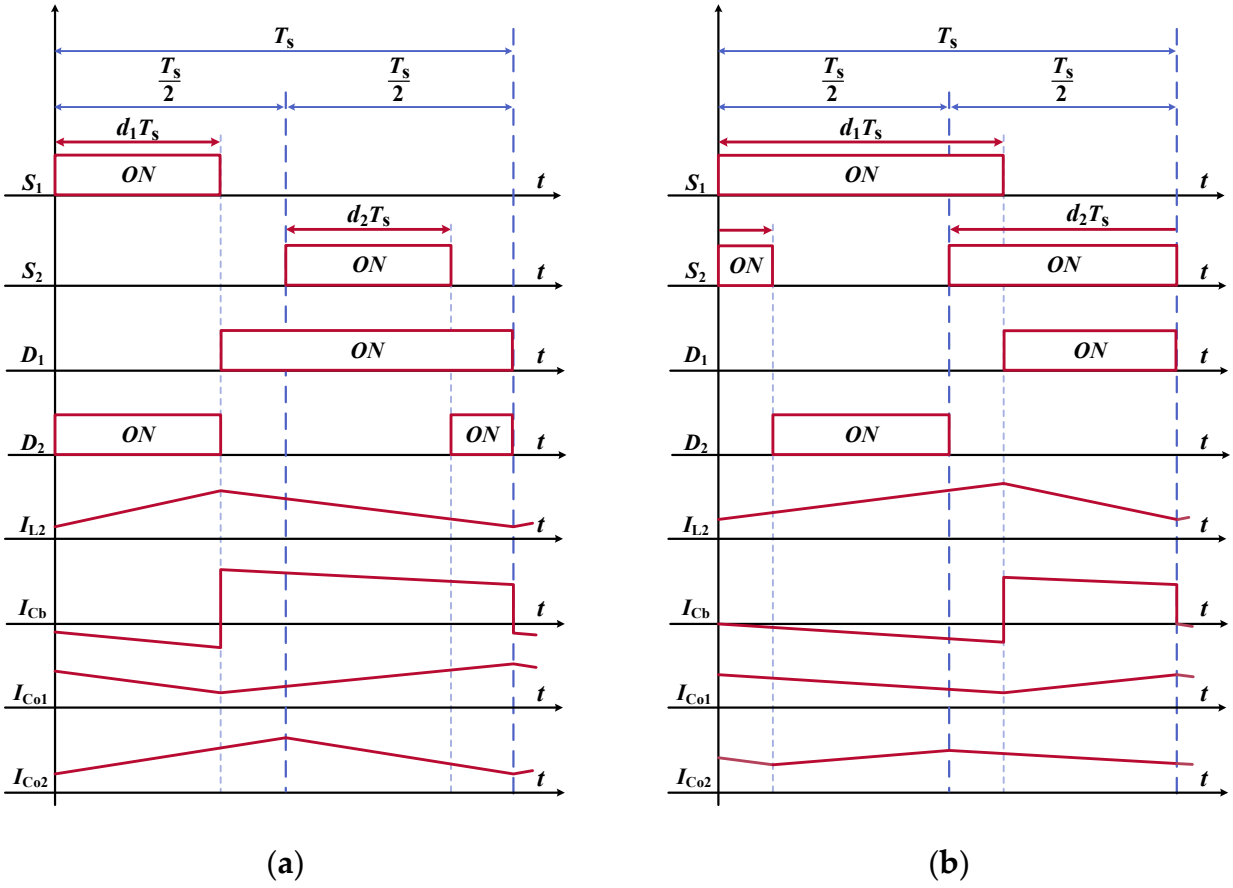



**Figure 3.** Main waveforms of the proposed rectifier: (**a**) $0 < d < 0.5$; (**b**) $0.5 \leq d < 1$.

In each operating mode, the branch currents will flow in different paths; correspondingly, the capacitors $C_{o1}$, $C_{o2}$, and $C_b$ and the inductors $L_1$ and $L_2$ will be in the status of charging or discharging. For example, when the circuit operates in mode (1, 0) as shown

in Figure 2, $S_1$ is in the "on" state, but $S_2$ is in the "off" state. Correspondingly, the split capacitor $C_{o1}$ is in the discharging state and the split capacitor $C_{o2}$ is in the charging state. Meanwhile, the capacitor $C_b$ is in the discharging state and the inductor $L_2$ is in the charging state. In summary, the operating status of $C_{o1}$, $C_{o2}$, $C_b$, and $L_2$ and the input voltage $v_i$ of the diode rectifier are all summarized in Table 1.

**Table 1.** The operating status of $C_{o1}$, $C_{o2}$, $C_b$, and $L_2$ and the input voltage $v_i$ of the diode rectifier.

| Modes | $S_1$ | $S_2$ | $L_2$ | $C_b$ | $C_{o1}$ | $C_{o2}$ | $v_i$ |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | C | D | D | D | 0 |
| 2 | 1 | 0 | C | D | D | C | $v_{o2}$ |
| 3 | 0 | 1 | D | C | C | D | $v_{o1} + v_b$ |
| 4 | 0 | 0 | D | C | C | C | $v_{o1} + v_{o2} + v_b$ |

[1] "C" denotes "charging" status and "D" denotes "discharging" status.

### 2.2. Mathematical Modeling

Applying KVL and KCL to the topology shown in Figure 1 yields the following mathematical model:

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = v_s - (1-d_1)(v_b + v_{o1}) - (1-d_2)v_{o2} \\ L_2 \frac{di_{L2}}{dt} = (1-d_1)v_{o1} - d_1 v_b \\ C_b \frac{dv_b}{dt} = i_{L1}(1-d_1) - d_1 i_{L2} \\ C_{o1} \frac{dv_{o1}}{dt} = i_{c1} = (i_{L1} + i_{L2})(1-d_1) - i_{o1} \\ C_{o2} \frac{dv_{o2}}{dt} = i_{c2} = i_{L1}(1-d_2) - i_{o2}. \end{cases} \tag{2}$$

Considering that the proposed rectifier is connected with a conventional three-level neutral point clamped (NPC) converter, the control target of the DC capacitor voltages $v_{o1}$ and $v_{o2}$ at the steady state is determined as

$$v_{o1} = v_{o2} = \frac{v_o}{2} \tag{3}$$

In a switching cycle, the input current $i_{L1}$ is considered as a constant value. Based on the volt-second balance principle, substituting (3) into (2), the following relationship can be obtained:

$$\begin{cases} v_b = \frac{1-d_1}{d_1} v_{o1} = \frac{1-d_1}{d_1} \frac{v_o}{2} \\ \lambda = \frac{v_o}{v_s} = \frac{2d_1}{1-d_1 d_2} \end{cases} \tag{4}$$

where $\lambda$ is the voltage transfer ratio of proposed rectifier. Combining (4) and Figure 1, the corresponding voltage stress $v_{s1}$ and $v_{s2}$ of $S_1$ and $S_2$ can be deduced as

$$\begin{cases} v_{s1} = v_b + v_{o1} = \frac{1-d_1}{d_1} \frac{v_o}{2} + \frac{v_o}{2} = \frac{v_o}{2d_1} \\ v_{s2} = v_{o2} = \frac{v_o}{2} \end{cases} \tag{5}$$

Equation (5) shows that compared to the dual SEPIC converter, the proposed hybrid rectifier has an active switch $S_2$ with lower voltage stress.

Since the proposed rectifier is a buck-boost rectifier and (4) gives the relationship between the voltage transfer ratio $\lambda$ and the duty cycles $d_1$ and $d_2$, the boundary of boost and buck function can be deduced as

$$\lambda = \frac{v_o}{v_s} = \frac{2d_1}{1-d_1 d_2} = 1 \Rightarrow d_2 = \frac{1}{d_1} - 2 \tag{6}$$

As shown in Figure 4, the voltage conversion ratio varies with the duty cycles $d_1$ and $d_2$. It is seen from (6) that, to achieve the buck and boost function of the proposed rectifier, $d_1$ and $d_2$ should satisfy

$$0 < d_2 \leq \frac{1}{d_1} - 2(\text{Buck}), \frac{1}{d_1} - 2 < d_2 < 1(\text{Boost}) \tag{7}$$

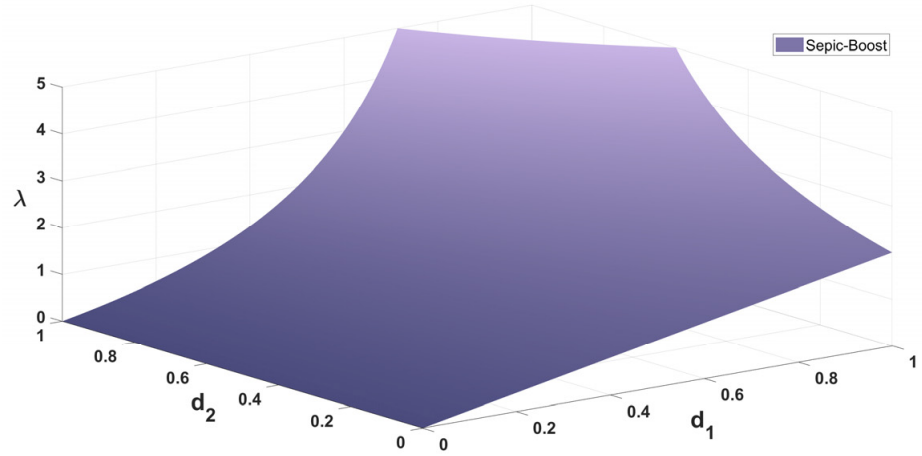


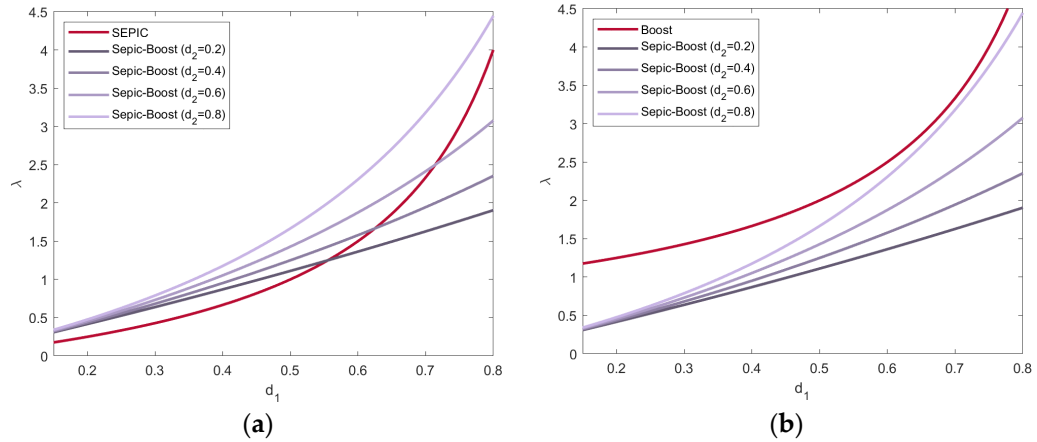

**Figure 4.** Voltage transfer ratio of the proposed rectifier $\lambda$.

The comparison between the proposed hybrid rectifier and other conventional rectifiers is as follows. The voltage transfer ratio $\lambda_p$ of a conventional SEPIC converter is given by

$$\lambda_p = \frac{d_1}{1 - d_1} \tag{8}$$

Figure 5a illustrates that the proposed rectifier starts to boost at a smaller duty cycle and achieves a larger boosting range by regulating $d_2$. In situations where the voltage transfer ratio $\lambda$ surpasses $\lambda_p$, a significant step-up in the static voltage gain can be achieved for higher output voltage scenarios. This condition is met when the following relationship holds true:

$$1 > \lambda = \frac{2d_1}{1 - d_1 d_2} > \lambda_p = \frac{d_p}{1 - d_p} \Rightarrow 2 - \frac{1}{d_1} < d_2 < 1 \tag{9}$$




(**a**) (**b**)

**Figure 5.** Comparison of voltage transfer ratio λ of the proposed rectifier: (**a**) with SEPIC rectifier; (**b**) with boost rectifier.

It can be concluded from (9) and Figure 5a that the proposed hybrid rectifier can achieve a higher step-up static voltage gain than a conventional SEPIC converter by regulating $d_2$.

The voltage transfer ratio $\lambda_b$ of a conventional boost converter is given by

$$\lambda_b = \frac{1}{1 - d_1} \tag{10}$$

Based on (6) and (10), the comparison diagram between $\lambda$ and $\lambda_b$ is indicated in Figure 5b. It can be concluded from Figure 5b that the voltage transfer ratio $\lambda_b$ of the conventional boost converter is larger than $\lambda$ of the proposed rectifier. In all duty cycle ranges, $\lambda_b$ remains greater than 1, rendering the traditional boost converter unsuitable for applications requiring lower output voltage or higher input voltage. Conversely, the proposed topology exhibits the voltage transfer ratio $\lambda_b$ below 1, the low duty cycle range. This indicates that the output DC-link voltage can be set lower than the peak input voltage, making it particularly suitable for scenarios requiring lower output voltages or wider input voltage ranges. In order to ensure that the proposed topology operates in buck mode, the duty cycle $d_2$ should satisfy

$$0 < d_2 < \frac{1}{d_1} - 2 \tag{11}$$

It can be concluded from the above analysis that compared to the conventional boost and SEPIC converters, the proposed rectifier is especially effective for obtaining a high step-up static voltage gain operating with low input voltage and a low step-up static gain for the high input voltage operation, which is suitable for a wider range of input voltage applications.

## 3. Control Strategy of the Hybrid Rectifier

### *3.1. Double Closed-Loop Control Strategy*

The control strategy discussed in this section should be able to achieve the following basic goals, which include keeping the DC capacitor voltages in balance, controlling the DC-link voltage constant at a given value, and achieving the high input power factor of the rectifier. To achieve these control goals, a combined control strategy of a voltage outer loop based on a PI controller and a current inner loop based on a PR controller is adopted in this paper. The block diagram of the double closed-loop control strategy is shown in Figure 6. The outer voltage loop is utilized to maintain the DC output voltage constant by employing a PI controller. The output signal of the voltage loop is taken as the input current reference of the current inner loop. With help of the phase-locked loop, the reference current signal output by the outer loop voltage controller can be expressed as

$$i_{L1}^{*} = \left[k_{pv}(v_o^{*} - v_o) + k_{iv}\int (v_o^{*} - v_o)dt\right]\frac{v_s}{V_m}\sin(\omega t + \varphi) \tag{12}$$

where $k_{pv}$ is the proportional gain and $k_{iv}$ denotes the integrational gain. $V_m$ and $\varphi$ are the amplitude and phase information of the power supply voltage, respectively, and $\omega$ is the rotational angular frequency of the power supply voltage.

The inner current loop is adopted to control the input current by taking advantage of the proportional-resonance (PR) control to accurately track the AC reference current signal and ensure that it is in phase with the power supply voltage [25]. The transfer function of the PR controller is as follows:

$$G_i(s) = k_{pi} + \frac{2k_r w_c s}{s^2 + 2k_r w_c s + w_o^2} \tag{13}$$

where $k_{pi}$ and $k_r$ are proportional gain and resonant gain, respectively, while $\omega_0$ and $\omega_c$ represent the resonant frequency and cut-off frequency. A block diagram of the double closed-loop control strategy transfer function is shown in Figure 7.

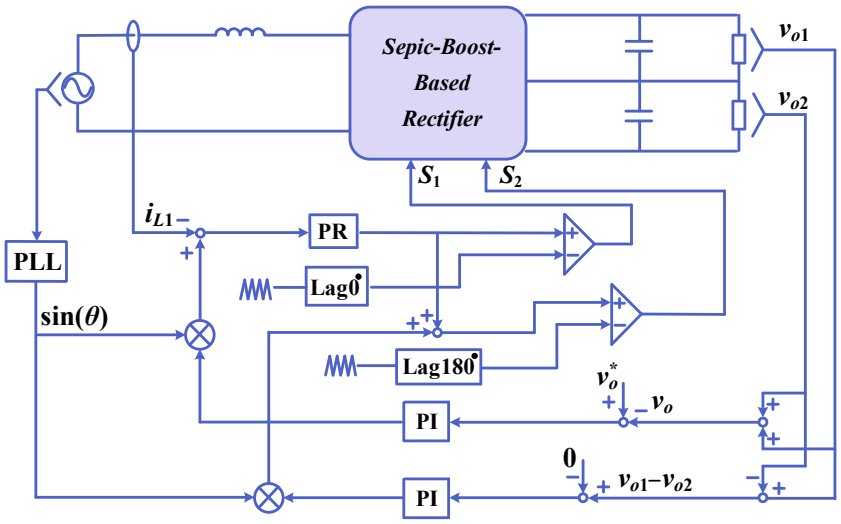



**Figure 6.** Diagram of the double closed-loop control strategy.

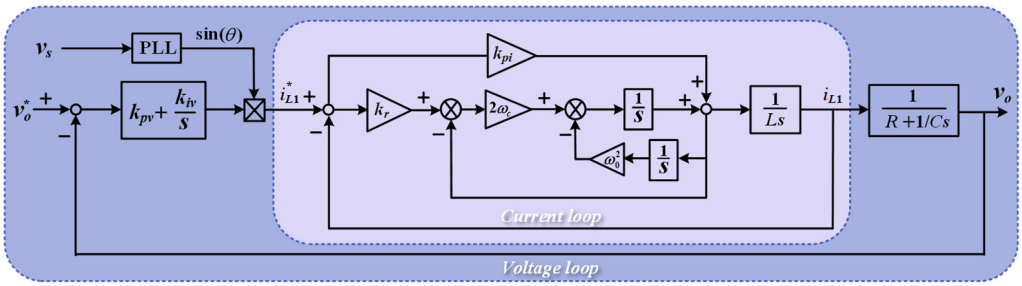



**Figure 7.** Block diagram of the system transfer function.

### *3.2. Balancing Control of the DC Capacitor Voltage*

The proposed rectifier consists of a SEPIC converter and a boost converter. Due to the different voltage transfer ratio between the boost converter and the SEPIC converter, if the additional DC capacitor voltage balancing control is not adopted, this will lead to the voltage unbalancing between $v_{o1}$ and $v_{o2}$. The detailed analysis is as follows.

It is seen from (2) in the previous section that the capacitor currents $i_{c1}$ and $i_{c2}$ of the DC side are given by

$$\begin{cases} i_{c1} = C_{o1}\frac{dv_{o1}}{dt} = (i_{L1}+i_{L2})(1-d_1) - i_{o1} \\ i_{c2} = C_{o2}\frac{dv_{o2}}{dt} = i_{L1}(1-d_2) - i_{o2}. \end{cases} \tag{14}$$

Based on the third line of (2), the inductor current $i_{L2}$ can be expressed as

$$i_{L2} = i_{L1}(\frac{1}{d_1} - 1) \tag{15}$$

Substituting (15) into (14), $i_{c1}$ and $i_{c2}$ can be deduced as

$$\begin{cases} i_{c1} = C_{o1}\frac{dv_{o1}}{dt} = i_{L1}(1/d_1 - 1) - i_{o1} \\ i_{c2} = C_{o2}\frac{dv_{o2}}{dt} = i_{L1}(1-d_2) - i_{o2}. \end{cases} \tag{16}$$

$d$ is defined as the duty cycle of the rectifier, which is employed to control the DC-link voltage. When the DC capacitor balancing control loops are disabled in the rectifier, $d_1$ and $d_2$ should satisfy

$$d = d_1 = d_2. \tag{17}$$

Substituting (17) into (16), (16) can be rewritten as

$$\begin{cases} i_{c1} = C_{o1}\frac{dv_{o1}}{dt} = i_{L1}(1/d-1) - i_{o1} \\ i_{c2} = C_{o2}\frac{dv_{o2}}{dt} = i_{L1}(1-d) - i_{o2}. \end{cases} \tag{18}$$

Since the average of $i_{c1}$ and $i_{c2}$ in a line-frequency cycle is equal to zero, based on (18), the relationship between the load current averages and the duty cycle $d$ can be expressed as

$$\begin{cases} \overline{i_{o1}} = \overline{i_{L1}(1/d-1)} \\ \overline{i_{o2}} = \overline{i_{L1}(1-d)} \end{cases} \tag{19}$$

where $i_{o1}$ and $i_{o2}$ can be considered as the constant values when $v_{o1}$ and $v_{o2}$ are in the steady state. However, when the duty cycle $d$ varies with time, due to $1/d-1 \neq 1-d$, which will also lead to the average of $i_{L1}(1/d-1)$ not equalling $i_{L1}(1-d)$, that is, $i_{o1} \neq i_{o2}$, and further affect the voltage balancing of $v_{o1}$ and $v_{o2}$ even under the balanced load, then, in order to achieve the voltage balancing between $v_{o1}$ and $v_{o2}$, the duty cycle variations $\Delta d_1$ and $\Delta d_2$ are added to $d_1$ and $d_2$, that is

$$d_1 = d + \Delta d_1, \text{and } d_2 = d + \Delta d_2 \tag{20}$$

Substituting (20) into (16), $i_{c1}$ and $i_{c2}$ can be rewritten as

$$\begin{cases} i_{c1} = i_{L1}(\frac{1}{d_1+\Delta d_1} - 1) - i_{o1} \\ i_{c2} = i_{L1}(1-d-\Delta d_2) - i_{o2}. \end{cases} \tag{21}$$

Based on the first and second lines of (2) in Section 2, the DC-link voltage $v_o$ can be deduced as

$$v_o = \frac{2v_s}{1/d_1 - d_2} \tag{22}$$

Under the balanced load, when the DC capacitor balancing control loops are disabled in the rectifier, substituting (17) into (22), $v_o$ can be rewritten as

$$v_o = \frac{2v_s}{1/d - d} \tag{23}$$

For the unbalanced load, when the duty cycle variations $\Delta d_1$ and $\Delta d_2$ are taken into consideration, substituting (20) into (22), $v_o$ can be deduced as

$$v_o = \frac{2v_s}{1/d - d + 1/(d+\Delta d_1) - 1/d - \Delta d_2}. \tag{24}$$

Combining (23) and (24), it can be concluded that the values of $\Delta d_1$ and $\Delta d_2$ will affect the balance of the DC-link voltage $v_o$, and in order to achieve the control decoupling from $v_o$, the duty cycle differences $\Delta d_1$ and $\Delta d_2$ should satisfy

$$\frac{1}{d+\Delta d_1} - \frac{1}{d} - \Delta d_2 = 0 \tag{25}$$

By simplifying (25), $\Delta d_1$ and $\Delta d_2$ should satisfy

$$\Delta d_1 = \frac{-d^2\Delta d_2}{1+\Delta d_2 d} = -d \times (1 - \frac{1}{1+\Delta d_2 d}). \tag{26}$$

It is seen from (26) that the relationship between $\Delta d_1$ and $\Delta d_2$ is nonlinear and complex. To simplify the control strategy, the value of $\Delta d_2 d$ is considered to be approximately zero. Correspondingly, the value of $\Delta d_1$ is equal to zero. Meanwhile, to avoid the effect of $\Delta d_2$

on $v_o$, the bandwidth of the DC capacitor voltage is set lower than the outer voltage loop, which will lead to $\Delta d_2 << d$.

When the DC-link voltage $v_o$ is controlled at the voltage reference, to achieve the voltage balancing between $v_{o1}$ and $v_{o2}$, the current difference between $i_{c1}$ and $i_{c2}$ is defined as $i_n$. Combining (21) and $\Delta d_1 = 0$, the current difference can be deduced as

$$i_n = i_{c1} - i_{c2} = i_{L1}[\frac{1}{d} - 1 - (1-d)] - i_{o1} + i_{o2} + \Delta d_2 i_{L1}. \tag{27}$$

Equation (27) indicates that the unbalanced DC capacitor current caused by $i_{o1} \neq i_{o2}$ or $i_{L1}(1/d - 1) \neq i_{L1}(1 - d)$ can be regulated by the duty cycle variation $\Delta d_2$. Thus, based on (27), the following relationship can be obtained:

$$C_{o1}\frac{dv_{o1}}{dt} - C_{o2}\frac{dv_{o2}}{dt} = \Delta d_2 i_{L1}. \tag{28}$$

Considering that the DC capacitors satisfy $C_{o1} = C_{o2} = C$, by applying the Laplace transformation to (28), the following dynamic equations are obtained

$$\Delta d_2(s) = \frac{v_{o1}(s) - v_{o2}(s)}{i_{L1}SC}. \tag{29}$$

Equation (29) shows that the duty cycle variation $\Delta d_2$ is responsible for controlling the balancing of the capacitor voltages $v_{o1}$ and $v_{o2}$, and the modulation index difference $\Delta m$ is utilized to generate $\Delta d_2$, where $k_{pd}$ and $k_{id}$ are the proportional gain and integrational gain of the DC capacitor voltages loop, respectively. In the controller of the DC capacitor voltage $v_{o2}$, $\Delta m$ is generated by the PI controllers and the basic control structure is shown in Figure 8.

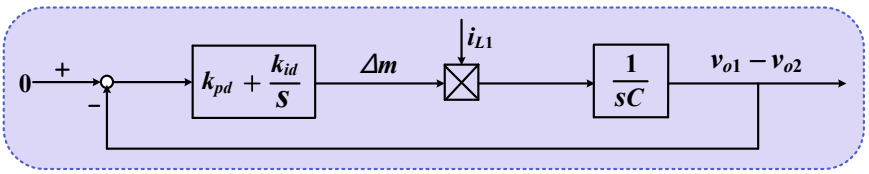



**Figure 8.** The basic control structure of the DC capacitor voltages loop.

## 4. Simulation and Experimental Verifications

To validate the proposed novel topology and its corresponding control strategy, simulations were conducted in the MATLAB/Simulink environment. Additionally, an experimental platform was set up, as illustrated in Figure 9.

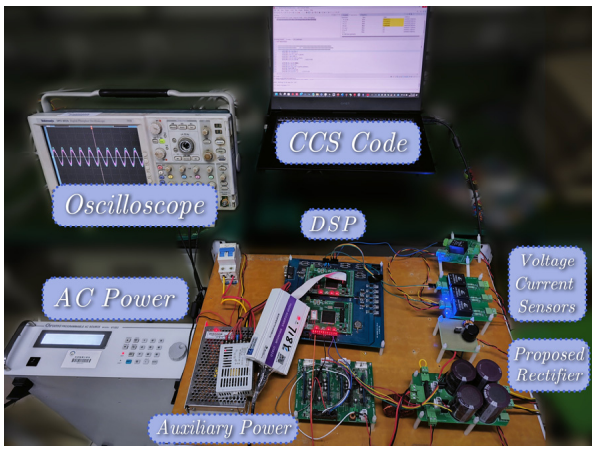



**Figure 9.** The experimental prototype.

Our experimental setup featured a TMS320F28335 DSP as the core controller, and the rectifier was constructed using discrete IGBTs (IKA10N60T) and diodes (VS-MUR820PBF). The Hall voltage sensor employed was VSM025A, and the Hall current sensor utilized was CSM005A. The key parameters utilized in both the simulation and experimental setup are listed in Table 2. The simulation waveforms of the proposed rectifier are presented in Figures 10–15.

**Table 2.** Ratings and circuit parameters.

| System Rating and Parameters | |
|---|---|
| power rating $P$ | 500 W |
| amplitude of phase-voltage $v_s$ | 155 V |
| the DC-link voltage $v_o$ | 200 V (Boost)<br>120 V (Buck) |
| switching frequency $f$ | 10 kHz |
| input side inductance $L_1$ | 3 mH |
| output side inductance $L_2$ | 2 mH |
| DC-link capacitors $C_{o1}$ and $C_{o2}$ | 470µF |
| output side capacitor $C_b$ | 47µF |
| **Controller Parameters** | |
| input current controller's bandwidth | 1 kHz |
| DC-link voltage controller's bandwidth | 40 Hz |
| DC capacitor voltage controller's bandwidth | 10 Hz |

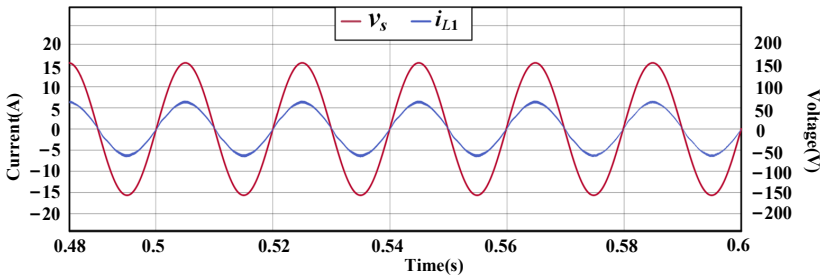



**Figure 10.** The power supply voltage $v_s$ and input current $i_{L1}$ simulation waveforms.

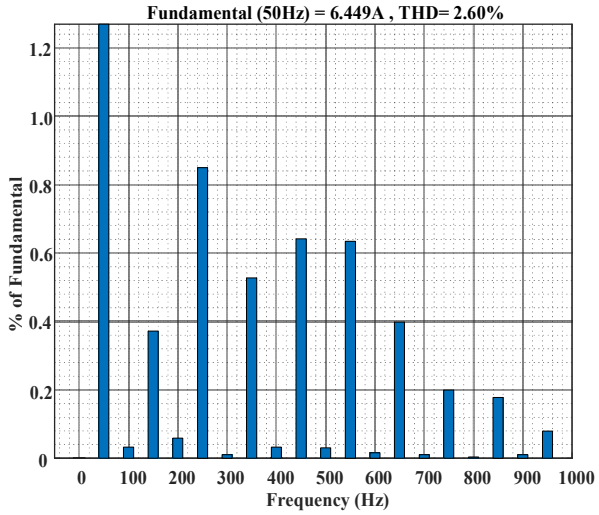



**Figure 11.** The THD analysis of input current $i_{L1}$.

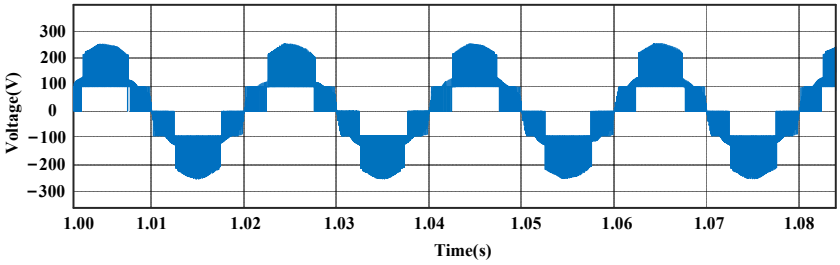



**Figure 12.** The input voltage of the single-phase diode bridge rectifier in boost mode.

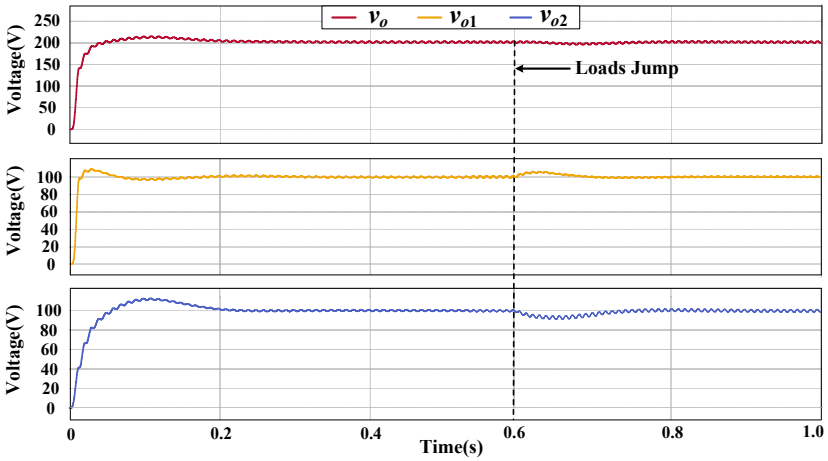



**Figure 13.** The DC capacitor voltages of the single-phase diode bridge rectifier in boost mode.

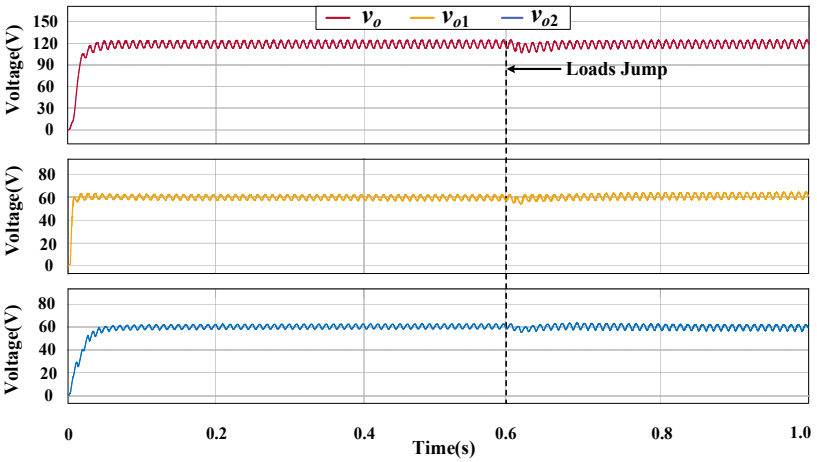



**Figure 14.** The DC capacitor voltages of the single-phase diode bridge rectifier in buck mode.

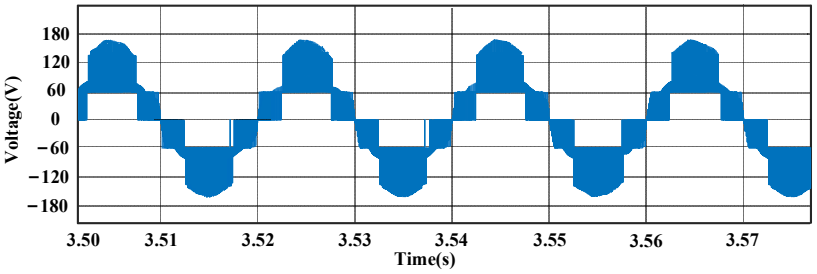



**Figure 15.** The input voltage of the single-phase diode bridge rectifier in buck mode.

Figures 10–13 depict the simulation waveforms of the proposed rectifier operating in boost mode. Figure 10 shows the simulation waveforms of input current $i_{L1}$ and power supply voltage $v_s$ of the rectifier operating under high power factor. Figure 11 shows the input current harmonics of the rectifier, and a THD of 2.60% indicates an acceptable input current quality. Figure 12 shows the input voltage of the single-phase diode bridge rectifier, which demonstrates that the novel rectifier can achieve approximately three voltage levels operation under the given DC output voltage 200 V, which is consistent with the theoretical analysis. Figure 13 gives the simulation waveforms of $v_o$, $v_{o1}$, and $v_{o2}$. It can be observed that the DC capacitor voltages $v_{o1}$ and $v_{o2}$ reach the reference voltage 100 V rapidly with a very small static error, and the DC output voltage $v_o$ is controlled stably at 200 V.

To verify the proposed capacitor voltage balancing control strategy, $R_1$ jumps from 250 W to 125 W, while $R_2$ jumps from 250 W to 375 W in the simulation. Figure 13 also shows that the DC capacitor voltages $v_{o1}$ and $v_{o2}$ and the DC-link voltage $v_o$ deviate from their stable value at the beginning of the load change, and then return to balanced again rapidly under the proposed DC capacitor voltage balancing control strategy.

Figures 14 and 15 depict the simulation waveforms of the proposed rectifier operating in buck mode. When the rectifier is in buck mode, the DC-link voltage $v_o$ is controlled at 120 V. For the same output power and power supply voltage, the input current $i_{L1}$ is consistent with the boost mode and will not be discussed here. However, the simulation waveforms of the input voltage of the single-phase diode bridge rectifier and the DC capacitor voltages $v_{o1}$ and $v_{o2}$ are different from the boost mode.

Figure 14 shows the DC capacitor voltages $v_{o1}$ and $v_{o2}$ simulation waveforms in buck mode. It is seen that the DC capacitor voltages $v_{o1}$ and $v_{o2}$ reach the reference voltage 60 V rapidly and return to balanced again rapidly under the load jump. The load jump has a smaller influence on the DC-link voltage $v_o$, and $v_o$ also reaches the reference voltage 120 V rapidly. Figure 15 gives the input voltage of the single-phase diode bridge rectifier in buck mode.

The experimental results are shown in Figures 16–21. Figure 16 gives the experimental waveforms of the input current $i_{L1}$ and power supply voltage $v_s$, which shows that the proposed rectifier is operating under high power factor with approximately sinusoidal input currents. The input current harmonic spectrum is shown in Figure 17. It shows that the input current contains some low-order harmonics (3th, 7th and 9th).

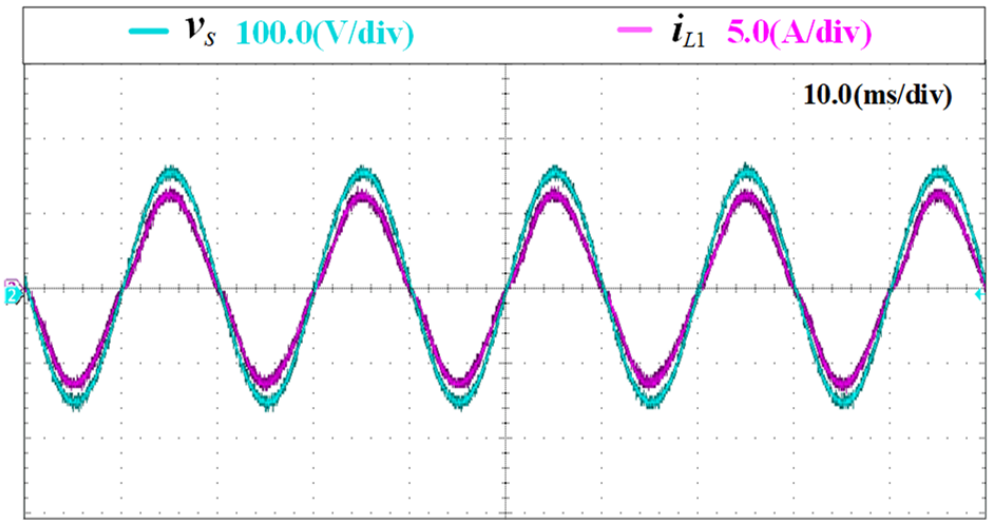



**Figure 16.** The power supply voltage $v_s$ and input current $i_{L1}$ experimental waveforms.

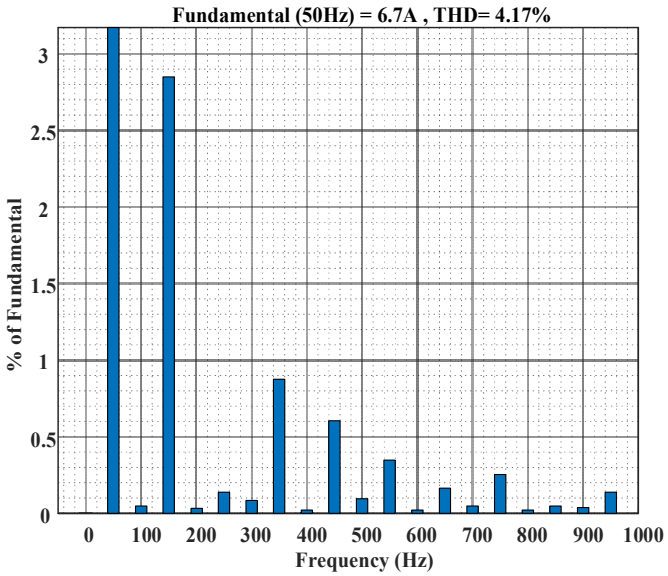



**Figure 17.** The input current $i_{L1}$ harmonic spectrum.

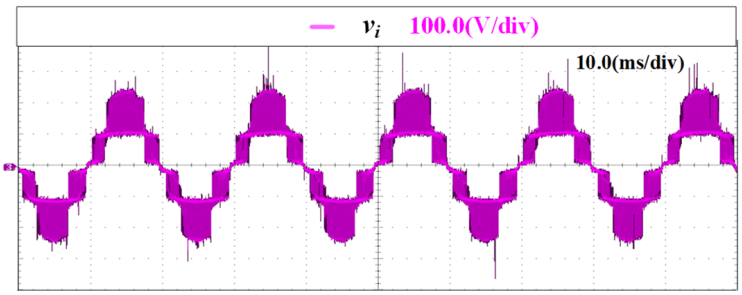



**Figure 18.** The input voltage of the single-phase diode bridge rectifier experimental waveforms.

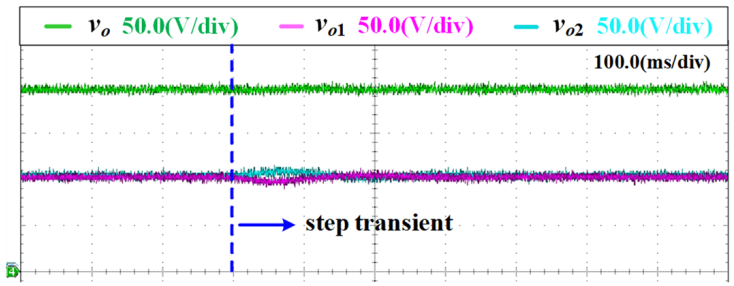



**Figure 19.** The experimental results of the DC-link voltage $v_o$ and the DC capacitor voltages $v_{o1}$ and $v_{o2}$ in boost mode.

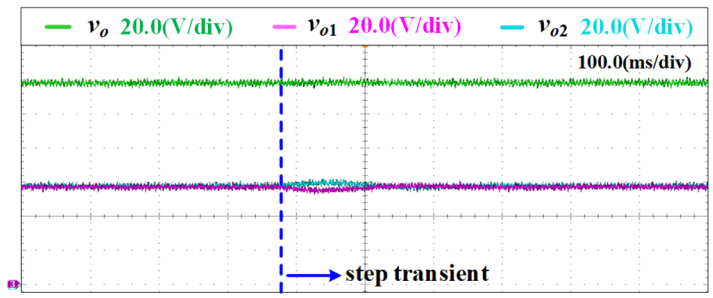



**Figure 20.** The experimental results of the DC-link voltage $v_o$ and the DC capacitor voltages $v_{o1}$ and $v_{o2}$ in buck mode.

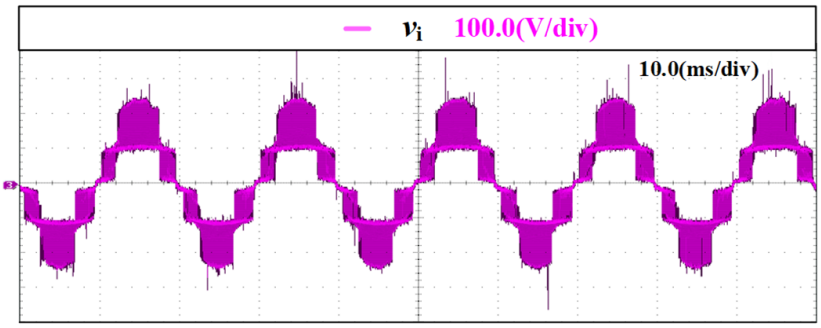
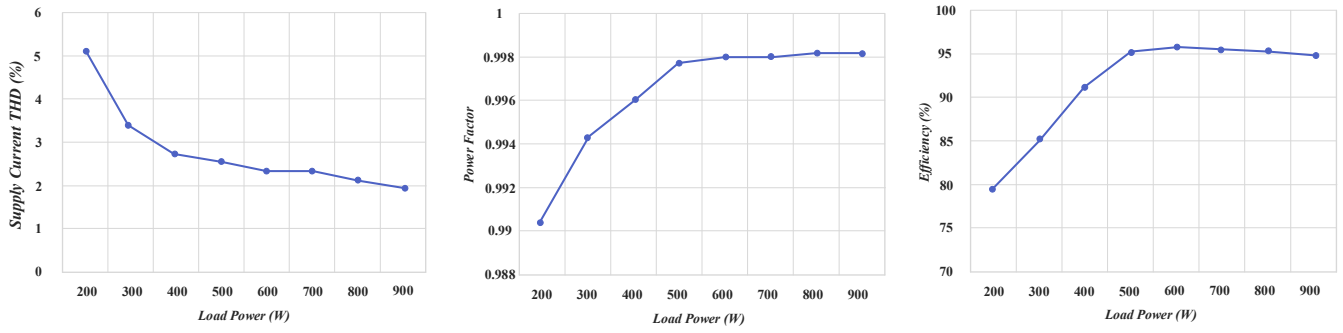



**Figure 21.** The experimental waveforms of the input voltage of the single-phase diode bridge rectifier in buck mode.

Figure 18 shows the experimental waveforms of the input voltage of the single-phase diode bridge rectifier operating under the given DC output voltage 200 V, which is consistent with the theoretical analysis. Figure 19 shows the experimental results of the DC-link voltage $v_o$ and the DC capacitor voltages $v_{o1}$ and $v_{o2}$ in boost mode. It can be seen that the DC capacitor voltages $v_{o1}$ and $v_{o2}$ reach the reference voltage 100 V rapidly with a very small static error, and the DC output voltage $v_o$ is controlled stably at 200 V. To verify the proposed capacitor voltage balancing control strategy, Figure 19 also indicates that $v_{o1}$ and $v_{o2}$, as well as $v_o$, deviate from their references at load step transient, and return to being in balance again after about 100 ms.

When the rectifier is in buck mode, the DC-link voltage $v_o$ is controlled at 120 V. For the same output power and power supply voltage, the input current $i_{L1}$ is consistent with the boost mode and will not be discussed here. Figure 20 indicates the experimental results of the DC-link voltage $v_o$ and the DC capacitor voltages $v_{o1}$ and $v_{o2}$ in buck mode. The experimental waveforms of the input voltage of the single-phase diode bridge rectifier operating under the given DC output voltage 200 V are shown in Figure 21.

Through simulation, Figure 22 has been obtained, which illustrates the performance of the proposed rectifier over wide load power conditions, depicting the curves of THD, PF, and efficiency as they vary with load power.




(**a**) (**b**) (**c**)

**Figure 22.** Performance of the presented rectifier under wide power conditions based on simulation: (**a**) supply current THD versus power curve; (**b**) operating power factor versus power curve; (**c**) efficiency versus power curve.

The above simulation and experimental results are consistent with the theoretical analysis, which verifies the correctness of the proposed balancing control strategy.

## 5. Conclusions

This paper introduces a novel SEPIC-boost-based power factor correction rectifier. Firstly, the limitations of traditional PFC are analyzed, and the notable performance charac-

teristics of the proposed rectifier are discussed. This is followed by a detailed description of the operating principles, mathematical model, and control design of the proposed topology, and the overall operation of the proposed rectifier is analyzed through simulation and experimental analysis.

The topology structure, theoretical analysis, control strategy, and experimental verification of the rectifier represent the primary contributions of this paper. In comparison with other rectifiers, the proposed SEPIC-boost-based rectifier features continuous current on the AC main circuit, lower voltage stress on active switches, a wider range of DC output voltage, elimination of secondary DC-DC converters, and high static voltage gain operation at low input voltage as well as low static gain operation at high input voltage. This makes it more suitable for applications such as electric vehicle charging.

To further enhance performance, the existing three-level topology could be expanded to a five-level topology to further reduce the voltage stress on active switches, and ultimately reduce THD to achieve improved current waveforms on the AC main circuit.

**Author Contributions:** Conceptualization, X.L. and H.C.; methodology, X.L. and Z.Z.; software, X.L. and W.Y.; validation, X.L., Y.S. and Z.Z.; writing—original draft preparation, X.L.; writing—review and editing, X.L., H.C., C.W. and Z.Z. All authors have read and agreed to the published version of the manuscript.

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**Conflicts of Interest:** The authors declare no conflicts of interest.

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