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CMOS Voltage-Controlled Oscillator with Complementary and Adaptive Overdrive Voltage Control Structures

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Abstract: This paper displays a voltage-controlled oscillator (VCO) with high performance implemented in 0.18 μm CMOS. The proposed CMOS VCO adopts a current-reused method, analog coarse and fine tuning mechanisms, and an adaptive overdrive voltage control structure to increase the overall performance, such as the power dissipation, phase noise, and tuning range, and has a robust start-up condition. The current-reused complementary structure with higher transistor transconductances is to save power consumption; the analog coarse and fine tuning mechanisms are to effectively widen the tuning range; and the adaptive overdrive voltage control technique is to change the transconductances of the transistors to improve power consumption by reasonably biasing the gate and body terminals in a class-AB mode to adjust the threshold voltage of the NMOS transistors. The proposed CMOS VCO adopts the class-AB mode to improve the overall performance and the start-up condition. The figure-of-merit (FOM) and FOM with tuning range (FOM_T) are used in evaluating the CMOS VCO performance. The measured phase noise at 1 MHz and 10 MHz offsets is –130.34 dBc/Hz and –150.96 dBc/Hz at the 3.38 GHz operating frequency, respectively. The proposed CMOS VCO has a tuning range between 2.85 and 3.62 GHz corresponding to 23.8% for the fifth-generation (5G) wireless communication applications. The proposed CMOS VCO core using a 1.4-V supply consumes 7.5 mW DC power. The FOMs and FOM_Ts at 1- and 10-MHz offsets are −192.2, −192.8, −199.7, and −200.3 dBc/Hz, respectively, from the 3.38 GHz output frequency.

Keywords: voltage-controlled oscillator; CMOS; coarse and fine tuning mechanisms; overdrive voltage control; phase noise

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1. Introduction

For the down-conversion mixer or the up-conversion mixer in a wireless communication system, the input local oscillation (LO) is the key source to demodulate or modulate with the receiving or transmitting data. The voltage-controlled oscillator (VCO) is one of the key devices in a synthesizer to implement the LO signal [1,2]. The VCO is important for the frequency control in the phase-locked loop (PLL). The PLL is a critical core for the synthesizer. The frequency quality of the VCO may affect the overall performance of the synthesizer. Lately, VCOs used in the fifth-generation (5G) wireless communication have drawn increasing interest [3,4]. The 5G technology is for mobile communications with high data rate demands. The low-frequency sub−6 GHz band in the 5G applications is an interesting consideration for the operation and design of the VCO. For the circuit implementation, VCOs fabricated in III–V processes could need more costs and have low integration for radio frequency (RF) integrated circuit applications [5]. VCOs implemented in the CMOS process are considerable because of their low-cost and high integration characteristic [5,6]. The VCO design in the CMOS silicon technology is very popular for the recently published works. There are several VCO design specifications that need to be considered, including the power dissipation, tuning range, and phase noise. Moreover, a robust start-up requirement for the VCO is to run an oscillation operation. Although the VCO phase noise can be improved effectively by using a feedback Class-C

method [7], the tuning range is not enough, and using more devices may increase chip area. The tuning range of the VCO in the feedback mode is only 2.3%, and the phase noise is −125 dBc/Hz at 1 MHz offset. Although the VCO increases the tuning range by using a series-parallel capacitor bank topology with small gain variation, both the power dissipation and phase noise still need to be improved [8]. The VCO tuning range is 18%, the phase noise is −113.7dBc/Hz at 1 MHz offset, and the power dissipation is 9.7 mW at 1.8 V supply. The *LC*-VCO phase noise can be improved by utilizing a self-adjusted current resource; however, the *LC*-VCO consumes more power [9]. The VCO tuning range is 19.8%, the phase noise is −128.04 dBc/Hz at 1 MHz offset, and the power dissipation is 11.7 mW. Furthermore, a VCO still needs a robust start-up condition to run an oscillation mechanism while consuming less DC power or existing a low-quality factor of the LC tank. The purpose of this paper is to present a high-performance class-AB VCO with the PMOS and NMOS complementary structures, the analog coarse and fine tuning mechanisms, and the adaptive overdrive voltage control technique to economically improve the power consumption, phase noise, and tuning range. The proposed class-AB VCO has an operating frequency of 3.38 GHz and a tuning range between 2.85 and 3.62 GHz for 5G wireless communication applications.

This paper is organized into three parts. The proposed CMOS VCO circuit is fully expounded in Section 2. Next, Section 3 displays the chip implementation and experimental results. At last, Section 4 presents a conclusion.

2. Proposed CMOS VCO Design

The conventional LC-type VCO could be used in high-frequency applications, as shown in Figure 1. This owns the differential outputs and has two symmetric circuits formed by the cross-coupled NMOS transistors M_{n1} and M_{n2} with the negative conductance, the varactors C_{v1} and C_{v2}, and the inductors L_1 and L_2. The differential output oscillation signals could be generated by the LC tank. The LC tank consists of the inductors L_1 and L_2, the varacotrs C_{v1} and C_{v2}, controlled by the control voltage V_C, and the parasitic capacitances. One of the differential output oscillation signals feeds back from the drain terminal of the transistor M_{n1} (or M_{n2}) to the gate terminal of the transistor M_{n2} (or M_{n1}). The control voltage V_C is utilized to adjust the biases of the varacotrs C_{v1} and C_{v2} to obtain the VCO tuning range. There is only one mechanism to control the tuning range of the VCO. However, the conventional LC-type VCO could need high power consumption to face the start-up condition when operating at high band. Moreover, the quality factor of the LC-tank is low due to the lossy feature fabricated in the silicon substrate. The size of the NMOS transistors needs to be increased to raise the negative conductance. Based on the power consumption issue, a complementary structure formed by the PMOS and NMOS transistor cross-coupled pairs could be utilized for the modified VCO. The method can obtain a high loop gain to decrease the DC current to alleviate the start-up condition and to add the voltage swings of the LC tank [10]. The VCO has the current-reused feature and the differential outputs. The LC tank of the VCO uses only an inductor connected between the drain terminals of the PMOS and NMOS transistor cross-coupled pairs to reduce the chip area. The cross-coupled pairs also offer negative resistances to compensate for the loss from the LC tank. The complementary PMOS and NMOS transistor structures are adopted for one of the proposed CMOS VCO concepts. Although the complementary VCO with the higher transconductance has the biasing current reusing ability to decrease power dissipation, the supply voltage (V_{DD}) needs to have a higher potential to meet the complementary operation under the fixed transistor threshold voltages. The phase nose and the output swings of the VCO could be limited by the low supply voltage. The oscillation frequency derived from the half-circuit model due to the symmetrical architecture is decided by the LC tank of the VCO. Generally, the VCO LC-tank is formed by the inductor, the varacotrs, and the parasitic capacitances. The tuning range is an important design parameter of the CMOS VCO. The tuning range is mainly achieved by controlling the capacitance differences of the varactors. The minimum and maximum capacitances of the

varactors are adjusted by controlling the biases of the varactors from 0 to the supply voltage (V_{DD}) for the analog tuning method. The high and low tuning ranges are decided by the minimum and maximum varactor capacitances, respectively. The analog tuning method is implemented by a controlled voltage (V_C). The widening tuning range can be obtained by increasing the equivalent capacitance differences of the circuit. The enlarge the equivalent capacitance differences to widen the tuning range is used for one of the proposed CMOS VCO concepts.

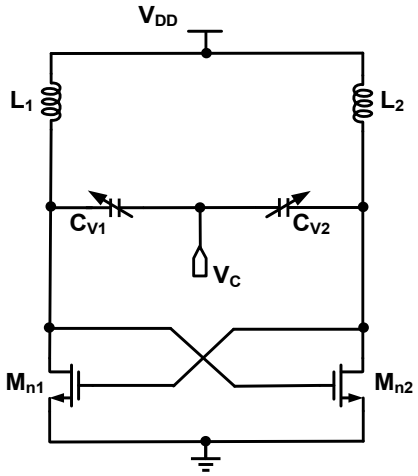


Figure 1. Conventional LC-type VCO schematic.

Although widening capacitance differences are intended to improve the tuning range of the CMOS VCO, the LC tank quality factor could be degraded. The VCO LC tank quality factor is a key decision for the start-up requirement. The quality factors of the passive devices need to be maximized to maintain the correct operation of the LC tank [11,12]. This can reduce the DC power dissipation to satisfy the start-up condition. However, the quality factors of the LC devices are usually not good due to the substrate lossy issue of the CMOS process. This exhibits an issue with the performance of the CMOS VCO. Although the VCO has a wide tuning range by adopting the larger varacotrs, both phase noise and power consumption could be influenced by the low quality factors of the varacotrs [13]. The phase noise of the VCO can be improved by enlarging the output swings. Although choosing the low gate terminal bias of the MOS transistor could improve the output swings in the class-C mode, this may suffer from the start-up requirement of running the oscillation function [7]. If the VCO relaxes the start-up requirement to operate in class-B mode, the power consumption may increase. Moreover, the performance of the VCO could be directly influenced by the process, voltage, and temperature variations. The threshold voltage of the MOS transistor could be reduced to alleviate power consumption and supply voltage by adjusting the body terminal bias [14]. Although the NMOS transistor threshold voltage could be modified by biasing the body terminal voltage, the pn-junction formed by the source and body terminals could be forwarded to generate the leakage current to influence the LC-tank quality factor [14]. The above benefit of the complementary structure formed by the PMOS and NMOS transistor cross-coupled pairs could be adopted to overcome the issue. The VCO running modes and the adjusting threshold voltage method are to improve the phase noise and start-up condition. This is also utilized for one of the proposed CMOS VCO concepts.

Based on the above statements, Figure 2 displays the proposed VCO schematic. This can effectively modify the overall performance, such as the power consumption, start-up requirement, tuning range, and phase noise, by adopting a current-reused complementary, analog coarse and fine tuning mechanisms, and an adaptive overdrive voltage control structure.

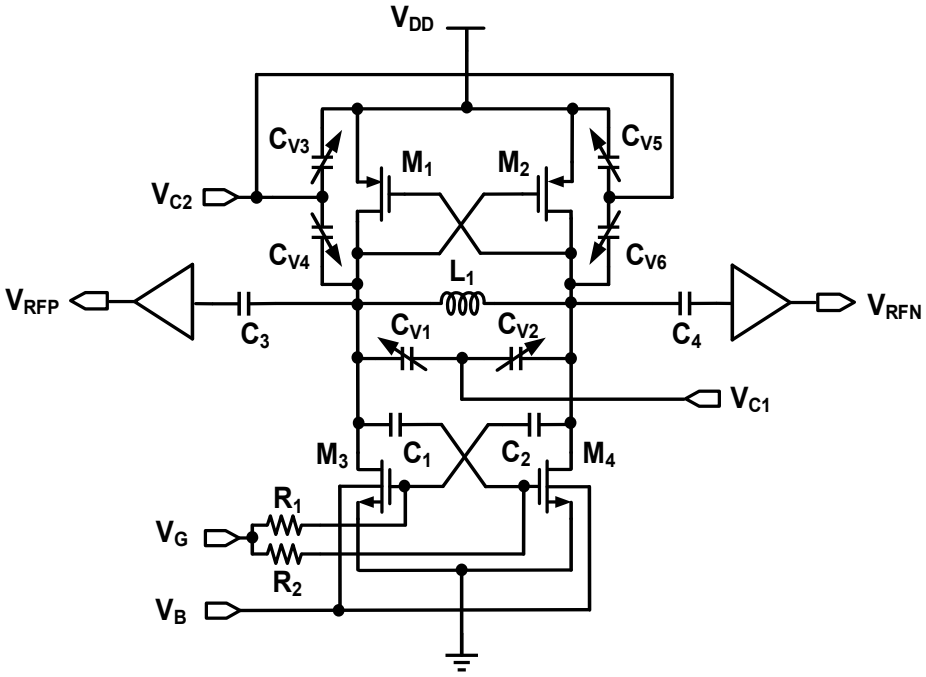


Figure 2. Schematic of the proposed CMOS VCO.

The proposed VCO is fully formed by two cross-coupled pairs, an inductor, varactors, the DC blocking capacitors, the coupling capacitors, the parasitic capacitances, and two output buffers. The two cross-coupled pairs are formed by the NMOS transistors M_3 and M_4, and the PMOS transistors M_1 and M_2. While keeping enough loop-gain situation, this contributes a current-reused function to switch off and on the PMOS and NMOS transistors at the same time to decrease the power dissipation. In addition, the two cross-coupled pairs form the negative resistance role to compensate for the CMOS LC tank power loss and stably maintain the oscillation mechanism. This also builds up the powerful transconductance ability to improve the LC tank quality factor and decrease the power dissipation in the meantime due to the current-reused ability. The proposed VCO has the symmetric layout consideration for the NMOS transistors M_3 and M_4, and the PMOS transistors M_1 and M_2 to ensure the same drain currents at the left and right sides.

The LC tank of the proposed VCO is mainly formed by the inductor L_1 connected between the drain terminals of the two cross-coupled pairs, the analog coarse and fine varactors C_{V1} and C_{V2} and C_{V3}, C_{V4}, C_{V5}, and C_{V6}, respectively, the parasitic capacitances. The analog coarse tuning varactors C_{V1} and C_{V2} are connected between the drain terminals of the PMOS and NMOS transistor cross-coupled pairs. The analog fine-tuning varactors C_{V3}, C_{V4} and C_{V5}, C_{V6} are connected between the drain and source terminals of the two PMOS transistors M_1 and M_2, respectively. The six varactors (C_{V1}–C_{V2}, C_{V3}–C_{V4} and C_{V5}–C_{V6}) are adopted in the circuit structure to enlarge the tuning range. The proposed CMOS VCO adopts the varactors C_{V1} and C_{V2} for the analog coarse tuning stage and C_{V3}, C_{V4}, C_{V5}, and C_{V6} for the analog fine tuning stage to add the tuning range, respectively. The proposed CMOS VCO needs two extra control pads, V_{C1} and V_{C2}, to adjust the capacitances of the six varactors. The analog coarse tuning stage is controlled by the control voltage V_{C1} to adjust the varactors C_{V1} and C_{V2}. Moreover, the analog fine tuning stage is controlled by the control voltage V_{C2} to adjust the varactors C_{V1} and C_{V2}. The large equivalent capacitance differences are useful to widen the proposed VCO tuning range. The capacitances of the varactors C_{V1} and C_{V2} are varied by the control voltage V_{C1} from 1.103 to 2.945 pF for the analog coarse tuning stage. The capacitances of the varactors C_{V3}, C_{V4}, C_{V5}, and C_{V6} are changed by the control voltage V_{C2} from 359.9 to 949.5 fF for the fine tuning stage. Both the two control voltages, V_{C1} and V_{C2}, are varied from 0 to 1.4 V (V_{DD}) to control the output oscillation frequency range of the proposed CMOS VCO. Through the

equivalent half-circuit analysis due to the symmetric architecture, the output oscillation frequency can be obtained as

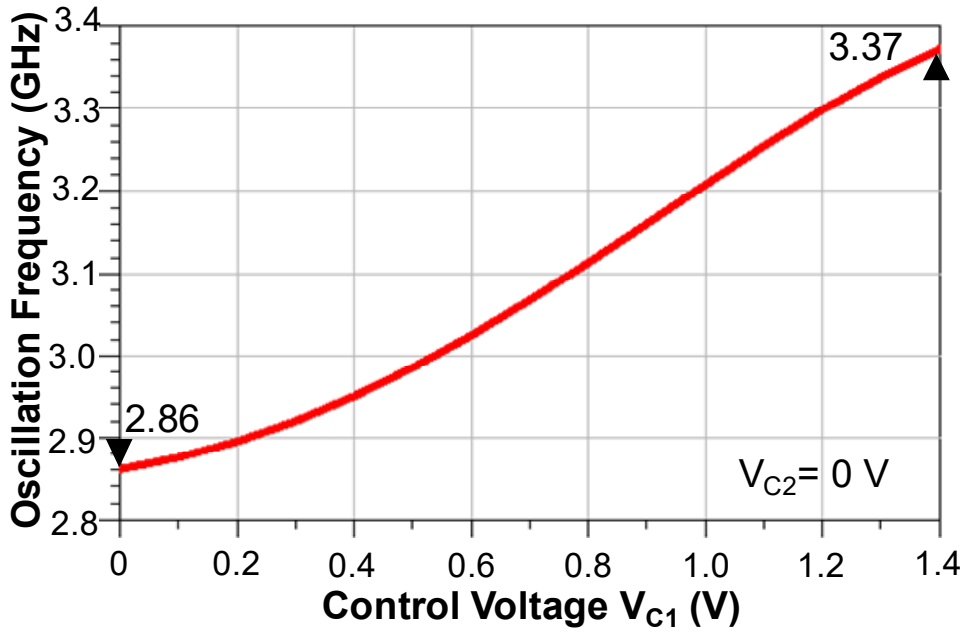
$$f_{\text{out}}(V_{C1,}V_{C2}) \approx \frac{1}{2\pi}\sqrt{\frac{1}{L_1[C_v(V_{C1,}V_{C2}) + C_P]}} \quad (1)$$

where C_V is the equivalent capacitances of the varactors controlled by the control voltage V_{C1} and V_{C2} and C_P is the parasitic capacitance. Figure 3a displays the simulated output tuning range between 2.86 and 3.37 GHz by varying the control voltage V_{C1} through 0 to 1.4 V at the control voltages V_{C2} of 0 V. Moreover, Figure 3b displays the simulated output tuning range between 2.99 and 3.59 GHz by varying the control voltage V_{C1} through 0 to 1.4 V at the control voltages V_{C2} of 1.4 V. The totally simulated output tuning range is from 2.86 to 3.59 GHz by the analog coarse and fine tuning mechanisms to widen the output oscillation frequency range. From the simulated results, the mechanism is very useful to improve the proposed VCO tuning range. Furthermore, silicon substrates in the CMOS process have the loss features to degrade the LC tank quality factor. Although the analog coarse and fine-tuning varactors C_{V1} and C_{V2} and C_{V3}, C_{V4}, C_{V5}, and C_{V6}, respectively, could impact the LC tank quality factor, the situation can be improved by using the class-AB mode from the threshold voltage adjustment. This is an effective and strong mechanism formed by the adaptive overdrive voltage V_{OV} (=$V_{GS} - V_t$) control technique to improve the start-up condition, phase noise and power dissipation of the proposed VCO including the process, voltage, and temperature variations. The adaptive overdrive voltage control technique consists of the NMOS transistor gate terminal and body terminal biases controlled by the voltages V_G and V_B, respectively.

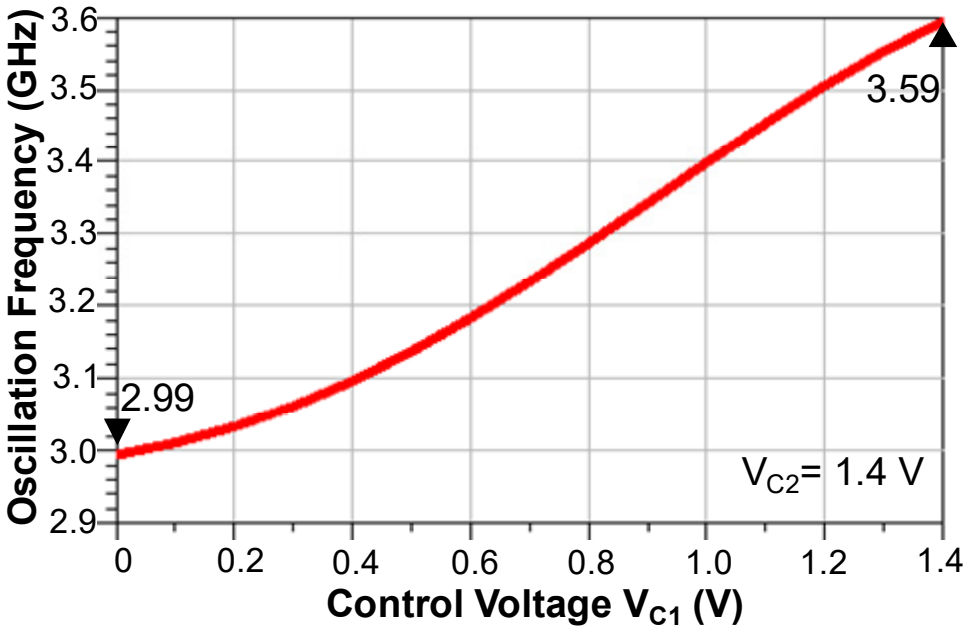
The gate terminals of the NMOS transistors M_3 and M_4 can be isolated with the drain terminals by the DC blocking capacitors C_1 and C_2 connected to the drain terminal and another side gate terminal of the NMOS transistors, respectively. The NMOS transistors M_3 and M_4 could be biased by the gate terminal control voltage V_G to adjust the suitable biasing current in the presented class-AB mode to ensure the oscillation mechanism and to acquire the enough output swings to improve the proposed CMOS VCO phase noise. Choosing the suitable threshold voltages of the NMOS transistors M_3 and M_4 can alleviate the supply voltage (V_{DD}) requirement and also satisfy the overdrive voltages V_{OV} (=$V_{GS} - V_t$) in the complementary structure. The gate terminal bias of the class-C VCO is a lower voltage than the threshold voltage and the start-up condition could be difficult. Through the gate bias of the class-B VCO is close to the threshold voltage to own a low DC power, the start-up condition is still an issue [15,16]. The VCO with class-B or class-C mode could have the worse start-up condition in the low quality factor of the LC tank. The proposed CMOS VCO uses the analog coarse and fine tuning mechanisms to widen the tuning range. This adopts six varactors, C_{V1} and C_{V2} for the coarse tuning stage, C_{V3}, C_{V4}, C_{V5} and C_{V6} for the fine-tuning stage, respectively, and may suffer the worse quality factor of the LC tank from running start-up requirement. Based on the possible issues of class-B or class-C mode and low quality factor of the LC tank of the VCO, the proposed CMOS VCO reasonably adopts the class-AB mode to satisfy the start-up requirement for ensuring the oscillation mechanism before entering the steady state. Moreover, the PMOS and NMOS transistor cross-coupled pairs of the proposed CMOS VCO form the negative resistance to compensate the loss from the proposed CMOS VCO LC tank. Generally, the class-AB VCO could carefully meet the LC tank quality factor to improve the phase noise. Another overdrive voltage control is the body terminal bias controlled by the voltage V_B. The threshold voltages of the NMOS transistors M_3 and M_4 can be adjusted to accelerate the start-up condition by utilizing the forward source-to-body voltage for the class-AB VCO operation. The transistors threshold voltages can be referred as

$$V_t = V_{t0} + \gamma(\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|}) \quad (2)$$

where Φ_F is the Fermi potential, γ is the body effect coefficient, V_{t0} is the zero-bias threshold voltage, and V_{SB} is the transistor source-to-body voltage [14]. Equation (1), the threshold voltage V_t can be reduced effectively while the forward V_{SB} decreases. Figure 4 shows the simulated threshold voltages of the NMOS transistors M_3 and M_4. When the body voltage is fed from −0.3 to 0.6 V when the source terminal voltage connected to the ground, the simulated threshold voltage V_t values are from 0.592 (V_{SB} = 0.3 V) to 0.401 V (V_{SB} = −0.6 V).



(**a**)



(**b**)

Figure 3. Simulated output tuning ranges of the proposed VCO by adjusting the control voltage V_{C1} from 0 to 1.4 V at (**a**) the control voltage V_{C2} of 0 V and (**b**) at the control voltage V_{C2} of 1.4 V.

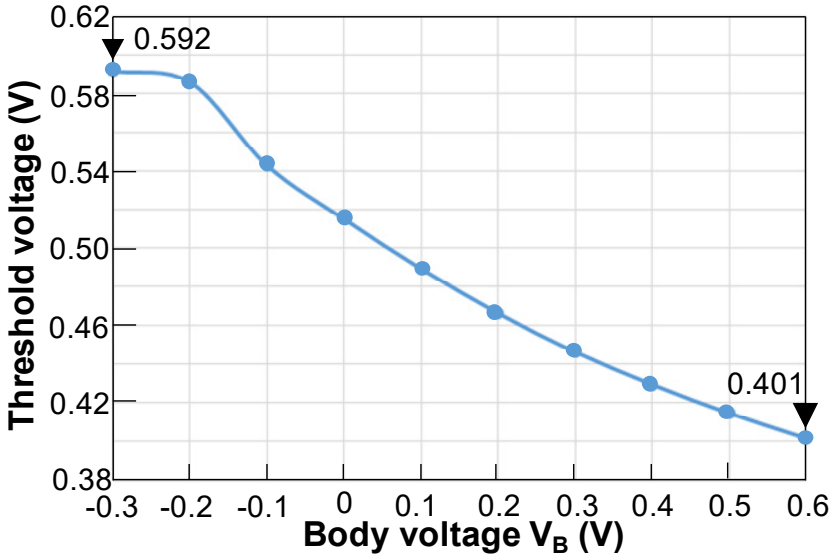


Figure 4. Simulated NMOS transistor threshold voltage versus the body voltage V_B.

The body terminal bias of 0.3 V is chosen for this work at the $V_{SB} = -0.3$ V condition. The simulated threshold voltage V_t is 0.446 V from Figure 4. The threshold voltages of the MOS transistors M_3 and M_4 could be reduced by adjusting the body terminal bias to decrease supply voltage and improve power consumption. The adaptive overdrive voltage control technique can be implemented by logically adjusting the gate or body terminal voltages of the NMOS transistors M_3 and M_4 to work in the optimization conditions.

The voltage of 0.6 V is given to the gate terminal biases of the NMOS transistors M_3 and M_4 for this work. The control voltage V_G of 0.6 V is greater than the controlled threshold voltage (V_t = 0.446 V) by using the forward source-to-body voltage at the body voltage V_B of 0.3 V for the proposed CMOS VCO. The drain-to-source voltages of the NMOS transistors M_3 and M_4 are higher than the overdrive voltages ($V_{OV} = V_{GS} - V_t$) to satisfy the transistor saturation regions in the class-AB mode for the proposed CMOS VCO. Figure 5 shows the simulated start-up condition with the threshold voltage V_t of 0.446 V and drain terminal voltages of the PMOS and NMOS transistor cross-coupled pairs at the gate terminal bias of 0.446 V. The simulated operation situation is in the class-B mode of the VCO. The simulated start-up time is about 5.6 ns in the class-B mode of the VCO. Moreover, Figure 6 shows the simulated start-up condition with the threshold voltage V_t of 0.446 V and drain terminal voltages of the PMOS and NMOS transistor cross-coupled pairs at the gate terminal bias of 0.6 V. The simulated operation situation is at in class-AB mode of the VCO. The simulated start-up time is about 1 ns at the class-AB mode of the VCO. Obviously, the class-AB mode of the VCO has the robust start-up time of 1 ns to successfully run the oscillation mechanism. The proposed CMOS VCO adopts the class-AB mode to strengthen the start-up requirement and improve the quality factor of the LC tank. Furthermore, the proposed class-AB CMOS VCO has a better drain waveform to improve the phase noise and decrease the power dissipation due to the complementary PMOS and NMOS cross-coupled pairs. The proposed class-AB VCO also increases the tuning range by adopting analog coarse and fine tuning mechanisms. Based on the overall design concepts, the current-reused complementary technique formed by the PMOS and NMOS transistor cross-coupled pairs, the analog coarse and fine tuning mechanisms, and the adaptive overdrive voltage control technique formed by reasonably offering the gate terminal and body terminal biases to adopt the class-AB mode are for improving the power consumption, phase noise, start-up condition, and tuning range.

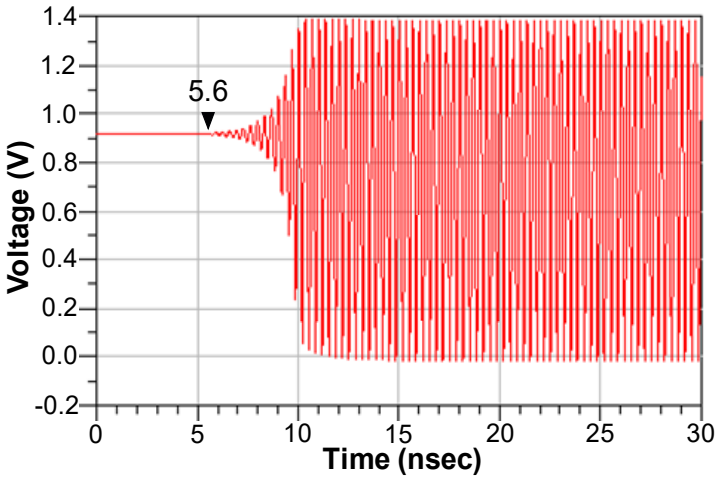


Figure 5. Simulated start-up condition with the threshold voltage of 0.446 V (V_G = 0.446 V).

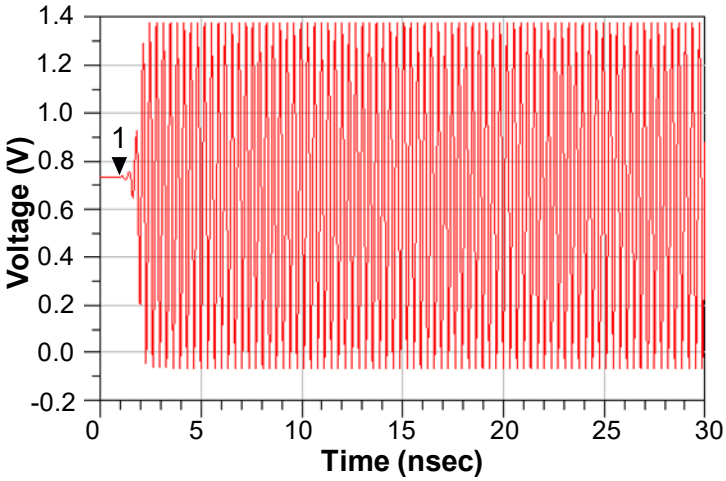


Figure 6. Simulated start-up condition with the threshold voltage of 0.446 V for the proposed class-AB VCO (V_G = 0.6 V).

The other device parameters of the proposed CMOS VCO are as follows. The aspect ratios of the PMOS transistors for the M_1 and M_2 and NOMS transistors for the M3 and M4 are 136 µm/0.18 µm and 96 µm/0.18 µm, respectively. The resistances of the MOS gate terminal biasing resistors R_1 and R_2 are 1.7 K. The capacitances of the DC blocking capacitors for the C_1 and C_2 and coupling capacitors for C_3 and C_4 are all 644.9 pF. The inductance of inductor L_1 of the proposed CMOS VCO LC tank is 2.19 nH.

3. Experimental Results

Figure 7 shows the proposed CMOS VCO measurement setup, and Figure 8 shows the proposed CMOS VCO chip micrograph. The chip's performance was measured by a spectrum analyzer and a signal source analyzer under on-wafer probing. The chip size, including testing pads, is 0.955 × 0.655 mm^2. While using a 1.4 V supply, the proposed CMOS VCO core dissipates a DC power of 7.5 mW. Figure 9 shows the measured operating frequency at 3.38 GHz with an output power of −0.86 dBm under the controlled voltages V_{C1} of 1.4 V and V_{C2} of 0 V without calibrating the 2.2 dB cable loss. The measured tuning range is from 2.85 to 3.38 GHz, as sweeping the controlled voltage V_{C1} from 0 to 1.4 V at the controlled voltage V_{C2} of 0 V. The measured tuning range is from 2.99 to 3.62 GHz, as sweeping the controlled voltage V_{C1} from 0 to 1.4 V at the controlled voltage V_{C2} of 1.4 V. The measured turning range results are shown in Figure 10. The measured CMOS VCO overall output frequency is from 2.85 to 3.62 GHz, including a tuning range of 23.8%.

From the 3.38 GHz carrier frequency, the measured CMOS VCO phase noise at 1 MHz and 10 MHz offsets is −130.34 dBc/Hz and −150.96 dBc/Hz, as shown in Figure 11, respectively. The figure of merit (FOM) and the FOM with tuning range (FOM_T) are often adopted to make a fair comparison for evaluating the VCO performance. The FOM and FOM_T [17,18] are expressed as

$$\text{FOM} = PN - 20\log_{10}\left(\frac{f_{\text{out}}}{\Delta f}\right) + 10\log_{10}\left(\frac{P_{DC}}{1mW}\right) \tag{3}$$

$$\text{FOM}_\text{T} = PN - 20\log_{10}\left(\frac{f_{\text{out}}}{\Delta f}\frac{TR(\%)}{10}\right) + 10\log_{10}\left(\frac{P_{DC}}{1mW}\right) \tag{4}$$

where PN is the phase noise, f_{out} is the oscillation frequency, TR (%) is the tuning range (%), and P_{DC} is the DC power consumption, and Δf is the offset frequency. From the (3) and (4) expressions, the FOM and FOM_T at 1 MHz offset are −192.2 dBc/Hz and −199.7 dBc/Hz, respectively. Next, the FOM and FOM_T at 10 MHz offset are −192.8 dBc/Hz and −200.3 dBc/Hz, respectively. Table 1 displays the CMOS VCO performance summary and comparison with previous fabricated in 0.18-µm process works. Based on Table 1, this work owns the good FOM and FOM_T by adopting the current-reused complementary structure, the coarse-fine-tuning method, and the adaptive overdrive voltage control technique.

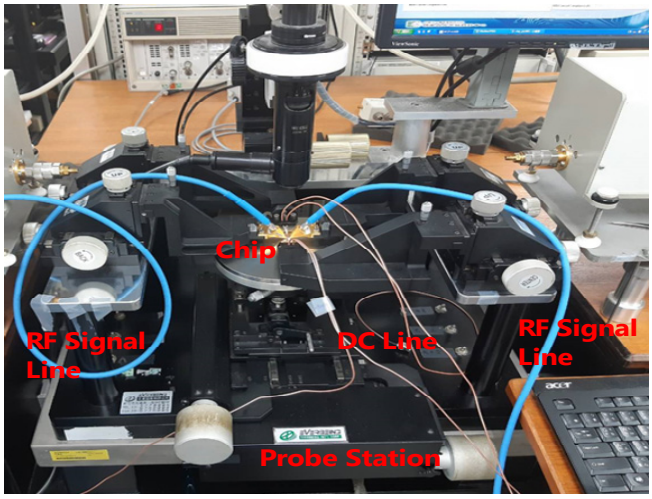


Figure 7. Measurement setup of the proposed CMOS VCO.

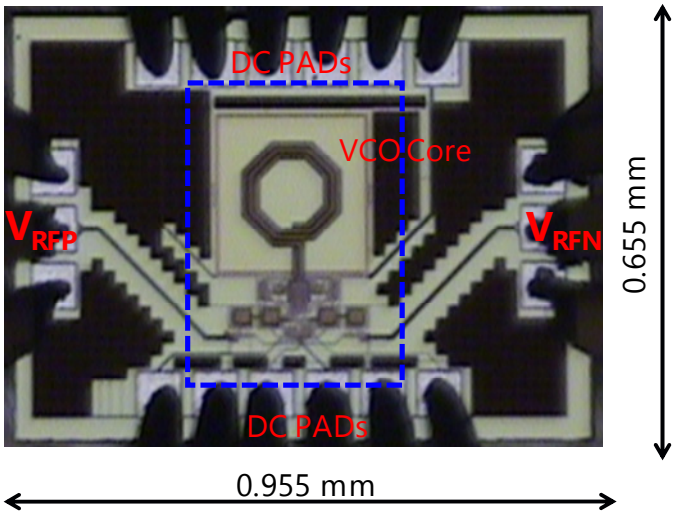


Figure 8. Micrograph of the proposed CMOS VCO.

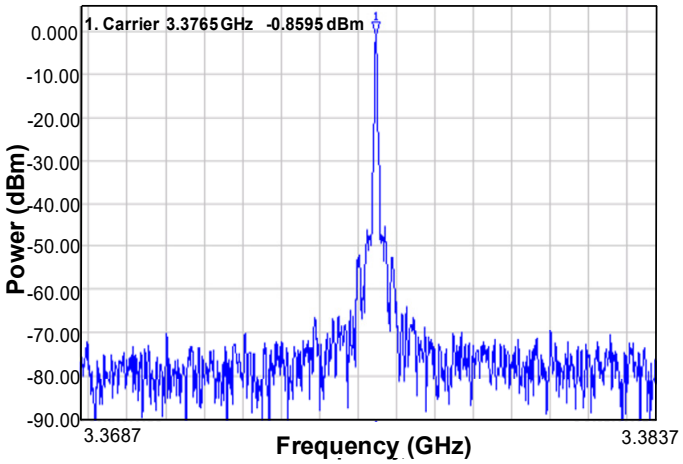


Figure 9. Measured VCO operating frequency.

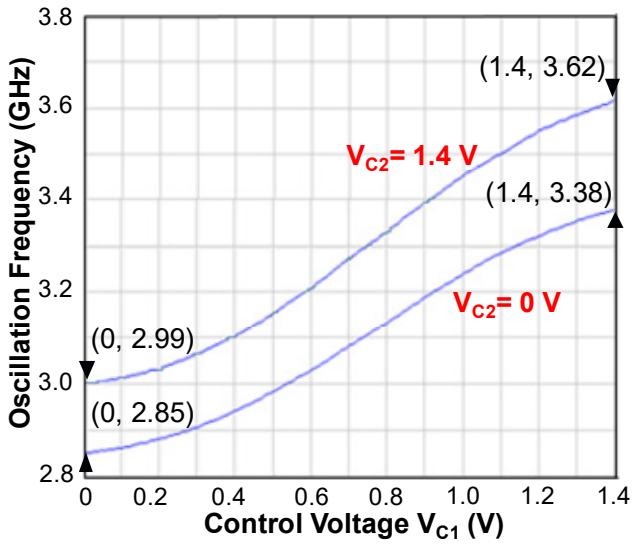


Figure 10. Measured output tuning ranges of the proposed CMOS VCO.

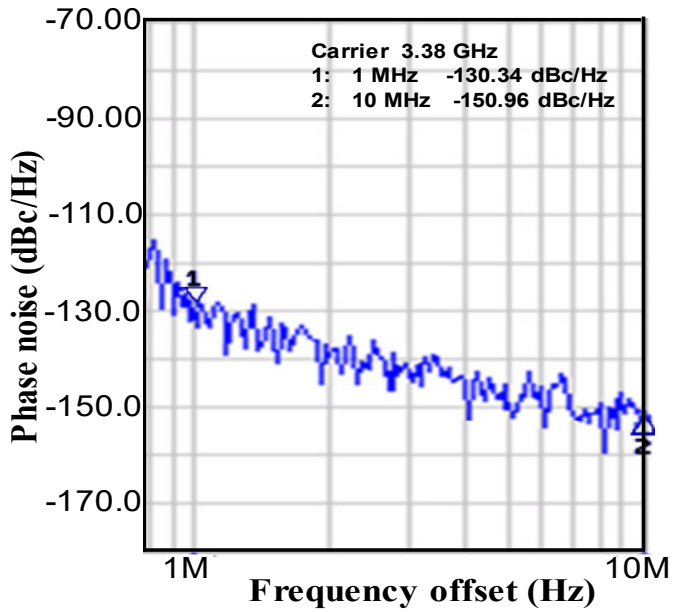


Figure 11. Measured CMOS VCO phase noise.

Table 1. Performance summary and comparison.

	This Work	[7]	[8]	[9]
Process (μm)	0.18	0.18	0.18	0.18
DC power (mW)	7.5	3.4	9.7	11.7
V_{DD} (V)	1.4	1.2	1.8	---
Output Frequency (GHz)	3.38	4.84	5.2	4.1
Tuning range (%)	23.8	2.3	18	19.8
PN@1MHz (dBc/Hz)	−130.34	−122	−113.7	−128.04
PN@10MHz (dBc/Hz)	−150.96	---	−132	---
FOM@1MHz (dBc/Hz)	−192.2	−190.4	−180	−189.3
FOM@10MHz (dBc/Hz)	−192.8	---	−184.5	---
FOM_T@1MHz (dBc/Hz)	−199.7	−177.6	−185	−195.2
FOM_T@10MHz (dBc/Hz)	−200.3	---	−189.6	---

4. Conclusions and Future Works

The proposed high-performance class-AB CMOS VCO with complementary and adaptive overdrive voltage control structures was successfully demonstrated. By owning the robust start-up condition, the analog coarse and fine tuning mechanisms, and the complementary structure, the proposed VCO overall performance is effectively modified, such as the tuning range, the phase noise, and the power dissipation. The proposed CMOS VCO has a wide tuning range between 2.85 and 3.62 GHz. From a 1.4 V supply, the proposed VCO core dissipates 7.5 mW DC power. Moreover, the FOM and FOM_T at 1 MHz offset are −192.2 dBc/Hz and −199.7 dBc/Hz, respectively. Finally, the FOM and FOM_T at 10 MHz offset are −192.8 dBc/Hz and −200.3 dBc/Hz, respectively. This work could be an important block of the phase-locked loop technique in a frequency synthesizer for the 5G wireless communication applications.

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