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Research on Asymmetrical Operation of Multilevel Converter-Type Solid-State Transformers Based on High-Frequency Link Interconnection

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Abstract: The large size of the sub-module (SM) capacitor is a typical problem in traditional modular multilevel converter-type solid-state transformers (MMC-SSTs). The MMC-SST based on high-frequency link interconnection is an effective solution for achieving lightweight capacitance. This structure can help to eliminate the symmetric SM fluctuating power, thereby reducing the SM capacitance. In a three-phase interconnected MMC-SST with low capacitance, potential risks may arise during transient processes, especially in cases of three-phase voltage asymmetry, such as large fluctuations in the SM voltage and unstable DC bus voltage. Aiming to solve this problem, this article re-analyzes the internal power characteristics of the MMC-SST under asymmetric operation and re-derives the SM capacitance constraint suitable for different degrees of three-phase voltage asymmetry. The new SM capacitance constraint enhances the asymmetric voltage ride-through capability of the MMC-SST. The new capacitance constraint is higher than that in symmetric operation, but it still has significant advantages in capacitance compared with the traditional MMC-SST.

Keywords: solid-state transformer; modular multilevel converter; asymmetric operation

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1. Introduction

Due to its high modularity, high voltage level, and high power quality characteristics, the modular multilevel converter-based solid-state transformer (MMC-SST) has wide application potential in new energy conversion, distribution networks, and traction systems [1,2], whether based on a half-bridge or full-bridge structure [3–5]. In other words, the MMC-SST is characterized by a large number of switches and large SM capacitors, which greatly limit its power density [6–8].

1.1. State-of-the-Art SM Capacitor Lightweight Methods for MMC-SSTs

To reduce the SM capacitance, several studies [9–11] adopted the injection of high-frequency common mode voltage on the AC side and the circulating current in the phase unit to suppress the voltage fluctuation. Injecting a sine wave significantly increases the peak current of the bridge arm and limits the output voltage amplitude, while injecting a square wave makes it difficult to track and control its circulating current. The authors of [12–17] proposed schemes for setting up power channels between sub-modules. This scheme needs to add a power flow control strategy to eliminate SM fluctuating power but cannot control the phase shift angle to 0 to achieve real-time fluctuating power elimination. Based on the above research, one study [18] proposed interconnecting SMs through high-frequency links (HFLs) controlled by a synchronous open-loop control, eliminating the need for closed-loop control. This approach eliminates the fluctuating power of SMs in real

time, realizes automatic voltage equalization of SMs, reduces the rating of capacitance from a few mF to μF, and significantly improves power density.

The method proposed in [18] can achieve a significant reduction in SM capacitance under three-phase symmetric operation. The DC/DC topology and modelling method discussed in [19] provides technical support for the high-frequency link design of the MMC-SST, while voltage asymmetry is a typical condition for grid-tied AC/DC conversion. In the MMC-SST system, especially after the lightweight design of the SM capacitor, the inertia of the system is reduced due to the reduction in capacitance. Therefore, the transient process represented by the three-phase voltage asymmetry merits more attention [20].

Under three-phase asymmetric operation, after the fault is detected, relay protection starts and cuts off the faulty grid. If the fault duration is too short for the relay protection to respond, the SST must operate under the three-phase asymmetric voltages and be capable of riding through in these conditions. Recently, the authors of [21] analyzed the working characteristics of conventional MMC under unbalanced operation and pointed out that, in the case of grid-side unbalance, positive-sequence and zero-sequence double-frequency circulating currents will increase in the MMC arms, which will lead to fluctuations in the DC-side current. The higher the grid-side voltage unbalance degree, the greater the DC-side current fluctuation. The authors of [22,23] analyzed the performance of the MMC system according to the voltage imbalance on the grid side caused by different types of AC side faults. The authors of [24,25] proposed control schemes to ensure the safe operation of the system when three-phase voltage unbalance occurs.

State-of-the-art methods for three-phase asymmetric operation mainly focus on the traditional MMC system. However, the MMC-SST exhibits three-phase SM interconnection characteristics, and the voltage asymmetric fault will be coupled between three phases, further complicating the already complex power relationship inside the MMC-SST. The lightweight strategy for MMC-SST represented in [18] can greatly reduce the size of the SM capacitor and, at the same time, increase the seriousness of potential risks under the asymmetric operation of three-phase voltage, including possible large voltage fluctuation of the SM capacitor and instability of the DC bus [13,26–28].

1.2. Contribution

Aiming to solve this problem, this article re-analyzes the internal power characteristics of the MMC-SST under asymmetric operation and re-derives the SM capacitance constraint suitable for different degrees of three-phase voltage asymmetry. The new SM capacitance constraint enhances the asymmetric voltage ride-through capability of the MMC-SST. This study is suitable not only for MMC-SST based on the open-loop synchronous modulation proposed in [18] to achieve capacitor lightweight but also for the closed-loop control-based schemes described in [12–17].

The rest of this article is organized as follows. Section 2 analyzes the characteristics of SM current during asymmetric operation. Section 3 analyzes the demand for SM capacitors and the impact on each port during asymmetric operation. Finally, it is verified by means of experiments that the system can operate stably under asymmetric conditions and asymmetric fault ride-through can be achieved.

2. Analysis of SM Current under Both Symmetric and Asymmetric Operation

2.1. Generation Principle of Fluctuating Power under Symmetric Operation

The topology of MMC-SST is shown in Figure 1, and the equivalent model of the MMC-SST AC/DC stage is shown in Figure 2, where u_j, i_j and U_{mvdc}, I_{mvdc} represent the voltage and current of medium-voltage AC (MVAC) and medium-voltage DC (MVDC) sides (j represents a, b, and c); u_{ju}, i_{ju}, F_{ju} and u_{jd}, i_{jd}, F_{jd} represent the voltage, current, and

switching function of the upper and lower arms. The voltage of the MVAC side under symmetric operation is as follows:

$$\begin{cases} u_j = U_{\mathrm{m}}\cos(\omega t + \theta_j) \\ i_j = I_{\mathrm{m}}\cos(\omega t + \theta_j + \phi) \end{cases} \tag{1}$$

where U_{m} and I_{m} are the amplitudes of MVAC voltage and current, respectively; θ_{j} is the initial phase angle of phase j; ϕ is the power factor.

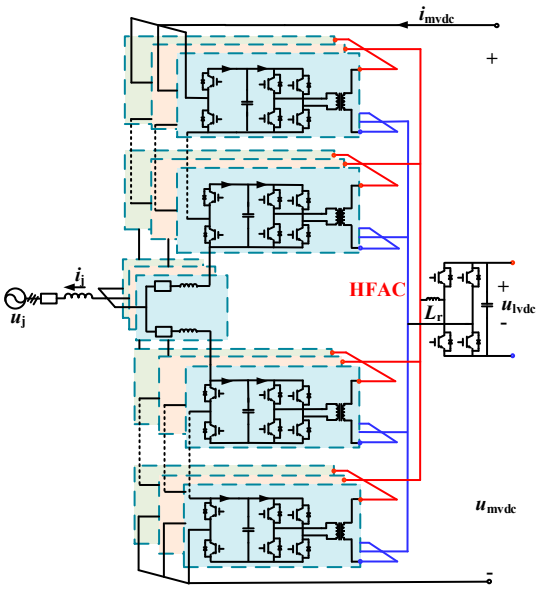


Figure 1. Topology of MMC-SST in the literature [18].

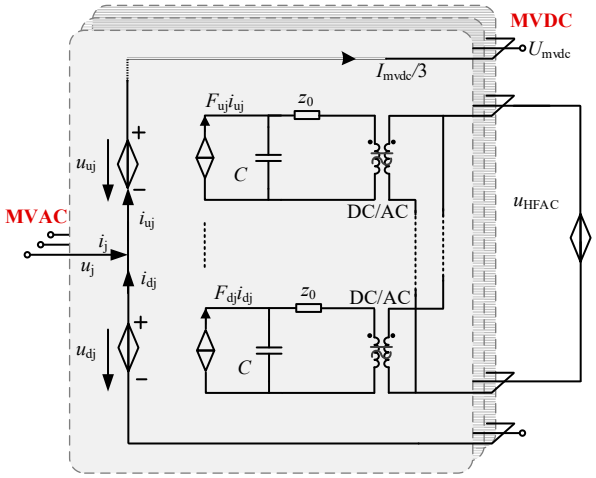


Figure 2. Equivalent model of MMC-SST AC/DC stage.

Taking the upper arm of phase j as an example, the voltage and current can be obtained from Kirchhoff's law as follows:

$$\begin{cases} u_{\mathrm{ju}} = \frac{1}{2}U_{\mathrm{mvdc}} - U_{\mathrm{m}}\cos(\omega t + \theta_{\mathrm{j}}) \\ i_{\mathrm{ju}} = \frac{1}{3}I_{\mathrm{mvdc}} + \frac{1}{2}I_{\mathrm{m}}\cos(\omega t + \varphi + \theta_{\mathrm{j}}) + I_{2\mathrm{j}}\cos(2\omega t + \theta_{2\mathrm{j}}) \end{cases} \tag{2}$$

The switching function of the upper arm can be obtained from the relationship between the voltage of the arm and the voltage of the MVDC bus:

$$F_{\mathrm{ju}} = \frac{u_{\mathrm{ju}}}{U_{\mathrm{mvdc}}} = \frac{1}{2}\left[1 - m\cos\left(\omega t + \theta_j\right)\right] \tag{3}$$

where m is the voltage modulation ratio of the MMC stage. Then, the current of the SM bus can be obtained as follows:

$$\begin{aligned} i_{\mathrm{cju}} \quad &= F_{\mathrm{ju}} i_{\mathrm{ju}} = i_{\mathrm{cju\_1}} + i_{\mathrm{cju\_2}} + i_{\mathrm{cju\_3}} = \tfrac{1}{6} I_{\mathrm{mvdc}} - \tfrac{1}{8} m I_{\mathrm{j}} \cos(\phi) \\ &- \tfrac{1}{6} m I_{\mathrm{mvdc}} \cos(\omega t + \theta_j) + \tfrac{1}{4} I_j \cos(\omega t + \phi + \theta_{\mathrm{j}}) - \tfrac{1}{4} m I_{\mathrm{j}} \cos(\omega t - \theta_{\mathrm{j}} + \theta_{2\mathrm{j}}) \\ &- \tfrac{1}{8} m I_{\mathrm{j}} \cos(2\omega t + \phi + 2\theta_{\mathrm{j}}) + \tfrac{1}{2} I_{2\mathrm{j}} \cos(2\omega t + \theta_{2\mathrm{j}}) \\ &- \tfrac{1}{4} m I_{2\mathrm{j}} \cos(3\omega t + \theta_{\mathrm{j}} + \theta_{2\mathrm{j}}) \end{aligned} \tag{4}$$

As can be seen from the above formula, the SM bus current includes a DC component and an AC component, and the latter is mainly based on the fundamental frequency $i_{\mathrm{cju\_1}}$, double frequency $i_{\mathrm{cju\_2}}$, and triple frequency $i_{\mathrm{cju\_3}}$. In the traditional MMC-SST, the AC component flows into the capacitor to form voltage fluctuations, resulting in the large size of the SM capacitor, which significantly reduces the power density of the system.

2.2. Fluctuating Power Decoupling Method in the Literature [18]

Based on the characteristics of current fluctuations of the SMs, the authors of [18] drew the following conclusions. In the AC component of the currents, the fundamental frequency components are three-phase positive-sequence symmetry, and the double-frequency components are negative-sequence symmetry, as shown in Figure 3. Since the suppression strategy of the arm circulating current is usually designed in conventional MMC, the triple-frequency component of the SM current caused by the arm circulating current can be ignored.

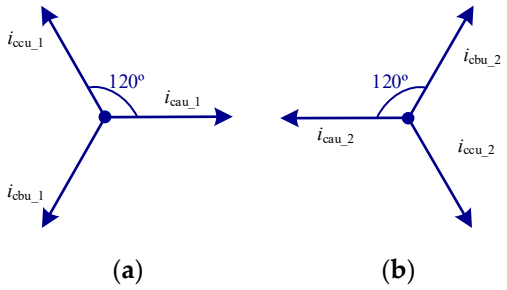


Figure 3. Characteristics of AC components of SM bus current: (**a**) fundamental frequency component; (**b**) double-frequency component.

The equivalent model of three-phase SMs and HFLs is shown in Figure 4, and the authors of [18] proposed that the primary side of the HFL adopt the synchronous modulation method. Due to the small loop impedance of the full-bridge structure of the HFL primary side, the three-phase SM capacitors exhibit switched-capacitor characteristics under synchronous modulation and are in a mutual clamping state, thereby preventing the fluctuation of the SM capacitor voltage from occurring. Ultimately, the fluctuating power is decoupled from the SM capacitor. The final current flow path of the three-phase SMs is shown in Figure 4, where the DC component realizes power exchange between the SM and the LVDC bus, and the AC component is mutually cancelled among the three phases.

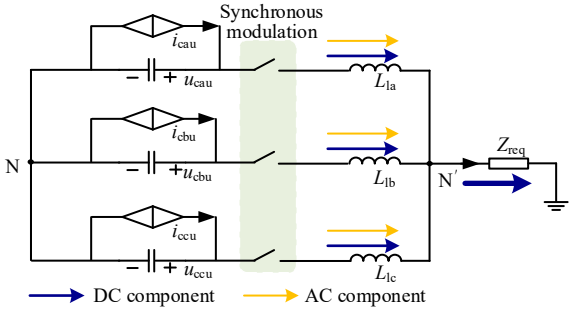


Figure 4. Flow path of three-phase SM currents.

After the ripple power is decoupled from the capacitor, the SM capacitor only needs to handle high-frequency switching harmonics, significantly reducing its size. The SM capacitance constraints of the traditional system and the MMC-SST can be obtained from the literature [18]:

$$C_{\mathrm{tra}} = \frac{I_{\mathrm{mvdc}}}{3m\omega\varepsilon U_{\mathrm{c}}\cos\phi}\left[1-\left(\frac{m\cos\phi}{2}\right)^2\right]^{\frac{3}{2}} \tag{5}$$

$$C_{\mathrm{MMC-SST}} = \frac{1}{6\varepsilon U_{\mathrm{mvdc}} f_{\mathrm{sm}}}\left(-\frac{I_{m\mathrm{vdc}}}{6}m^2 - \frac{I_m}{8}m^2 + \frac{I_m}{4}m\right) \tag{6}$$

2.3. Analysis of SM Current under Asymmetric Operation

The authors of [18] proposed the SM fluctuating power decoupling method based on synchronous modulation of the HFL primary method, which was realized using the three-phase symmetric property of SM fluctuating power. However, in the case of three-phase asymmetric operation, three-phase SM fluctuating power cannot achieve mutual cancellation, and the voltage fluctuations with large amplitudes will be generated under the capacitance constraint derived from Equation (6), which will cause larger arm circulating currents and MVDC bus voltage fluctuations.

Therefore, the SM capacitance constraints in [18] will no longer be applicable under three-phase asymmetric operation. In addition, the MMC-SST system is a three-phase interconnected structure whose internal flow mechanism and further impact on port power quality change. All of these need to be re-analyzed and new SM capacitance constraints need to be derived under three-phase asymmetric operation.

When a three-phase asymmetric fault occurs in the grid, the voltage and current will contain negative-sequence components. At this time, the grid-side phase-j voltage u_{j} and phase-j current i_{j} can be expressed as

$$\begin{cases} u_{\mathrm{j}} = U_{\mathrm{m+}}\cos(\omega t+\theta_{\mathrm{j+}}) + U_{\mathrm{m-}}\cos(\omega t+\theta_{\mathrm{j-}}) \\ i_{\mathrm{j}} = I_{\mathrm{m+}}\cos(\omega t+\phi_{\mathrm{j+}}) + I_{\mathrm{m-}}\cos(\omega t+\phi_{\mathrm{j-}}) \end{cases} \tag{7}$$

where $U_{\mathrm{m+}}$ and $U_{\mathrm{m-}}$ are the positive-sequence and negative-sequence voltage amplitudes, respectively, and $I_{\mathrm{m+}}$ and $I_{\mathrm{m-}}$ are the positive-sequence and negative-sequence current amplitudes. The phase-j voltage and current of the upper arms can be expressed as follows:

$$\begin{cases} u_{\mathrm{ju}} = \frac{1}{2}U_{\mathrm{mvdc}} - u_{\mathrm{j}} \\ i_{\mathrm{ju}} = I_{\mathrm{jdc}} + \frac{1}{2}i_{\mathrm{j}} \end{cases} \tag{8}$$

where U_{dc} is the MVDC-side voltage of the MMC, and I_{jdc} is the DC amount in the phase-j bridge arm current. The ratios of the positive- and negative-sequence voltage amplitudes to the MVDC-side voltage can be defined as λ_+ and λ_-.

$$\begin{cases} \lambda_+ = \frac{U_{m+}}{U_{\mathrm{mvdc}}} \\ \lambda_- = \frac{U_{m-}}{U_{\mathrm{mvdc}}} \end{cases} \tag{9}$$

Then, the upper arm switching function can be expressed as follows:

$$F_{\mathrm{ju}} = \frac{u_{\mathrm{ju}}}{U_{\mathrm{mvdc}}} = \frac{1}{2} - \lambda_+ \cos(\omega t + \theta_{j+}) - \lambda_- \cos(\omega t + \theta_{j-}) \tag{10}$$

Using (7)–(10), the fluctuating current of the upper arm SMs can be obtained as shown in (11). In (11), I_d is the DC part of the SM input current; $I_{f\text{-}1}$ and $I_{f\text{-}2}$ are the fundamental frequency component; I_{2f} is the double-frequency component, which is in negative sequence between three phases; $I_{2f\text{-}0}$ is also the double-frequency component, but it is in zero sequence between three phases. The phase sequence of each AC component is shown in Figure 5.

$$\begin{aligned} F_{\mathrm{ju}} i_{\mathrm{ju}} \quad = & \underbrace{\frac{1}{2} I_{\mathrm{jdc}} - \frac{1}{4}\lambda_+ [I_{m+}\cos(\theta_{j+} - \phi_{j+}) + I_{m-}\cos(\theta_{j+} - \phi_{j-})] - \frac{1}{4}\lambda_- [I_{m+}\cos(\theta_{j-} - \phi_{j+}) + I_{m-}\cos(\theta_{j-} - \phi_{j-})]}_{I_d} \\ & \underbrace{+\frac{1}{4}[I_{m+}\cos(\omega t + \phi_{j+}) + I_{m-}\cos(\omega t + \phi_{j-})]}_{I_{f-1}} \underbrace{-I_{jdc}[\lambda_+ \cos(\omega t + \theta_{j+}) + \lambda_- \cos(\omega t + \theta_{j-})]}_{I_{f-2}} \\ & \underbrace{+\frac{1}{4}\lambda_+ I_{m+}\cos(2\omega t + \theta_{j+} + \phi_{j+}) + \frac{1}{4}\lambda_- I_{m-}\cos(2\omega t + \theta_{j-} + \phi_{j-})}_{I_{2f}} \\ & \underbrace{+\frac{1}{4}\lambda_+ I_{m-}\cos(2\omega t + \theta_{j+} + \phi_{j-}) + \frac{1}{4}\lambda_- I_{m+}\cos(2\omega t + \theta_{j-} + \phi_{j+})}_{I_{2f\_0}} \end{aligned} \tag{11}$$

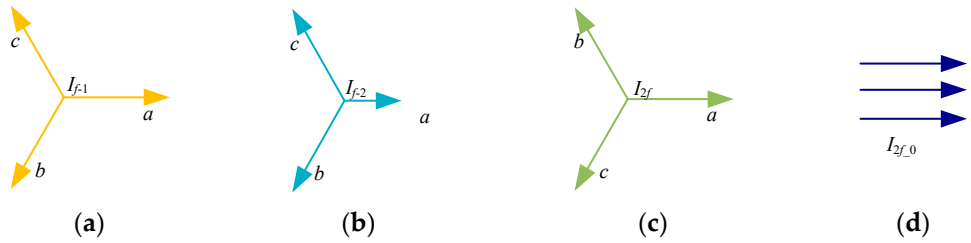


Figure 5. Phase sequence diagram: (**a**) first part of fundamental frequency component; (**b**) second part of fundamental frequency component; (**c**) double-frequency component; (**d**) zero-sequence part of double-frequency component.

During three-phase asymmetric operation, the amplitudes of AC and DC currents in the three-phase arms are no longer the same, so $I_{f\text{-}2}$ is not three-phase symmetric. At the same time, the zero-sequence component $I_{2f\text{-}0}$ is generated by the interaction of the positive- and negative-sequence voltage and current. Therefore, $I_{2f\text{-}0}$ cannot realize the offset by the HFL. Only I_{f1} and I_{2f} are still three-phase symmetric and cancel each other out. In summary, the low-frequency voltage fluctuation of SM cannot be eliminated completely under the asymmetric conditions, which does not satisfy the premise in [18].

The overall control block is shown in Figure 6. The MMC stage adopts an external MVDC voltage loop and an inner MVAC current loop control, and due to the existence of the high-frequency AC (HFAC) bus, the SM voltages can achieve self-balance, so as to simplify the control loop of the overall system. The modulation method of MMC stage is carrier phase shift SPWM (CPS-SPWM). The HFL stage adopts the phase shift PWM method, and the power flow between LVDC bus and SMs is realized by the phase shift angle. Under the control scheme of the MMC stage, as shown in Figure 6a, the AC-side current is kept balanced to avoid worse effects on the converter when the load is heavier. In the MMC-SST system, the zero-sequence component of the SM fluctuating current can be attenuated to a certain extent in this way, but there are still a large number of zero-sequence components caused by the asymmetry of the grid-side voltage. How the MMC-SST operates in this case will be analyzed in the next section.

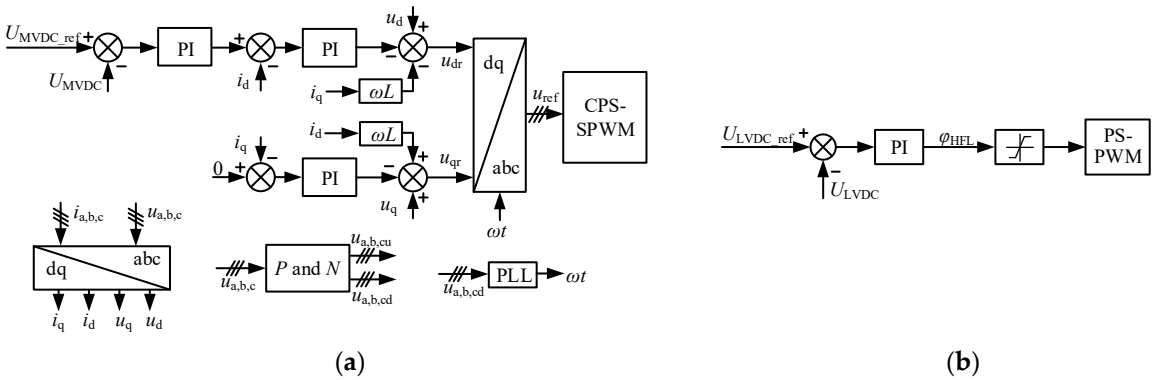


Figure 6. MMC control strategy: (**a**) MMC stage; (**b**) HFL stage.

3. Current Characteristics of SM under Asymmetric Operation

Under the HFL synchronous modulation, as shown in Figure 7, the SM capacitor works in the switched-capacitor mode, so the three-phase SM capacitors can be considered equivalent connecting in parallel, thereby mutually clamping each other. Therefore, the zero-sequence harmonic current generated by the three-phase asymmetric operation can be shared by all the three-phase SM capacitors connected in parallel.

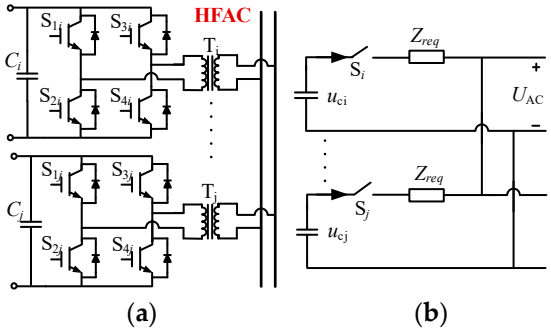


Figure 7. SM interconnected structure: (**a**) SM capacitor connection method; (**b**) equivalent parallel circuit.

Taking the amplitude drop of phase A as an example, it is assumed that U_m is the AC-side voltage amplitude during three-phase symmetric operation, and K_a is the unbalance coefficient (K_a can take values from 0 to 1). The phase-A voltage amplitude can be expressed as $U_a = K_a \cdot U_m$. Assuming that the initial phase angle of the grid-side voltage is 0, the positive- and negative-sequence voltages of the AC side obtained with the symmetric component method are as follows:

$$\begin{cases} u_{au} = \frac{K_a+2}{3} U_m \cos(\omega t) \\ u_{bu} = \frac{K_a+2}{3} U_m \cos(\omega t - 2/3\pi) \\ u_{cu} = \frac{K_a+2}{3} U_m \cos(\omega t + 2/3\pi) \end{cases} \tag{12}$$

$$\begin{cases} u_{ad} = \frac{1-K_a}{3} U_m \cos(\omega t + \pi) \\ u_{bd} = \frac{1-K_a}{3} U_m \cos(\omega t + \pi + 2/3\pi) \\ u_{cd} = \frac{1-K_a}{3} U_m \cos(\omega t + \pi - 2/3\pi) \end{cases} \tag{13}$$

When the current amplitude on the AC side is balanced, the currents of the upper arms can be expressed as follows:

$$\begin{bmatrix} i_{au} \\ i_{bu} \\ i_{cu} \end{bmatrix} = \frac{I_{mvdc}}{K_a+2}\begin{bmatrix} K_a \\ 1 \\ 1 \end{bmatrix} + \frac{I_{m+}}{2}\begin{bmatrix} \cos(\omega t+\varphi) \\ \cos(\omega t+\varphi-2/3\pi) \\ \cos(\omega t+\varphi+2/3\pi) \end{bmatrix} + \frac{I_{m-}}{2}\begin{bmatrix} \cos(\omega t+\varphi) \\ \cos(\omega t+\varphi+2/3\pi) \\ \cos(\omega t+\varphi-2/3\pi) \end{bmatrix} \quad (14)$$

Equation (9) can be rewritten as follows:

$$\begin{cases} \lambda_+ = \frac{K_a+2}{3}\frac{U_m}{U_{mvdc}} \\ \lambda_- = \frac{1-K_a}{3}\frac{U_m}{U_{mvdc}} \end{cases} \quad (15)$$

On the condition that the output power is constant and the AC-side current is balanced, the AC-side current amplitude under the grid voltage unbalance state can be expressed as follows:

$$I'_m = \frac{3}{K_a+2} I_m \quad (16)$$

According to (11)–(16), the low-frequency fluctuating current i_{sm} of the SM capacitors which cannot be offset by the HFL can be expressed as follows:

$$\begin{aligned} i_{sm} &= i_{cau} = i_{cbu} = i_{ccu} \approx \frac{F_{au}i_{au}+F_{bu}i_{bu}+F_{cu}i_{cu}}{3} \\ &= -\frac{2I_{mvdc}(1-K_a)}{3(K_a+2)}(\lambda_+-\lambda_-)\cos(\omega t) + \frac{1}{4}\lambda_- I'_m \cos(2\omega t+\varphi) \end{aligned} \quad (17)$$

4. Analysis of Asymmetric Fault Ride-through Capability of MMC-SST

To more clearly describe the performance and characteristics of the MMC-SST in three-phase asymmetric operation, the waveforms used in the analysis are simulated waveforms with the same operating conditions as those in [18], which are as follows: rated power, 1 MW; MVDC voltage, 12 kV; MVAC line-to-line voltage, 6 kV; LVDC voltage, 750 V; number of SMs per arm, 4; SM capacitance, 20 μF; fundamental frequency, 50 Hz; switching frequency of MMC stage, 2 kHz; DC/DC stage, 10 kHz.

4.1. Impact on HFL

In the single-phase voltage drop fault, the single-phase-to-ground short-circuit fault has the most serious consequences. Therefore, in order to analyze the impact of asymmetric faults on HFL, the HFL input current is analyzed in normal and single-phase-to-ground short-circuit fault conditions. Figure 8a,b show the input currents of the HFL during normal conditions and when the phase-A voltage drops to 0, respectively. In Figure 8b, the current flowing into the HFL is no longer symmetric.

The results in Figure 8c,d were obtained after filtering out the high-frequency harmonics. The DC, fundamental frequency, and double-frequency contents of the current are shown in Figure 8e,f. Under normal conditions, the contents of each part in the three phases are the same. When the voltage of phase A drops to 0 and the output power remains unchanged, the fundamental frequency component in the HFL current increases by 63.5%, indicating that the AC-side input current increases. Because the voltage of phase A drops, the power that can be output by phase A is reduced, and the DC content in phase A is lower than that of the other two phases, with phase A providing 18.4% power and phase B and phase C each providing 40.8% power.

In summary, when the power grid is operating asymmetrically, the internal current characteristics of the MMC-SST change due to its three-phase interconnected structure, and the core change is that the DC components of the HFL three-phase input currents are no longer the same. In addition, as the phase-A voltage of the MVAC port drops and the power remains constant, the fundamental frequency component in the AC component becomes larger and no longer exhibits three-phase symmetry.

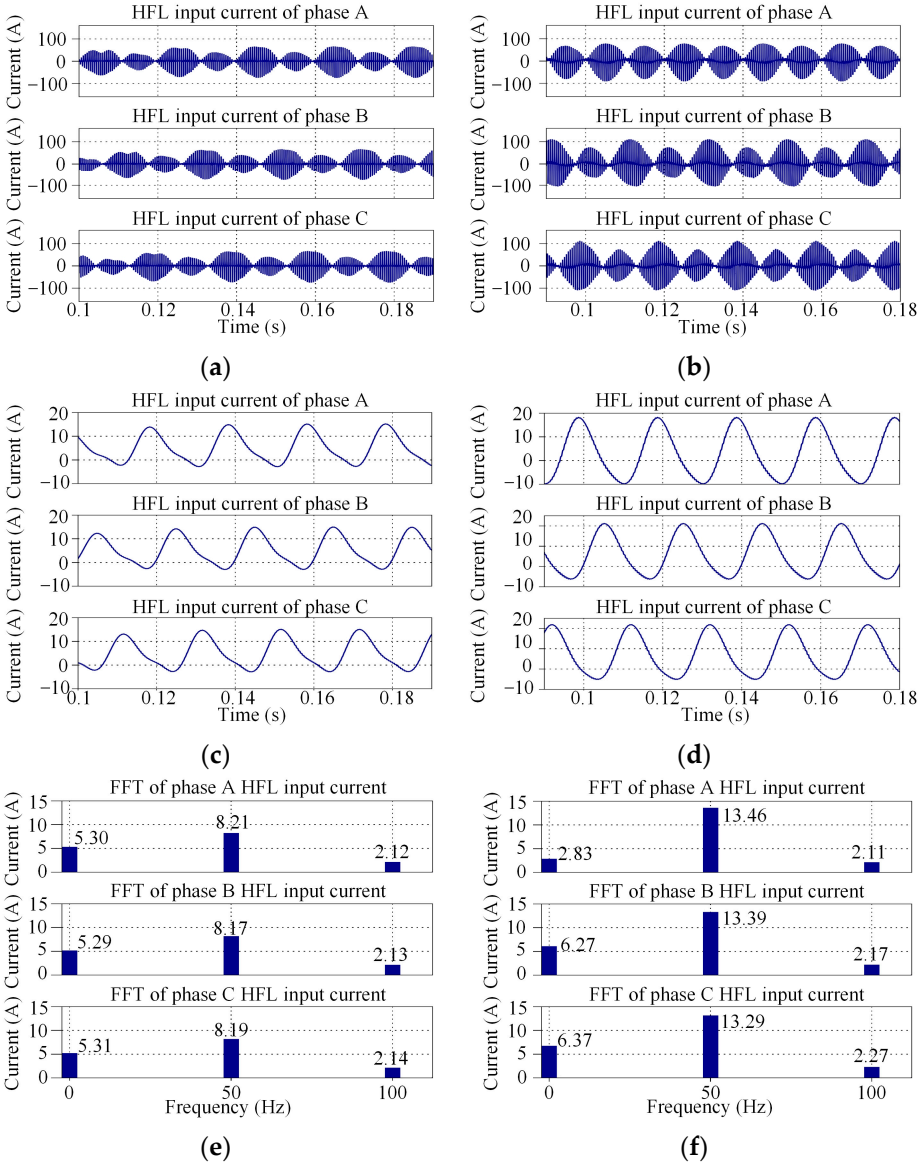


Figure 8. Input current of HFL: (**a**) HFL input current in normal state; (**b**) HFL input current in asymmetric state; (**c**) filtered HFL input current in normal state; (**d**) filtered HFL input current in asymmetric state; (**e**) Fourier analysis in normal state; (**f**) Fourier analysis in asymmetric state.

4.2. Impact on SM Voltage and MVDC Current with Input AC Current Control

Figure 9 shows all SM voltage waveforms during asymmetric operation. The parameter of the SM capacitor in [18] only considers the three-phase symmetric state, and the capacitance is 20 μF. It can be seen from Figure 9 that even if the phase-A voltage drops to 0, the voltages of all SMs are the same under different voltage sags, which indicates that the topology can still achieve voltage clamping under an asymmetric state. However, when the voltage drop is more than 30%, the SM voltage fluctuation will exceed 5%, which will increase the voltage and current stress of the switching device, increase the device loss, and threaten the system's safety. Switching devices are usually selected according to 1.5 to 2 times the rated voltage and current. It can be seen from Equation (16) that when the current amplitude of the AC side is 0, the amplitude increases the most seriously to about 1.5 times that of the normal case, and SM voltage fluctuation is within 18.3%. The voltage and current stress experienced by the switching devices are all within the margin range.

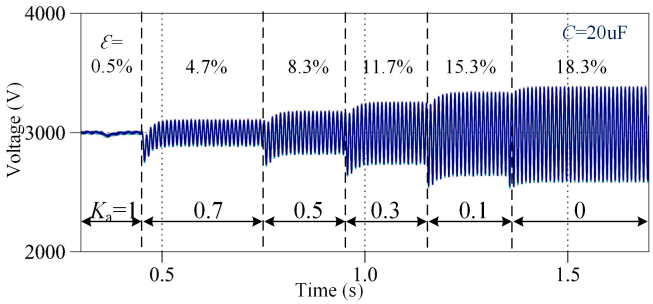


Figure 9. SM voltage with 20 μF capacitor during grid-side voltage asymmetric operation.

Unbalanced voltage faults cause power fluctuations on the MVDC side, as shown in Figure 10. When the MMC-SST operates symmetrically in three phases, the MVDC bus current fluctuation is only 0.3%, and when the voltage of phase A drops to 0, the MVDC bus current fluctuation reaches 16.2%. According to the usual device selection principle, the peak current fluctuation is still within the safety margin of the device. If the fault is not solved in time, the power quality of the load side will be affected.

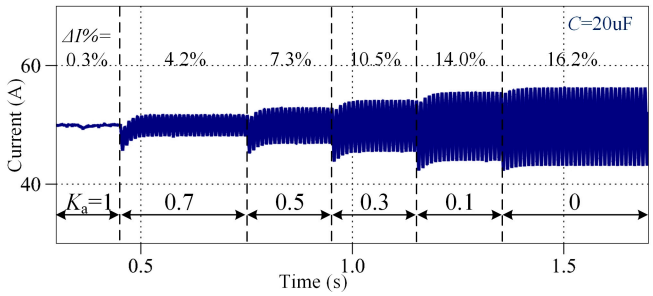


Figure 10. MVDC current with 20 μF capacitor during grid-side voltage asymmetric operation.

In summary, when the MMC-SST runs asymmetrically, the three-phase SM fluctuating power cannot completely cancel itself because it is no longer symmetric, resulting in low-frequency fluctuations in the SM capacitor voltage, and the three-phase asymmetry leads to DC bus current fluctuations, reducing the MVDC bus distribution quality.

4.3. Performance of Three-Phase Voltage Unbalanced Operation

Figure 11 shows the grid-side voltage and current waveforms, which maintain relative balance when the phase-A voltage drops to 0. The system can still operate normally under the fault condition and can achieve unbalanced voltage fault ride-through under the control shown in Figure 6. However, unbalanced voltage faults cause power fluctuations on the MVDC side, reducing the quality of power conversion.

Although the switching device operates within the margin range during faults, large fluctuations still threaten system safety. In order to ensure the safe and stable operation of the system before the fault is removed, this study re-analyzed the new constraint of SM capacitance under asymmetric faults. The above analysis and simulation waveforms were based on the consistency of parameters of HFL and three-phase SM cascade circuits. In actual engineering, the parameters are biased, which has a potential impact on the above analysis, which is also a problem worthy of attention in future in-depth research.

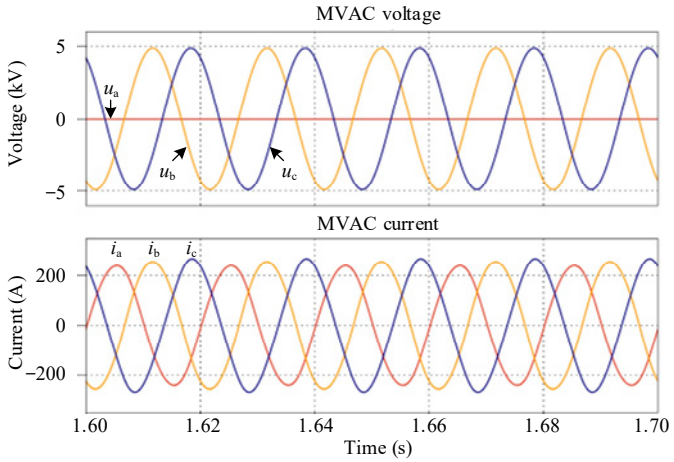


Figure 11. MVAC current with 20 μF capacitor during grid-side voltage asymmetric operation.

5. Capacitance Constraint of SM in Asymmetric Operation

From the analysis in Section 4, it can be seen that in the event of a single-phase voltage drop, the MMC-SST system in [18] can still operate stably. However, the SM voltage fluctuation and the current fluctuation on the MVDC side will increase with the degree of voltage drop. If the fault is not solved in time, the fluctuation can seriously affect the safety of the device. To ensure that the system can achieve safer asymmetric fault ride-through and reduce the impact on the switch and MVDC side during the fault period, it is necessary to use a capacitor suitable for asymmetric operation to suppress fluctuations.

Based on the mathematical model shown in Equation (17), the relationship between the SM current i_{sm} and the asymmetric coefficient K_a and the phase angle is shown in Figure 12. When $K_a = 1$, i.e., when the grid operates symmetrically, the three-phase SM currents are mutually cancelled based on symmetry, so that the SM current i_{sm} remains zero throughout the full AC cycle. As K_a decreases continuously, i.e., as the degree of three-phase asymmetry gradually increases, i_{sm} also increases. When K_a is 0, i.e., when the voltage in phase A drops to 0, i_{sm} reaches its maximum value. In MMC-SST operation under asymmetric conditions, the SM current i_{sm} reaches its peak value when $\omega t = \pi$, and its valley value when $\omega t = \pi/2$.

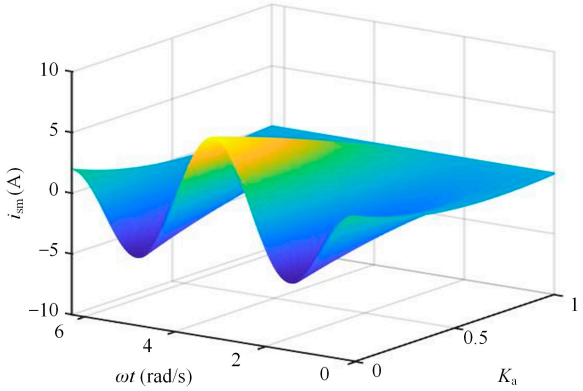


Figure 12. Graph showing relationship between i_{sm}, ωt, and K_a.

The above-mentioned changes clearly indicate that the higher the degree of three-phase asymmetry, the larger the magnitude of the SM current i_{sm}, and, consequently, the larger the SM capacitor voltage fluctuation.

In addition, it can be seen that in a line-frequency cycle, the capacitor is charged when i_{sm} is more than 0, and the capacitor is discharged when i_{sm} is less than 0. According to (14)–(17), the SM current i_{sm} can be rewritten as follows:

$$i_{sm} = -\frac{2(1-K_a)(2K_a+1)U_m}{9(K_a+2)U_{mvdc}} I_{mvdc}\cos(\omega t) + \frac{(1-K_a)U_m}{4(K_a+2)U_{mvdc}} I_m \cos(2\omega t + \varphi) \quad (18)$$

When operating under an asymmetrical grid voltage, the amplitude of SM current fluctuation is mainly determined by the voltage imbalance factor K_a, as well as the voltage and current amplitudes at the MVAC and MVDC ports, U_m, I_m, U_{mvdc}, and I_{mvdc}.

When operating under a symmetrical three-phase voltage, i.e., $K_a = 1$, from the above equation, it can be seen that the SM current is $i_{sm} = 0$ at this time, meaning that the fluctuating currents between SMs are mutually cancelled based on the three-phase symmetry. When $K_a < 1$, as K_a decreases, the SM current increases continuously, reaching its maximum value when $K_a = 0$. The zero-crossing point of i_{sm} can be calculated as follows:

$$\begin{cases} S_1 = \arccos\frac{4I_{mvdc}+8K_aI_{mvdc}+\sqrt{2}\sqrt{8I_{mvdc}^2(2K_a+1)^2+81I_m^2}}{18I_m} \\ S_2 = \arccos\frac{4I_{mvdc}+8K_aI_{mvdc}-\sqrt{2}\sqrt{8I_{mvdc}^2(2K_a+1)^2+81I_m^2}}{18I_m} \end{cases} \quad (19)$$

Because the SM capacitor voltage is always greater than zero, the maximum energy absorbed or released by the SM capacitor in a line cycle can be obtained by integrating the power between the two zero-crossing points of the SM current i_{sm}. Assuming that the voltage fluctuation rate generated by i_{sm} in one switching cycle is ε, the capacitance required by the SM during asymmetric operation to suppress the low-frequency zero-sequence fluctuating current can be expressed as follows:

$$\begin{aligned} \Delta C &= \frac{\Delta Q}{\varepsilon U_c} = \frac{\int_{S_1}^{S_2} i_{sm} d(\omega t)}{\omega\varepsilon U_c} \\ &= \frac{U_m}{\omega\varepsilon U_c U_{mvdc}} \frac{(1-K_a)}{(K_a+2)} \left\{ \frac{I_m}{8}[\sin(2S_2) - \sin(2S_1)] - \frac{2I_{mvdc}(2K_a+1)}{9}[\sin(S_2) - \sin(S_1)] \right\} \end{aligned} \quad (20)$$

With the same parameter requirements as the simulation platform in [18], under the condition of $\varepsilon = \pm 5\%$, the relationship between C and K_a is shown in Figure 13, and C can be obtained as follows:

$$C = C_{MMC-SST} + \Delta C \quad (21)$$

where $C_{MMC\text{-}SST}$ can be obtained from the SM capacitance constraint of the MMC-SST as shown in Equation (6). As shown in Figure 13, when $K_a > 0.2$, the required capacitance level is 10 μF. When $K_a < 0.2$, the required capacitance level is 100 μF. When K_a is 1, the capacitance is still determined according to [18].

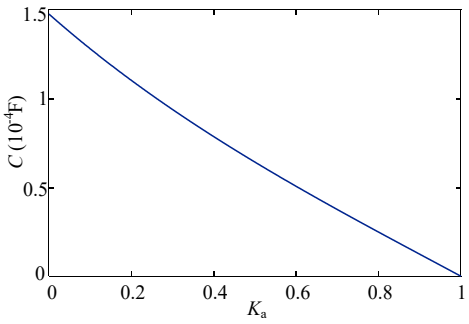


Figure 13. Graph showing relationship between C and K_a.

Generally, three-phase asymmetry is the result of grid faults such as short-circuiting, and long-term large asymmetry is not allowed for medium- and high-voltage nets; thus,

the capacitor would be evaluated according to the fault ride-through operation. The grid connection requires the system to have the ability to run stably for 625 ms when the voltage drops to 20%. When the voltage drops by 80%, that is, K_a is 0.2, the SM capacitor is set to 100 μF according to (19). In Figure 14, the SM voltage fluctuation is significantly suppressed, and even if the phase-A voltage drops to 0, the SM voltage fluctuation is still within 5%.

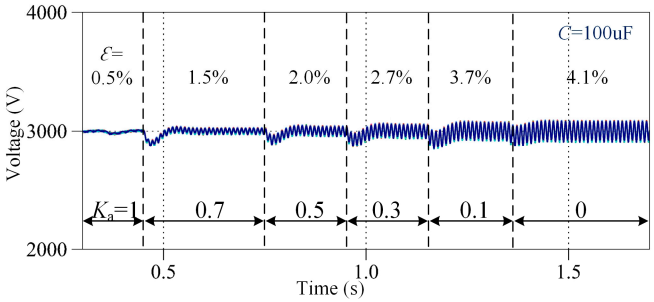


Figure 14. SM voltage with 100 μF capacitor during grid-side voltage asymmetric operation.

Figure 15 shows the current ripple on the MVDC side when the system operates with a 100 μF capacitor. Comparing Figure 9, it can be seen that the fluctuation has been significantly suppressed. Although the capacitance value determined by considering unbalanced voltage is an order of magnitude higher than that in [18], it still has great advantages compared with other types of reduced capacitance schemes.

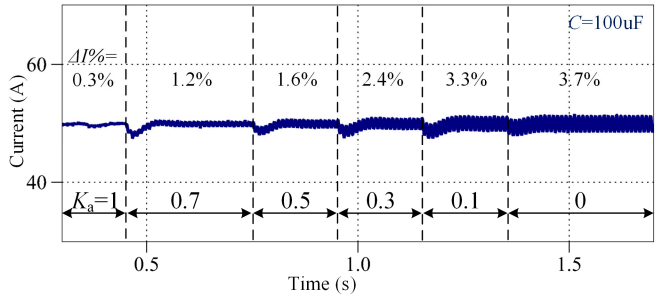


Figure 15. MVDC current with 100 μF capacitor during grid-side voltage asymmetric operation.

6. Experimental Verification

To further verify the reliability of the system operating under asymmetric state, the experimental verification of asymmetric operation is carried out under the experimental power level in [18]. Under the condition of $\varepsilon = \pm 5\%$, the SM capacitance in [18] is 35 μF under symmetric operation. The asymmetric operation test case in the experiment is a 50% voltage drop of phase A, and the capacitance constraint derived from Equation (20) is 85 μF. The experimental parameters are summarized in Table 1, and the prototype is shown in Figure 16.

Table 1. Experimental parameters.

Parameters	Value
Rated active power/P	5 kW
MVDC voltage/u_{MVDC}	750 V
MVAC voltage/u_{x}	375 V
LVDC voltage/u_{LVDC}	250 V
Fundamental AC frequency/f	50 Hz
CPS PWM frequency/f_{SM}	2 kHz
Arm inductance/L_{arm}	2.5 mH
Capacitance of SM/C	85 μF
Number of SMs per arm/n	3

Table 1. *Cont.*

Parameters		Value
Transformer turns ratio/n_t		1:1
HFL switching frequency/f_1		20 kHz
MMC voltage controller	proportional gain	0.176
	integral gain	35.2
MMC current controller	proportional gain	5.3
	integral gain	113.3
HFL voltage controller	proportional gain	0.02
	integral gain	655

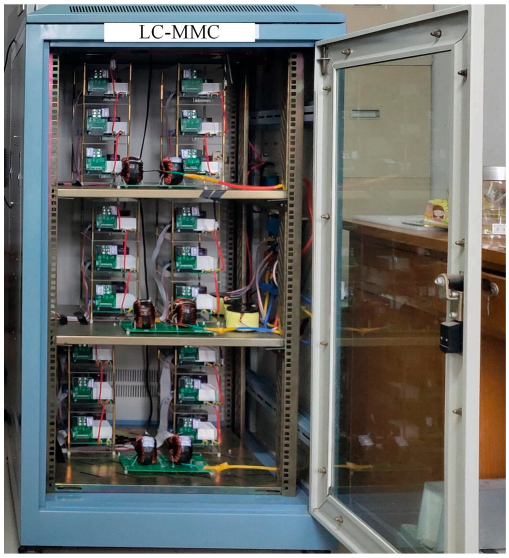


Figure 16. Experimental prototype.

6.1. Asymmetric Operation Verification

When the MMC works in the inverter state, the voltage of the phase-A load drops to 50% of the voltages of phases B and C. Figure 17 shows the load voltage and current waveforms on the AC side of phases A and B. The AC output current is kept symmetric when the voltage of phase A drops to 50%.

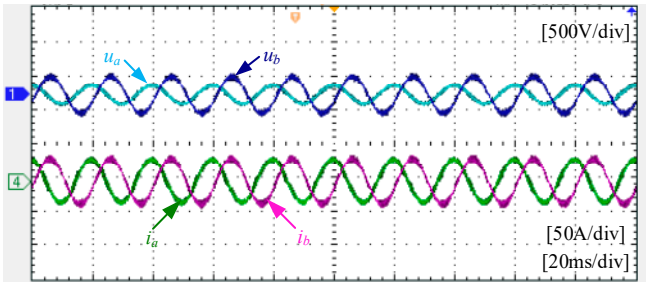
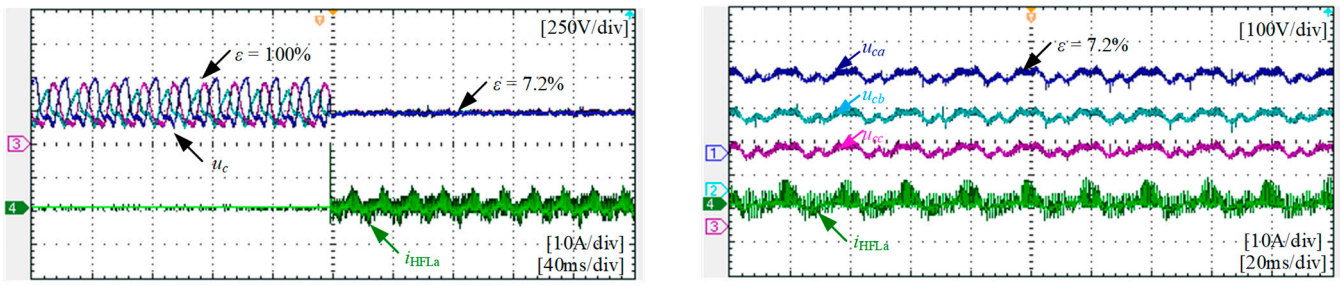


Figure 17. Experimental results of AC-side voltage asymmetry operation.

Figure 18 shows the three-phase SM voltage and HFL input current of phase A during asymmetric operation. It can be seen from Figure 18a that the SM voltages fluctuate greatly and are not symmetric during asymmetric operation. After switching to the HFL, the SM voltage fluctuation is significantly reduced and the voltage equalization is achieved. It can be seen from Figure 18b that the capacitor voltage fluctuation rate is 7.2%. The SM capacitor voltage fluctuation rate is 4% during symmetric operation in [18]. The 50% drop in the output voltage of phase A in the MVAC side will increase the SM voltage fluctuation

in the system, but it can still run safely and stably. Figure 19 shows the test waveforms of the MMC-SST under symmetric operation conditions. Due to the increased SM capacitance constraint determined in this study compared to that in [18], the SM voltage fluctuation rate is only ±1.6%.



(**a**) (**b**)

Figure 18. Experimental results of the three-phase SM voltage and the phase-A HFL input current when the HFL is put into operation: (**a**) dynamic process of HFL input; (**b**) steady-state results after HFL input.

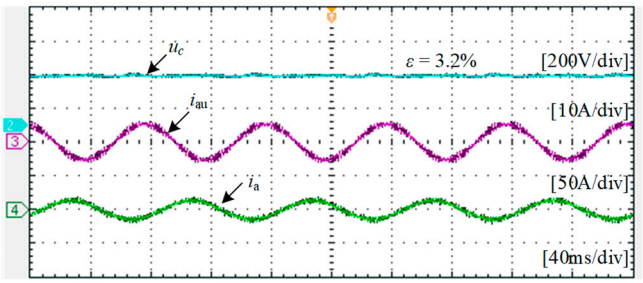


Figure 19. Experimental results of the MMC-SST under symmetric operation.

Table 2 summarizes the comparison results of the performance of the two capacitance constraints in symmetric and asymmetric operation conditions. The SM capacitance calculated using the traditional MMC-SST capacitance constraint in Equation (5) is 550 μF. According to [18], after the SM capacitor lightweighting design in the MMC-SST, the SM capacitance is 35 μF, with a symmetric operation SM voltage fluctuation rate of ±4%, which meets the safety standard of ±5%. However, in asymmetric operation, the SM voltage fluctuation rate reached ±16.7% as calculated, exceeding the safety range. The new SM capacitance constraint re-analyzed in this study for the MMC-SST is 85 μF, with symmetric operation SM capacitance voltage fluctuation of ±1.6% and asymmetric operation SM capacitance voltage fluctuation of ±3.6%, both within the safety range.

Table 2. Comparison of SM capacitance constraints.

	MMC-SST in [18]	**This Article**
SM capacitance	35 μF	85 μF
Reduction compared to traditional MMC-SST	93.6%	84.5%
SM voltage fluctuation rate under symmetric operation	±4%	±1.6%
SM voltage fluctuation rate under asymmetric operation	±16.7%	±3.6%

Voltage asymmetry is a typical operating condition, and this study focused on the analysis of operation under voltage asymmetry and the derivation of SM capacitor constraints for MMC-SST grid-tied systems. In both off-grid and grid-forming states, voltage asymmetry can have various causes, such as large single-phase loads and different short-

circuit ratios between phases, which may pose potential threats to system stability [29,30] and will be a key focus in future research.

6.2. Dynamic Performance Verification

Figure 20 shows the waveforms of the SM voltage on the upper arm of phase A and the output voltage on the LVDC side. When the system operates under asymmetric conditions, the load is connected to the LVDC side and the SM voltage remains stable, that is, the system can still operate stably when the system is connected to the LVDC-side load during asymmetric operation. Figure 21 shows the experimental results of the power side of MVDC, where the power is stepped from 50% to 100%. During the dynamic process, the response of the power step process is relatively fast. Moreover, the SM voltage is not greatly disturbed and can maintain stability. The experimental results show that the dynamic characteristics are good under the SM capacitance constraint redetermined in this study.

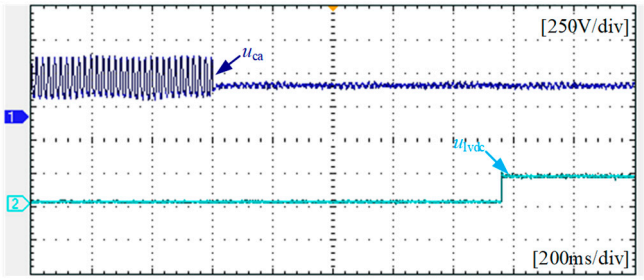


Figure 20. Experimental results of the dynamic process of the LVDC-side access load.

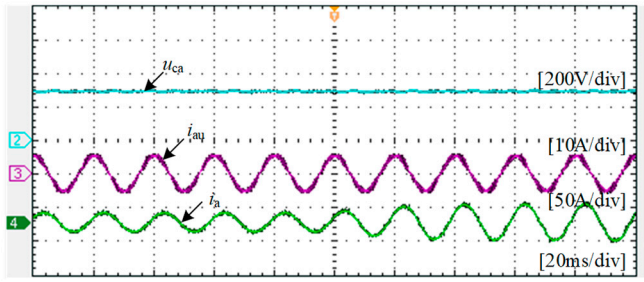


Figure 21. Experimental results of the dynamic process of MVAC power increasing.

7. Conclusions

When the grid voltage experiences an asymmetric fault, the precondition that failed for the MMC-SST in [18] can completely eliminate the SM voltage fluctuation under small capacitance value conditions. In this study, the capacitor current of SMs and the operating characteristics in the MMC-SST under asymmetric conditions were analyzed. As shown above, when the grid-side voltage is unbalanced, the system can still achieve SM automatic voltage equalization, but the SM fluctuating power cannot be completely eliminated by the HFL. When the grid-side voltage drops by more than 30%, the SM voltage fluctuation in the low-SM-capacitance MMC-SST system is large and cannot guarantee safe operation, and the DC-side power fluctuates significantly.

A new SM capacitor capacitance constraint relationship related to the degree of voltage drop was obtained. Selecting the capacitor under this constraint can ensure that the SM voltage fluctuation is within a safe range, and the DC-side power fluctuation is relatively small, which ensures that the system completes asymmetric fault ride-through. The new capacitance constraint is higher than that in [18], but it still has significant advantages in capacitance compared with traditional MMC-SSTs.

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