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Curvature-Compensated Bandgap Voltage Reference with Low Temperature Coefficient

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Abstract: Resistance errors in bandgap reference (BGR) circuits often cause deviations in design indicators, and it is true that utilizing various compensation techniques mitigates the impact of resistance errors. In this paper, an original BGR circuit with 180 nm BCD processing is presented, which uses an improved high-order compensation and curvature compensation. The proposed BGR contains four main blocks, including a start-up stage, a first-order temperature compensation stage, a high-order temperature compensation stage, and a curvature compensation stage. Meanwhile, a trimming resistor array structure is designed to revise the temperature coefficient (TC) deviation of the test output voltage from the theoretical design value. Through wafer-level laser trimming technology, the measurement results are achieved with very little difference from the theoretical design value. The proposed BGR provides a stable reference voltage at 1.25 V with a low TC and strong power supply rejection (PSR). Within temperatures ranging from −45 °C to 125 °C, the measured TC shows an optimal value at 4.2 ppm/°C and the measured PSR shows −100 dB.

Keywords: bandgap reference; high-order temperature compensation; curvature compensation; low temperature coefficient; high power supply rejection ratio

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1. Introduction

Bandgap reference (BGR) is essential to all types of integrated circuits [1–3] as outstanding chip properties are dependent on power supply stability. An ideal power supply can effectively prevent the system from being interfered with by temperature fluctuation and noise [4–7]. To mitigate the negative impact on power supply induced by various non-ideal factors in practical working scenarios, it is important to develop an inner power supply which is insensitive to temperature and outer power supply fluctuation [8–10]. Therefore, the invention of bandgap reference has met this demand and has greatly improved chip performance.

With the development of chip manufacture technology, a shrinking chip size has become an irreversible trend, which results in decreasing the channel length of MOSFETs in CMOS technology. Therefore, improving performance has become even more challenging. Bandgap reference with a high power supply rejection (PSR) and a low temperature coefficient (TC) is always required in chip design. In practice, there is a significant difference between the simulated and tested values of BGR, which is attributed to resistance errors and material errors during chip processing [11–15]. Generally speaking, the improvement of TC mainly depends on the adjustment of resistance [16,17], but, in practice, it has been found that resistance value errors always lead to deviations in TC. In order to compensate

for the insufficient resistance precision, the method of relative error of resistance is often used [18–21]. By setting a set of resistors with consistent aspect ratios in the temperature compensation circuit and output circuit, the large TC caused by insufficient resistance precision can be avoided.

This work proposes improved high-order compensation and curvature compensation to address the changes in TC caused by resistance errors. At the same time, a trimming resistor array [22–24] is designed, and the metal wires at both ends of the resistor are cut short using laser trimming technology to modify the resistance value. The laser trimming method uses a laser beam with a 10 μm diameter to cut the resistor array, which can be operated on the wafer. As a result, the precise adjustment in the reference voltage and TC is achieved, and it can be operated in batches, ultimately forming a batch of stable high-performance products.

This paper is organized as follows: Section 2 introduces principles that guide the design of the proposed BGR. Section 3 presents the simulation results of various performance parameters of the BGR, while Section 4 gives the conclusion.

2. Principles of the Proposed BGR

Bandgap reference utilizes electrical devices with different temperature coefficients to achieve a reference voltage or current insensitive to temperature and supply voltage fluctuation. Typically, due to good stability and repetitiveness, BJTs have become the core of those circuits, whose base-emitter voltage V_{BE} can be written as a function of temperature [25–28]:

$$V_{BE} = V_{g0} - \frac{T}{T_k}\left[V_{g0} - V_{BE}(T_k)\right] - (\eta - \alpha)V_T \ln\left(\frac{T}{T_k}\right) \quad (1)$$

where V_{g0} is the base-emitter voltage of BJT when $T = 0\ K$, η is a process-dependent constant ranging from 3.6 to 4, and α is the index of collector current I_C to the absolute temperature T.

Principles of all types of BGR derive from this equation. By introducing different coefficients to each term, it is possible to eliminate temperature-dependent terms. For instance, first-order temperature compensation can be realized by simply adding up the PTAT current (current proportional to the absolute temperature) and the CTAT current (current complementary to the absolute temperature) produced by V_{BE} and the voltage difference ΔV_{BE} between two BJTs with different current densities, respectively. The typical value of BGR output is around 1.25 V. As high-order terms in Equation (1) still exist, the temperature coefficient (TC) of first-order temperature compensation BGR is usually above 10 ppm/°C. Therefore, other types of compensation are required to achieve a lower TC.

The block diagram of the proposed BGR is given in Figure 1. As is shown in Figure 1, besides a start-up circuit stage, a current mirror and a first-order temperature compensation stage, the proposed BGR consists an improved high-order temperature compensation stage and a curvature compensation stage, which are both effective in improving the TC. The main function of the start-up circuit is to provide the initial state for BGR during the power on process, ensuring that the current mirror can output current normally. The first-order temperature compensation circuit is mainly used for the initial temperature compensation of the current generated by the current mirror. The high-order compensation circuit is used for the secondary temperature compensation of the current after the initial temperature compensation. The curvature compensation circuit is used for the higher-order compensation of the current after the secondary temperature compensation, ultimately obtaining a current that is minimally affected by temperature, which is further converted into a reference voltage V_{ref} that is minimally affected by temperature through resistance. The two compensation methods will be explained in detail in the following sections. Figure 2 shows the start-up circuit and first-order temperature compensation circuit of BGR. In the start-up circuit, a transient mirror current is provided to the first-order temperature compensation circuit after powering on, which is fed back to the start-up circuit through an

internal differential amplifier to stabilize the mirror current. After the power on process is completed, the start-up circuit stops working. At this time, Q2 and Q1 form a bandgap temperature compensation circuit, outputting PTAT (I_1) and CTAT (I_2) currents. Resistor R_3 is the trimming resistor module of the first-order temperature compensation circuit, where the laser continuous trimming technology may be used to obtain compensation currents that are close to the design values.

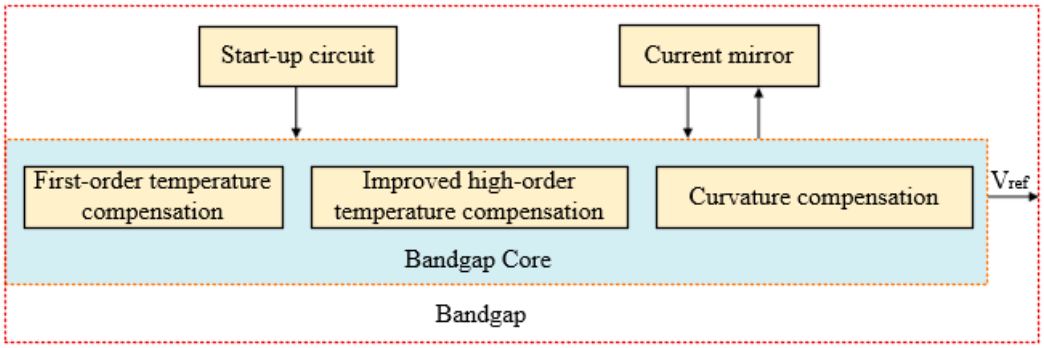


Figure 1. The block diagram of the proposed BGR.

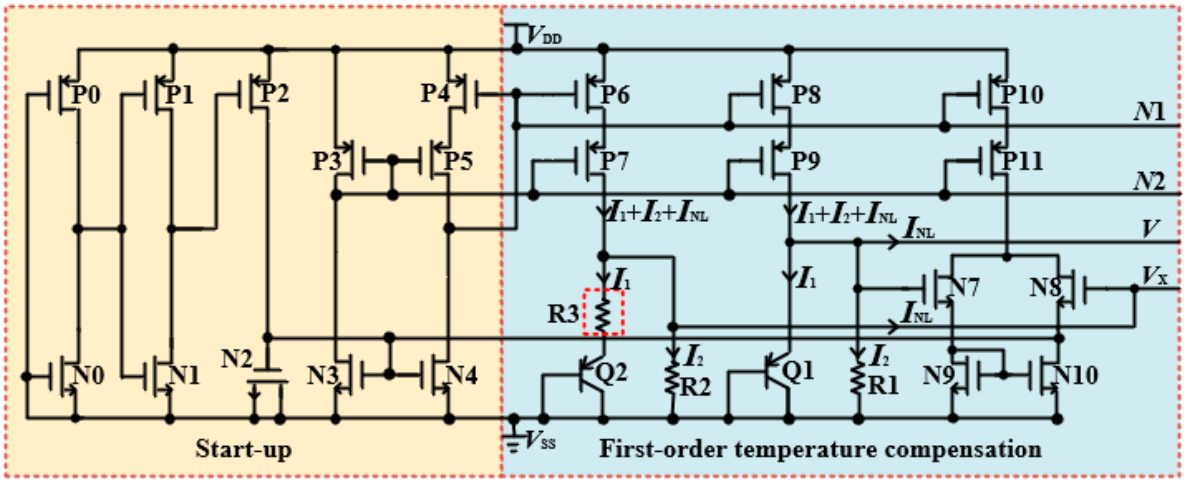


Figure 2. BGR with start-up and first-order temperature compensation (R3 in the dashed box is a resistor module used for trimming).

2.1. High-Order Temperature Compensation

High-order temperature compensation aims to eliminate the logarithmic term $(\eta - \alpha)V_T \ln\left(\frac{T}{T_k}\right)$ in Equation (1), which can be solved by introducing a logarithmic current. Assuming two BJTs with two types of bias current, one is the PTAT current; the other is temperature-independent. According to this assumption, the V_{BE} of the two BJTs can be written as

$$V_{BE1} = V_{g0} - \frac{T}{T_k}\left[V_{g0} - V_{BE}(T_k)\right] - (\eta - 1)V_T \ln\left(\frac{T}{T_k}\right) \quad (2)$$

$$V_{BE2} = V_{g0} - \frac{T}{T_k}\left[V_{g0} - V_{BE}(T_k)\right] - (\eta - 2)V_T \ln\left(\frac{T}{T_k}\right) \quad (3)$$

If we apply $V_{BE1} - V_{BE2}$ to resistor R_{NL}, a logarithmic current I_{NL} will be produced. I_{NL} can be expressed by

$$I_{NL} = \frac{\Delta V_{BE}}{R_{NL}} = \frac{V_T}{R_{NL}} \ln\left(\frac{T}{T_0}\right) \quad (4)$$

By adding I_{NL} to the PTAT(I_1) current and the CTAT(I_2) current generated by first-order temperature compensation BGR, the high-order terms in Equation (1) can be eliminated. However, we assume that the two BJTs have the same $V_{BE}(T_k)$ as previously to achieve Equation (4), which is not the case in the actual circuit. Therefore, errors should exist in the practical reference voltage produced by the BGR based on this principle. To solve the problem, improved high-order temperature compensation is utilized in the proposed BGR given in Figure 3. In this structure, OTA adopts a voltage following method, which produces an isolation effect and prevents the I_{NL} current from flowing into the transistor Q3 (I_{NL} flowing into the Q3 will cause the $I_1 + I_2 + I_{\mathrm{NL}}$ mirror compensation current to be introduced with an additional current, thereby affecting the operation of the high-order compensation circuit). From Equation (4), it can be seen that OTA with voltage following ensures that the threshold voltage of the Q3 and Q1 transistors forms a voltage difference ΔV_{BE} at both ends of the R_{NL}, further obtaining the current I_{NL} with high-order temperature compensation characteristics, which reduces the TC value to some extent.

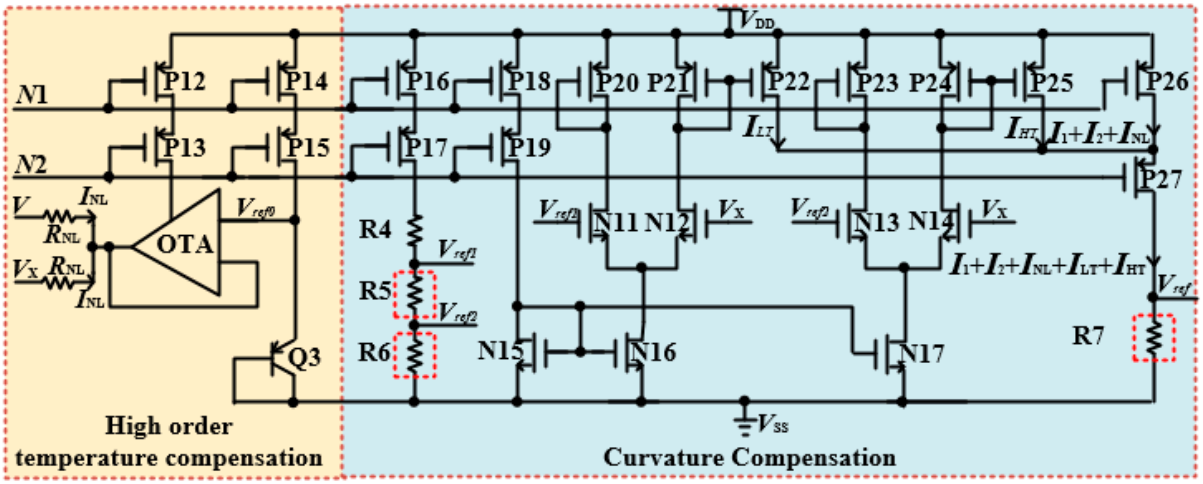


Figure 3. BGR with high-order temperature compensation and curvature compensation (R5–R7 in the dashed box are resistor modules used for trimming).

2.2. Curvature Compensation

Another effective high-order temperature compensation is curvature compensation, the basic idea of which is diving a certain temperature range into several sub-ranges and introducing compensation to each part. As is shown in Figure 3, I_1 is the PTAT current while I_2 is the CTAT current. P_{16} and P_{17} mirror the sum of $I_1 + I_2 + I_{\mathrm{NL}}$, where the I_{NL} is the high-order compensation current induced by Q1 and Q3. Then, a high-order temperature compensated reference voltage V_{bgr} is generated. Using R_4, R_5, and R_6, two other reference voltages, V_{ref1} and V_{ref2}, are produced:

$$V_{ref1} = V_{bgr} \cdot \frac{R_5 + R_6}{R_4 + R_5 + R_6} \tag{5}$$

$$V_{ref2} = V_{bgr} \cdot \frac{R_6}{R_4 + R_5 + R_6} \tag{6}$$

N_{16} mirrors I_1+ I_2 + I_{NL} and produces a bias current for N_{11} and N_{12}. N_{11} and N_{12} compare V_{ref1} and V_X, V_{BE} of Q_1, and generate a compensation current I_{LT}, which is copied by P_{22}. The process is the same as the way to generate compensation current I_{HT}. If proper conditions allow P_{11} and P_{12} to work in the sub-threshold region, the current flows through can be expressed by

$$I_{sub} = I_{D0} \frac{W}{L} \exp\left(\frac{V_{GS} - V_{th}}{mV_T}\right) \tag{7}$$

where I_{D0} is a constant, $\frac{W}{L}$ stands for the width/length ratio of the MOSFET, and m represents sub-threshold slope, which is also a constant. For two differential pairs, bias current can be expressed by

$$I_s = I_1 + I_2 + I_{\mathrm{NL}} = I_{11} + I_{12} = I_{13} + I_{14} \tag{8}$$

Combining (5), (6), and (7), assuming that $\left(\frac{W}{L}\right)_{11} = \left(\frac{W}{L}\right)_{12} = \left(\frac{W}{L}\right)_{13} = \left(\frac{W}{L}\right)_{14}$, $V_{th11} = V_{th12} = V_{th13} = V_{th14}$, I_{12} and I_{14} can be re-written as

$$I_{12} = \frac{I_{\mathrm{s}}}{1 + \exp\left(\frac{V_{ref1} - V_X}{mV_T}\right)} \tag{9}$$

$$I_{14} = \frac{I_{\mathrm{s}}}{1 + \exp\left(\frac{-V_{ref2} + V_X}{mV_T}\right)} \tag{10}$$

The compensation current I_{CO} flows through R_7, which is the sum of I_{12} and I_{14}. At very low temperatures, $I_s \approx I_{12}$. As the temperature increases, I_{12} decreases and equals 0 at a certain temperature T'. As the temperature exceeds T', I_{14} starts to increase and at high temperatures $I_s \approx I_{14}$. Therefore, I_s shows a different trend from that of BGR without curvature compensation. Eventually, the reference voltage produced by the proposed BGR can be expressed by the following equation:

$$V_{ref} = I_{CO}R_7 = (I_1 + I_2 + I_{NL} + I_{LH} + I_{HT})R_7 \tag{11}$$

2.3. Implementation of Proposed BGR

As is shown in Figures 2 and 3, the proposed BGR consists of five blocks: a cascode current mirror, a start-up circuit stage, a first-order temperature compensation stage, an improved high-order temperature compensation stage, and a curvature compensation stage. As the system powers up, the start-up circuit works to get the rest of the system functioning. Q_1– Q_2, R_1– R_3 forms the core of the first-order temperature compensation stage, which generates the PTAT and CTAT currents. The emitter–area ratio N of Q_1 and Q_2 is set to 7 out of layout consideration. The ratio of R_1/R_2 is set to 1. There also exists a differential operational amplifier (opamp) to keep the voltage drop of R_2 and Q_1 equal. It is essential to note that the bias current is provided to the opamp through the cascode current mirror, which enhances system power supply rejection (PSR). In Figures 2 and 3, assuming that the gain of the operational amplifier (opamp) is A, the current mirror adopts a cascode structure, and its output impedance increases, expressed as Equation (12). PSR can be equivalent to approximately the reciprocal of the output gain, expressed as Equation (13).

$$R_{out} = g_{m27}(r_{26}||r_{25}||r_{22}.r_{27})\ ||R_7 \tag{12}$$

$$PSR = \frac{\nabla V_{ref}}{\nabla V_{DD}} \approx \frac{1}{AR_{out}} \tag{13}$$

where g_{m27} is the gain of P_{27}, while r_{22}, r_{25}, r_{26}, and r_{27} are the output resistors of P_{22}, P_{25}, P_{26}, and P_{27}, respectively.

Q_3 and R_{NL} provide high-order temperature compensation by producing a logarithmic current I_{NL} to sum with the PTAT and CTAT currents. An OTA is also included in this stage to improve compensation precision. According to Equation (4), the value of R_{NL} is approximately $\frac{R_1}{\eta - 1}$. The OTA is a conventional two-stage differential one without Miller compensation. The curvature compensation stage provides more precise temperature compensation. Firstly, V_{ref1} and V_{ref2} are decided according to the value of V_X, which is the V_{BE} of Q_1. Then, the ratio of $R_5 + R_6$, R_6 and $R_4 + R_5 + R_6$ is determined according to Equations (5) and (6). By a curvature compensation circuit, the segmented compensation currents I_{LT} and I_{HT} are generated to compensate the mirror output current again.

2.4. Trimming Resistor Array Design

In order to solve the problem of TC changes caused by resistance errors, this work designs a trimming resistor array. Using laser trimming technology, cut the metal wires at both ends of the resistor short, ultimately completing the modification of the resistance value. The trimming resistor modules R_3 (Figure 2) and R_5–R_7 (Figure 3) adopt the same structure, as shown in Figure 4, where n represents the number of series resistors and is determined by the resistance values of R_3 and R_5–R_7. The red dashed line markers "×" in Figure 4 indicate the cutting points for laser trimming, with a maximum of m = 32 parallel resistors. The trimming accuracy ∇R obtained by cutting off one of the red markers is shown in Equation (14), where, when m = 32, the minimum accuracy value obtained is about 0.1%.

$$\nabla R = \frac{1}{m(m-1)} 100\% \tag{14}$$

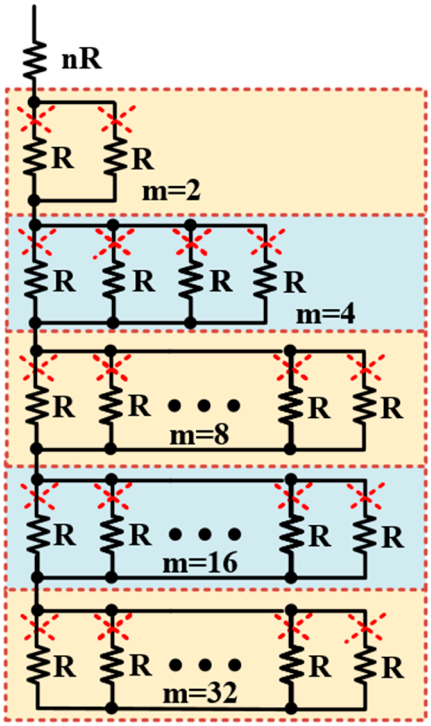


Figure 4. The designed trimming resistor array.

3. Simulation and Experimental Results

The reference voltage V_{ref_1st} produced by first-order temperature compensation BGR, and the reference voltage $V_{ref-high}$ produced by high-order temperature compensation BGR is given in Figure 5. According to the plot, over a wide temperature range from −40 °C to 125 °C, it is apparent that the TC of BGR is significantly lower after high-order temperature compensation (14.04 ppm/°C compared to 25.2 ppm/°C).

The reference voltage $V_{ref-high}$ produced by high-order temperature compensation BGR and compensation current I_{CO} are presented in Figure 6. The simulation results suggest that reference voltage $V_{ref-high}$ and compensation current I_{CO} show a complementary trend, which indicates that curvature compensation can effectively reduce V_{ref0}'s fluctuation with temperature. In addition, V_X, V_{ref1}, and V_{ref2}'s relationship with temperature is given in Figure 7, and determines the slope of I_{CO}.

The simulation result of the TC of the proposed BGR is compared with that of the high-order temperature-compensated BGR in Figure 8. It can be concluded from the simulation results that the curve of reference voltage V_{ref} versus temperature exhibits second-order

compensation properties after curvature compensation, which dramatically reduces the TC from 14.04 ppm/°C to 3.6 ppm/°C.

The Monte Carlo simulation result (500 samples) of reference voltage is presented in Figure 9. The maximum value of V_{ref} is 1.271 V, while the minimum is 1.238 V. The corner (tt, ss, and ff) simulation results of the reference voltage produced by the proposed BGR are presented in Figure 10. The proposed BGR has a different TC and output voltage at different corners, which are summarized and compared in Table 1.

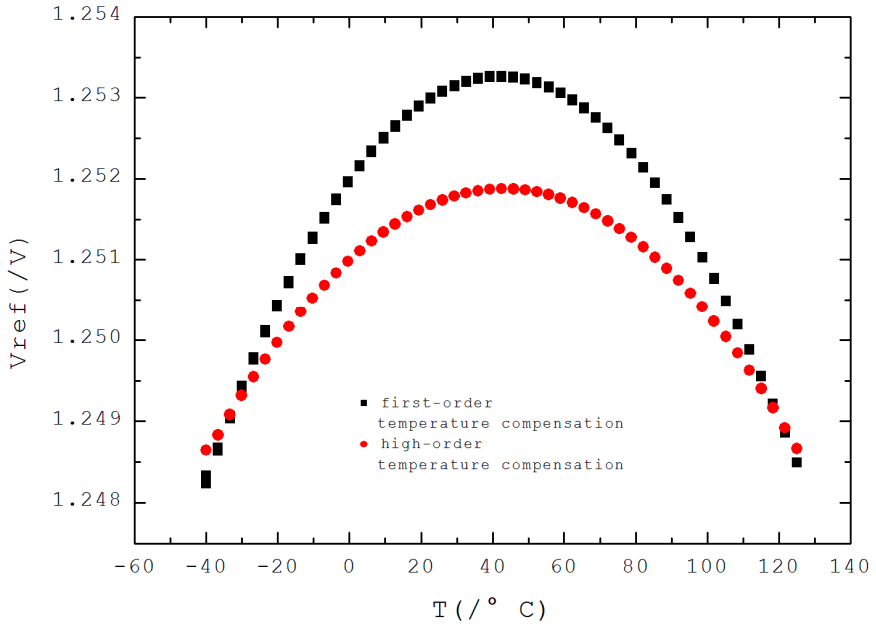


Figure 5. Reference voltage produced by first-order and high-order temperature-compensated BGR.

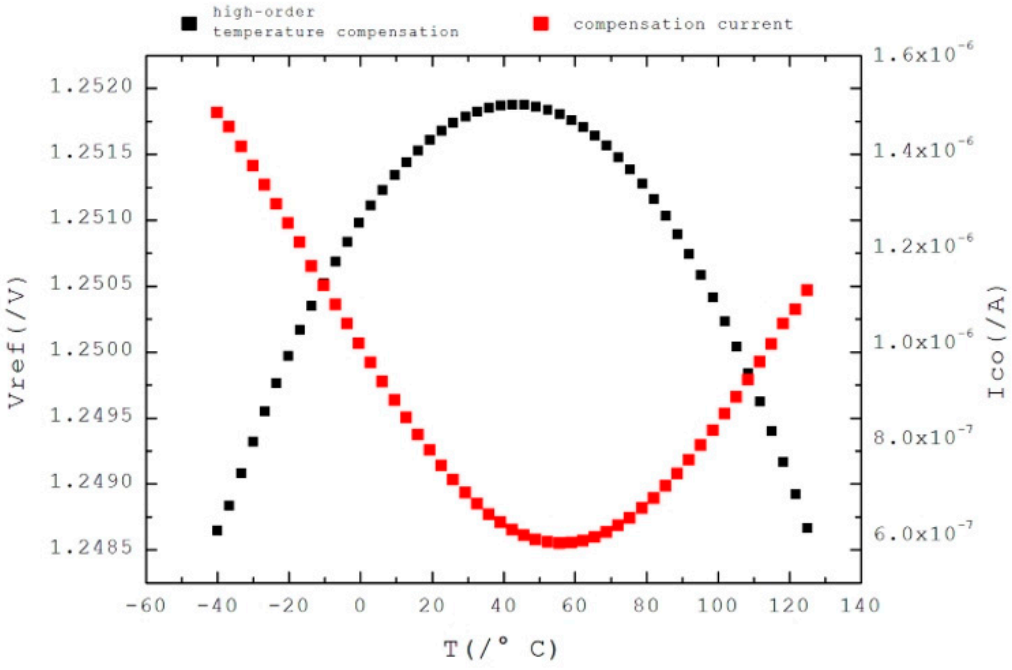


Figure 6. Reference voltage produced by first-order temperature-compensation BGR and compensation current I_{CO}.

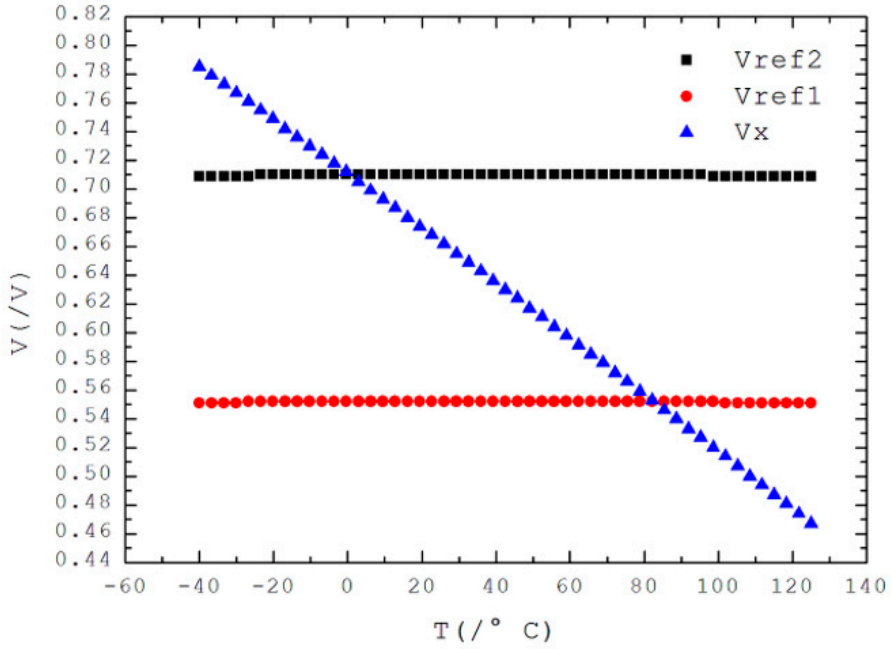


Figure 7. V_X, V_{ref1}, and V_{ref2}'s relationship with temperature.

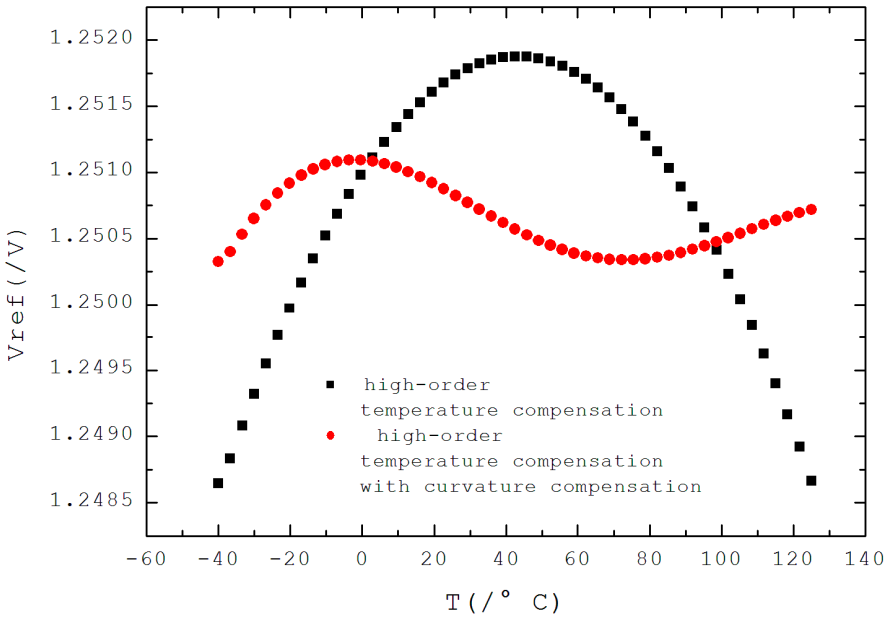


Figure 8. Reference voltage produced by improved high-order temperature-compensated and curvature-compensated BGR.

Table 1. Various important performance parameters of the proposed BGR at different corners.

	ff [#]	ss [#]	tt
TC (ppm/°C)	14.04	12.16	3.6
Line Regulation (mV/V)	0.6	0.52	0.15
V_{ref} (V)	1.259	1.259	1.255
PSR@DC (dB)	−110	−105	−110

[#] Without trimming.

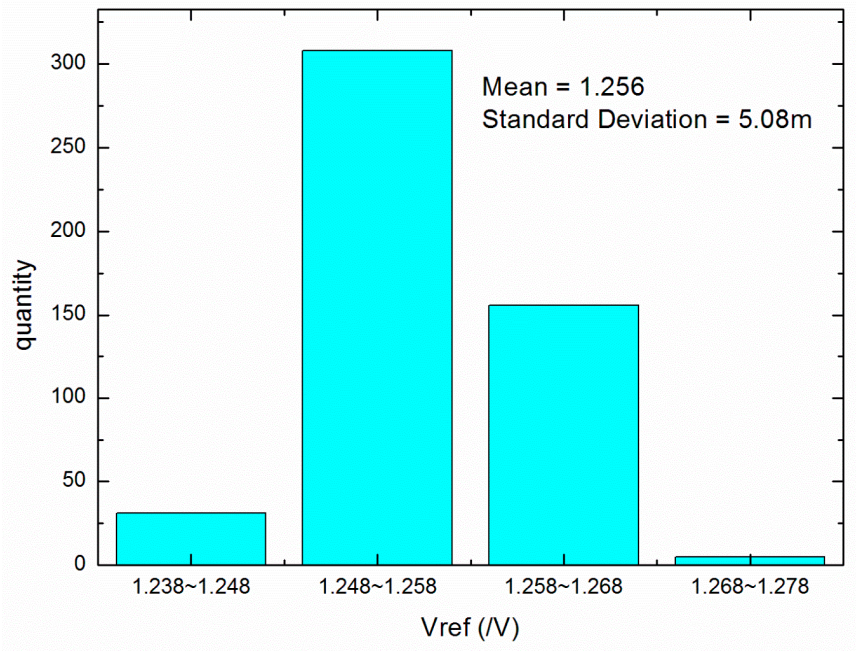


Figure 9. Monte Carlo simulation results of reference voltage.

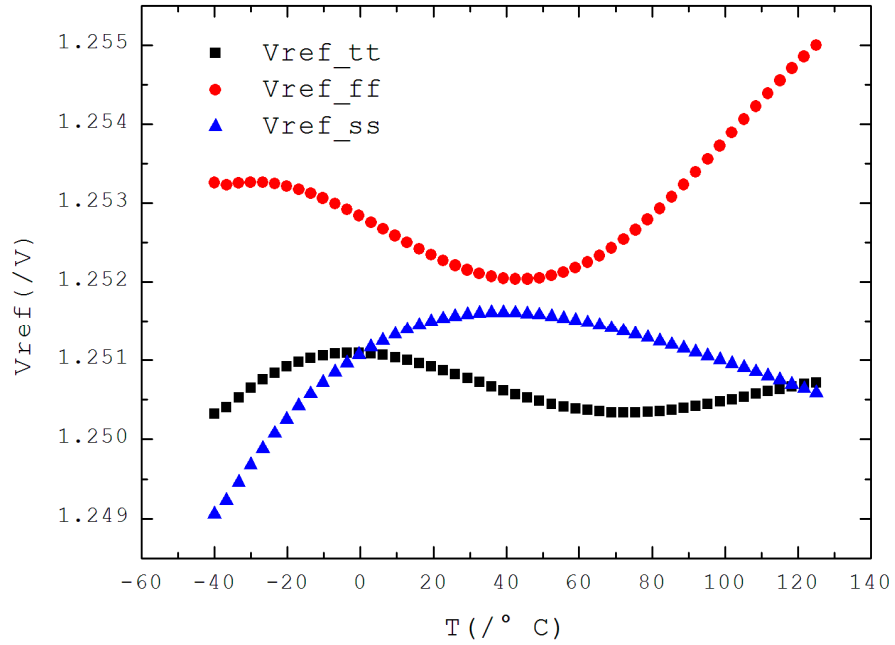


Figure 10. Corner simulation results (tt, ss, and ff) of reference voltage.

The Monte Carlo simulation result (500 samples) of the reference voltage TC is presented in Figure 11. The maximum value of *TC* is 32.43 ppm/°C, while the minimum is 3.38 ppm/°C.

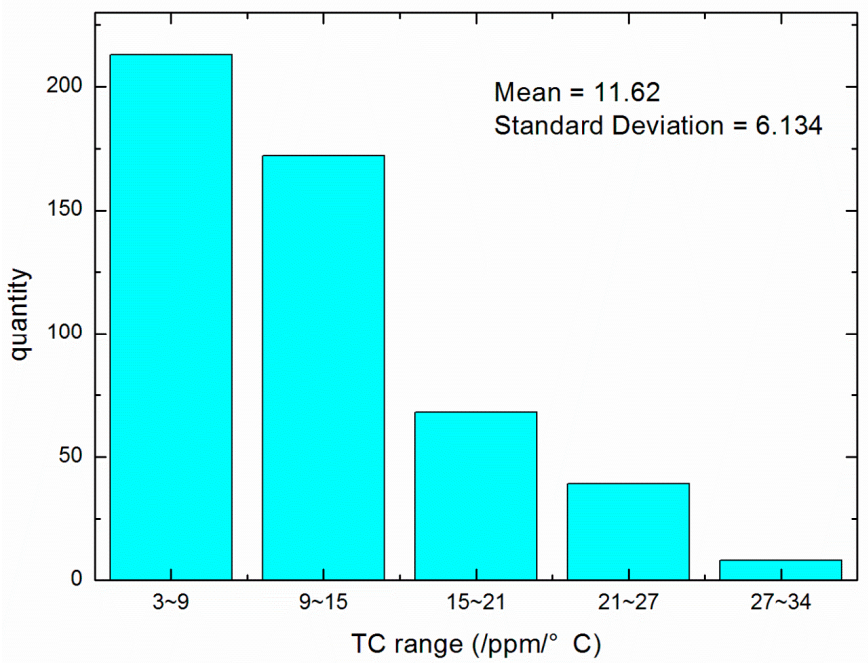
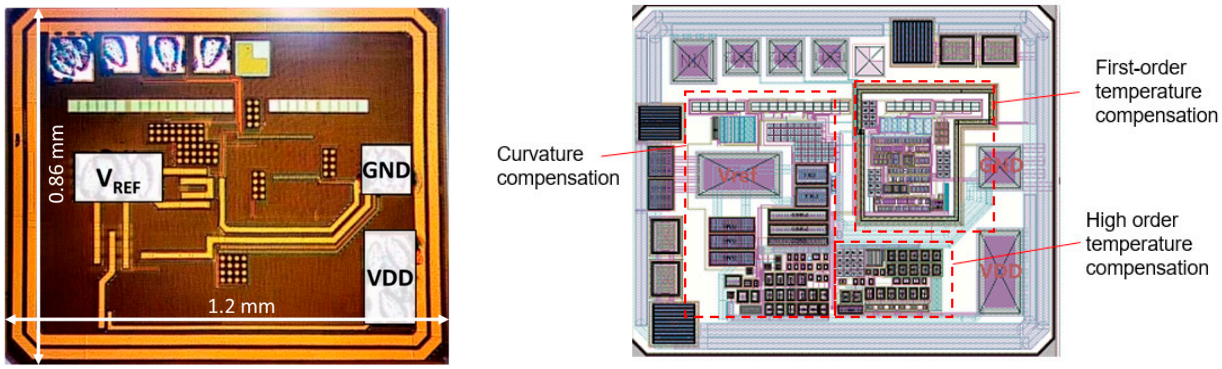


Figure 11. Monte Carlo simulation results of TC.

Figure 12 presents the experiment sample for the proposed BGR, and it is found that the processing deviation is close to the tt process angle. The die is trimmed on the wafer using a laser trimming system. Before the trimming, the overall temperature deviation is obtained through the testing performance of the die, and a trimming plan is confirmed. The resistance values of resistors R3, R5, R6, and R7 are changed through laser trimming technology. Finally, the voltage output value at a specific temperature point is obtained.



(**a**) (**b**)

Figure 12. (**a**) The actual photograph and (**b**) layout for the proposed BGR.

The error between this experiment and the simulation can be improved by precise trimming, and the laser continuous trimming can make the experimental results closer to the simulation results. Twenty samples were tested. The tested temperature coefficients of the samples without trimming are shown in Figure 13a, and there is a certain deviation in the output voltage compared to the simulation results. Figure 13b shows that the average voltage is about 1.25 V and the sample variance is around 0.38 mV. The above samples were trimmed and subjected to temperature coefficient testing again. The voltage parameters were improved, as shown in Figure 14a. According to Figure 14b, the average voltage is about 1.25 V, and the sample variance is around 0.16 mV. Laser trimming methods can effectively improve process deviations, and the worst and best temperature coefficients are 7.5 ppm/°C and 4.2 ppm/°C, respectively. Various important performance parameters of

the proposed BGR are summarized and compared in Table 2. Compared with other BGRs in previous reports [4,9], although the proposed BGR has a larger area due to the trimming resistor array design, the TC and PSR are excellent.

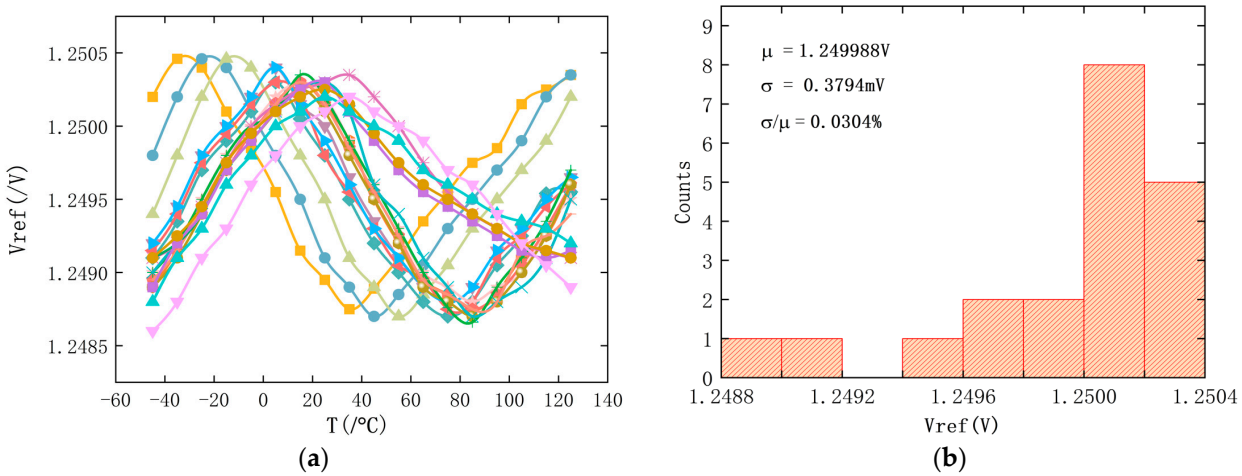


Figure 13. For the samples without trimming, (**a**) the test V_{ref} related to temperature, corresponding to (**b**) the average voltage and the sample variance.

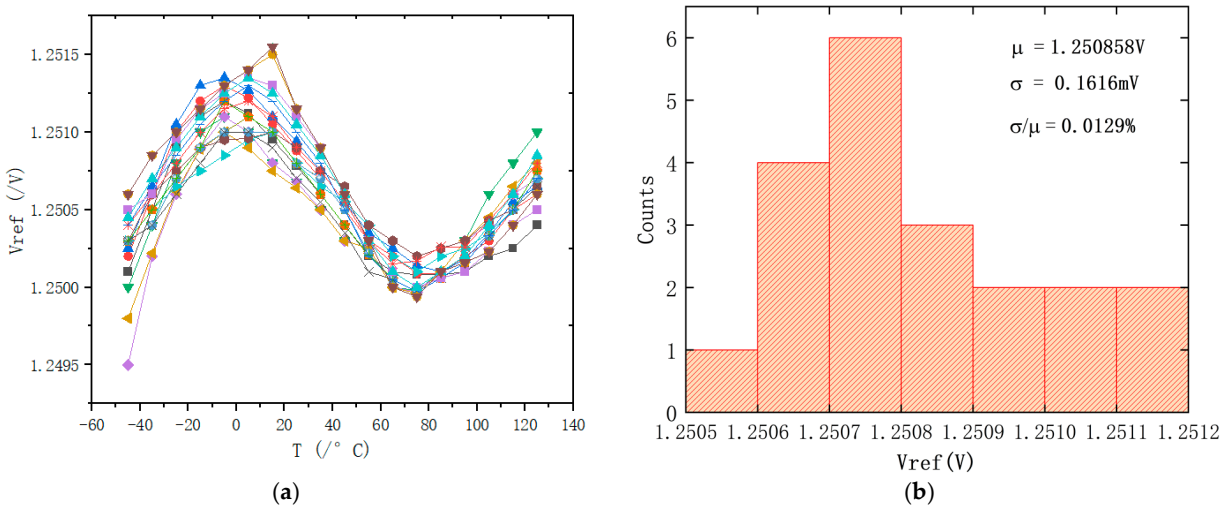


Figure 14. For the samples with trimming, (**a**) the test V_{ref} related to temperature, corresponding to (**b**) the average voltage and the sample variance.

Table 2. Parameter comparison of BGR between our work and previous reports.

	This Work	[4]	[9]	[2]
Process (nm)	180	180	180	55
Year	2024	2023	2023	2023
Reference voltage (V)	1.25	1.18	2.56	N/A
V_{DD} (V)	3–5	3.3	5	3.3
Temperature range (°C)	−45–125	−60–160	−40–150	−50–120
TC (ppm/°C)	4.2	5.72	14.89	3.78
σ/μ%	0.0129	N/A	N/A	N/A
PSR @Hz (dB)	−100@DC	−93.26@DC	−68@DC	−63.1@100
Power (μW)	127.8	245.2	5.12	139.03
Active area (mm^2)	1.03	0.072	0.0925	0.044

4. Conclusions

In this paper, a bandgap reference circuit with a low temperature coefficient and high PSR using 180 nm BCD processing is designed. This work introduces a low TC and high PSR circuit structure, which is achieved by high-order temperature compensation and curvature compensation techniques. Moreover, a trimming resistor array structure is proposed to address the TC deviation of the output voltage from the theoretical design value. Through wafer level laser trimming technology, the measured bandgap reference results are very close to the theoretical design value. The measured results show that the proposed BGR produces a stable reference voltage at 1.25 V, whose TC has reached 4.2 ppm/°C. In addition, the proposed BGR is also insensitive to power supply fluctuation, reflected by the very high PSR at −100 dB; the proposed BGR is applicable in systems that require high precision.

Author Contributions: X.L.: Conceptualization, Methodology, Software, Writing—Original Draft; J.L.: Methodology, Investigation, Writing—Original Draft, Writing—Review and Editing; M.Q.: Writing—Review and Editing, Supervision, Project administration, Funding acquisition; B.Z.: Project administration, Funding acquisition. All authors have read and agreed to the published version of the manuscript.

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