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6.5 kV SiC PiN and JBS Diodes' Comparison in Hybrid and Full SiC Switch Topologies

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Abstract: This work investigates the performance of state-of-the-art non-commercial 6.5 kV Silicon Carbide (SiC) PiN and Junction Barrier Schottky (JBS) diodes in hybrid (Si IGBT with SiC diode) and full SiC (SiC MOSFET with SiC diode) switch topologies. The static and dynamic performance has been systematically evaluated at distinct temperatures, gate resistances and currents for each configuration. The SiC PiN diode presented higher current density capability and lower leakage current density than the JBS diode. Moreover, in most cases, the SiC PiN diode-based topologies demonstrated slightly higher total switching losses compared to the SiC JBS diode-based equivalent configurations. A loadability analysis in a three-level NPC converter is presented to evaluate the potential of each configuration in a converter application. The SiC PiN technology presented a 25% power extension compared to the SiC JBS technology with similar efficiency at typical industrial drives switching frequency operation when comparing same-active-area diode technologies. Finally, a long-term reliability test (H3TRB) is presented to demonstrate the SiC PiN diode technology's potential for operation in harsh environments. Such characteristics show the advantage of the 6.5 kV SiC PiN diode when a high current density (>100 A/cm^2), high efficiency and reliability are required.

Keywords: SiC PiN diode; SiC Junction Barrier Schottky (JBS) diode; SiC MOSFET; Si IGBT; hybrid topology; neutral point clamped inverter (NPC); power electronics; power losses

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1. Introduction

Silicon Carbide (SiC) devices present significant potential for medium-voltage applications due to lower conduction and switching losses than their silicon-based counterparts [1]. Such devices are particularly promising for megawatt converters such as industrial motor drives, traction inverters and grid-tied converters, enabling considerable energy savings, footprint reduction, topology simplification and performance improvements [2–4]. However, due to the higher costs of SiC devices, adopting full SiC-based solutions is still a challenge. Hybrid topologies, mixing Silicon (Si) Insulated Gate Bipolar Transistors (IGBTs), SiC Metal Oxide Field Effect Transistors (MOSFETs) and diodes (Si and SiC), emerge as an alternative solution where good performance and lower costs can be achieved [5–12].

The optimal power semiconductor selection is generally based on the electrical performance, ruggedness, reliability, and associated cost of the device in the power converter. Hybrid topologies require further investigation of the interaction between power devices made from different materials (e.g., Si and SiC) in the same circuit. This fact increases the design possibilities and requires a more comprehensive trade-off analysis of the device attributes and their effects on the power electronic converter performance.

Due to the commercial availability of 1.2 and 1.7 kV SiC diodes and MOSFETs, systematic investigations on the static and dynamic performance of SiC devices compared to Si devices under different temperatures and setup conditions have been reported [13–15]. Consequently, such studies allowed for several application-oriented investigations of full

SiC-based power converters [16,17]. In addition, new multilevel hybrid topologies with state-of-the-art modulation and control techniques to enhance performance at an acceptable cost have been investigated [5–12].

In the 3.3 kV class, engineered samples of 3.3 kV SiC MOSFET modules have been characterized [18–20], and system simulations have been performed for industrial drive applications [3]. For railway traction, SiC-based converters are being investigated [4], and commercial train lines have already implemented these [21,22]. Regarding hybrid solutions, a hybrid 3.3 kV module [23] has been characterized and evaluated through electro-thermal simulations in a traction converter application. Hybrid topologies are also of great interest to this voltage class [24].

For the 6.5 kV voltage class, no SiC commercial devices are available at the moment. Consequently, fewer investigations on these devices have been reported compared to the lower-voltage classes. Since the 6.5 kV class will inevitably come to market and presents excellent prospects in high-power industrial drive applications [11,25], further investigations are required. A typical diode application in the medium-voltage range is as a clamping device in multilevel topologies [11,12,25].

Previous works on 6.5 kV SiC diodes reported the static and dynamic characterization of SiC PiN diodes with Si IGBTs [11,25–31] and MOSFET body diode or Schottky barrier diodes in full SiC configuration [32–36]. Furthermore, the static characterization of Junction Barrier Schottky (JBS) diodes [37] and the dynamic characterization of JBS diodes with Si IGBTs based on Spice models [12] and at room temperature for a fixed current value [31] have been reported. Each work investigated a unique configuration, and a systematic investigation of the device performance at different temperatures, current loads, and gate resistances was performed by a few works for a limited number of configurations, not encompassing all operational conditions and switch topology combinations. This occurs because most papers focus on characterizations at nominal conditions and one specific temperature to prove device functionality or safe operation area using a specific device configuration. Thus, a reliable systematic performance comparison between both diode technologies under identical conditions and for all possible configurations is not possible. In addition, there is a lack of available systematic data for power electronics researchers to evaluate the potential of these high-voltage technologies in power converter applications.

This work compares 6.5 kV SiC PiN and JBS diode technologies switched with state-of-the-art Si-IGBTs and SiC-MOSFETs. All devices were fabricated in the same laboratory and tested in the same system, thus allowing for a precise performance comparison. The impact of distinct temperatures, gate resistances and current loads has been addressed. Furthermore, a comparison with Si PiN diodes is given to depict the potential of Wide Band-Gap (WBG) technology. The impact of these diode technologies on a Three-Level-Neutral Point Clamped (3L-NPC) converter application has also been investigated, observing the maximum allowed switching frequency and power for each configuration, as well as efficiency. Finally, a long-term reliability test on the SiC PiN diode has been addressed to evaluate its potential in harsh environments. This paper is organized as follows: Section 2 details the devices characterized and the test bed setup conditions. Section 3 provides the static and dynamic characterizations for each configuration, evaluates the power switch topologies in a 3L-NPC converter application, and characterizes the SiC PiN diode's long-term reliability in a High-Temperature, Humidity Reverse Bias (H3TRB) test setup. Finally, Section 4 presents the main conclusions of this work.

2. Materials and Experimental Methods

The experiments were performed on state-of-the-art, non-commercial 6.5 kV SiC PiN and JBS diodes, presenting the same active area of 0.4 cm × 0.4 cm (0.65 cm × 0.65 cm total chip area). This characteristic allows for a comparison of both technologies with the same wafer area usage. Consequently, similar device prices are expected, allowing for fair cost versus performance comparisons. The fabrication details of the SiC PiN diode are reported elsewhere [31]. The diode chip was soldered and wire-bonded on a copper base plate with

an insulator-based package, as demonstrated in Figure 1. The controlled switches used in the experiments to evaluate diode performance and their effects on the circuit are a state-of-the-art 6.5 kV SiC MOSFET [32] and a commercial 6.5 kV Si IGBT (nominal current: 25 A). In addition, a commercial 6.5 kV Si PiN diode (nominal current: 75 A) was used for qualitative comparison with the WBG technology since the current rating of the Si diode is much higher than the expected current rating for the investigated diodes. All devices were fabricated at Hitachi Energy, Zürich, Switzerland.

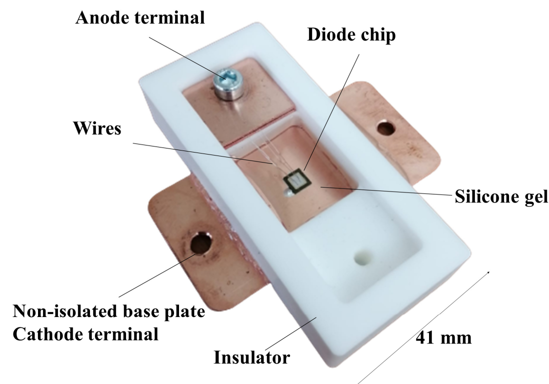

Figure 1. Device package. The diode chip is soldered on a non-isolated base plate (cathode terminal) and wire-bonded to the anode terminal.

Static characterization was performed with a Keysight B1505A Power Device Analyzer (Keysight Technologies, Santa Rosa, CA, USA). Dynamic characterization was performed in a double-pulse tester at a nominal switching voltage (V) of 3.6 ± 0.1 kV, estimated main loop stray inductance ($L\sigma$) of around 200 nH and gate voltages (V_G) of +15 V/−10 V. The pulse duration defines the current load, and gate resistance is changed manually in a commercial gate drive unit. The tested gate resistance values are 30 Ω and 50 Ω, typical values for such power switches. Lower gate resistance values may present increased ringing during switching [32]. The designed double-pulse tester, which is shown in Figure 2, has hotplates to control the devices' temperature. A solid-state-circuit breaker (SCCB) was added to avoid catastrophic damage in case of device failure. High-bandwidth voltage probes (CT4028 (DigiKey, Thief River Falls, MN, USA)—220 MHz) for voltage monitoring and high-bandwidth coaxial current shunt (SDN-10 (Emerson Electric Co., Ferguson, MO, USA)—2000 MHz) for power switch current measurement were employed. The inductor current was monitored by a Rogowski coil (CWT Mini50 HF (Power Electronic Measurements Ltd., Nottingham, UK)—50 MHz) to obtain the diode current indirectly by subtracting the inductor from the controlled switch current. A 500 MHz oscilloscope (Keysight MSOX3054T (Keysight Technologies, Santa Rosa, CA, USA)—500 MHz, 5 GSa/s) performs the curves acquisition and K-type thermocouples characterize the devices' temperature with an error of ±2 °C. The packaging was placed on top of the hotplate with a thermal interface material to improve heat spreading and to isolate the hotplate from the device.

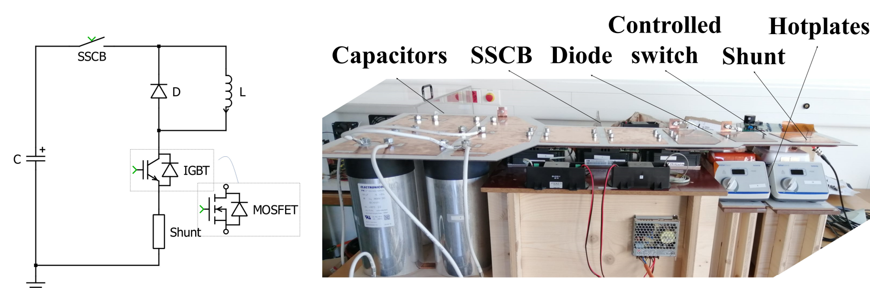

Figure 2. Double-pulse tester schematic and system photo.

3. Results and Discussion

3.1. Device Characterization

3.1.1. Static Characterization

The current density (current divided by chip active area) versus on-state voltage curves from the fabricated 6.5 kV SiC PiN and JBS diodes and the commercial 6.5 kV Si PiN diode are demonstrated in Figure 3. At room temperature (25 °C), for current densities higher than 40 A/cm^2, the SiC PiN diode presents lower voltage drops compared to the SiC JBS diode. This fact is exemplified at the current density of 80 A/cm^2, where the SiC PiN diode has a forward voltage drop of ~3.6 V, whereas the SiC JBS presents one of ~6.1 V. At 125 °C, such behavior is reinforced, with the SiC PiN diode presenting the lowest voltage drops for current densities higher than 12 A/cm^2. Thus, the SiC PiN diode is advantageous for high-current density designs and high-temperature operation, presenting lower losses. Another characteristic is that the SiC PiN diode presents a knee voltage reduction that improves its current conduction at high temperatures [11,26]. In contrast, the SiC JBS diode lessens its current density capability caused by increased resistance with higher temperatures [37], presenting a strong temperature dependence, as shown in Figure 3. Alternatively, the SiC JBS diode is a better option compared to the SiC PiN diode for current densities lower than 12 A/cm^2 at 125 °C (or 40 A/cm^2 at 25 °C), where the SiC PiN diode's high built-in voltage reduces its current capability in the low-current-density regime. The Si PiN diode presents a better current capability compared to the SiC JBS diode, but worse than that of the SiC PiN diode at high current densities (>80 A/ cm^2 at 25 °C).

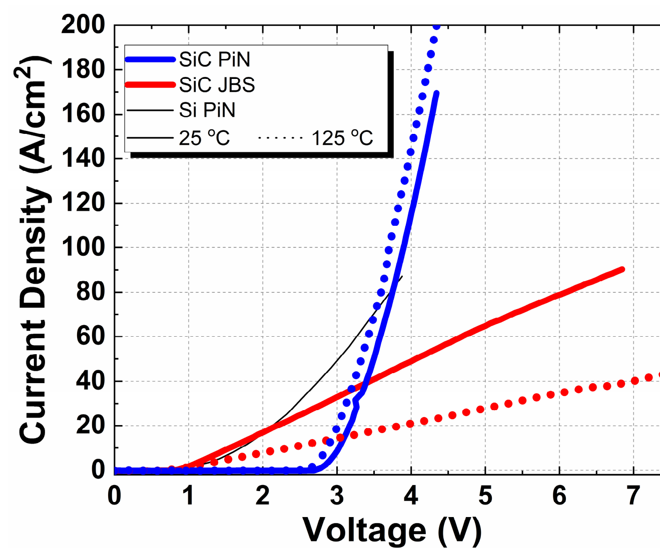

Figure 3. Forward characteristic curves from the 6.5 kV SiC PiN, SiC JBS, and Si PiN diodes at 25 °C and 125 °C. The solid line curves are at 25 °C and the dotted line curves at 125 °C. The SiC PiN diode presents the highest current density capability.

The lower leakage current density is another characteristic of the SiC PiN diode, as shown in Figure 4. In the <5 kV range, it presents around 10^{-8} A/cm^2 compared to the SiC JBS diode leakage current density of about 10^{-3} A/cm^2, and Si PiN diode's leakage current density of around 10^{-6} A/cm^2. At higher voltages (>5 kV), the SiC PiN diode presents an increase in the leakage current but with values below the SiC JBS diode technology. These devices operate in the final application with typical blocking voltages of around 3.6 kV. Low leakage current is essential to ensure reliable high-voltage operation by reducing the blocked state's power losses.

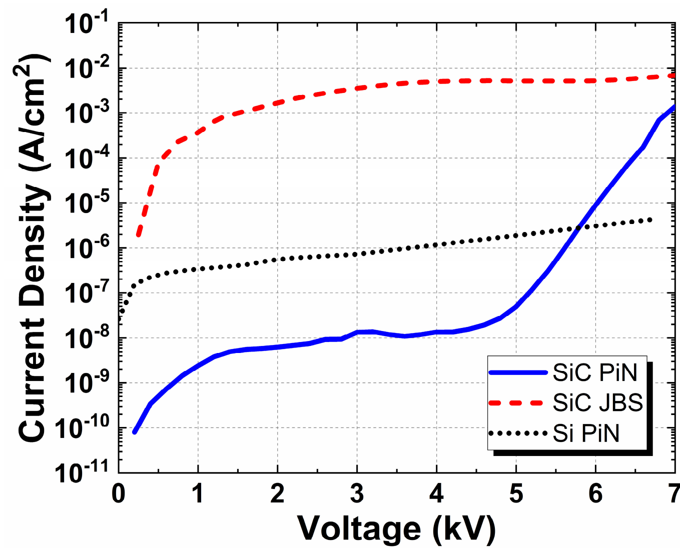

Figure 4. Reverse blocking characteristic curve from the 6.5 kV SiC PiN, SiC JBS, and Si PiN diodes at 25 °C. The SiC PiN diode presents the smallest leakage current density up to around 6 kV.

3.1.2. Dynamic Characterization

Figures 5 and 6 show dynamic curves of the switch configurations investigated in this paper. The influence of the SiC diodes on the turn-on of controlled switches (Si IGBT and SiC MOSFET) is demonstrated in Figure 5 for a switching current of 11 A, gate resistance of 30 Ω and junction temperature of 125 °C. The IGBT turn-on curves (Figure 5a) depict a considerable diode influence caused by its reverse recovery current. At the full Si configuration, we can see an overshoot current of ~74 A caused by the high reverse recovery current of the Si PiN Diode. With the substitution of the Si PiN diode by the SiC PiN and JBS diodes (hybrid configurations), an overshoot current reduction is observed, presenting peak currents of ~36 A and ~17 A, respectively. The overshoot current reduction is essential to minimize turn-on losses and stress on the controlled switch (due to the high peak power density). The measured turn-on dv/dt of the Si IGBT switched with Si PiN, SiC PiN, and SiC JBS diodes is in the range of 5 V/ns.

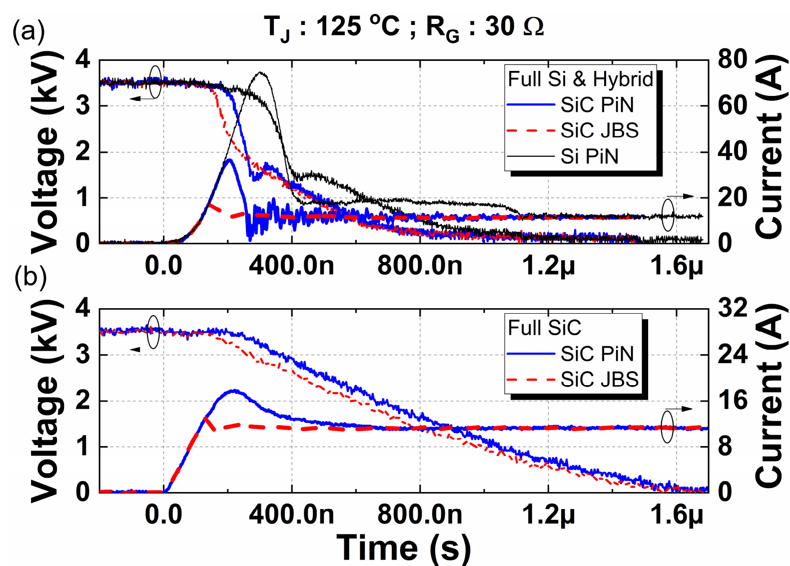

Figure 5. (**a**) 6.5 kV IGBT turn-on curves when switched with SiC PiN, SiC JBS and Si PiN diodes. (**b**) 6.5 kV SiC MOSFET turn-on curves when switched with SiC PiN and SiC JBS diodes. All curves were obtained at 3.6 ± 0.1 kV, I~11 A, R_G = 30 Ω, T_J = 125 °C, and Lσ~200 nH.

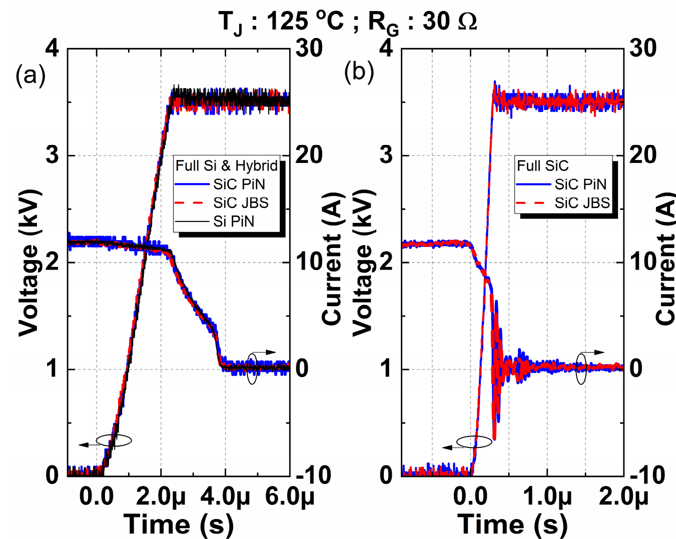

Figure 6. (**a**) 6.5 kV IGBT turn-off curves when switched with SiC PiN, SiC JBS and Si PiN diodes. (**b**) 6.5 kV SiC MOSFET turn-off curves when switched with SiC PiN and SiC JBS diodes. All curves were obtained at 3.6 ± 0.1 kV, I~11 A, R_G = 30 Ω, T_J = 125 °C, and Lσ~200 nH.

Regarding the SiC MOSFET turn-on (full SiC configurations), Figure 5b shows the SiC PiN diode configuration with a slightly higher overcurrent peak of ~17 A than the JBS diode configuration (~13 A). The measured turn-on dv/dt of the SiC MOSFET switched with SiC PiN and SiC JBS diodes is in the range of 2.8 V/ns. The SiC MOSFET configurations presented slower dv/dt during turn-on compared to IGBT. Such an effect is related to the MOSFET pitch design, which has a purely capacitive nature. Larger pitches lead to devices presenting slower voltage variations at the turn-on process, consequently increasing turn-on losses [32]. Faster devices with lower pitches are possible at the cost of lower short-circuit capability time [32]. The SiC JBS diode presented the smallest reverse recovery current in all configurations due to the lack of minority carriers stored during forward operation [38]. The decrease in the switch overcurrent peak from 36 A (IGBT switch configuration) to 17 A (SiC MOSFET switch configuration) when switched with the SiC PiN diode is mainly related to the slower dv/dt swing when switched with the SiC MOSFET. This effect is mainly capacitive, where higher dv/dt causes higher peaks and shorter reverse recovery duration, as observed in Figure 5.

A systematic investigation of the temperature effects for distinct load currents in the turn-on switching losses is demonstrated in Figure 7. The full Si configuration presents the highest IGBT turn-on losses mainly caused by the large Si PiN diode reverse recovery current, as shown in Figure 5. The hybrid configurations present the lowest losses for most of the switched load current range. Such a fact happens due to the faster dv/dt of the IGBT during turn-on compared to the SiC MOSFET configuration. Additionally, the SiC PiN hybrid configuration presents slightly higher losses than the hybrid JBS configuration and is sensitive to temperature variations. This sensitivity is caused by the SiC PiN diode reverse recovery charge increasing with temperature, as shown in Figure 8, affecting the IGBT turn-on losses. This charge is responsible for the large reverse recovery currents during the diode turn-off process and presents temperature dependence [28]. The SiC JBS diode presents no reverse recovery charge dependence on the temperature, as demonstrated in Figure 8, not affecting the switch turn-on losses. These characteristics are expected since JBS diodes are majority carrier devices without minority carriers injected in the drift layer during forward operation [38]. The small reverse recovery current presented by the JBS diode is based on the junction capacitive effect that is temperature-independent [38]. For the full SiC configurations, the SiC MOSFET presented higher turn-on losses at lower temperatures when switched with the SiC JBS diode. Such an effect agrees with other medium-voltage classes of SiC MOSFETs switched with Schottky barrier and body diodes [18,19]. This fact

occurs due to the increased di/dt and dv/dt of the SiC MOSFET at higher temperatures [19], generating faster switching times and lower losses. On the other hand, the SiC PiN diode presents a reverse recovery charge increase at higher temperatures (Figure 8). Thus, it tends to increase MOSFET switching losses as temperature increases. Such a counterbalancing effect with the SiC MOSFET temperature characteristics imposes a more temperature-independent behavior on the turn-on losses of the SiC MOSFET switched with the SiC PiN diode, as shown in Figure 7a.

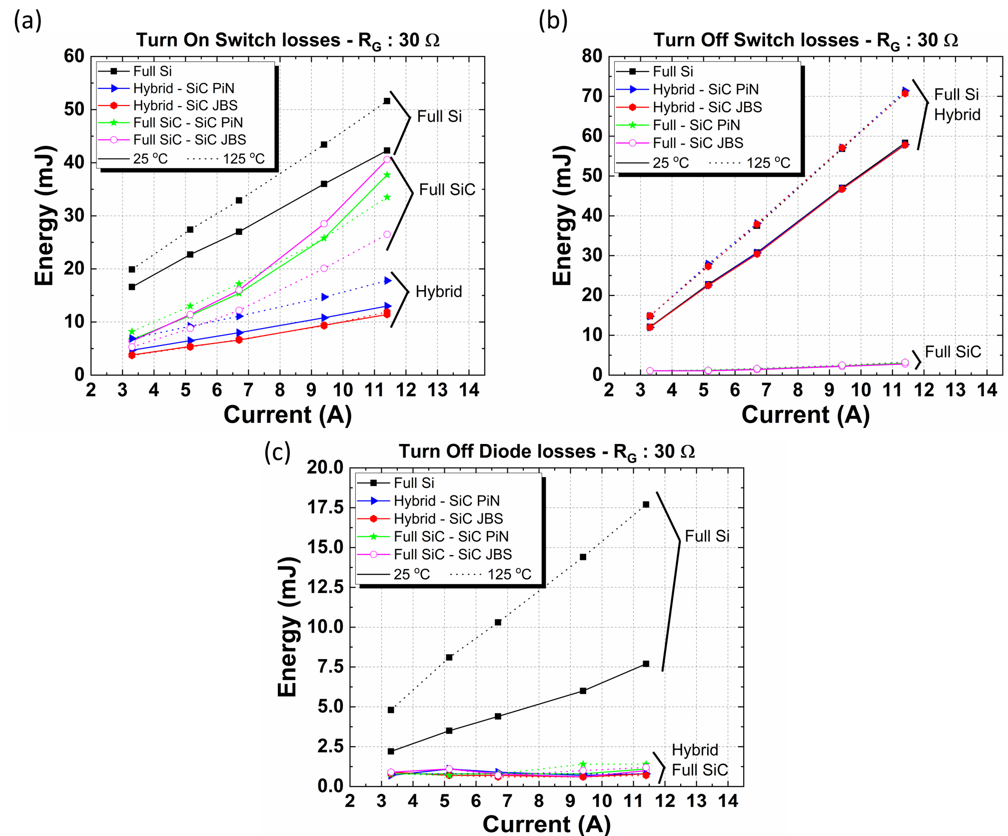

Figure 7. (**a**) Turn-on switch losses versus current for the full Si, hybrid and full SiC configurations. (**b**) Turn-off switch losses for the full Si, hybrid and full SiC configurations. (**c**) Turn-off diode losses for the full Si, hybrid and full SiC configurations. The results were obtained at 3.6 ± 0.1 kV, R_G = 30 Ω, T_J = 25 °C and 125 °C, and Lσ~200 nH.

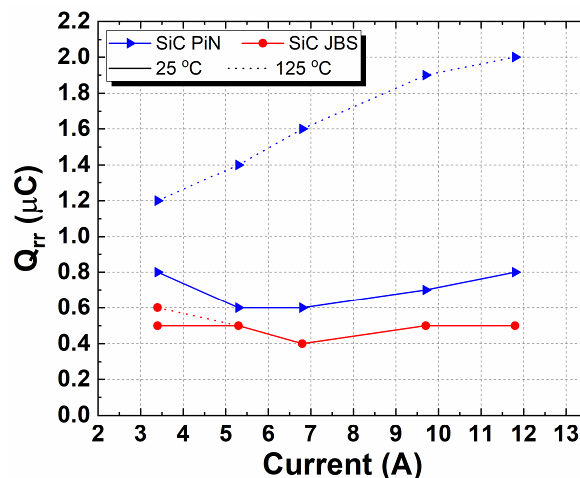

Figure 8. SiC diodes reverse recovery charges at 25 °C and 125 °C. The error for each measurement is ±0.1 μC. Data obtained from the hybrid configuration.

The Si IGBT turn-off curves, shown in Figure 6a, indicate that the diodes have almost no influence on the turn-off characteristics of the controlled switch, preserving the same shape for all combinations, as expected. The hybrid and full Si configurations have a total switching time of ~4 µs. A similar behavior to the IGBT curves is observed for the SiC MOSFET turn-off curves in Figure 6b. The different types of diodes presented almost no effect on the curves. Due to the inclusion of a WBG-controlled switch, a faster switching time of ~500 ns was achieved with an increased ringing. The effects observed in Figure 6 can be reinforced in Figure 7b, in which the turn-off losses depend only on the controlled switch (IGBT or MOSFET). The full and hybrid Si configurations presented the highest losses, reaching values close to 70 mJ, while the full SiC configurations presented losses smaller than 5 mJ. Such small values are related to the fast switch time during turn-off of the WBG switch. The SiC MOSFET turn-on losses dominate the total SiC MOSFET switching losses. An alternative to avoid such high losses is using soft-switching methods to improve power converter efficiency [19].

The diode reverse recovery curves, shown in Figure 9, for a switching current of 11 A, gate resistance of 30 Ω, and junction temperature of 25 °C reinforce the previously discussed effects on the turn-on characteristics of the controlled switches. At 25 °C, the full SiC configuration presents a slower switching time of around 2.5 µs (Figure 9b) compared to the switching time at 125 °C of around 1.6 µs (see SiC MOSFET turn-on curve in Figure 5b). Such switching time reduction and its effects were previously discussed for the full SiC–SiC JBS configuration. Furthermore, the qualitative behavior regarding the reverse current peak for each configuration is kept the same, with the Si PiN diode presenting the highest reverse recovery current, followed by the SiC PiN and SiC JBS diodes. The diode turn-off and MOSFET/IGBT turn-on curves are complementary because the turn-on of the IGBT/MOSFET happens at the same time as the diode turn-off in a double-pulse setup (half-bridge configuration). Consequently, due to Kirchhoff's circuital law, voltage and current are complementary. Regarding switching losses, Figure 7c shows the Si PiN diode with the highest loss values. The SiC diodes presented turn-off losses smaller than 1 mJ in the investigated current range in all configurations. This indicates that the diode losses can be further reduced by implementing SiC PiN and JBS diodes. In addition, the diode losses are low compared to the total switching losses, which are sometimes neglected in the power converter's efficiency calculations [20].

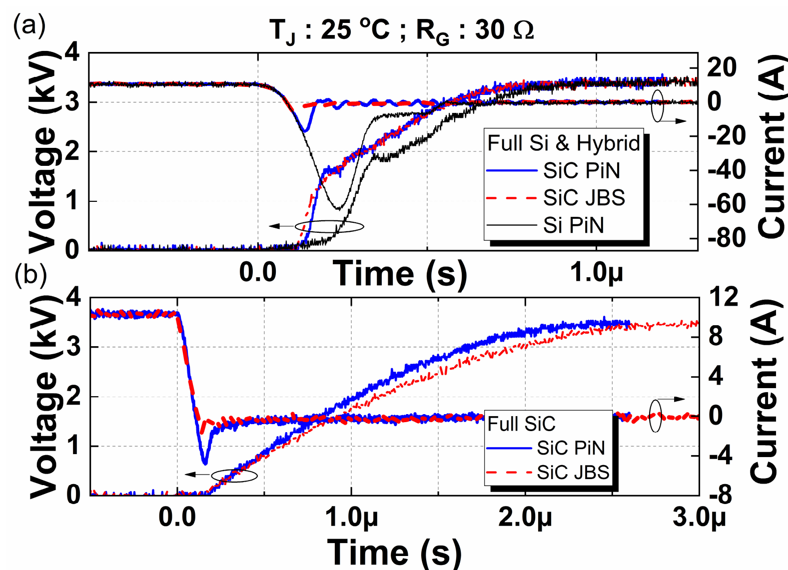

Figure 9. (**a**) 6.5 kV SiC PiN, SiC JBS and Si PiN diode turn-off curves when switched with Si IGBT. (**b**) 6.5 kV SiC PiN and SiC JBS diode turn-off curves when switched with SiC MOSFET. All curves were obtained at 3.6 ± 0.1 kV, I~11 A, R_G = 30 Ω, T_J = 25 °C, and Lσ~200 nH.

The overall switching losses from each configuration, summing up turn-on, turn-off switch losses and turn-off diode losses, are demonstrated in Figure 10 at a fixed gate resistance of 30 Ω. The full SiC configurations presented the lowest losses, followed by the hybrid and full Si configurations. The inclusion of SiC diodes reduces the turn-on switch losses as well as the diode losses when compared to Si diodes. The full Si and hybrid switch topologies presented a more pronounced temperature dependence, with increased losses at higher temperatures. Finally, the full SiC configuration with the SiC PiN diode presented an almost temperature-independent behavior, while for the SiC JBS diode configuration, the losses decreased at higher temperatures.

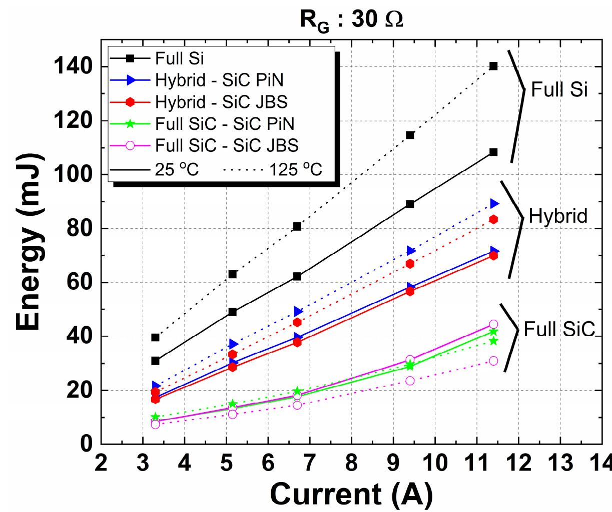

Figure 10. Total switching losses versus current for the full Si, hybrid and full SiC configurations at a constant gate resistance R_G = 30 Ω. The results were obtained at 3.6 ± 0.1 kV, T_J = 25 °C and 125 °C, and Lσ~200 nH.

The effect of gate resistance on the total switching losses is demonstrated in Figure 11. Higher gate resistance values increase switching losses caused by longer switching times. Such a strategy can be used when slower switching times are required due to EMC constraints and when a lower diode reverse recovery peak current is desired to reduce the stress on the power switch.

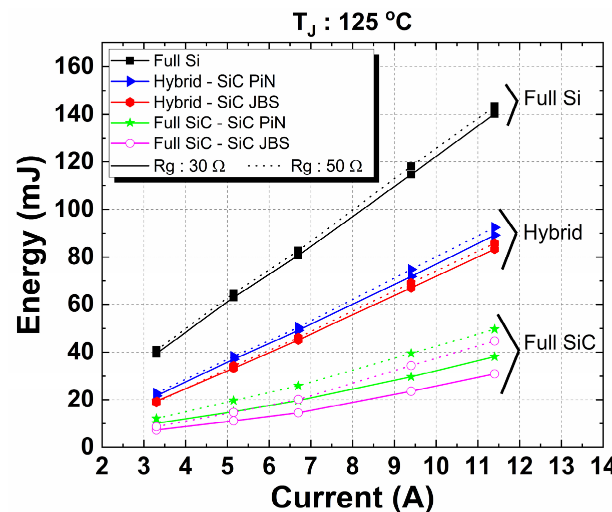

Figure 11. Total switching losses versus current for the full Si, hybrid and full SiC configurations at a constant temperature T_J = 125 °C. The results were obtained at 3.6 ± 0.1 kV, R_G = 30 Ω and 50 Ω, and Lσ~200 nH.

Figure 12 shows the reverse peak diode current for different gate resistances. Higher gate resistance reduces the di/dt rate during switching, thus reducing the reverse peak current [39]. The gate resistance value presents a larger influence on the full Si and hybrid SiC PiN diode configurations. The full SiC configurations, independently of the diode technology, presented a low gate resistance influence on the diode reverse recovery peak current. Furthermore, the hybrid SiC PiN configuration presented the highest reverse peak current after the full Si configuration. This is caused by the higher reverse recovery charge of the PiN technology compared to the JBS design. In addition, the faster voltage variation during the IGBT turn-on compared to the SiC MOSFET contributes to the increased current peak. All other configurations presented low reverse recovery currents with values lower than 9 A for the whole current range. As expected, the lowest reverse recovery peak current occurs with the full SiC-SiC JBS configuration, caused by the combination of the JBS technology's low reverse recovery charge and the low SiC MOSFET dv/dt during turn-on.

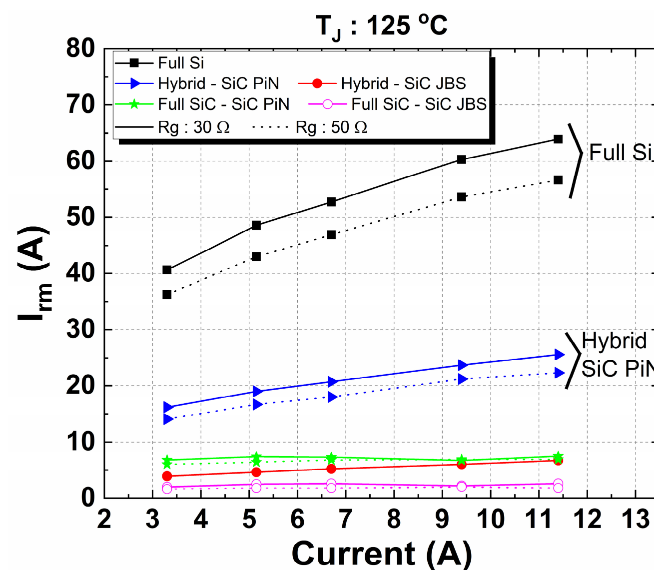

Figure 12. Diode reverse recovery peak current versus forward current for the full Si, hybrid and full SiC configurations at a constant temperature T_J = 125 °C. The results were obtained at 3.6 ± 0.1 kV, R_G = 30 Ω and 50 Ω, and Lσ~200 nH.

Regarding IGBT reliability, the higher stress caused by the SiC PiN diode compared to the SiC JBS diode in hybrid configurations does not significantly impact the power switch reliability. This fact is justified since IGBTs are designed to operate with a Si PiN diode that imposes a much higher reverse recovery peak current stress to the IGBT switch, as shown in Figure 5a. At the full SiC configuration, the SiC PiN diode imposes a reverse recovery current of ~6 A versus a ~2 A current imposed by the SiC JBS diode. This current has an almost constant behavior for different switched load currents, as shown in Figure 12. Independently of the chosen diode technology, the obtained reverse recovery current does not impose harsh conditions on the designed SiC MOSFET [32].

3.2. Performance Evaluation in Inverter System (3L-NPC)

In order to evaluate the potential benefits of the SiC diodes in distinct configurations in a converter system, we simulated a three-phase NPC inverter topology. Such a topology is typically used in high-power medium-voltage applications like industrial drives, FACTS, active front-end converters and shipboard power applications [12,25,40]. Figure 13a shows an NPC phase-leg for full Si and hybrid configurations, and Figure 13b shows one for full SiC configurations. The detailed simulated configurations are demonstrated in Table 1. The hybrid configurations present two possible alternatives: Dout, Din, and Dnpc as SiC PiN (hybrid–SiC PiN configuration) or SiC JBS (hybrid–SiC JBS configuration) diodes.

The controlled switches in the hybrid configurations are Si IGBTs (I). Finally, the full SiC configurations comprise SiC MOSFETs as the main switches (M) with their respective body diodes (Dout and Din). Such anti-parallel diodes are the common choice to reduce wafer area and costs, not requiring additional external diodes [41]. The clamping diodes (Dnpc) can be composed of SiC PiN (full SiC–SiC PiN configuration) or SiC JBS (full SiC–SiC JBS configuration) diodes.

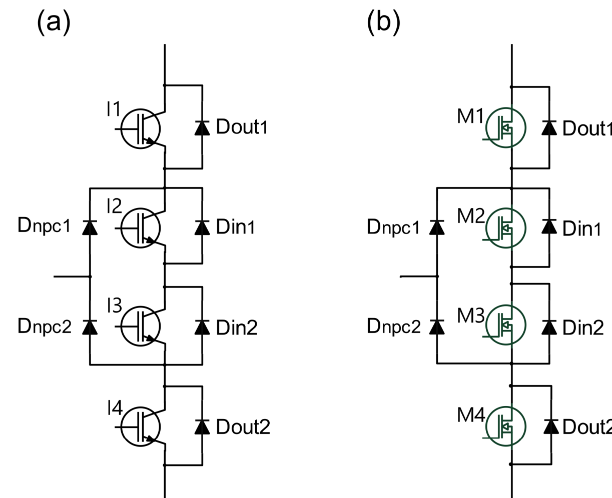

Figure 13. Phase-leg of a 3L-NPC converter. (**a**) Configuration with Si IGBTs, (**b**) configuration with SiC MOSFETs.

Table 1. Semiconductor configurations for inverter simulation.

Configurations	I or M	D_{in}	D_{out}	D_{npc}
Hybrid–SiC PiN	Si IGBT	SiC PiN	SiC PiN	SiC PiN
Hybrid–SiC JBS	Si IGBT	SiC JBS	SiC JBS	SiC JBS
Full SiC–SiC PiN	SiC MOSFET	Body diode	Body diode	SiC PiN
Full SiC–SiC JBS	SiC MOSFET	Body diode	Body diode	SiC JBS

The electrothermal model was developed with the software PLECs. The devices' electrical characteristics (static and dynamic) used in the simulation are from Section 3, for a gate resistance of 30 Ω and junction temperatures of 25 and 125 °C. For the switching losses at higher currents than the ones characterized in Section 3, a linear extrapolation was performed. The static characteristics from the controlled switches and SiC MOSFET body diode were characterized with a Keysight B1505A Power Device Analyzer at junction temperatures of 25 and 125 °C. Each device was thermally modeled as individual chips soldered on typical substrates used in power modules [42,43], as shown in Figure 14. A multilayer Cauer-type thermal network was considered with an assumed heat spreading of 45° [42,43]. Table 2 shows each layer's calculated RC lumped values, considering the dimensions and material properties of the SiC PiN and JBS diodes. Such modeling was performed for all devices according to their specific dimensions and materials' parameters [42,43]. In addition, a heatsink with a thermal resistance of 0.04 K/W was considered.

Table 3 shows a summary of the converter specifications. We implemented an SPWM modulation technique. Since the devices in this topology present unequal temperature distribution, we considered the most critical operating condition that limits the converter's maximum power rating. Such a condition occurs when one device achieves the maximum allowed junction temperature at the maximum output current allowed. This condition is reached at a maximum modulation factor (m = 1) and load power factor of 1, as demonstrated by [11].

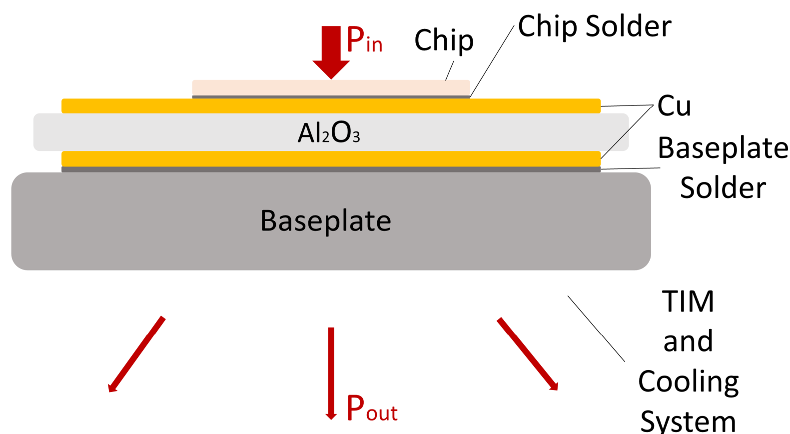

Figure 14. Construction of a chip soldered on a substrate placed inside a module.

Table 2. Parameters for the materials of the SiC diode module.

Layers	Thickness (mm)	Density (kg/m^3)	Specific Heat (J/kg °C)	Thermal Conductivity (W/m °C)	Thermal Resistance (K/W)	Thermal Capacitance (J/K)
Chip	0.45	3210	750	350	8.0357×10^{-2}	1.7334×10^{-2}
Chip solder	0.05	9700	260	78	4.0064×10^{-2}	2.0176×10^{-3}
Copper	0.25	8900	397	386	3.5857×10^{-2}	1.5955×10^{-2}
Al_2O_3	1	3700	880	18	1.8365	9.8494×10^{-2}
Copper	0.25	8900	397	386	1.4215×10^{-2}	4.0246×10^{-2}
Base solder	0.1	9700	260	78	2.5432×10^{-2}	1.2713×10^{-2}
Base	3	8900	397	386	7.4702×10^{-2}	1.1028
Thermal grease	0.1	2250	NA	1	5.6497×10^{-1}	

Table 3. Inverter simulation parameters.

DC link voltage	7.2 kV
Output frequency	50 Hz
Output Voltage	4.16 kV
Ambient temperature	40 °C
Max junction temperature	125 °C
Switching frequency	500–20,000 Hz

Figure 15a,b show the simulation results for the hybrid and full SiC configurations. In the hybrid case, until 24 A output current, the limiting devices that achieve the maximum junction temperature are I1 and I4 (out switches). Up to this current limit, both configurations present similar behavior in terms of switching frequency and efficiency. The SiC JBS presents slightly higher switching frequency capability at sub loads due to the slightly lower switching losses of this configuration, as shown in Figure 10. At higher currents (>24 A), the NPC diode conduction losses start to present a larger influence, being the limiting device in terms of maximum junction temperature. On the other hand, the SiC PiN configuration can extend the output power up to 30 A, presenting a significant 25% load current extension in relation to the 24 A at the same switching frequency of 500 Hz. Such current load extension is essential in the industrial MV drive market that operates at

switching frequencies in the range of 500 Hz, significantly lowering the converter cost per kW by around 25% by using the same active area diodes.

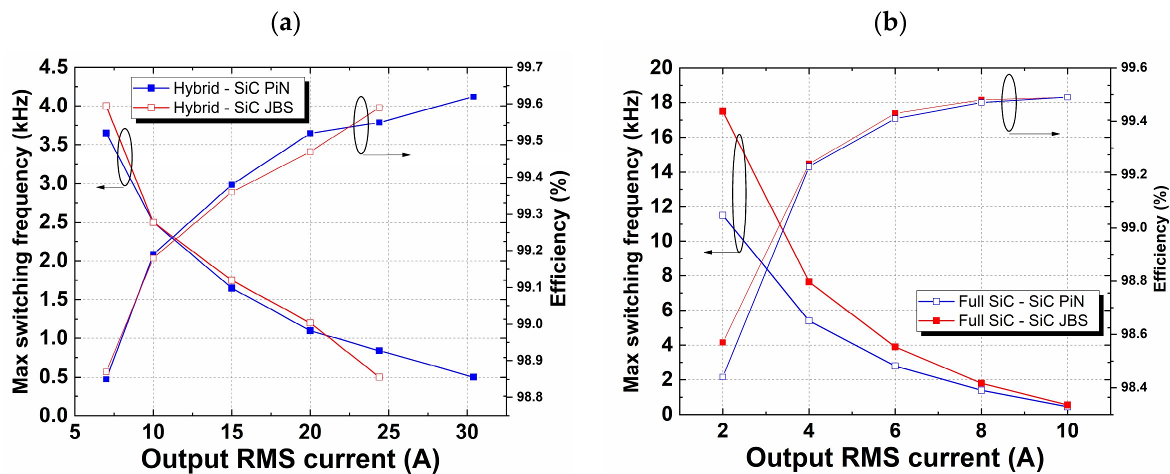

Figure 15. Maximum switching frequency allowed for distinct nominal output currents (thermal criteria of 125 °C) and converter efficiency. (**a**) Hybrid configurations, (**b**) full SiC configurations.

Figure 15b shows the simulation results for the full SiC configuration. It is essential to mention here that the SiC MOSFET device has an estimated current rating of 8 A [32], being the limiting device to achieve higher load currents. The hybrid configurations could achieve higher currents due to the IGBT device's current rating of 25 A. Naturally, the comparison in this case between the hybrid and full SiC configurations is not fair; so, the analysis is limited to comparing diode technologies with the same active area under the same switch configuration (hybrid or full SiC). At the full SiC switch topology, the SiC JBS configuration presents higher switching capability in the current range investigated, mainly due to its slightly lower switching losses. The gap difference reduces and reaches zero at 10 A load current, where the overall conduction losses dominate. Most industrial drive designs push the current rating limits to reduce the converter cost per kW. Furthermore, several industrial drive designs do not require output filters [3]. Thus, high switching frequency designs are not advantageous due to the degradation of efficiency, increased heatsink volume [3] (lower power density) and lower power ratings. Given such characteristics, the designers focus on reaching higher current ratings, which the SiC JBS diode presents disadvantages. It is important to emphasize that the JBS temperatures achieved are lower than 60 °C for the limit cases simulated. Consequently, this device is not operating close to its limit, with this not being the critical component to limit the converter power rating. In cases where cooling may be set differently (e.g., the same heatsink for different switches), creating thermal coupling between different switches, or higher current rating switches are used, the temperature may be further increased. In such a case, the SiC JBS technology can become a limiting factor in the converter power rating due to its low current capability at higher temperatures.

3.3. Long-Term SiC PiN Diode Ruggedness (H3TRB)

The long-term reliability of the fabricated 6.5 kV SiC PiN diodes under high humidity conditions was evaluated in a H3TRB test [44]. Two diodes were submitted to a reverse bias (V) of 5.2 kV (80% of 6.5 kV), an ambient temperature of 85 °C, 85% relative humidity and 1000 h duration. Each DUT leakage current channel is monitored individually, and a switch protection (S) opens in case of device failure to avoid significant damage (Figure 16a). The results in Figure 16b show that both diodes successfully passed the test, enduring the 1000 h without sudden failure. The higher initial leakage current observed for DUT 1 is a systematic measurement error related to a different shunt resistor initially measuring the current. The shunt resistor value was changed to improve the measurement

accuracy (higher sensitivity) at around 80 h (abrupt break in the curve shape). After this change, the shunt resistors were kept the same for the rest of the measurement to have the same sensitivity and fairly compare the current evolution during the test. Additionally, these shunt resistors also need time to reach steady-state and stabilize their temperature, influencing the measured current accuracy in the beginning of the measurements. It is also important to mention that these two devices did not increase leakage current during the test, indicating no blocking degradation in the chip. These results show the potential of this device to operate in harsh conditions in the field. It is important to emphasize that this is one standard test performed by manufacturers during device qualification. Further tests should be performed during a qualification campaign to allow for new device designs in the field [45].

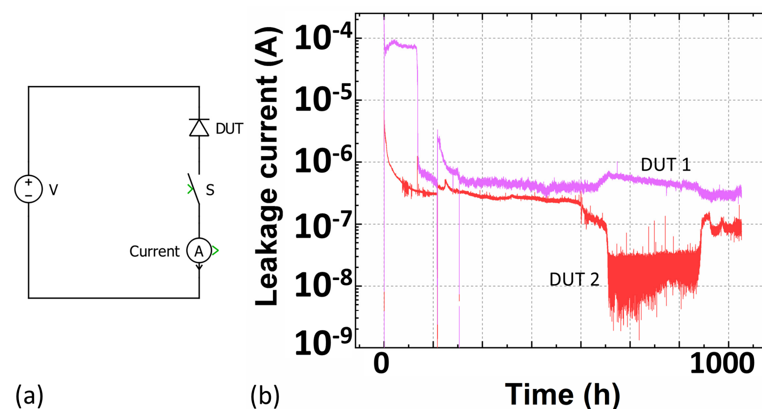

Figure 16. (**a**) One-channel H3TRB circuit schematic. (**b**) Leakage current monitoring of two DUTs during the 1000 h test.

4. Conclusions

The implementation of the 6.5 kV SiC PiN and JBS diodes significantly reduced the controlled switch's turn-on losses as well as the diode reverse recovery loss. This enables the design of power converters with higher efficiency. From both SiC diode technologies, the SiC PiN diode configurations presented slightly higher total switching losses than the JBS diode configurations for most tested conditions. Furthermore, the SiC PiN diode also presented a higher current density capability at high temperatures and lower leakage current, enabling high-power-density designs. Such characteristics are observed in a three-level NPC inverter, with the SiC PiN technology presenting a 25% power extension compared to the SiC JBS technology at the same switching frequency when comparing same-active-area diode devices. Small advantages of the SiC JBS diode technology are present in the low-current-density designs, where higher switching frequencies may be achieved. However, such characteristics are not usual in most industrial drive designs where the current rating limits tend to be pushed as the most effective way to reduce the converter cost per kW. Finally, an industrial standard reliability test also demonstrated long-term endurance in harsh environmental conditions, showing the SiC PiN diode prospect for reliable power electronic designs.

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References

1. Mihaila, A.; Knoll, L.; Bianda, E.; Bellini, M.; Wirths, S.; Alfieri, G.; Kranz, L.; Canales, F.; Rahimo, M. The current status and future prospects of SiC high voltage technology. In Proceedings of the 2018 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 1–5 December 2018; pp. 440–443. [CrossRef]
2. Parashar, S.; Kumar, A.; Bhattacharya, S. High Power Medium Voltage Converters Enabled by High Voltage SiC Power Devices. In Proceedings of the 2018 International Power Electronics Conference (IPEC-Niigata 2018—ECCE Asia), Niigata, Japan, 20–24 May 2018; pp. 3993–4000. [CrossRef]
3. Marzoughi, A.; Burgos, R.; Boroyevich, D. Investigating Impact of Medium-Voltage SiC Mosfets on Medium-Voltage High-Power Industrial Motor Drives. *IEEE J. Emerg. Sel. Top. Power Electron.* **2019**, *7*, 1371–1387. [CrossRef]
4. Ding, R.; Dou, Z.; Qu, Y.; Mei, W.; Liu, G. Analysis on characteristic of 3.3-kV full SiC device and railway traction inverter converter design. *IET Power Electron.* **2022**, *15*, 978–988. [CrossRef]
5. Belkhode, S.; Shukla, A.; Doolla, S. Split-Output Hybrid Active Neutral-Point-Clamped Converter for MV Applications. *IEEE J. Emerg. Sel. Top. Power Electron.* **2021**, *2*, 184–195. [CrossRef]
6. Yin, T.; Lin, L.; Shi, X.; Jing, K. A Si/SiC Hybrid Full-bridge Submodule for Modular Multilevel Converter with Its Control Scheme. *IEEE J. Emerg. Sel. Top. Power Electron.* **2023**, *11*, 712–721. [CrossRef]
7. Belkhode, S.; Shukla, A.; Doolla, S. A Highly Efficient Si/SiC-based Hybrid Active NPC Converter with a Novel Modulation Scheme. *IEEE Trans. Ind. Appl.* **2022**, *58*, 7445–7456. [CrossRef]
8. Diao, F.; Li, Y.; Du, X.; Zhao, Y. An Active Hybrid Modulation Strategy for a Si/SiC Hybrid Multilevel Converter. *IEEE Open J. Power Electron.* **2021**, *2*, 401–413. [CrossRef]
9. Rujas, A.; López, V.M.; Bediaga, A.G.; Berasategi, A.; Nieva, T. Railway Traction DC-DC converter: Comparison of Si, SiC-hybrid, and Full SiC versions with 1700 V power modules. *IET Power Electron.* **2019**, *12*, 3265–3271. [CrossRef]
10. Zhang, L.; Zheng, Z.; Li, C.; Ju, P.; Wu, F.; Gu, Y.; Chen, G. A Si/SiC Hybrid Five-Level Active NPC Inverter With Improved Modulation Scheme. *IEEE Trans. Power Electron.* **2020**, *35*, 4835–4846. [CrossRef]
11. Filsecker, F.; Álvarez, R.; Bernet, S. The Investigation of a 6.5-kV, 1-kA SiC Diode Module for Medium Voltage Converters. *IEEE Trans. Power Electron.* **2014**, *29*, 2272–2280. [CrossRef]
12. Mirzaee, H.; De, A.; Tripathi, A.; Bhattacharya, S. Design Comparison of High-Power Medium-Voltage Converters Based on a 6.5-kV Si-IGBT/Si-PiN Diode, a 6.5-kV Si-IGBT/SiC-JBS Diode, and a 10-kV SiC-MOSFET/SiC-JBS Diode. *IEEE Trans. Ind. Appl.* **2014**, *50*, 609–619. [CrossRef]
13. Fuentes, C.D.; Kouro, S.; Bernet, S. Comparison of 1700-V SiC-MOSFET and Si-IGBT Modules Under Identical Test Setup Conditions. *IEEE Trans. Ind. Appl.* **2019**, *55*, 7765–7775. [CrossRef]
14. Zhang, L.; Yuan, X.; Wu, X.; Shi, C.; Zhang, J.; Zhang, Y. Performance Evaluation of High-Power SiC MOSFET Modules in Comparison to Si IGBT Modules. *IEEE Trans. Power Electron.* **2019**, *34*, 1181–1196. [CrossRef]
15. Qi, J.; Yang, X.; Li, X.; Tian, K.; Mao, Z.; Yang, S.; Song, W. Temperature Dependence of Dynamic Performance Characterization of 1.2-kV SiC Power MOSFETS Compared With Si IGBTs for Wide Temperature Applications. *IEEE Trans. Power Electron.* **2019**, *34*, 9105–9117. [CrossRef]
16. Park, K.-B.; Burkart, R.M.; Agostini, B.; Soeiro, T.B. Application of 1.7-kV 700-A SiC Linpack to Optimize LCL Grid-Tied Converters. In Proceedings of the 2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019—ECCE Asia), Busan, Republic of Korea, 27–30 May 2019; pp. 127–133. [CrossRef]
17. Fabre, J.; Ladoux, P.; Piton, M. Characterization and Implementation of Dual-SiC MOSFET Modules for Future Use in Traction Converters. *IEEE Trans. Power Electron.* **2015**, *30*, 4079–4090. [CrossRef]
18. Marzoughi, A.; Burgos, R.; Boroyevich, D. Characterization and Performance Evaluation of the State-of-the-art 3.3 kV 30 A Full-SiC MOSFETS. *IEEE Trans. Ind. Appl.* **2019**, *55*, 575–583. [CrossRef]
19. Marzoughi, A.; Wang, J.; Burgos, R.; Boroyevich, D. Characterization and Evaluation of the State-of-the-art 3.3-kV 400 A SiC MOSFETS. *IEEE Trans. Ind. Electron.* **2017**, *64*, 8247–8257. [CrossRef]
20. Kicin, S.; Burkart, R.; Loisy, J.-Y.; Canales, F.; Nawaz, M.; Stampf, G.; Morin, P.; Keller, T. Ultra-Fast Switching 3.3 kV SiC High-Power Module. In *PCIM Europe*; IEEE: Piscataway, NJ, USA, 2020; pp. 150–157, ISBN 978-3-8007-5245-4.
21. Rujas, A.; Lopez-Martin, V.M.; Jauregi, A.; Larzabal, I.; Nieva, T. Railway inverter for metro application with 3.3 Kv Full-SiC MOSFET modules. In Proceedings of the 2021 IEEE Vehicle Power and Propulsion Conference (VPPC), Gijon, Spain, 25–28 October 2021. [CrossRef]
22. Sato, K.; Kato, H.; Fukushima, T. Development of SiC Applied Traction System for Next-Generation Shinkansen High-Speed Trains. *IEEJ J. Ind. Appl.* **2020**, *9*, 453–459. [CrossRef]
23. Li, D.; Li, X.; Chang, G.; Qi, F.; Packwood, M.; Pottage, D.; Wang, Y.; Luo, H.; Dai, X.; Liu, G. Characterization of a 3.3-kV Si-SiC Hybrid Power Module in Half-Bridge Topology for Traction Inverter Application. *IEEE Trans. Power Electron.* **2020**, *35*, 13429–13440. [CrossRef]

24. Guo, Z.; Li, H.; Dong, X. A Self-Voltage Balanced Hybrid Three-Level MV Inverter Using 3.3-kV SiC MOSFET Module With False-Trigger-Proof Design. *IEEE J. Emerg. Sel. Top. Power Electron.* **2022**, *10*, 6854–6864. [CrossRef]
25. Filsecker, F.; Álvarez, R.; Bernet, S. Evaluation of 6.5-kV SiC p-i-n Diodes in a Medium Voltage, High Power 3L-NPC Converter. *IEEE Trans. Power Electron.* **2014**, *29*, 5148–5156. [CrossRef]
26. Peters, D.; Bartsch, W.; Thomas, B.; Sommer, R. 6.5 kV SiC PiN Diodes with Improved Forward Characteristics. *Mater. Sci. Forum* **2010**, *645–648*, 901–904. [CrossRef]
27. Peters, D.; Thomas, B.; Duetemeyer, T.; Hunger, T.; Sommer, R. An Experimental Study of High Voltage SiC PiN Diode Modules designed for 6.5 kV/1 kA. *Mater. Sci. Forum* **2011**, *679–680*, 531–534. [CrossRef]
28. Devaty, R.P.; Dudley, M.; Chow, T.P.; Neudeck, P.G. Characterization of Packaged 6.5 kV SiC PiN-Diodes up to 300 °C. *Mater. Sci. Forum* **2012**, *717–720*, 957–960. [CrossRef]
29. Bartsch, W.; Elpelt, R.; Schoerner, R.; Dohnke, K.-O.; Bloecher, B.; Koerber, K. Bipolar 6.5 kV-SiC-Diodes: On the Road to Industrial Application. In Proceedings of the 2005 European Conference on Power Electronics and Applications, Dresden, Germany, 11–14 September 2005; pp. 1–7. [CrossRef]
30. Elasser, A.; Agamy, M.S.; Nasadoki, J.; Loose, P.A.; Bolotnikov, A.V.; Stum, Z.; Raju, R.; Stevanovic, L.; Mari, J.; Menzel, M.; et al. Static and Dynamic Characterization of 6.5-kV 100-A SiC Bipolar PiN Diode Modules. *IEEE Trans. Ind. Appl.* **2014**, *50*, 609–619. [CrossRef]
31. Sundaramoorthy, V.; Mihaila, A.; Spejo, L.; Minamisawa, R.A.; Knoll, L. Performance Comparison of 6.5 kV SiC PiN Diode with 6.5 kV SiC JBS and Si Diodes. *Mater. Sci. Forum* **2022**, *1062*, 588–592. [CrossRef]
32. Knoll, L.; Mihaila, A.; Kranz, L.; Bellini, M.; Wirths, S.; Bianda, E.; Papadopoulos, C.; Rahimo, M. Dynamic Switching and Short Circuit Capability of 6.5 kV Silicon Carbide MOSFETs. In Proceedings of the 2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Chicago, IL, USA, 13–17 May 2018; pp. 451–454. [CrossRef]
33. Kawahara, K.; Hino, S.; Sadamatsu, K.; Nakao, Y.; Yamashiro, Y.; Yamamoto, Y.; Iwamatsu, T.; Nakata, S.; Tomohisa, S.; Yamakawa, S. 6.5 kV Schottky-Barrier-Diode-Embedded SiC-MOSFET for Compact Full-Unipolar Module. In Proceedings of the 2017 29th International Symposium on Power Semiconductor Devices and IC's (ISPSD), Sapporo, Japan, 28 May–1 June 2017; pp. 41–44. [CrossRef]
34. Sakaguchi, T.; Aketa, M.; Nakamura, T.; Nakanishi, M.; Rahimo, M. Characterization of 3.3 kV and 6.5 kV SiC MOSFETs. In *PCIM Europe*; IEEE: Piscataway, NJ, USA, 2017; pp. 39–43, ISBN 978-3-8007-4424-4.
35. Sabri, S.; Van Brunt, E.; Barkley, A.; Hull, B.; O'Loughlin, M.; Burk, A.; Allen, S.; Palmour, J. New Generation 6.5 kV SiC power MOSFET. In Proceedings of the 2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Albuquerque, NM, USA, 30 October–1 November 2017; pp. 246–250. [CrossRef]
36. Du, Y.; Tang, X.; Wei, X.; Sun, S.; Yang, F.; Zhao, Z. Dynamic performance of 6.5 kV SiC MOSFETs body diodes and anti-parallel Schottky barrier diodes. *J. Power. Electron.* **2023**, *23*, 1028–1040. [CrossRef]
37. Mihaila, A.; Knoll, L.; Kranz, L.; Bianda, E.; Alfieri, G.; Bellini, M.; Papadopoulos, M.; Rahimo, M. Performance Evaluation of SiC JBS Diodes Rated for 6.5 kV Applications. *Mater. Sci. Forum* **2018**, *924*, 597–600. [CrossRef]
38. GeneSiC. 1200 V SiC JBS Diodes with Ultra-Low Capacitive Reverse Recovery Charge for Fast Switching Applications. Available online: https://genesicsemi.com/technical-support/sic-schottky-mps/app-notes/1008%20JBS%20Reverse%20Recovery.pdf (accessed on 29 April 2023).
39. Baliga, B.J. *Fundamentals of Power Semiconductor Devices*; Springer: Cham, Switzerland, 2019.
40. Madhusoodhanan, S.; Hatua, K.; Bhattacharya, S.; Leslie, S.; Ryu, S.-H.; Das, M.; Argarwal, A.; Grider, D. Comparison study of 12 kV n-type SiC IGBT with 10 kV SiC MOSFET and 6.5 kV Si IGBT based on 3L-NPC VSC applications. In Proceedings of the 2012 IEEE Energy Conversion Congress and Exposition (ECCE), Raleigh, NC, USA, 15–20 September 2012. [CrossRef]
41. Spejo, L.B.; Akor, I.; Rahimo, M.; Minamisawa, R.A. Life-cycle energy demand comparison of medium voltage silicon IGBT and silicon carbide MOSFET power semiconductor modules in railway traction applications. Power Electron. *Dev. Comp.* **2023**, *6*, 100050. [CrossRef]
42. Ma, K.; He, N.; Liserre, M.; Blaabjerg, F. Frequency-Domain Thermal Modelling and Characterization of Power Semiconductor Devices. *IEEE Trans. Power Electron.* **2016**, *31*, 7183–7193. [CrossRef]
43. Xu, M.; Ma, K.; Zhong, Q.; Liserre, M. Frequency-Domain Thermal Modelling of Power Modules Based on Heat Flow Spectrum Analysis. *IEEE Trans. Power Electron.* **2023**, *38*, 2446–2455. [CrossRef]
44. Jormanainen, J.; Mengotti, E.; Soeiro, T.B.; Bianda, E.; Baumann, D.; Friedli, T.; Heinemann, A.; Vulli, A.; Ingman, J. High Humidity, High Temperature and High Voltage Reverse Bias—A Relevant Test for Industrial Applications. In *PCIM Europe*; IEEE: Piscataway, NJ, USA, 2018; pp. 563–569, ISBN 978-3-8007-4646-0.
45. Mengotti, E.; Bianda, E.; Baumann, D.; Schlottig, G.; Canales, F. Industrial approach to the chip and package reliability of SiC MOSFETs (Invited). In Proceedings of the 2023 International Reliability Physics Symposium (IRPS), Monterey, CA, USA, 26–30 March 2023. [CrossRef]

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