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Article

Mechanism and Control Strategies for Current Sharing in Multi-Chip Parallel Automotive Power Modules

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Abstract: Multi-chip parallel power modules are highly favored in applications requiring high capacity and high switching frequency. However, the dynamic current imbalance between parallel chips caused by asymmetric layouts limits the available capacity. This paper presents a method to optimize dynamic current distribution by adjusting the lengths and connection points of bond wires. For the first time, a response surface model and nonlinear constraint optimization algorithm are introduced, along with parameter analysis based on finite element methods, to establish the response surface models for the parasitic inductance of bond wires and DBC (direct bonded copper). By leveraging the optimization goals for parasitic inductance and the analytical expressions of all response surfaces, the dynamic current sharing issue was transformed into a nonlinear constrained optimization problem. The solution to this optimization problem identified the optimal connection points for the bond wires, enhancing dynamic current sharing performance. Simulations and experiments were conducted, revealing that the optimized automotive-grade module exhibited a significant reduction in current differences between parallel branches, from 41.7% to 5.03% compared with the original design. This indicated that the proposed optimization scheme for adjusting bond wire connection points could significantly mitigate current disparities, thereby markedly improving current distribution uniformity.

Keywords: multi-chip parallel power modules; automotive grade; dynamic current sharing; response surface model; nonlinear constrained optimization

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1. Introduction

In recent years, the demand for high-performance automotive power modules has surged, driven by the rapid evolution of electric and hybrid vehicles. These power modules are crucial for managing the electrical energy generated by vehicle power trains, ensuring efficiency, reliability, and optimal performance. Among various architectures, multi-chip parallel configurations are particularly appealing due to their ability to distribute thermal and electrical loads across multiple chips, thereby enhancing power density and efficiency. However, the dynamic current balancing among these chips presents significant challenges, particularly under varying operational conditions. Dynamic current imbalance can lead to excessive thermal stress, reduced reliability, and premature failure of power modules. Consequently, achieving an optimal balance of the dynamic current is essential for maintaining the performance and longevity of these modules [1,2].

The current imbalance in multi-chip power modules includes both static and dynamic current imbalances [3–6]. Under static operating conditions, all parallel chips remain continuously conductive, and the current through each chip is primarily influenced by its inherent electrical characteristics. Variations in these intrinsic characteristics can lead to uneven current distribution; however, this non-uniformity can be effectively mitigated by selecting chips from the same production batch and implementing rigorous screening procedures [7,8]. The issue of dynamic current sharing is more complex as it involves differences in parasitic parameters, such as inductance and capacitance, among the parallel branches [9]. These discrepancies can result in uneven current distribution among the parallel chips during dynamic operating conditions, such as during switching transitions. Addressing the current balancing issue in multi-chip parallel configurations, particularly the dynamic current sharing problem, has become a critical focus in both domestic and international research aimed at enhancing the reliability of automotive-grade power modules. To effectively alleviate mismatched dynamic currents, it is essential to comprehensively understand the mechanisms underlying dynamic current imbalance. The literature sources [10,11] indicate that the variability of parameters such as on-resistance and threshold voltage significantly affects both static and dynamic current balancing. Furthermore, the packaging pin configurations introduce parasitic inductances at the drain and common-source terminals, which also contribute to the consistency of current distribution among parallel devices [12,13]. Previous research has proposed various methods to mitigate dynamic current imbalance among parallel chips. Reference [14] introduced a method based on coupled inductors to eliminate uneven currents in parallel branches. Reference [15] presented a source inductance compensation technique, which reduced the asymmetry of parasitic parameters among different current branches, thereby enhancing current sharing effectiveness. Reference [16] proposed an active compensation method that achieved current sharing among parallel chips by controlling the turn-on and turn-off delays of the driver. In some studies, passive components [17,18], such as resistors, choke coils, and differential capacitors, are encapsulated into power modules to address current imbalances caused by electrical characteristics mismatches. However, these approaches require additional components in the existing systems, increasing complexity and implementation challenges, making them unsuitable for large-scale applications.

In light of the reliability risks potentially introduced by new packaging processes, as well as the need for a delicate balance between performance, cost, and reliability in power modules, this paper proposes a more flexible approach. Specifically, it adjusts the connection points of the power bond wires to balance dynamic currents. In this method, the lengths of the bond wires and the copper circuit lengths between adjacent chip power bond wires are simultaneously optimized to achieve dynamic current balance. This approach offers greater degrees of freedom. Furthermore, it introduces a response surface model and nonlinear optimization algorithms for the first time, facilitating the determination of the optimal positions for bond wire and copper circuit connections.

The specific steps of the proposed method are as follows. First, by investigating the mechanisms underlying dynamic current imbalance in multi-chip parallel configurations, the optimization objectives for various parasitic inductances are identified. Next, a response surface model for the parasitic inductance of the bond wires and copper circuits is established using finite element method (FEM) parameter analysis. The analytical expressions for the response surfaces can be approximated through numerical fitting. Based on the optimization objectives for parasitic inductance and the analytical expressions of all response surfaces, the dynamic current sharing issue is transformed into a nonlinear constrained optimization problem, which can be readily solved using mathematical software. Solutions to this nonlinear optimization problem allow for the determination of optimal connection points for the bond wires and copper circuits, thereby enhancing dynamic current sharing performance.

The remainder of this paper is structured as follows: Section 2 summarizes the optimization objectives for various parasitic inductances by analyzing the mechanisms of dynamic current imbalance in multi-chip parallel power modules. Section 3 employs finite element analysis to perform parameter analysis and establish a response surface model for the parasitic inductance of the bond wires and direct bonded copper (DBC). The dynamic current sharing problem is then reformulated as a nonlinear constrained optimization problem using the optimization objectives for parasitic inductance and the analytical expressions of the response surfaces. By solving this nonlinear optimization problem, the optimal connection points for the bond wires can be determined, thereby improving current sharing capabilities. In Section 4, simulations and experiments are conducted to validate the effectiveness of the proposed method. Finally, Section 5 concludes the paper.

2. Dynamic Current Sharing Mechanism in Multi-Chip Parallel Automotive Modules

2.1. Configuration of Automotive Power Modules

This study focused on a typical 750 V/600 A automotive power module, with its packaging and topology structures shown in Figure 1. The module features a three-phase full-bridge topology, consisting of UVW phases, each with identical chip selection and layout. Each phase includes upper and lower arms, where each arm contains two sets of 750 V/300 A IGBT chips and fast recovery diodes (FRDs). Given the identical chip selection and layout for all three phases, this study conducted current-sharing tests solely on the U phase.

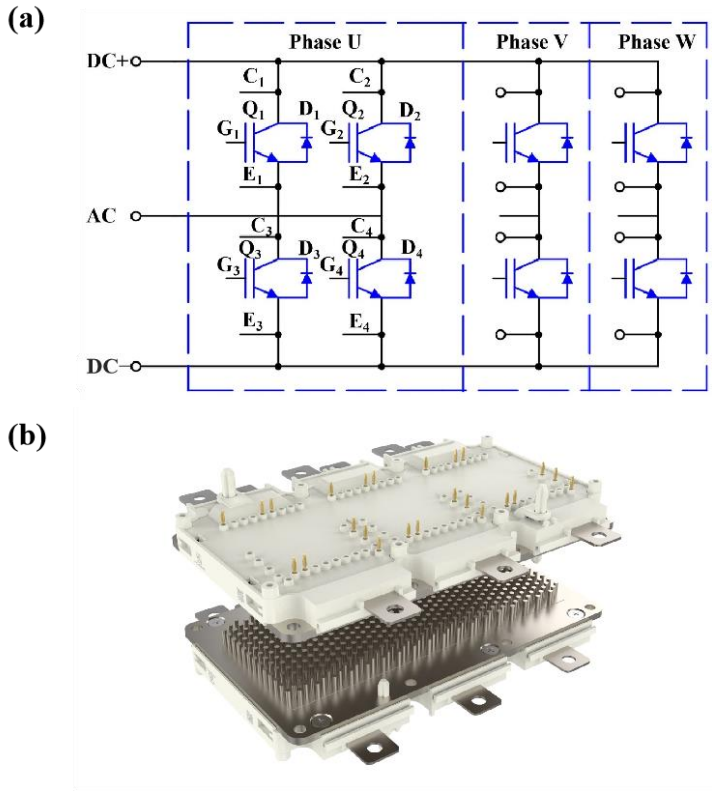

Figure 1. Topology and physical structure of automotive multi-chip parallel module: (**a**) topological diagram and (**b**) physical structure diagram.

2.2. Current Sharing Testing Platform and Results

Figure 2a shows a lower half bridge that served as the power module to be measured, specifically Q_3 to Q_4. All the chips on the platform were equipped with the same drive to control the switch. Figure 2b shows the principle circuit diagram and test platform. The equipment and their models are listed in Table 1.

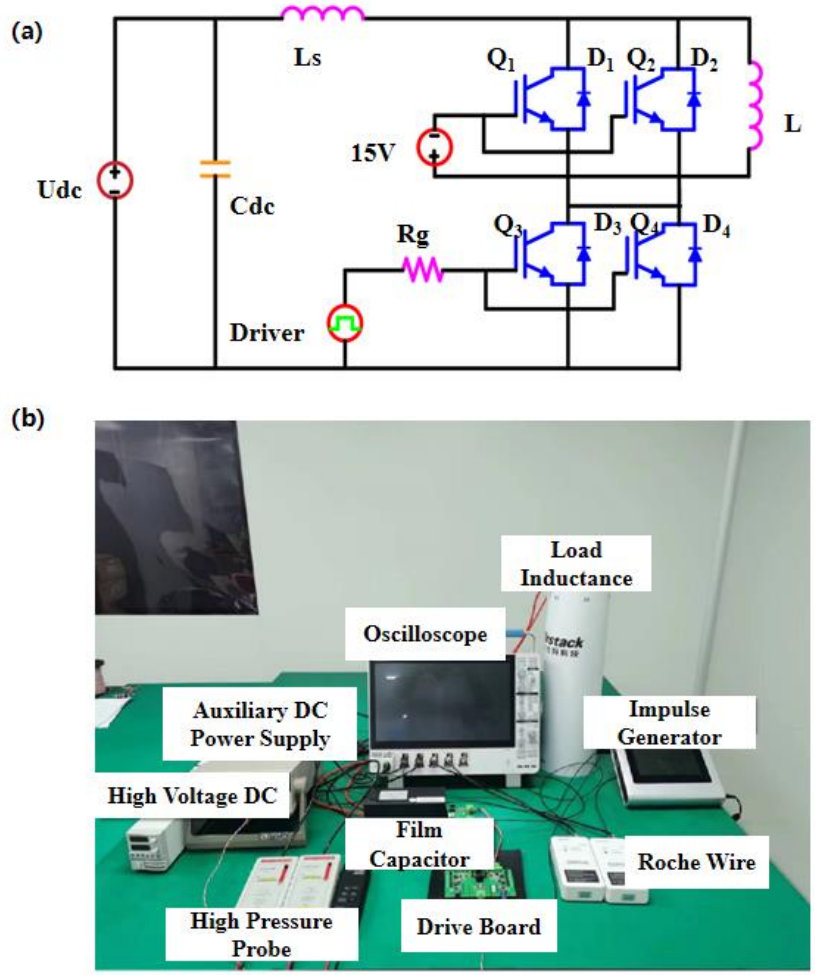

Figure 2. Schematic diagram of test circuit and physical diagram of test platform: (**a**) schematic diagram of test current and (**b**) physical diagram of test platform.

Table 1. Dynamic characteristic test equipment and their models.

Equipment	Model
Oscilloscope	MSO56 5-BW-500
Impulse generator	QTJ15610A
High voltage DC	TDK Z+ 650-1
Auxiliary DC power supply	ITECH IT6302
High pressure probe	Tek THDP0200
Roche wire	IWATSU SS-286A
Load inductance	FS-L-500
Drive board	FZ1200R33KF2C
Film capacitor	/

In the current sharing experiment, based on application conditions, the bus voltage U_{dc} was set to 400 V, the load current was 300 A, and the system stray inductance L_s was 30 nH. To avoid interference caused by inductance saturation and high-frequency skin effects, relevant parameters were optimized during measurement. The load inductance L was set to 20 μH, and the DC bus capacitor C_{dc} was 800 μF. The gate drive turn-on resistance R_{gon} was 3.6 Ω, and the gate drive turn-off resistance R_{goff} was 7.5 Ω.

Figure 3 shows the module at a bus voltage of 400 V and a load current of 300 A. The current distribution imbalance was used to describe the differences in current among the

branches in the multi-chip parallel system. The calculation formula for the current distribution imbalance is given by

$$\delta_i = \frac{\Delta i_c}{i_{ave}} = \frac{\max\left(i_{c1}, i_{c2}...i_{ck}\right) - \min\left(i_{c1}, i_{c2}...i_{ck}\right)}{\left(i_{c1} + i_{c2}...+ i_{ck}\right)/k}. \quad (1)$$

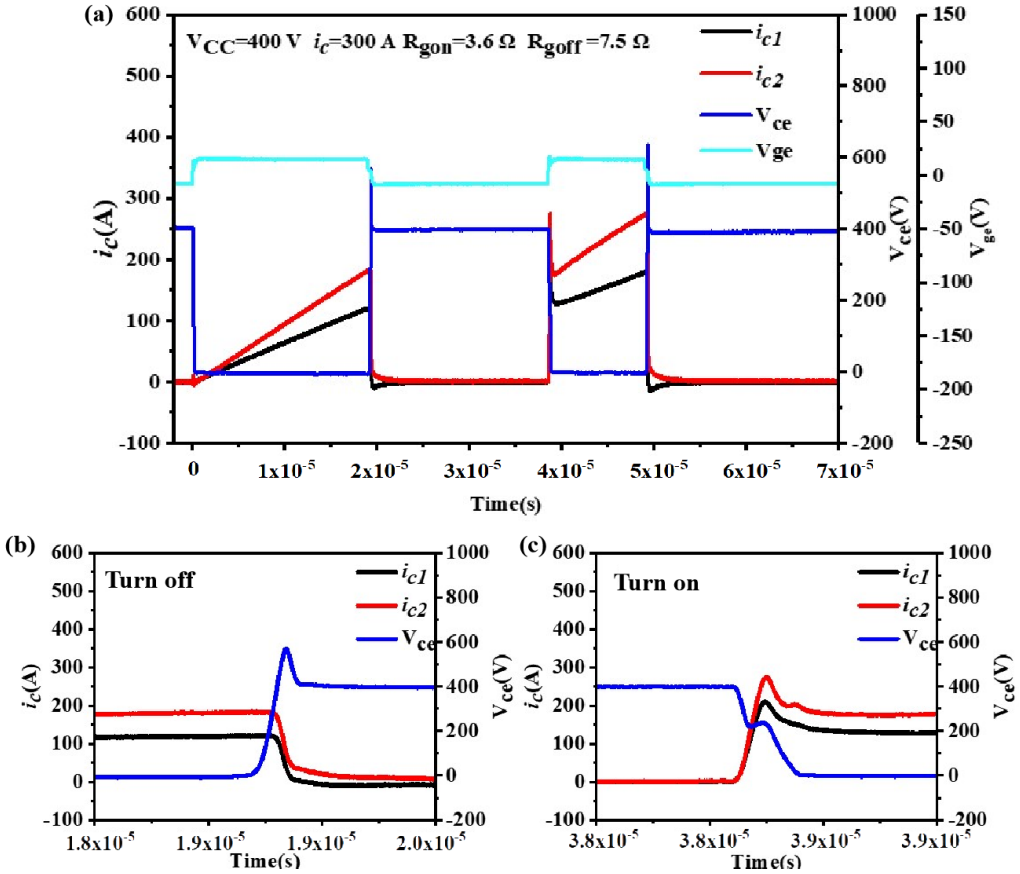

Figure 3. Dynamic current distribution results of two parallel chips in the module at a load current of 600 A: (**a**) double pulse test waveform, (**b**) dynamic current distribution of turn-off current for two parallel chips, and (**c**) dynamic current distribution of turn-on current for two parallel chips.

In the formula, the symbol δ_i symbolizes the discrepancy in the distribution of current, i_{ave} is the average current of the interconnected circuitry of the chip, and i_{ck} is utilized to represent the highest current value on the connection circuit.

Figure 3a demonstrates that when the load current of the multi-chip coupling module was 300 A, the currents of the two supports were calculated to be 181.3 A and 118.7 A, respectively, using Formula (1) to measure the imbalance of the coupled support current. The current imbalances of 41.7% indicated a significant disparity in the distribution of the two support currents.

2.3. Analysis of Dynamic Current Equalization Mechanism

The current distribution of the linked chip was analyzed separately for the effects of L_c, L_e, and L_g during the power module's turn-on and turn-off. To streamline the analytical circuitry, a dual pulse test equivalent circuit model of the multi-chip and associated standard power module was created, as depicted in Figure 4.

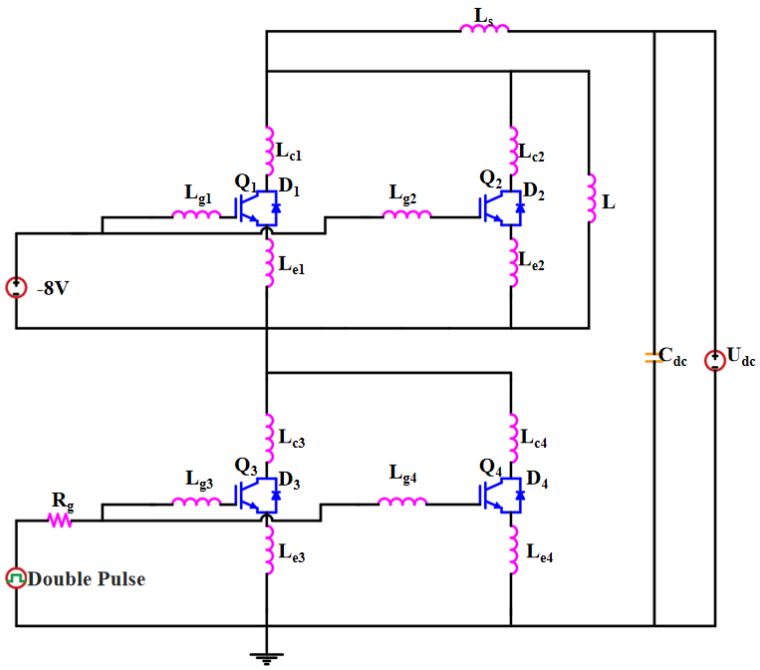

Figure 4. Equivalent circuit model for double pulse testing of multi-chip parallel automotive power modules.

When the IGBT chip was switched on and off, it operated in the saturation zone. In the case of a multi-chip power module, the combined electrode current of the two chips can be expressed as

$$\begin{cases} i_{c1} = g_{f1}(V_{ge1} - V_{th1}) \\ i_{c2} = g_{f2}(V_{ge2} - V_{th2}) \end{cases}. \tag{2}$$

For the chip, the gate voltage V_{ge} and the emit-gate voltage were important, while for the power chip, the threshold voltage V_{th} was crucial. The interconnector of the chip, unit A/V, can be represented as g_f. The calculation method for the intercom is given as [18]

$$g_f = \frac{\mu_n C_{OX} Z_{CH}}{2L_{CH}}(V_{ge} - V_{th}) = \beta[V_{ge} - V_{th}]^2. \tag{3}$$

In the given formula, μ_n represents the rate at which the carrier transfers; Z_{CH} and L_{CH} denote the breadth and length of the canyon, respectively; and C_{OX} represents the unit area capacitor of the mercury layer, which can be mathematically stated as

$$C_{OX} = \frac{\varepsilon_{OX}}{t_{OX}}. \tag{4}$$

The variable ε_{OX} denotes the dielectric constant of silicon dioxide, and t_{OX} represents the thickness of the mercury layer.

Formula (2) states that the power chip can be represented as a regulated current source. The analogous circuit design of the multi-chip coupling module is depicted in Figure 5.

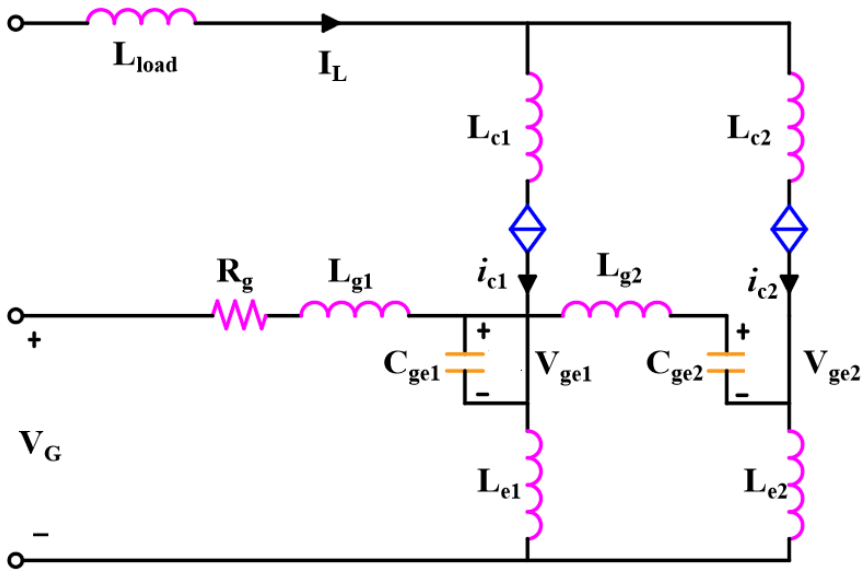

Figure 5. Multi-chip coupled module equivalent circuit chart.

This study examined the dynamic average current behavior of interconnected modules. To achieve consistency, the same batch of IGBT chips with the same specifications was employed. These chips underwent strict filtering to maintain the same threshold voltage V_{th} and chip cross-conductor g_f values. Therefore, Formula (2) can be derived by dividing into smaller parts:

$$\begin{cases} g_{f1} = g_{f2} \\ \dfrac{di_c}{dt} = g_f \dfrac{dv_{ge}}{dt} \\ V_{th1} = V_{th2} \end{cases}. \tag{5}$$

Based on the circuit diagram in Figure 5 and using the Kirchhoff voltage law (KVL), we can analyze the gate emission voltage V_{ge} in relation to the gate current:

$$V_{ge} = V_G - R_g C_{ge} \frac{dV_{ge}}{dt} - L_g C_{ge} \frac{d^2 V_{ge}}{dt^2} - L_e \frac{di_c}{dt}. \tag{6}$$

In order to simplify the analysis, we took the concentration electrode i_c and the emit-gate current i_e to be approximately equal. According to the analysis, the parasitic inductance was influenced by the negative feedback from the gate inductance L_e to the gate voltage V_{ge} of the gate transmission. This, in turn, affected the switching and shutdown properties of the power module in the multi-chip coupling module on any of the chip supports. Formulas (2) and (6) can be obtained by combining them:

$$i_{c1} - i_{c2} \approx g_f (L_{e2} - L_{e1}) \frac{di_L}{3dt}. \tag{7}$$

From Formula (7), it can be derived that during the switching process of the power module, this branch current imbalance was approximately positively correlated with the corresponding differences. Thus, it could be determined that the former was linearly related to the imbalance of each branch inductance. When the device was turned on, due to the influence of inductance at both ends of the driver circuit, a reverse voltage was formed,

which changed the voltage between the collector and emitter, thereby affecting the collector current and its distribution. As the inductance L_e of each branch increased, the voltage and current between the collector and emitter decreased.

The modeling research focused on the module depicted in Figure 1. This module was a three-phase full bridge construction, and the arrangement of the three phases was identical. Therefore, we only needed to analyze and construct the equivalent circuit model of one phase, as illustrated in Figure 6.

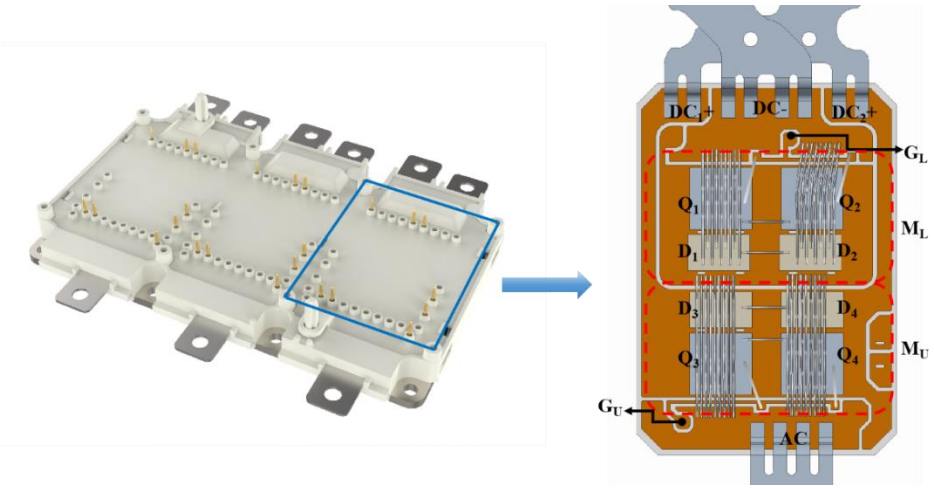

Figure 6. Single-phase direct bonded copper (DBC) layout of multi-chip coupled power module for vehicle standard.

The study utilized the limited element software Q3D 2020 to establish a simulation analysis model for the quantification of parasitic parameters. According to the relevant design manual, it was known that the typical opening time at a normal temperature of 25 °C was 280 ns (R_g = 5 Ω). In this investigation, the opening time variation was calibrated to the scan frequency range, which was set between 1 and 100 MHz. The relevant parameter is displayed in Table 2.

Table 2. Results of extracting the Q3D parasitic parameter of the chip at 10 MHz.

Parameter	Value	Physical Meaning
L_{c1}, R_{c1}	10.23 nH, 1.87 mΩ	Parasitic parameters of parallel chip collector
L_{c2}, R_{c2}	10.47 nH, 1.95 mΩ	
L_{c3}, R_{c3}	13.46 nH, 2.01 mΩ	
L_{c4}, R_{c4}	11.23 nH, 1.99 mΩ	
L_{g1}, R_{g1}	10.71 nH, 1.86 mΩ	Parasitic parameters of parallel chip gate
L_{g2}, R_{g2}	14.07 nH, 2.41 mΩ	
L_{g3}, R_{g3}	18.14 nH, 3.24 mΩ	
L_{g4}, R_{g4}	32.52 nH, 4.60 mΩ	
L_{e1}, R_{e1}	9.94 nH, 1.413 mΩ	Parasitic parameters of parallel chip emitter
L_{e2}, R_{g2}	9.73 nH, 1.352 mΩ	
L_{e3}, R_{g3}	12.10 nH, 1.592 mΩ	
L_{e4}, R_{g4}	8.32 nH, 1.426 mΩ	

From the data in Table 2, it can be seen that the asymmetry in the layout led to differences in loop parasitic parameters, which in turn affected the uniformity of current distribution. Based on the results from the above figures and tables, the parasitic inductance of

the two power loops in the lower bridge arms could be calculated using the following expression:

$$\begin{cases} L_{\sigma 3} = L_{c3} + L_{e3} = 25.56\text{nH} \\ L_{\sigma 4} = L_{c4} + L_{e4} = 19.55\text{nH} \end{cases}. \tag{8}$$

Formula (9) displays the inductance imbalance of the distribution for each power circuit:

$$\delta_L = \frac{\max\left(L_{\sigma 3}, L_{\sigma 4}\right) - \min\left(L_{\sigma 3}, L_{\sigma 4}\right)}{L_{ave}}. \tag{9}$$

In the given formula, δ_L represents the inductance imbalance; L_{ave} denotes its mean value; and $L_{\sigma 3}, L_{\sigma 4}$ refer to the lower arm and the inductance value on the connecting pathway, respectively. Each correlates to its respective inductance value. Based on a detailed investigation (9), the observed imbalance was 26.7%.

3. Response Surface Model of Parasitic Inductance

The response surface model could help establish the relationship between selected design parameters and selected responses. Through this method, this article attempts to determine the relationship between critical geometric parameters and parasitic inductance. An analytical expression for the response surface could be obtained through numerical fitting to assist in evaluating the parasitic inductance in power modules. In traditional power modules, parasitic inductance is mainly caused by the connection lines and copper traces on DBC. Therefore, this section discusses the response surface model of the bonding line and the bonding point position on DBC separately.

3.1. Response Surface Model for the Parasitic Inductance of Bonding Wires

The diagram above illustrates the correlation between the shape and size of the emission clutch in the original power module. In practical production scenarios, it is not feasible to frequently modify the clutch's diameter d and arc height h, as this significantly affects the product's reliability. The diameter of the bond wire line in Figure 7 is 15 mil, which is equivalent to 0.375 mm. The length of the key junction line, l_w, is measured in millimeters. The height of the keyword junction, h, is 2 mm. The length of the key point junction, l_a, can be determined based on the detection results, and it is found to be 1.2 mm for a key junction line with an a diameter of 0.375 mm. The gap of the button junction, a, is 0.8 mm in this study. Typically, a higher number of connector roots leads to improved flow performance. However, this improvement is limited by the aluminum coil area factor, and the connection is usually not bigger than nine rows. Therefore, in this part, we only considered the distance between the two welding points of the connection.

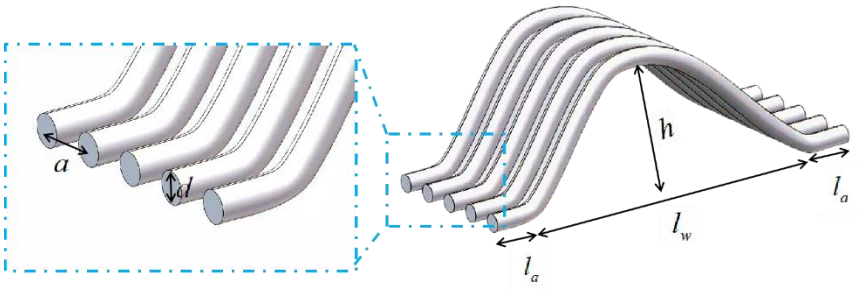

Figure 7. Schematic diagram of the bond wire dimension parameters.

$$L_W = 0.00648 l_w^2 + 0.34628 l_w + 0.38965. \tag{10}$$

The fitting error of Formula (10) is obtained using the following formula:

$$\Delta L_W = \left| L_{FIT} - L_{FEM} \right|. \tag{11}$$

In the formula, L_{FIT} represents the fitted inductance value, while L_{FEM} represents the simulated inductance value.

The parasitic inductance values of the bonding wires at various lengths were determined by analysis using the Q3D model. The data were then subjected to fitting analysis to provide the fitting function and curves for the inductance L_W and length l_w, as shown in Figure 8a and Figure 8b, respectively. Upon analysis, it could be determined that the maximum residual of Figure 8b was less than 0.094 nH, indicating a high level of accuracy in the fitted function.

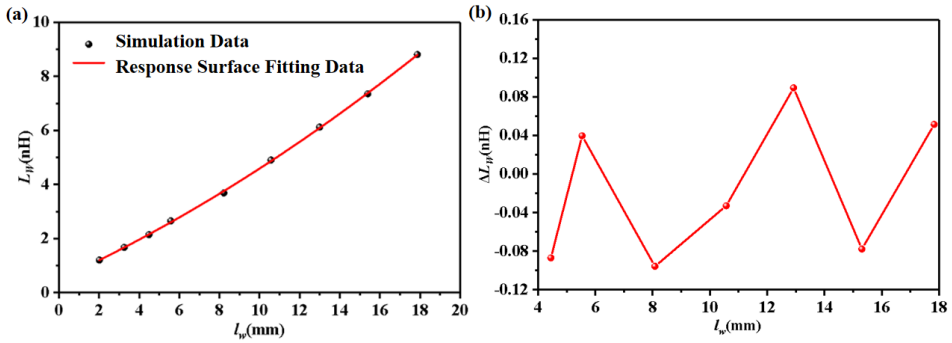

Figure 8. Response surface fitting results and residuals for bond wire inductance and length: (**a**) response surface fitting results and (**b**) response surface fitting residuals.

3.2. Response Surface Model for the Parasitic Inductance of Copper Traces on DBC

Figure 9 shows the DBC layout and chip position diagram of the studied power module. The positions of the bonding wires on the DBC are denoted as W_1 and W_2. The parasitic inductance L_{cuW1} between the aluminum wire bonding point and the power terminal AC in loop 1 and the parasitic inductance L_{cuW2} between the aluminum wire bonding point and the power terminal AC in loop 2 affected the dynamic current sharing performance. Since the overall shape of the aluminum wire was fixed, the parasitic inductance of the aluminum wire depended on the bonding point positions on the DBC. As shown in Figure 9, a coordinate system was established with the left edge of the AC copper layer of the upper bridge arm as the origin. The two coordinate points in Figure 9 correspond to the bonding points of the two sets of bonding wires. Theoretical analysis showed that adjusting the positions of these two coordinate points W_1 and W_2 would change the corresponding inductance values.

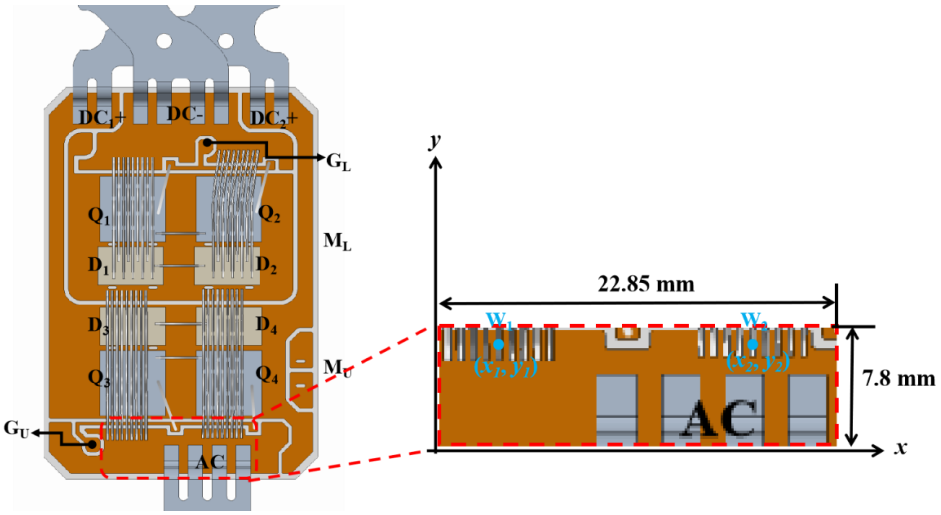

Figure 9. The layout of the DBC and the location of the chip.

The experiment utilized the parasitic inductance L_{cuW1} and L_{cuW2} as response values, while x_1, x_2, x_3, and x_4 were used as response factors. The experimental parasitical electromagnets were obtained using ANSYS Q3D.

The contrast analysis indicated that the average of the discrepancies in the Cubic model was greater, resulting in an ideal matching performance. Thus, according to the contrasting outcomes, Formula (12) represents the calculation function of the parasitic inductance employed in the Cubic model:

$$\begin{aligned} L_{cuW1} &= 564.56 - -225.231x_1 - 74.63y_1 \\ &+17.92x_1y_1 + 31.37x_1^2 + 4.61y_1^2 \\ &-1.19x_1^2y_1 - 0.33x_1y_1^2 \\ &-1.47x_1^3 - 0.18y_1^3 \end{aligned} \quad . \tag{12}$$

An examination of Figure 10 reveals that when x_1 was held constant, the L_{cuW1} exhibited a progressive increase as y_1 increased. Similarly, when y_1 remained unchanged, it also increased in conjunction with x_1. When comparing the two, the impact of y_1 on L_{cuW1} was considerably more than the magnitude of x_1.

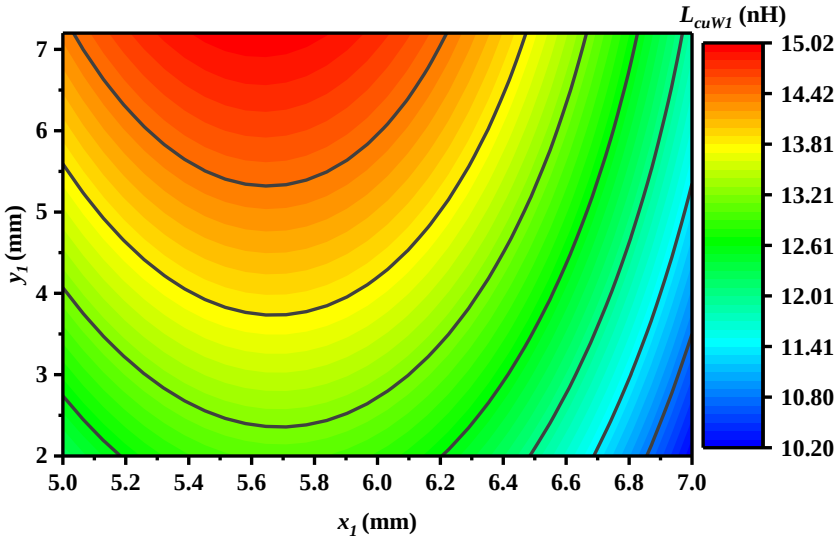

Figure 10. Parasitic inductance L_{cuW1} with x_1 and y_1 response surface results.

Based on the data presented in the table, it can be concluded that the Cubic model exhibited the highest differential, indicating a superior matching effect. Considering this information, the inductance L_{cuW2} utilized the parasitic inductance calculation function, which was specifically tailored to the Cubic model, as expressed by Formula (13):

$$\begin{aligned} L_{cuW2} = & -253.43 + 45.042x_2 - 31.197y_2 \\ & +0.181x_2y_2 - 2.433x_2^2 + 12.268y_2^2 \\ & +0.008x_2^2y_2 - 0.112x_2y_2^2 \\ & +0.043x_2^3 - 1.38y_2^3 \end{aligned} . \tag{13}$$

The response curve of coordinate points x_2 and y_2 is as shown in Figure 11. Specific analysis of this diagram shows that when x_2 was fixed, L_{cuW2} gradually increased as y_2 increased, and when y_2 remained unchanged, the parasitic inductance L_{cuW2} first increased and then decreased with the increase in x_2.

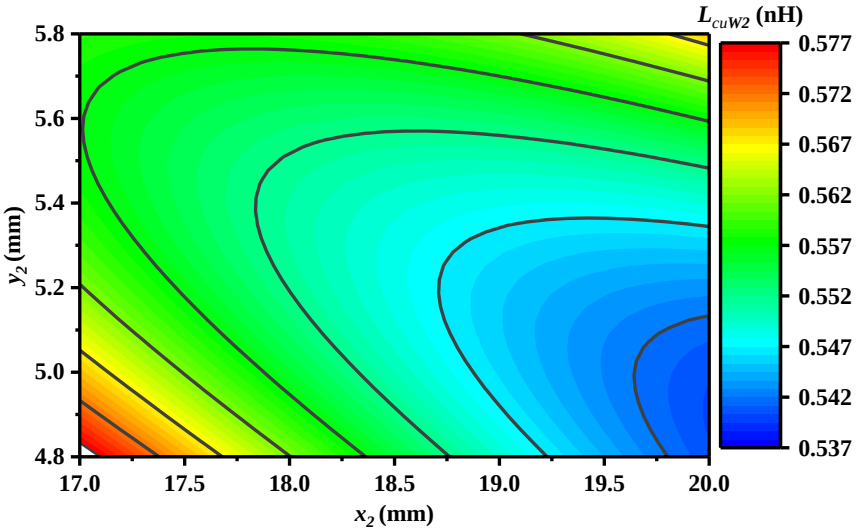

Figure 11. Parasitic inductance L_{cuW2} with x_2 and y_2 response surface results.

4. Automotive Power Module Equivalent Current Optimization Mathematical Model

4.1. The Theory and Evaluation Indicators of Inductance Optimization of the Lower Arm of the Bridge

According to the previous study, it is evident that the inductance connectivity conditions resulted in significant parasitic differences between the two connected branches. Specifically, the supporting circuit 1 exhibited the highest level of electromagnetism, while support 2 had the lowest level. Typically, the discrepancies are assessed based on the inductance imbalance, which is indicated by the following expression:

$$\delta_L = \frac{\Delta L_a}{L_{ave}} \times 100\% . \tag{14}$$

In the formula, ΔL_a and L_{ave} are the extreme differences and mean values of the gate parasitic inductance emitted by the two connected power circuits, calculating the formula as

$$\begin{cases} \Delta L_a = \max\left(L_{\sigma 3}, L_{\sigma 4}\right) - \min\left(L_{\sigma 3}, L_{\sigma 4}\right) \\ L_{ave} = \dfrac{L_{\sigma 3} + L_{\sigma 4}}{2} \end{cases} . \tag{15}$$

Based on the analysis in the previous section, $L_{\sigma 3}, L_{\sigma 4}$ are the range and mean value of the parasitic inductance of the emitter in the two parallel branch power circuits, respectively. The calculation formulas are

$$\begin{cases} L_{\sigma 3} = L_{W3} + L_{cuW1} + L_{c3} \\ L_{\sigma 4} = L_{W4} + L_{cuW2} + L_{c4} \end{cases}. \tag{16}$$

Replacing Formulas (14) and (15) with Formula (16) can obtain

$$\delta_L = \frac{L_{W3} + L_{cuW1} + L_{c3} - L_{W4} - L_{cuW2} - L_{c4}}{\left(L_{W3} + L_{cuW1} + L_{c3} + L_{W4} + L_{cuW2} + L_{c4}\right)/2}. \tag{17}$$

Figure 9 shows that since the chip layout was a symmetrical distribution, the emission gate inductance L_{c3} and L_{c4} were approximately equal, so $L_{c3} = L_{c4}$, and each chip was connected in the same way, so $L_{W3} = L_{W4}$.

Thus, Formula (18) can be changed to

$$\delta_L = \frac{L_{cuW1} - L_{cuW2}}{\left(2L_{W3} + L_{cuW1} + 2L_{c3} + L_{cuW2}\right)/2}. \tag{18}$$

As is known from Formula (18), differences in parasitic inductance can be suppressed and interconnected by the following methods.

(1) Reducing the Extreme Difference ΔL_a

Formula (18) determines that a decrease in L_{cuW1} or an increase in L_{cuW2} can be deducted from the extreme difference ΔL_a. By changing the position of the welding point of the bond wire, the extreme difference ΔL_a can be achieved in reducing the parasitic inductance of the joint circuitry.

(2) Increasing Average Inductance L_{ave}

Based on the analysis, raising the average value of L_{ave} can effectively decrease δ_L can enhance the current perpendicularity. Study discovered that there is not a strong correlation between L_{ave} and the average current. However, increasing the current after L_{ave} will result in a substantial shock and noticeable inductance interference (EMI). In situations where EMI interference occurs, it may lead to abnormal switch behavior. Moreover, this can further exacerbate the disparity in current distribution within the chip, negatively impacting its performance.

According to the findings of the research above, the main objective of this current optimization procedure should be to minimize the large variation in parasitic inductance ΔL_a, while the optimized average L_{ave} value relatively unaffected.

4.2. Key Line Position Optimization Algorithm

The power module analyzed in this study had a DBC with a copper layer thickness of 0.3 mm. The DBC configuration and chip position chart for the module may be seen in Figure 8. The major joints on the DBC were located at W_1 and W_2, respectively. The presence of parasitic inductance L_{cuW1} and L_{cuW2} in circuit 1 and circuit 2, respectively, between the aluminum cord connector and the power terminal AC, affected the dynamic current median current performance. This was because the positions of these parasitic inductances on the DBC depended on the fixed overall shape of the aluminum cable. Figure 9 illustrates that the left edge of the bridge arm AC copper layer serves as the original point for constructing coordinates, whereas the higher left margins of the bridge arm AC copper layer are considered the origin point. The two coordinate points in Figure 9 represent the respective bond wire locations of the two sets of bond wire. This indicates that the position

adjustment of two coordinates, W_1 and W_2, can be accomplished by altering the parasitic inductance.

To successfully minimize the disruption caused by layout adjustments during the study process, it was crucial to restrict the angle of deviation θ of the link within the restrictions imposed by the procedure. Specifically, the angle should not exceed 30°. Simultaneously, it was important that the primary intersection did not disrupt the terminal. By considering these limitations together, we could establish the locations for the two primary intersections:

$$\begin{cases} 5 \le x_1 \le \dfrac{\sqrt{3}}{3} y_1 + 5, 2 \le \mathrm{y}_2 \le 7.2 \\ 17 \le x_2 \le \dfrac{\sqrt{3}}{3} y_2 + 17, 2 \le y_2 \le 3 \end{cases} . \tag{19}$$

Based on the previous chapter analysis, the calculation formula of the inductance of all parts of the linked circuitry can be obtained:

$$\begin{aligned} &L_{cuW1} = 564.56 - 225.231x_1 - 74.63y_1 + 17.92x_1y_1 + 31.37x_1^2 \\ &+4.61y_1^2 - 1.19x_1^2y_1 - 0.33x_1y_1^2 - 1.47x_1^3 - 0.18y_1^3 \\ &L_{cuW2} = -253.43 + 45.042x_2 - 31.197y_2 + 0.181x_2y_2 - 2.433x_2^2 \\ &+12.268y_2^2 + 0.008x_2^2y_2 - 0.112x_2y_2^2 + 0.043x_2^3 - 1.38y_2^3 \\ &\Delta L_a = 817.99 - 225.231x_1 - 74.63y_1 + 17.92x_1y_1 + 31.37x_1^2 \\ &+4.61y_1^2 - 1.19x_1^2y_1 - 0.33x_1y_1^2 - 1.47x_1^3 - 0.18y_1^3 - 45.042x_2 \\ &+31.197y_2 - 0.181x_2y_2 + 2.433x_2^2 - 12.268y_2^2 - 0.008x_2^2y_2 \\ &+0.112x_2y_2^2 - 0.043x_2^3 + 1.38y_2^3 \end{aligned} . \tag{20}$$

Formula (20) states that the original query may be represented as finding the least value of the function ΔL_a. In order to solve this, certain constraints must be satisfied. When assessing the arrangement of the inductance, we designated δ_L as the indicator. The particle cluster algorithm is a highly efficient and innovative technique that is extensively employed in problem-solving optimization. This method primarily relies on the search for the optimal particle, taking into account the adaptability of various continuous iterative optimizations, in order to achieve the optimal solution that satisfies the given constraints. In comparison analysis, this method demonstrated several advantages, including low parameters, high accuracy, high real-time capabilities, and wide applicability in various problem-solving domains. Hence, this approach was also employed in this research to enhance the efficiency of the search for solutions. Currently, utilizing Matlab 2016a for programming is the most optimal method. To obtain the most efficient coordinates for the front and rear bond wire, refer to Table 3.

Table 3. Optimized front and rear bond wire coordinates.

Variable	Initial Value	Optimized Value
x_1	5	6.7
y_1	5.8	4.7
x_2	20	17.5
y_2	5.8	5.4

The combined circuit inductance results for the initial modules and the optimized modules are shown in Table 4. Using the inductance imbalance δ_L as an evaluation indicator, the optimized module and the interconnected circuit inductance difference ΔL_a was greatly reduced. Compared with the initial program, the optimized program showed

a reduction in the source gate inductance imbalance δ_L from 26.7% to 4.21%, significantly reducing the inductance differences between the original module's joint support pathways. Figure 12 shows the DBC configuration of the initial automotive power module and the ideal arrangement following critical point optimization.

Table 4. Optimized front and rear bond wire coordinates.

	$L_{\sigma 3}$ **(nH)**	$L_{\sigma 4}$ **(nH)**	ΔL_a **(nH)**	L_{ave} **(nH)**	δ_L **(%)**
Initial module	25.56	19.55	6.01	22.55	26.7
Optimized module	20.85	19.99	0.86	20.42	4.21

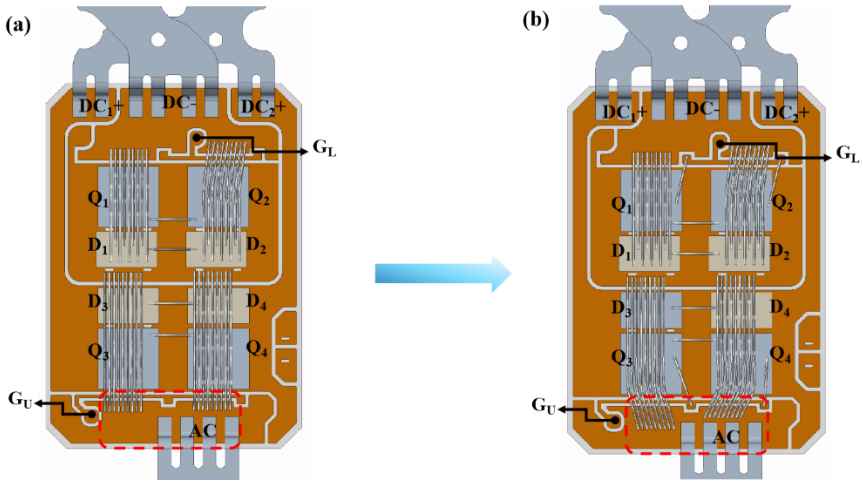

Figure 12. DBC layout of initial modules and optimized modules: (**a**) initial modules and (**b**) optimized modules.

4.3. Verification of the Effectiveness of Current Sharing Optimization

To prevent any mismatch of device settings, the chip was chosen beforehand. For the multi-chip and connected dynamic test platform, based on the application conditions, the bus voltage Udc was set to 400 V, the load current was 300 A, and the system stray inductance Ls was 30 nH. To avoid interference caused by inductance saturation and high-frequency skin effects, the relevant parameters were optimized during measurement. The load inductance L was set to 20 μH, and the DC bus capacitor Cdc was 800 μF. The gate drive turn-on resistance Rgon was 3.6 Ω, and the gate drive turn-off resistance Rgoff was 7.5 Ω. The gate turn-on voltage Vgeon and gate turn-off voltage Vgeoff were set to 15 V and −8 V, respectively.

The analysis of Figure 13 and Table 5 reveals a substantial decrease in the current differential values between the optimized designed automotive modules. Specifically, the reduction was from 41.7% to 5.03% when compared with the initial modules and connected support routes. The research demonstrated that the optimization suggested could enhance the issue of multi-chip and uneven flow in the automotive power module.

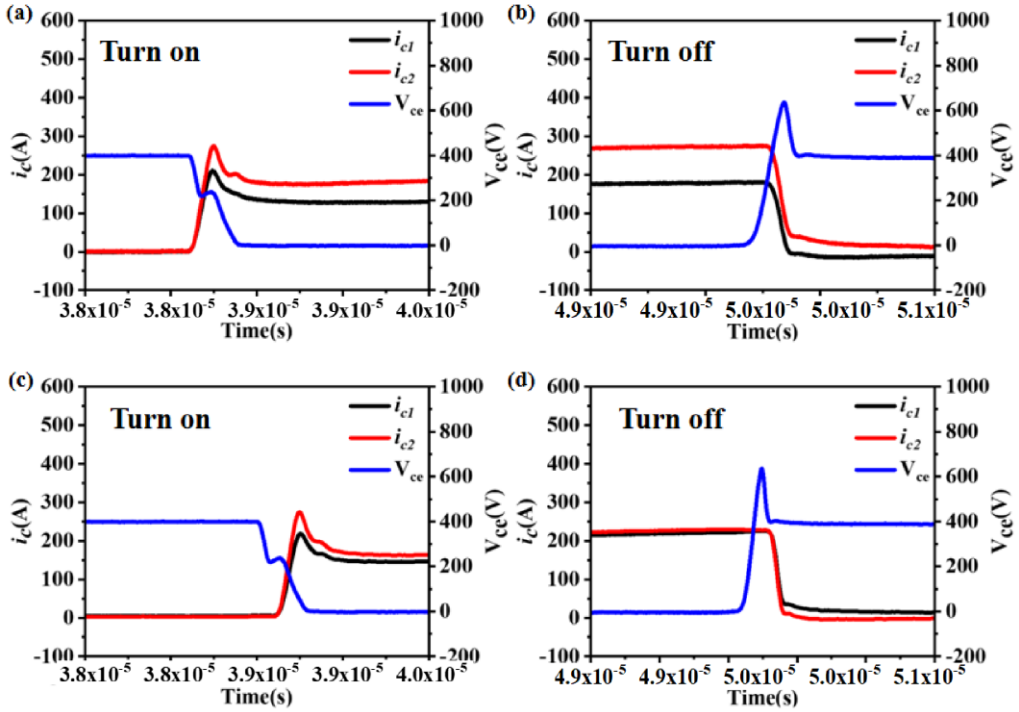

Figure 13. Measured switching waveforms of two branch circuits in initial and optimized automotive modules: (**a**) measured turn-on current waveform of the initial module, (**b**) measured turn-off current waveform of the initial module, (**c**) measured turn-on current waveform of the optimized module, and (**d**) measured turn-off current waveform of the optimized module.

Table 5. Comparison of parallel branch currents in half-bridge during turn-off process: initial vs. optimized.

Parameter	Initial Experimental Value	Optimized Experimental Value
i_{c1} / A	181.3	154
i_{c2} / A	118.7	146
Δi_c / A	62.6	8
i_{ave} / A	150	150
δ / %	41.7	5.03

5. Conclusions

This paper analyzes the dynamic characteristics of a typical automotive multi-chip parallel module, thoroughly exploring the key factors affecting dynamic current sharing in power modules. It elucidates the mechanism of multi-chip parallel current sharing in power modules. Through the study of the parasitic inductance in the power circuit and its impact on dynamic current sharing, a theoretical model for internal current sharing in multi-chip parallel modules and a parasitic parameter model for power modules are established. Additionally, a method to optimize dynamic current distribution by adjusting the length of bond wires and the connection points of bond wires is proposed. Experimental validation showed that the current sharing test results of the optimized design for the automotive module significantly reduced the current difference between parallel branches compared with the initial design, from 41.7% to 5.03%. This indicated that the proposed optimization scheme for adjusting bond wire bonding positions can significantly suppress current differences, thereby markedly improving current distribution uniformity and enhancing the module's current-carrying performance, demonstrating a clear advantage of this optimization method.

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