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Electro-Thermal Co-Optimization Design of GaN MMIC PA

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Abstract: A method of electro-thermal co-optimization design for the Gallium nitride (GaN) monolithic microwave integrated circuit (MMIC) power amplifier (PA) is introduced in this paper. Due to the self-heating effect of the GaN high electron mobility transistor (HEMT), it is necessary to pay attention to the influence of thermal resistance change on circuit performance when designing a high-power RF PA. For this purpose, a three-dimensional finite element analysis model of GaN multi-gate HEMT is developed. The thermal resistance and junction temperature of the device under a RF dynamic current are extracted by heat transfer simulation and can be substituted into the temperature node of the transistor model for PA circuit simulation design. To verify the proposed method, a Class AB MMIC PA was designed and tested using a 0.15-μm GaN-on-SiC process. Through the application of the above methods, the designed PA performance is optimized and achieves the performance of over 60% power-added efficiency (PAE) and 38 dBm saturation power (Psat) within a compact area of 1.6 mm × 2.2 mm. It is demonstrated that the proposed method can effectively improve the consistency of simulation results and measurement results, which can be a valuable reference for high-power MMIC PA design.

Keywords: GaN HEMT; power amplifier; MMIC; electro-thermal simulation; thermal resistance; finite element analysis model; dynamic current

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1. Introduction

With the growing demand for mobile device networking, base station transceivers require greater output power and bandwidth. As a third-generation semiconductor, gallium nitride (GaN) is increasingly used in high-frequency and high-power device manufacturing [1]. The GaN high electron mobility transistor (HEMT) has the advantages of high breakdown voltage and power density, as well as good frequency characteristics, which is a better candidate for designing power amplifiers (PA) in base station transceivers [2]. However, the self-heating effect of GaN transistors under high-power operating conditions will cause serious module heating, reducing the system's stability and life [3–6]. Therefore, in order to improve the performance and reliability of the transceiver, it is important to perform thermal management of devices and circuits under high-power density [7].

Recently, there have been many reports on the thermal analysis of GaN HEMT and integrated circuits. Based on the coupling effects of ballistic–diffusive heat conduction and heat spreading in the GaN HEMT heat conduction model, Chen et al. analyzed the impact of substrate thickness, GaN thickness, and substrate materials on channel temperatures [8]. Considering conformal mapping technology to convert the device structure into a simple geometric shape, Mao et al. proposed an analytical thermal model of GaN HEMT, which can be used to analyze and predict the highest channel temperature and thermal coupling between multiple gates [9]. Hao's group proposed a thermoelectric analysis model based on embedded microfluidic cooling, which embeds the coolant into the SiC substrate of the GaN HEMT through microchannels to suppress the self-heating effect [10,11]. However, except for the studies of the thermal impact of transistors under DC, there are few papers on the heating situation under radio frequency (RF) large signals for a PA.

In the GaN PA design, Park et al. considered the thermal coupling between multiple transistors and optimized the layout through simulation, which reduced the junction temperature of the PA by 10 degrees Celsius [12]. Okamoto et al. verified through simulation that GaN-on-SiC and GaN-on-GaN substrates have similar thermal resistances and designed a 50 W PA by optimizing the heat dissipation structure, which helps to keep the maximum channel temperature below 200 °C, making it more reliable [13]. Zhou et al. used FE simulation to optimize the layout and obtain the thermal resistance of the device for circuit design and realized a compact 40 W GaN PA monolithic microwave integrated circuit (MMIC) while controlling the junction temperature to less than 200 °C [14]. However, in their studies, the influence of junction temperature and the change in thermal resistance with power and temperature are not fully considered.

It is known that the impact of self-heating effects on transistors will eventually be reflected in circuit performance. To solve this problem, in this paper, a three-dimensional finite element analysis model of GaN multi-gate HEMT is developed. The thermal resistance and junction temperature of the device under a RF dynamic current are extracted by heat transfer simulation and are substituted into the temperature node of the transistor model for a PA circuit simulation design.

The remainder of this paper is organized as follows. In Section 2, a GaN HEMT finite element (FE) analysis model is developed, and the thermal resistance and junction temperature under a dynamic current are extracted. Section 3 describes the electro-thermal co-optimization design of the GaN MMIC PA. Thermal resistance and junction temperature were introduced through thermal nodes to optimize the accuracy of the HEMT model. To verify the proposed method, a Class AB PA was designed. Section 4 is the measurement results and analysis, showing the consistency of the simulation results and measurement results of the designed PA. Section 5 provides the conclusion of this paper.

2. Electro-Thermal Model of GaN HEMT

The heat generated by the power amplifier mainly comes from the self-heating effect of the GaN HEMTs during the operation. In order to consider the thermal effects of transistors during circuit design, electro-thermal models can be developed to help predict the heating of transistors. In previous work, a commercial GaN HMET die was used for thermal modeling and extraction of thermal resistance [15]. In this paper, we extend this method to new chip manufacturing processes and make the extracted thermal resistance parameters more conveniently used in circuit design.

A depletion model structure of the GaN HEMT developed in this work is based on the transistor-with-individual-backvia (ISV) devices of a 0.15-μm GaN-on-SiC process. Compared with the transistor-with-outside-backvia (OSV) devices, ISV devices are individually grounded for each source. Although this structure has a larger area, it increases the distance between the adjacent group of channels and has a huge grounding hole, which is more conducive to heat dissipation. Therefore, ISV transistors are more suitable for designing high-power amplifiers. The structure of the ISV GaN HEMT is shown in Figure 1, and the key characteristics of the process are shown in Table 1.

Table 1. Key characteristics of the proposed GaN HEMT model.

Process Layer/Materials	Thickness (μm)	Dimensions (μm)	Thermal Conductivity λ_{th} (W/(m·K))
Protect and SiN_x layers	~0.74	/	60
MET1 and MET2 layers	1.1 & 4	/	317
GaN	~2	1400 × 1400	165 × ((300/T)^0.49)
SiC substrate	100	1400 × 1400	374 × ((300/T)^1.49)
Die-attach layer ($Au_{80}Sn_{20}$)	40	1450 × 1780	57
Heat sink (Cu)	200	5000 × 5000	400

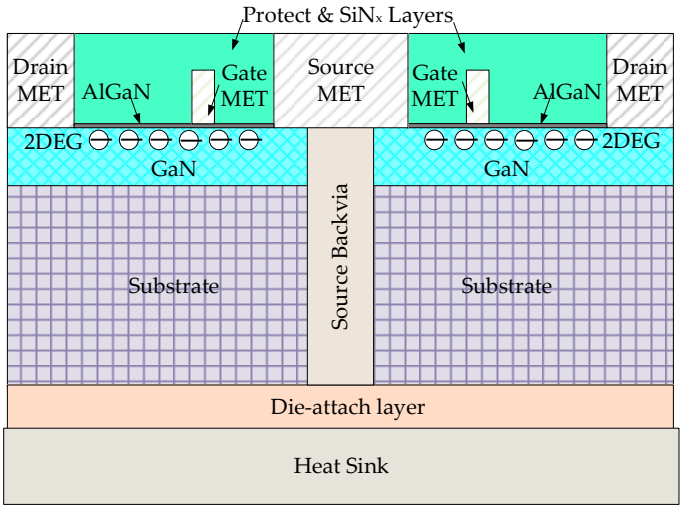

Figure 1. Structure diagram of an ISV GaN HEMT (not scale).

A GaN HEMT that can be used in power amplifiers is constructed using the process. The transistor consists of two 8-gate transistors with a single gate length of 100 µm connected in parallel. The adjacent source metal of the two tubes is merged in the layout to reduce the size of the parallel tubes, which can reduce the length of the drain output microstrip line, thereby reducing losses and improving the efficiency of the transistor. Based on our work of reference [15,16], a 3D FE electro-thermal simulation model was developed, as shown in Figure 2a. The heat source is set at the gates, and the constant temperature surface is at the bottom of the heat sink. The characteristics of the GaN HEMT, AuSn layer, and heat sink are listed in Table 1.

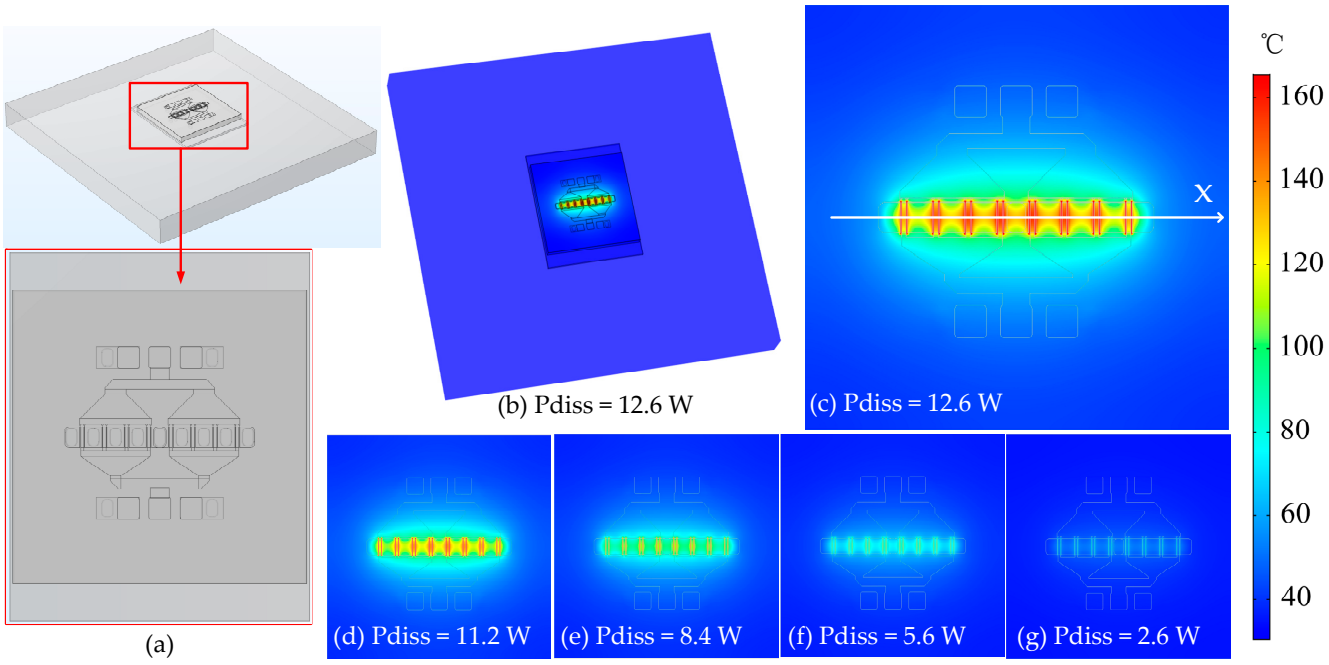

Figure 2. (**a**) 3D FE analysis model of the proposed GaN HEMT and (**b**–**g**) its temperature distribution. (**b**) is the 3D image, and (**c**–**g**) are the top surface temperature distributions of the device at different dissipated powers.

The static power consumption of the transistor is about 2.6 watts when the gate voltage is −1.7 V and the drain voltage is 28 V. Under RF working conditions, the transistor operates at a dynamic current that is much larger than the quiescent current. Some values between the static current and the highest dynamic current are taken for transistor thermal analysis. The thermal simulation results of the transistor surface thermal distribution under different powers are pictured in Figure 2. Figure 2b is a 3D view of the simulation results of the entire model. We can see that the temperature spreads outward along the heat source. Figure 2c–g show the top surface temperature distribution under different dissipation powers. As the dissipation power increases, the surface temperature also rises, and the heat conduction becomes more obvious. Figure 3 shows the temperature distribution of the HEMT's channels along the *x*-axis shown in Figure 2c. When the dissipated power Pdiss = 12.6 W, the highest temperature reaches 170 °C. Due to thermal coupling, the highest temperature occurs near the middlemost gate and gradually decreases toward both sides. Obviously, the temperature of the GaN HEMT under a dynamic current will become very high, which makes it necessary to analyze the effect of the thermal resistance changes with temperature on circuit performance [16].

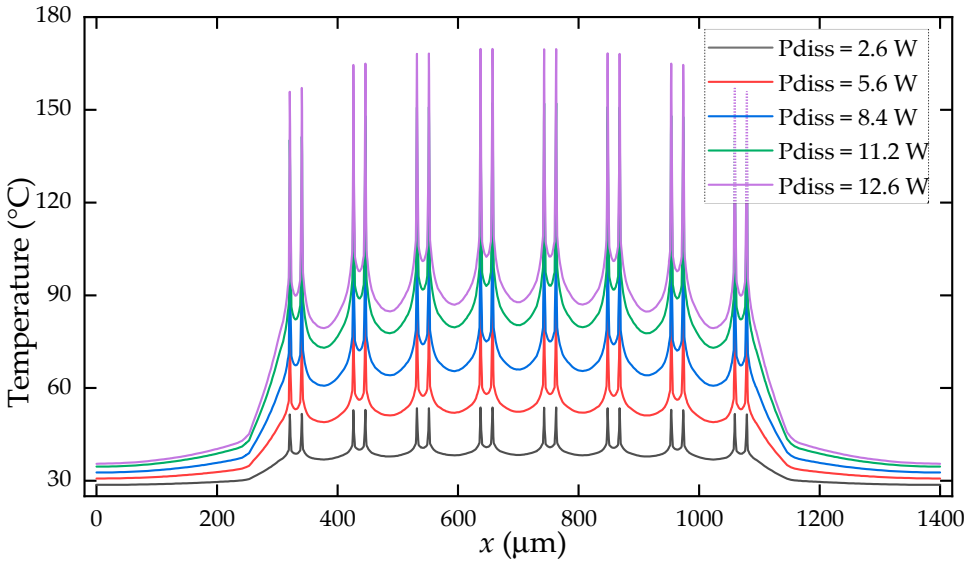

Figure 3. Channel temperature distribution along the *x*-axis.

Figure 4 shows the thermal resistance from the channel to the substrate's bottom of the transistor at different dissipated powers. It can be seen that the thermal resistance of the transistor increases as the power dissipated increases. Furthermore, the thermal resistance can be used for circuit design to improve the consistency of the simulation and measurement comparison. Because the dissipated power is mainly consumed in the form of heat energy, the temperature of the chip will rise as the dissipated power increases. Due to the thermal resistance changing with temperature, a trend equation to express the changes in thermal resistance will make the circuit simulation results more reliable.

The trends of junction temperature and thermal resistance as the dissipated power changes are fitted into linear curves, respectively. The fitting curve equation of the junction temperature change is

$$y_1 = 11.67x + 22.2 \quad (1)$$

and the fitting curve equation of thermal resistance change is

$$y_2 = 0.94x + 7.57. \quad (2)$$

These two equations represent the trend of the junction temperature value y_1 and the thermal resistance value y_2 changing with the dissipated power value x. It is worth noting

that they have no actual physical meaning and will change with different parameters, such as the device structure. They need to be extracted for different device models.

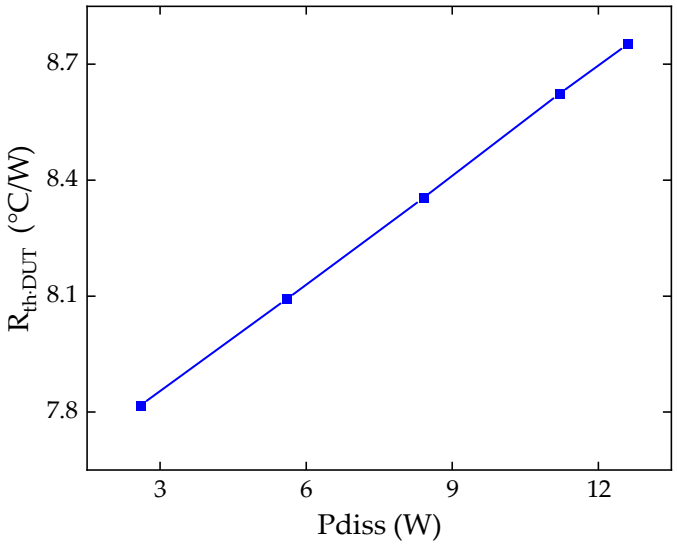

Figure 4. Thermal resistances of GaN HEMT vary with dissipated power.

3. Electro-Thermal Co-Design of GaN PA

Gallium nitride HEMTs have high-power density and can achieve greater output power in a smaller area. Currently, the commercial GaN MMIC process is dominated by depletion-mode devices. Limited by process and cost, the on-chip mainly contains amplifier tubes and matching, and the bias is implemented off-chip. A single-stage PA biased in class AB was designed in this paper for analysis. The class AB PA works in amplification mode, and its conduction angle, linearity, and efficiency are all in the middle of class A and class B, achieving a compromise between efficiency and linearity.

The 0.15-μm GaN HEMT process is used for the MMIC design. In order to achieve a saturated output power of 5 watts, the amplification stage uses two parallel ISV transistors with a length of 8 × 100 μm. The drain operating voltage is 28 V; the gate voltage is −1.7 V, biasing the circuit in class AB; and the static drain current is 92 mA.

Circuit stability is an important prerequisite for ensuring the normal operation of the power amplifier. Thus, before PA design, it is necessary to design the stable structure of the amplification stage to ensure that the transistor can work in a stable state. Some common methods to improve stability include connecting a resistor in series with the gate, a resistor and capacitor in parallel with the gate, or an inductor in series with the source. As shown in Figure 5a, an RC parallel stable structure is used at the input end of the transistor, and a resistive loss R_p is added to the gate power branch to eliminate low-frequency oscillation [17]. In addition, a 50 Ω resistor is connected in parallel between the gates of the two transistors to further improve the loop stability of the transistor.

Since the heat of the PA is mainly concentrated in the amplification stage, and the layout of the circuit also has a certain impact on the heat dissipation of the chip, the layout design of the amplification stage needs to be fully considered during the design. After iterative design and simulation, the proposed amplification stage layout is shown in Figure 5b. As seen in Figure 5b, we added a large-area double-layer metal microstrip structure on the front end of the gate. These structures can not only help the progressive transmission of RF signals but also serve as a way to dissipate heat. Heat can be transferred into these metal structures through the gate. Since they are at the input end, these structures have less impact on circuit performance, and the parasitic parameters they bring can also be solved through matching.

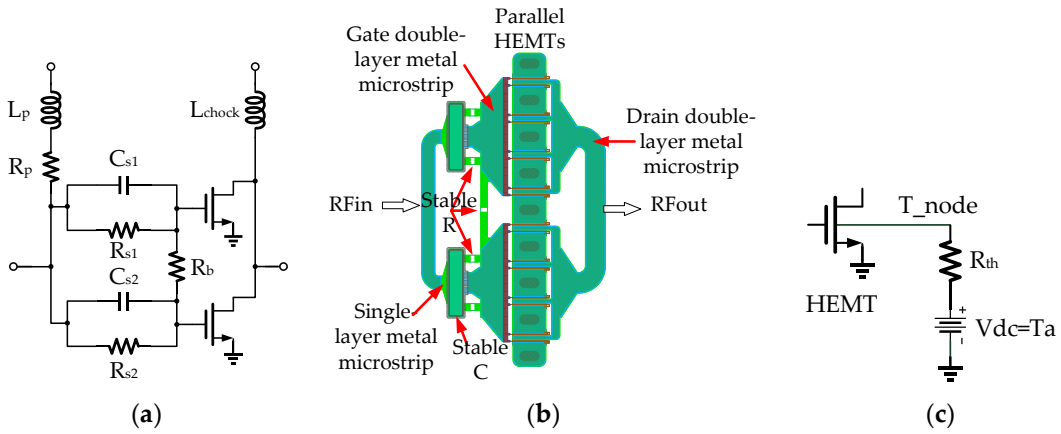

Figure 5. (**a**) Stability design of amplification stage and (**b**) its layout. (**c**) is the temperature node of the transistor.

In the GaN HEMT simulation model, a design solution considering thermal resistance is provided, as shown in Figure 5c. By connecting a resistor representing the thermal resistance and a regulated power supply representing the temperature at the temperature node, the electro-thermal co-design of the circuit can be easily performed. In addition to the thermal resistance of the chip itself, the thermal resistance brought by other parts, such as the heat sink in the test structure, can also be considered. For considering the impact of the self-heating effect of GaN HEMT on the circuit, the temperature and thermal resistance fitting curves Equations (1) and (2) extracted from the modeling in Section 2 are substituted into the T_node parameters of the device model.

After adding the temperature node parameters, as shown in Figure 5c, the stability post-simulation of the stable structure circuit in Figure 5b is performed. The simulation results of the stability coefficient are shown in Figure 6a. The μ-factor is often used to judge the stability of a circuit. The μ-factor is defined as the minimum distance in the Γ_L-plane between the origin of the unit Smith chart and the unstable region, where

$$\mu \equiv \frac{1 - |S_{11}|^2}{|S_{22} - S_{11}^* \Delta| + |S_{12} S_{21}|}. \quad (3)$$

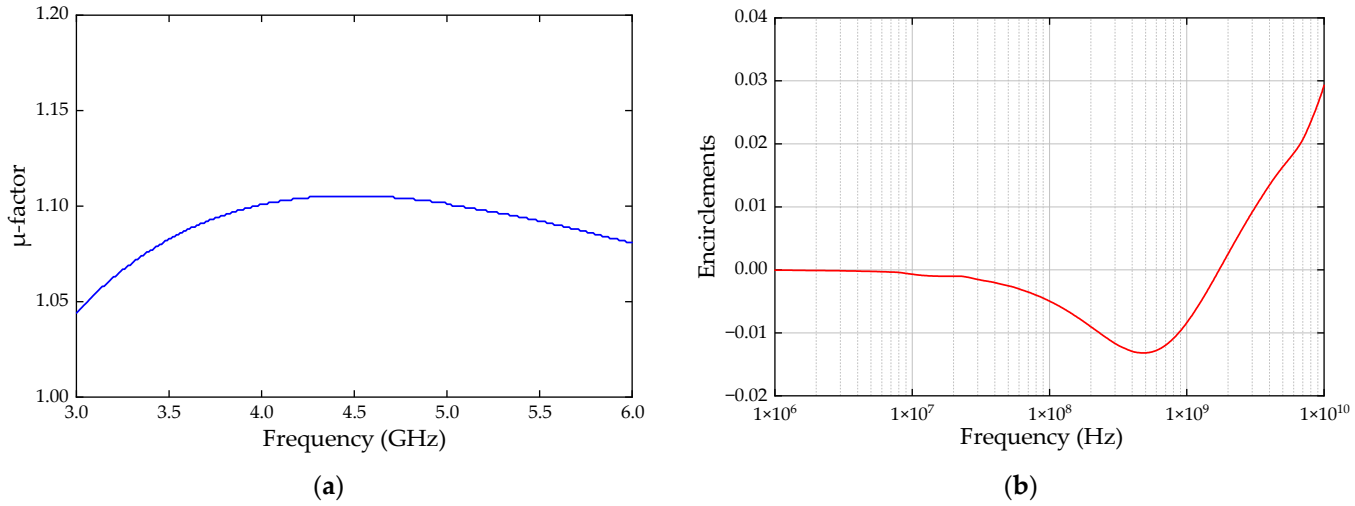

Figure 6. (**a**) Stability μ-factor of the designed structure of amplification stage and (**b**) its encirclements.

When $\mu > 1$, the output stability circle is outside the Smith chart, and there is no unstable region in the Smith chart, which indicates the circuit is unconditionally stable [18].

It can be seen from Figure 6a that the stability coefficients k and μ factors are both greater than 1, which means the circuit structure, considering the thermal resistance and channel temperature, is unconditionally stable in 3–6 GHz. Meanwhile, its encirclements of the amplification stage are less than 1 within 10 GHz, as shown in Figure 6b, and there is no clockwise encirclement of return difference around the origin, which proves the proposed circuit structure can work stably within 10 GHz.

In the amplification stage design, the method of electro-thermal co-operative optimization design is embedded, as shown in Figure 7. An electro-thermal FE analysis model was established for the amplification stage's layout to extract the thermal resistance and junction temperature under different dissipated powers. The extracted values are generated into Formulas (1) and (2) for post-simulation of the circuit, and the performances of the circuit, such as PAE and Psat, are obtained. In order to achieve more satisfactory circuit performance, layout parameters such as the transistor spacing and shape of the microstrip line can be modified. A satisfactory layout of the amplification stage can be obtained through several iterations of simulation. Using the post-simulation results, the relationship between Pdiss and the input signal power can be obtained to optimize the input of the FE model. During the iteration process, changes in the layout also require the coefficients of Formulas (1) and (2) to be revised accordingly.

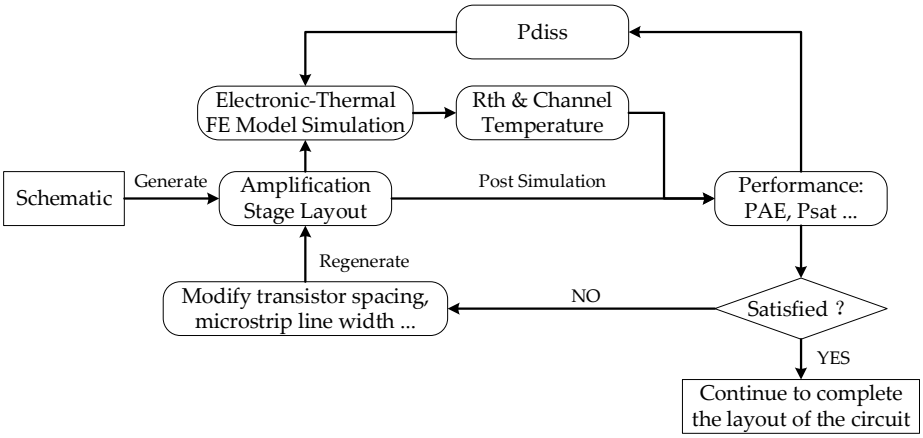

Figure 7. Schematic diagram of electro-thermal co-optimization design of MMIC PA.

Based on the amplification stage stable structure, the circuit is designed using load-pull and source-pull to find the appropriate input and output matching impedances. The input power is 28 dBm, the center frequency is 4.8 GHz, and the static current is 92 mA. After iterative calculation, the optimal source impedance and load impedance are obtained, as shown in the Smith chart in Figure 8. The corresponding optimal load impedance is

$$Z_{Lopt} = (15.3 + j \times 43)\ \Omega\,, \tag{4}$$

and the optimal source impedance is

$$Z_{Sopt} = (19.3 + j \times 27.2)\ \Omega. \tag{5}$$

At the optimal impedance, the optimal power-added efficiency (PAE) of the ideal PA is 73%, and the saturated output power (Psat) is 38.8 dBm. Actually, the optimal load impedance is relatively small so that the output can use simple conjugate matching. The input matching uses a high-pass Π-shaped matching network, and third-order high-pass filtering can increase the bandwidth. The input–output matching structure is shown in Figure 9. Among them, C_{i1} and C_{o1} are DC blocks. RF chock is implemented using microstrip lines, which will have a larger area than the inductor. However, because the drain current flows through the RF chock, using a double-layer microstrip line is more reliable than an inductor and can withstand larger currents. C_{trap} will form a trap with

the parasitic L_{trap} around 7 GHz to reduce out-of-band interference. C_{DeC} with 30 pF is a decoupling capacitor that is used to suppress the interference of AC signals on DC, reduce the impact of the parts outside the pad on circuit performance, and improve stability.

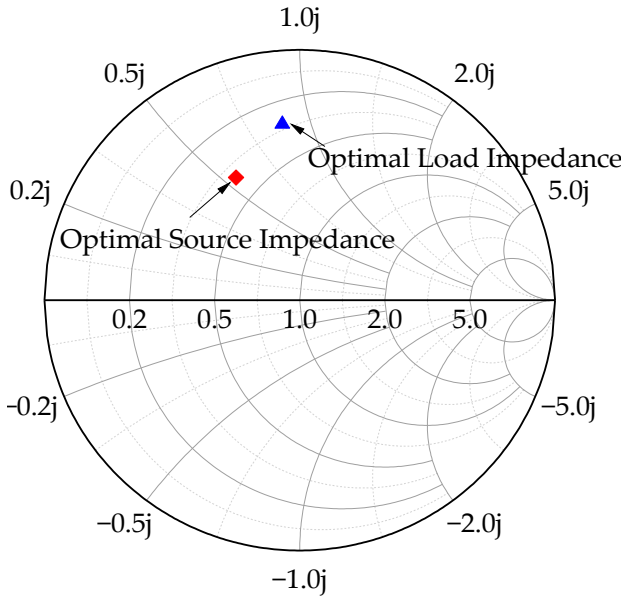

Figure 8. The optimal load and source impedance plotted in the Smith chart.

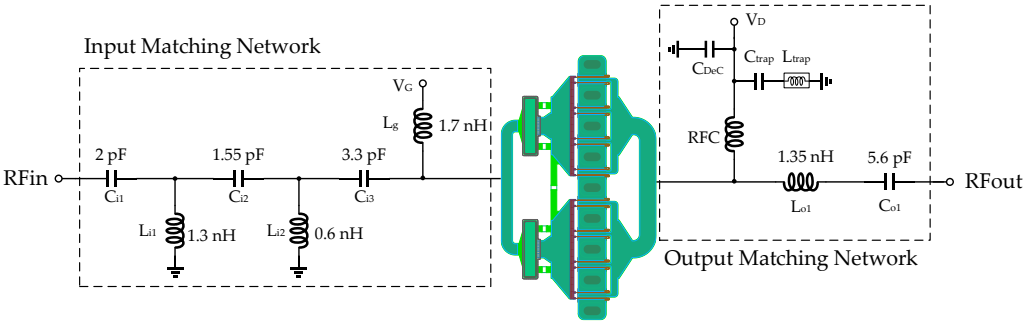

Figure 9. Circuit schematic of the proposed Class AB PA.

The final PA layout of Figure 9 is shown in Figure 10. In order to facilitate measurement, the ground–signal–ground (GSG) RF pad with a spacing of 150 µm was used for both the signal input and output. The DC PAD uses a supply–ground (SG) array to facilitate the use of a DC probe card with decoupling capacitors to power up the chip. To avoid device breakdown caused by gate leakage current, a 1 kΩ resistor was added outside the gate decoupling capacitor. Since the HEMT is voltage-driven, the reduction of gate current has little impact on the device's performance, and a larger decoupling capacitor can also reduce the impact of this resistance on matching.

Combined with the impact of the self-heating effect on transistor performance, the fitting curve parameters of thermal resistance and junction temperature are added to the T_node. The post-simulation results in Figure 11a show that the µ-factors of the PA circuit are over 1 at 0–12 GHz, which means that the circuit is stable in this frequency band according to Equation (3). As shown in Figure 11b, in the range of 4.2 GHz to 5.4 GHz, the small signal gain of the PA is 13.8–15.9 dB. The saturated drain efficiency reached 52.6–66.8%.

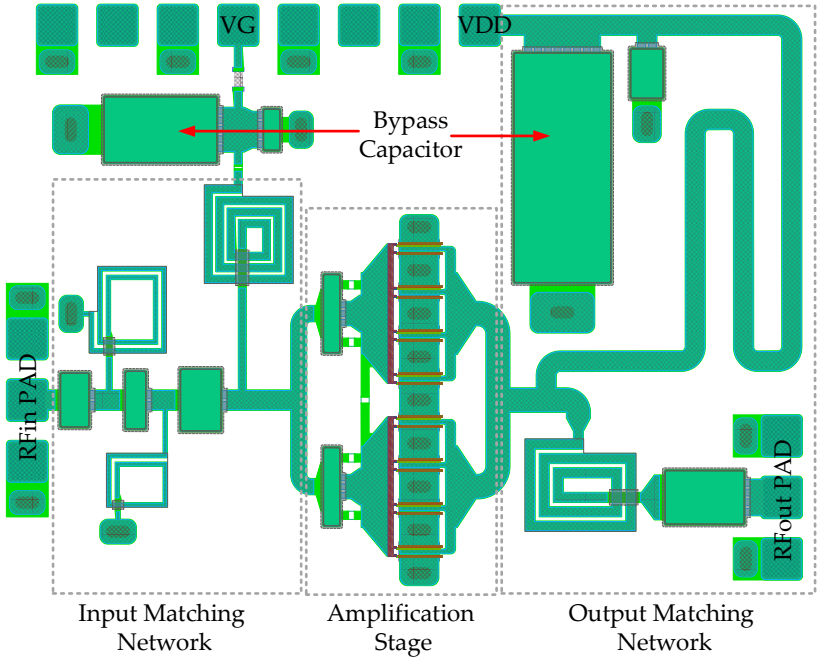

Figure 10. Layout of the designed Class AB PA.

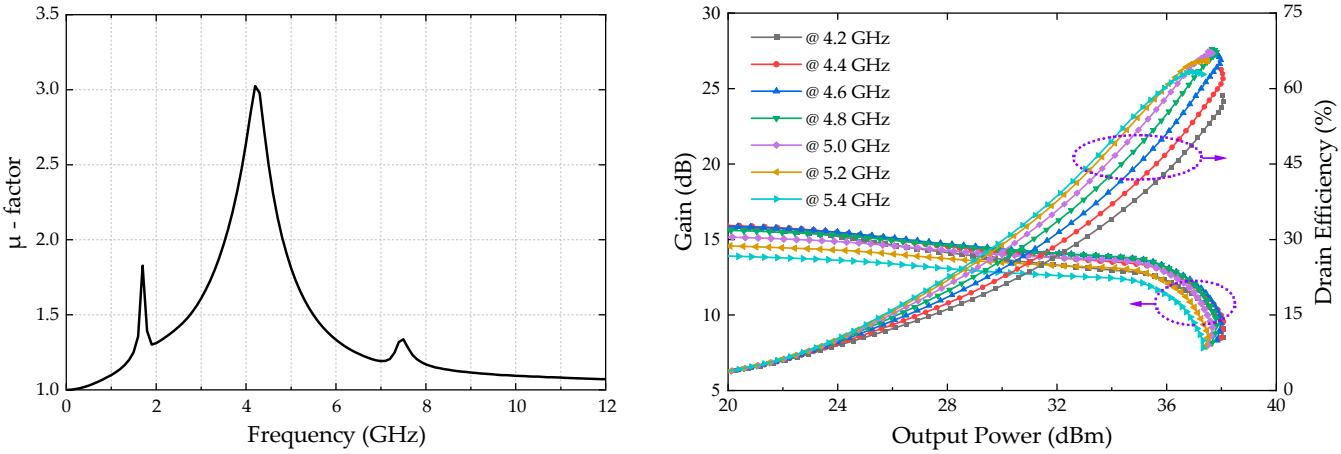

Figure 11. (**a**) Simulated stability μ-factor and (**b**) simulated gain and DE versus output power at different operation frequencies.

4. Measurement Results and Discussion

The chip microphoto of the proposed Class AB PA is shown in the middle of Figure 12, with an area of 1.6 mm × 2.2 mm, including the pads. In order to ensure good heat dissipation conditions of the chip, the chip is placed on the steel probe table directly for measurement. Both the DC supply and the RF signal are carried out by inserting the probe. The DC supply uses a custom SG DC probe with a set of decoupling capacitors between each set of signals and the ground. The continuous wave (CW) RF signal is transmitted to the chip using Cascade's Z40-P-GSG-150 probe. After calibration, the impact of the probe and RF cables on the chip performance is removed. During the test, the DC bias of the chip is maintained at the drain voltage of 28 V, and the drain static current is 92 mA.

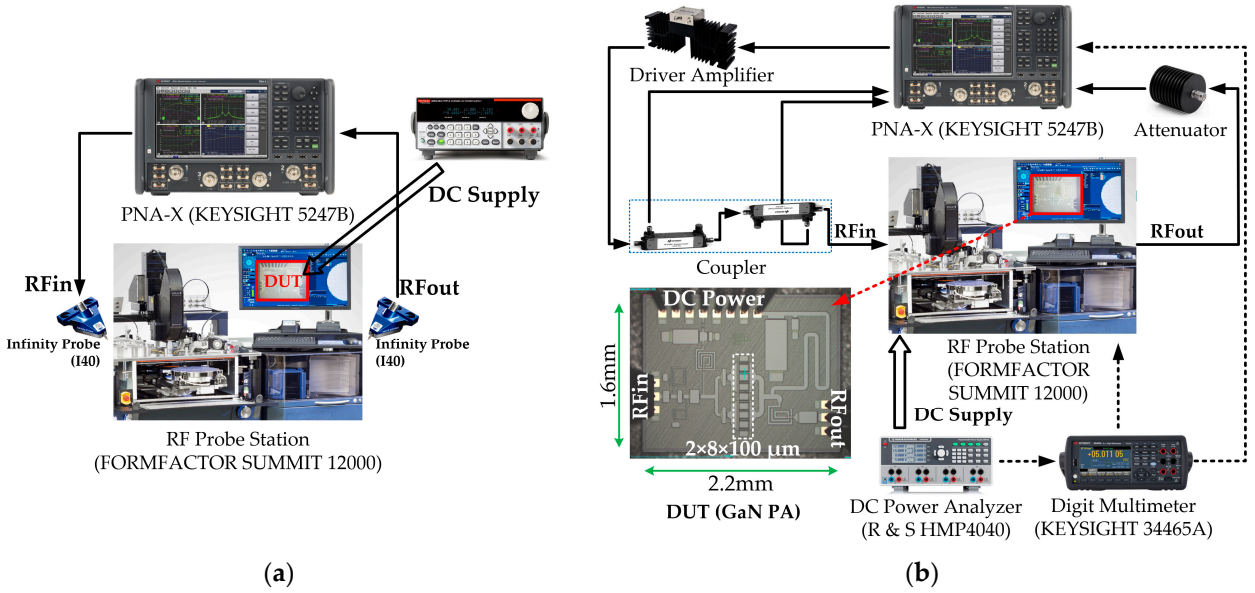

Figure 12. Measurement configuration of (**a**) small signal and (**b**) large signal.

Keysight 5247B PNA-X is used for small and large signal measurements. The measurement configuration is set in Figure 12. The input signal amplitude is −30 dBm at the small signal measurement, and the test range is from 1 MHz to 12 GHz. The measurement results are shown in Figure 13a. Comparing with the simulation results, it can be seen that the S-parameters of the proposed PA fit well in the range of 4.2–5.4 GHz. Due to the influence of the accuracy of the simulation device model and ground parasitic inductance, the gain is about 0.5 dB smaller than the simulation. In addition, the position of a trap was shifted from 7.4 GHz to 6.5 GHz due to the parasitic inductance between ideal ground and actual ground. Since the input RF signal power is very small during the small signal test, the drain current does not increase significantly, so the heating of the chip is almost the same as under DC. The change in thermal resistance is also relatively small.

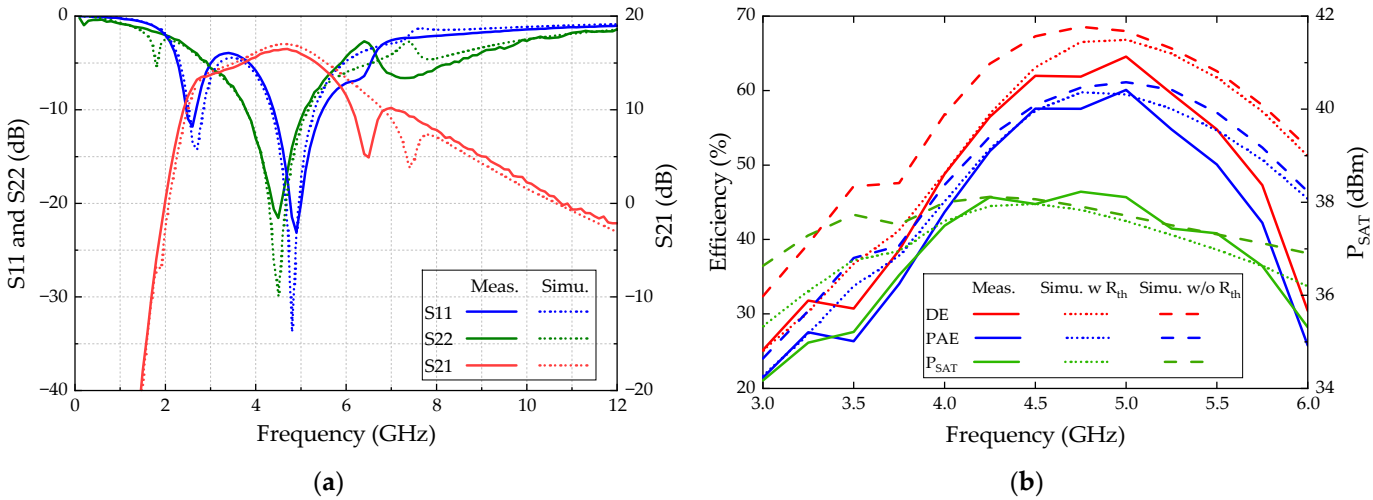

Figure 13. Measured and simulated (**a**) S-parameters, (**b**) DE, PAE, and P_{sat} versus frequency.

Since the signal power output by the PNA-X is limited, a driver amplifier (Mini-Circuits ZVE-3W-83+) was added to the signal input end to amplify the input power during large signal testing. Figure 13b shows the measurement results. At 4.2–5.4 GHz, the output saturation power (Psat) is 37.3–38.0 dBm, the drain efficiency (DE) is 61.8–68.1%, and the PAE is 52.5–60.5%.

Since the dynamic current of the transistor is much larger than the static current under large signals, the impact of the temperature increase on the change in the transistor thermal resistance cannot be ignored. Therefore, the prediction of thermal resistance has a high value for the accuracy of the simulation results. It can be seen from Figure 13b that the consistency between the simulation results and the measurement results of the design considering the thermal resistance change is better than that of the solution that does not consider it. Compared with the simulation results, the measured results of the saturated power in the frequency band are slightly larger, with a maximum difference of 0.6 dBm. Due to the significant increase in thermal power consumption caused by the mismatch, the self-heating effect is worsened, and the efficiency at high frequencies deviates greatly from the simulation.

It is seen that, through electro-thermal co-design, a PA with good consistency between testing and simulation results was proposed. During the design process, the trend equations of thermal resistance and junction temperature values were used for simulation. Compared with the thermal resistance parameters embedded in the device model, this trend equation can reflect the changes in thermal resistance and junction temperature as the dissipated power changes, making the circuit simulation more accurate.

5. Conclusions

In this paper, the method of electro-thermal co-optimization design for the GaN MMIC PA was carried out. In order to consider the impact of changes in thermal resistance with temperature on large-signal performance in circuit design, an FE analysis electro-thermal simulation model of the PA amplification stage was developed. The junction temperature and thermal resistance were extracted from the model, and the trend equation of their values changing with the dissipated power was obtained to optimize the device model. Through an iterative optimization of the layout and device model parameters, the proposed PA achieves more than 60% PAE and 38 dBm saturation power in a compact area of 1.6 mm $\times$ 2.2 mm. Compared with traditional design methods, the proposed PA achieves better consistency between simulation and measurement after considering the change in thermal resistance with temperature under the large signal. Moreover, the proposed method of electro-thermal co-optimization design has a certain universality and can provide a reference for high-power PA designers to consider the impact of heating.

In addition, this paper mainly focuses on the electro-thermal co-optimization design of PA in the sub-6 GHz band. At higher frequencies, in addition to the influence of t RF dynamic current, the effect of increasing frequency on the lattice vibration of the material leading to a change in the heating state also needs to be more considered, which will be the further improvement direction of this design method.

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