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The Design and Dynamic Control of a Unified Power Flow Controller with a Novel Algorithm for Obtaining the Least Harmonic Distortion

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Abstract: This study investigates the control and dynamic operation of the Unified Power Flow Controller made of shunt and series converters, a Static Synchronous Compensator, and a Static Synchronous Series Compensator, respectively, connected back-to-back through a common DC-link capacitor. The model of a 48-pulse Voltage Source Converter is constructed from a three-level Neutral Point Clamped converter, which allows the total harmonic distortion to be reduced. An optimal conduction angle tracking system of the three-level inverter is designed to minimize distortion by detecting proper harmonic component elimination. Starting from the six-step modulation strategy, the *dq* decoupled control schemes of both compensators in open and closed loops are presented. Finally, the MATLAB-Simulink model of the power flow controller is implemented and analyzed. The results show that the controller can track the power changes and apply a suitable voltage to the power system so that the power flow can be controlled. This way, the power flow controller dynamically improves the voltage and power quality across the power network while simultaneously improving the transient stability of the system. It can eliminate all system disturbances resulting from oscillations and harmonics in voltage and current within a very short time. The procedural approach used to model and simulate the Unified Power Flow Controller, as well as the new algorithm used to obtain the harmonic number that minimizes the total harmonic distortion, can be applied to any AC power system.

Keywords: UPFC; THD optimization; STATCOM; SSSC; six-step modulation

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1. Introduction

Among the Flexible AC Transmission Systems (FACTSs), there is the so-called Unified Power Flow Controller (UPFC), which is considered one of the most flexible converters to control and optimize the power flow in transmission lines combining interesting characteristics that are typical for FACTS equipment made with shunt and series converters. Thanks to these features, a UPFC can regulate, at the same time, the voltage and phase angle and operate series compensation. Thus, with a UPFC, the transmission line can be compensated with active and reactive power independently controlled [1], and it is possible to increase the power flux up to the thermal limit of a critical bond line without having a reduction in the stability margin.

Figure 1 shows a schematic diagram of a UPFC consisting of two Voltage Source Converters (VSCs). As can be seen, one VSC is connected in series to the connection line between the sending bus coming from a generator and the transmission line through a transformer (T1), while the other VSC is connected in shunt to the line through another transformer (T2). The DC output of the shunt VSC is connected to the DC input of the series converter. As usual, the DC voltage of this bus is kept constant with the support of a special capacitor bank.

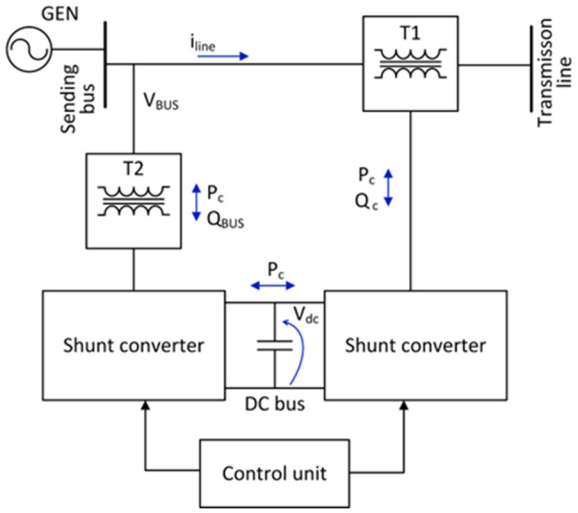


Figure 1. Schematic diagram of a UPFC made with two back-to-back VSCs.

The series converter, the so-called Static Synchronous Series Compensator (SSSC), takes care of controlling the amplitude and angle of the voltage added in series with the line, thus modulating the real and reactive power exchanged with the line. The reactive power is generated by this inverter, while the real power comes from the DC bus. The independent control of the active and reactive powers flowing through the transmission line is permitted precisely because the controlled voltage is applied in series to the bus in question. This characteristic of being able to control the flow of power in the desired quantity brings clear advantages to power system managers. For example, it facilitates decreases in the power flow of an overloaded line, thus mitigating the problem of congestion of the power distribution system.

Instead, the shunt converter draws the real power needed by the series converter from the line between the sending bus and the transmission line. Of course, the shunt inverter also exchanges reactive power with the sending bus, but this may not be controlled. The shunt converter is responsible for regulating both the UPFC bus voltage (generating the appropriate amount of reactive power) and the voltage across the DC-link capacitor [2].

A UPFC can operate in several modes. Among these, there is the automatic power flow (P and Q) control. In this mode, the reactive current is automatically regulated, applying a droop control with a defined characteristic. Then, once the reference values of active and reactive power (P_{ref}, Q_{ref}) are set, the series converter regulates them [1]. This feature of the UPFC makes it very interesting for use in modern microgrids where droop control is widely used [3] to facilitate load sharing among different sources, enable stable operation in islanded mode, and enhance resilience and stability by providing a decentralized control mechanism.

In this work, we will focus on the voltage control mode of the shunt converter and the automatic power flow operation mode of the series converter. We will consider both stationary and dynamic conditions.

In the literature, UPFCs have traditionally been used to improve power quality issues such as harmonic distortion, even without passive filters [4]. The authors of [5] present a new sensitivity analysis index that uses a genetic algorithm to find the optimal size and location of the UPFC to improve the distribution system's power quality characteristics, as tested on the IEEE 14-bus network. The results reveal that active and reactive power losses are reduced by 55% and 11%, respectively, while total harmonic distortion (THD) decreases from 27.12% when the UPFC is not utilized to 11.11% when it is installed. Furthermore, ref. [6] investigates the impact of a modular multilevel converter (MMC)-based UPFC on power grid harmonics when the MMC is modulated using the nearest level modulation (NLM) technique and operated with various sub-module numbers and voltage modulation ratios. Moreover, ref. [7] recommends using a 48-pulse gate turn-off (GTO) thyristor-based

UPFC to reduce THD in the transmission line. The implemented solution reduces grid current THD from 43.93% without UPFC to 1.81% with UPFC. In addition, the authors of [8] suggest a UPFC system for THD reduction in a 20 MW grid-connected wind farm. The THD at various nodes in the system is tested, and the findings reveal that at one node, the voltage THD decreases from 29.21% without the UPFC to 2.54% with the UPFC.

At the device level, the UPFC is often composed of multi-level inverters (MLIs), which are utilized to enhance power while decreasing the harmonics of AC-side converter waveforms. Compared to the traditional two-level VSIs, the stepwise output voltage is the major advantage of MLIs. However, one of the most difficult challenges in the field of MLIs is calculating the optimal switching/conduction angles for power switches so that low-order harmonics are eliminated in the output signal waveforms [9]. Nature-inspired algorithms such as Particle Swarm Optimization (PSO), the Bee Algorithm (BA), the Genetic Algorithm (GA), Ant Colony Optimization (ACO), and others are commonly used to solve complex, non-linear, and transcendental equations, resulting in selective harmonic elimination (SHE) for THD minimization. The authors of [10] employ the Moth Flame Optimization (MFO) technique to determine the optimal switching angles of an 11-level cascaded H-bridge MLI so as to reduce the THD of the converter output voltage waveform. In [11], GA optimization is used to determine the optimal switching angles for a seven-level Nested Neutral Point Clamped (NNPC) converter to minimize THD in the output voltage waveform. The authors of [12] present a technique for minimizing THD in a seven-level cascaded H-bridge MLI with resistive load using the Teaching–Learning-Based Optimization (TLBO) algorithm, demonstrating that this optimization technique outperforms previous strategies such as the GA. In [13], the Marine Predator Algorithm (MPA) is proposed for solving transcendental non-linear equations in a selective harmonic elimination technique to obtain optimum switching angle values to control a three-phase 11-level cascaded H-bridge MLI. They claim that the proposed algorithm is more efficient and accurate than other algorithms like TBLO, hybrid-PSO, and the Flower Pollination Algorithm (FPA). Reference [14] uses Artificial Neural Networks (ANNs) to generate optimum switching angles for the elimination of undesirable lower-order harmonics to minimize the THD in both five-level and seven-level cascaded H-bridges. In [15], the authors use the Whale Optimization Algorithm (WOA) for SHE in a single-phase 11-level inverter to find the optimal conduction angles that minimize the THD. The WOA produces better results than other algorithms like PSO and the Firefly Algorithm (FA) in terms of inverter performance, convergence rate, and computational overhead.

As illustrated above, it is important to choose the optimal harmonic component (m) and conduction angle (σ) of the MLI to achieve the minimum THD in the design of the UPFC VSI. In [16], m is selected with a specific value for a three-level NPC-based MLI, but there is no detailed clarification about this choice. Hence, here, we propose an optimal m-tracking system to minimize the THD with an optimal value of m. The goal is to generate an m value in the range of 2 to 120, along with the corresponding THD at a 60 Hz fundamental frequency. The m value is only changed when the THD reaches saturation by calculating the difference between two consecutive samples (ΔTHD) under a certain threshold, where the THD at that m remains almost the same. At the next stage, a function is applied to track the minimum THD and its corresponding m. These values are utilized in simulations of the Static Synchronous Compensator (STATCOM) and SSSC. This configuration produces a near-sinusoidal output voltage.

This paper is organized as follows: First, the six-step modulation of a three-level Neutral Point Clamped (NPC) converter will be performed, followed by a transformer arrangement to form a 48-pulse VSC. Then, the proposed algorithm for THD minimization by optimal m tracking is described. Next, the STATCOM modeling and simulations are shown. Following that will be the open-loop simulation of the SSSC, after which the model of the whole UPFC with the closed loop will be implemented in the ways already outlined, and then we conclude the work.

2. Power Converter Design

2.1. Power Topology

The three-level NPC power converter can achieve a three-level phase-to-neutral voltage to generate a sinusoidal voltage of higher quality. The more sinusoidal nature of the three-level NPC is due to an increase in levels which reduces the harmonic issue that relieves the dependency on the filter. Moreover, the use of such multilevel converters increases the efficiency of the conversion process, as all devices are switched at the fundamental grid frequency [17].

The schematic representation of the diode-clamped three-level inverter is shown in Figure 2. The DC-bus voltage includes three levels of two series-connected bulk capacitors, C_1 and C_2. If V_{dc} is the voltage of the DC bus, the output voltage, V_{an}, can assume three levels, $V_{dc}/2$, 0, and $-V_{dc}/2$, when the switch pairs S_{1a} and S_{2a}, S_{2a} and S_{1b}, and S_{1b} and S_{2b} are switched ON, respectively. The output voltage phase-neutral waveform for one of the phases is shown in Figure 3.

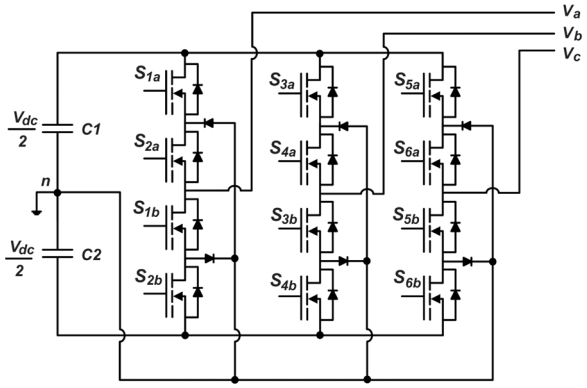


Figure 2. Schematic of the diode-clamped three-level inverter.

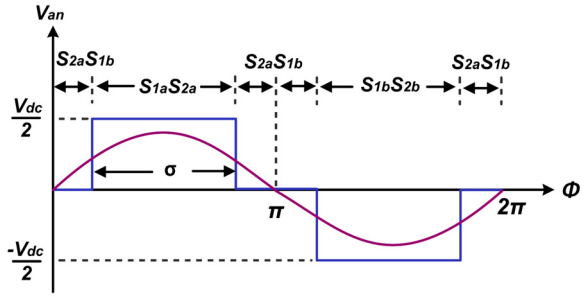


Figure 3. V_{an} phase voltage (three-level blue trace) of the diode-clamped VSC inverter in Figure 2 compared with the grid sinusoidal phase voltage (purple trace).

From the Fourier analysis of the waveform in Figure 3 [18], the RMS value of the m-th order odd harmonic of the VSC output voltage is given by Equation (1), while the general formulation used to compute the conduction angle (σ) of the three-level inverter as defined by [16] is given by Equation (2):

$$V_{rms\_m} = \frac{2\sqrt{2}V_{dc}}{m\pi}\sin\left[m\left(\frac{\sigma}{2}\right)\right] \quad (1)$$

$$\sigma = 180^{\circ}\left(1 - \frac{1}{m}\right) \quad (2)$$

where m is the order of the harmonic components.

For example, if we set σ = 172.5° (corresponding to a zero-vector angle of 3.75°), inverting Equation (2), we obtain m = 24 and the 23rd and 25th harmonic components are

negligible. This arrangement creates a nearly sinusoidal output voltage because the lowest significant harmonic component is the 47th one [16]. This will be demonstrated with a new algorithm.

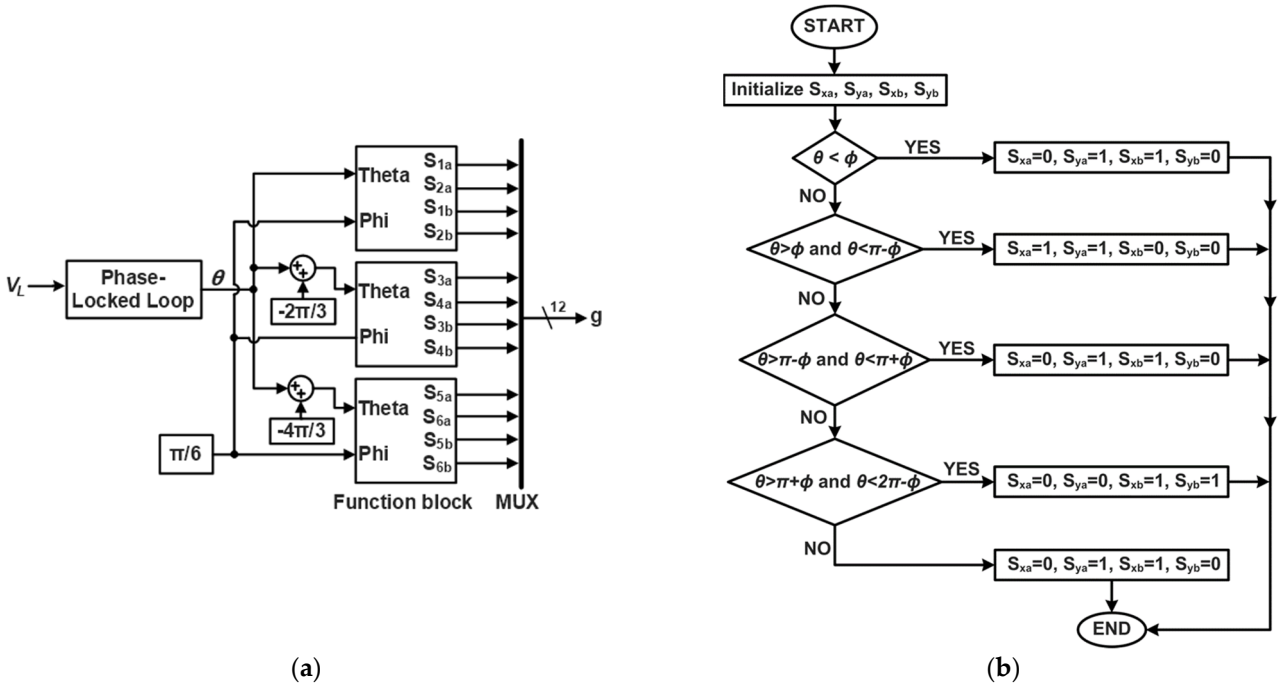
From Equation (1), we can observe that the magnitude of the output voltage can be changed by varying the sigma angle while keeping the DC-link voltage constant. This principle will come in handy for the STATCOM control.

2.2. Modulation

The modulation is designed with a six-step operation. It can be carried out using either indirect control, where the sigma angle shown in Figure 3 is fixed, or direct control, where the sigma angle is variable. In the indirect control, the DC-link voltage is made to vary, while in the direct control, the sigma angle is varied to vary the converter output voltage by keeping the DC-link voltage constant.

In this work, the indirect control modulation strategy was chosen for the STATCOM, while the direct control approach was used for the SSSC.

The MATLAB-Simulink 2022b implementation of the six-step modulation is carried out using the switching sequence shown in Figure 3, and a MATLAB script is written to execute this. Figure 4a shows the block diagram of the subsystem implemented in Simulink to obtain the three-level converter waveforms. Here, each leg of the inverter is implemented with a MATLAB function, receiving two parameters, which are the theta value from the phase-locked loop (PLL) block, which has a sinusoidal phase voltage of the grid as input, and another angle called *phi*, which is just half the zero-angle value. For example, in Figure 4a, the phi angle is set to 30°. V_{dc} can be set to a variable saved in the Workspace of MATLAB. Outside each function block of a phase leg, a phase shift of 120° is set. Then, each phase voltage of the VSC output is phase-shifted from the other phase voltage by 120°. Figure 4b shows the flow chart of the program implemented in each of the function blocks shown in Figure 4a to generate the PWM signals of each of the switches in each phase leg. In Figure 4b, x = 1, 3, 5 while y = 2, 4, 6, which are used to denote the various switches according to both Figures 2 and 4a.



(**a**) (**b**)

Figure 4. (**a**) System block diagram for generating the MOSFET gate switching pulses and three-level phase voltages. (**b**) Flowchart for generating PWM signals.

2.3. Forty-Eight-Pulse Voltage Source Converter

In the previous part, a three-level NPC converter with a six-step (or six-pulse) modulation was designed at the switching frequency of 60 Hz. Nevertheless, the goal is to accomplish a 48-pulse voltage at the converter output. The NPC converter provides another step in the voltage (three levels), so only four converters are required to have 48 pulses [19]. Figure 5 shows the configuration used to obtain the 48-pulse VSC. As can be seen from the figure, to produce a 48-pulse VSC, there is an establishment between four three-level diode-clamped multilevel inverters with a specific phase shift between them. Each three-level bridge generates a voltage on the secondary windings of four different Phase-Shifting Transformers (PSTs).

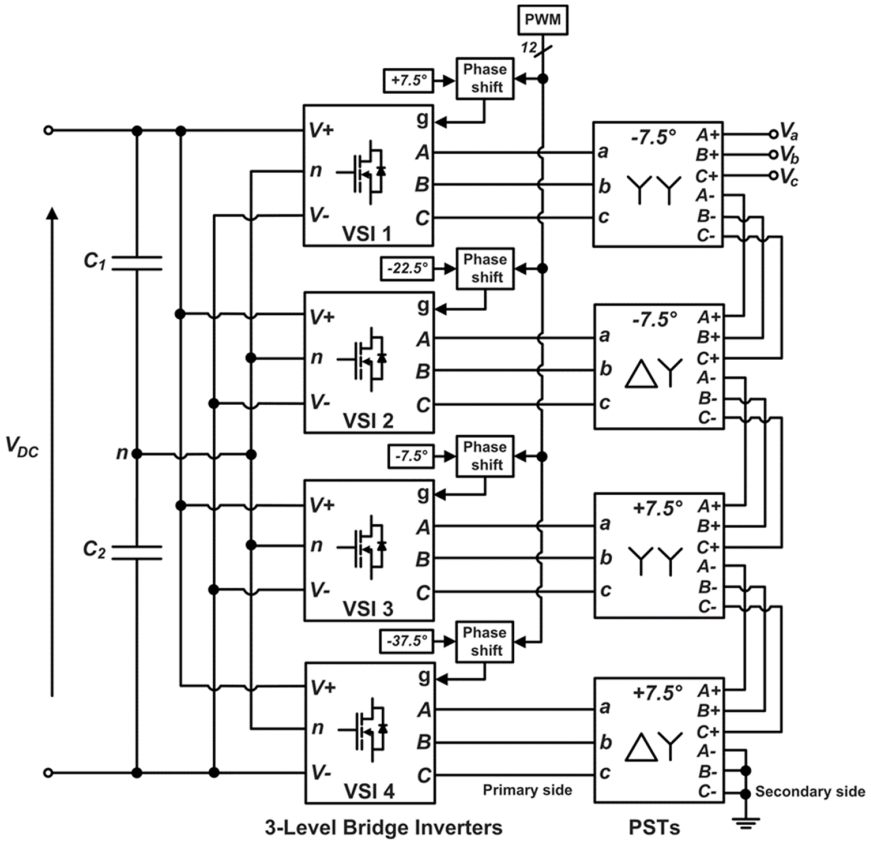


Figure 5. Forty-eight-pulse VSC topology implemented in Simulink.

There are two 1:1-turn-ratio transformers with a wye configuration at the primary side, the other two with a turns ratio equal to 1:$\sqrt{3}$, and a Δ primary configuration. The PSTs' secondary windings are in series and the proper pulse pattern angles as shown in Figure 5. The secondary windings of the PST at the bottom of Figure 5 are wye-connected, and the other PSTs' secondary windings are connected in series between them. This way, on the secondary side, we have a wye configuration composed of three branches, each made by four windings in series [16].

By combining four three-level VSCs to obtain a 4 $\times$ 6-pulse converter, as seen in Figure 5, the PST number required is decreased to half of that needed in a traditional 48-pulse operation. Moreover, this combined multi-level and multi-pulse topology also has the added advantage that it produces significantly less THD compared to that of a traditional 48-pulse inverter, with the selective elimination of the 23rd and 25th harmonics, as shown in Section 2.1, setting an optimum sigma angle of 172.5° and phi equal to 3.75°.

Figure 6a shows the phase-A-to-neutral voltages of the four three-level diode-clamped inverters, while Figure 6b shows the three-phase generated voltages. Figure 6c depicts the series of harmonic amplitudes from an FFT analysis. Figure 6d shows how the harmonic distortion obtained with the Multi-Pulse Converter (MPC) compares to that obtained with

the NPC topology. We see that the steady-state THD of the MPC over the simulation time is 3.78%, which is far less than that of the NPC (43.28%). This shows the benefit of the MPC topology in improving power quality by drastically reducing the THD of the voltage and current waveforms.

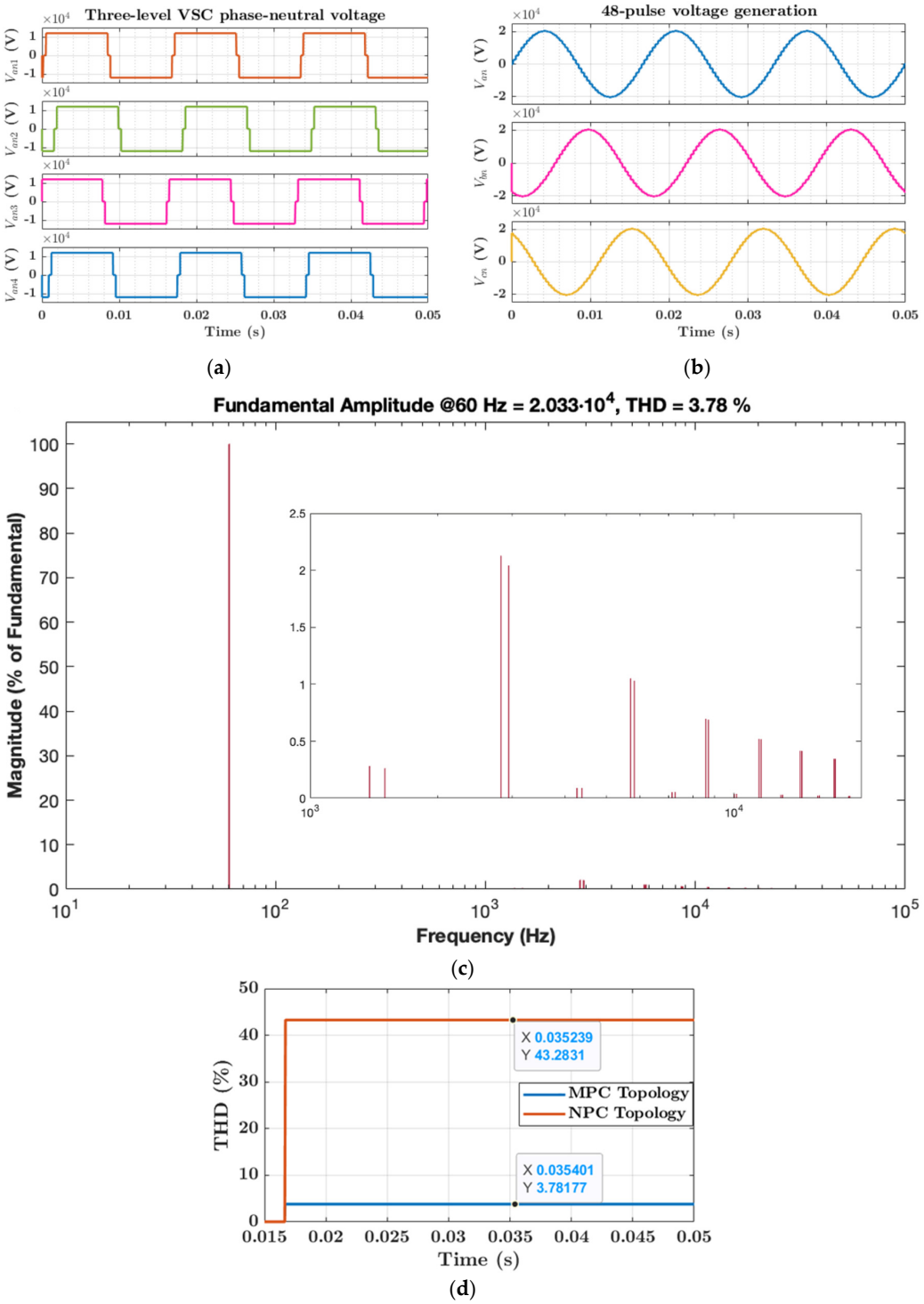


Figure 6. (**a**) Three-level NPC phase (A) voltages in 48-pulse configuration with *phi* = 3.75°; (**b**) 48-pulse output phase voltages; (**c**) amplitude of the harmonics composing the 48-pulse output voltage obtained by the FFT analysis; (**d**) THD with MPC and NPC topologies.

The excessive harmonics generated by the NPC converter into the power system increase the power losses and thermal stress on the equipment, reduce the utilization of the

electric energy, disrupt control systems, interfere with communication systems, affect the electromagnetic torque of motors and generators, may cause unwanted resonant conditions, and may cause the malfunctioning of system or plant equipment. Although both passive and active filters can be employed to eliminate undesired harmonic effects on the AC side of the converter, passive filters cause delays in system response and suffer from resonance concerns, and active filters have a high starting cost, particularly in high-power applications. The usage of MPC topologies mitigates most, if not all, of the difficulties raised by the NPC due to its very low harmonic content.

2.4. Algorithm for THD Minimization by Optimal m Tracking

From Equation (2), the m value must be appropriately monitored to reach an optimum conduction angle for obtaining the least THD.

In the proposed algorithm, a comparison between two consecutive samples of THD (ΔTHD) is considered. Once ΔTHD does not show any significant variation in a specific number of samples, m will change its value. This way, the THD will be examined based on the variation of the m value.

There are two thresholds to set up:

- ΔTHD_{thres}, which is a desired tolerance, indicating where the change in THD between two consecutive samples over time is smaller than it, which means their values are almost the same.
- A counter (C) indicates the repetition number of $\Delta THD < \Delta THD_{thres}$ and a counter threshold (C_{thres}) is utilized to change the m value. Once C reaches C_{thres}, it will be reset to 0 automatically. Algorithm 1 shows the pseudocode for changing the value of m.

Algorithm 1 m tracking

```
if ΔTHD < ΔTHD_thres
    C+ = 1
end if
if C = C_thres
    m+ = 1
    C = 0
end if
```

For instance, given a threshold C_{thres} of 20,000 and a tolerance ΔTHD_{thres} = 0.001, m will automatically increase by 1 if, after 20,000 sampling periods, the change in THD is still less than 0.001.

Once THD as a function of m has been obtained, it is then possible to search its absolute minimum value, identifying the optimum value of the harmonic number (m_{opt}). In the Algorithm 2, the minimum THD and its index are detected, and then the value of m is evaluated at the detected index. THD_{min} and m_{opt} are then the last values at the end of the iterative process.

Algorithm 2 Identification of the optimal m

```
THD_min = min(THD)
Index_min = find(THD == THD_min)
m_min = m(Index_min)
```

Figure 7a shows a block diagram of the optimal m-finding algorithm, which has been explained above, while Figure 7b illustrates how this algorithm has been implemented in MATLAB-Simulink. Figure 7c shows the relationship between the THD and the corresponding harmonic number (m). We can then use this figure to determine the optimum m and the least THD as m_{opt} = 24 and THD_{min} = 0.0378, respectively. Then, setting m = 24 gives a conduction angle of 172.5°, which produces a near-sinusoidal signal.

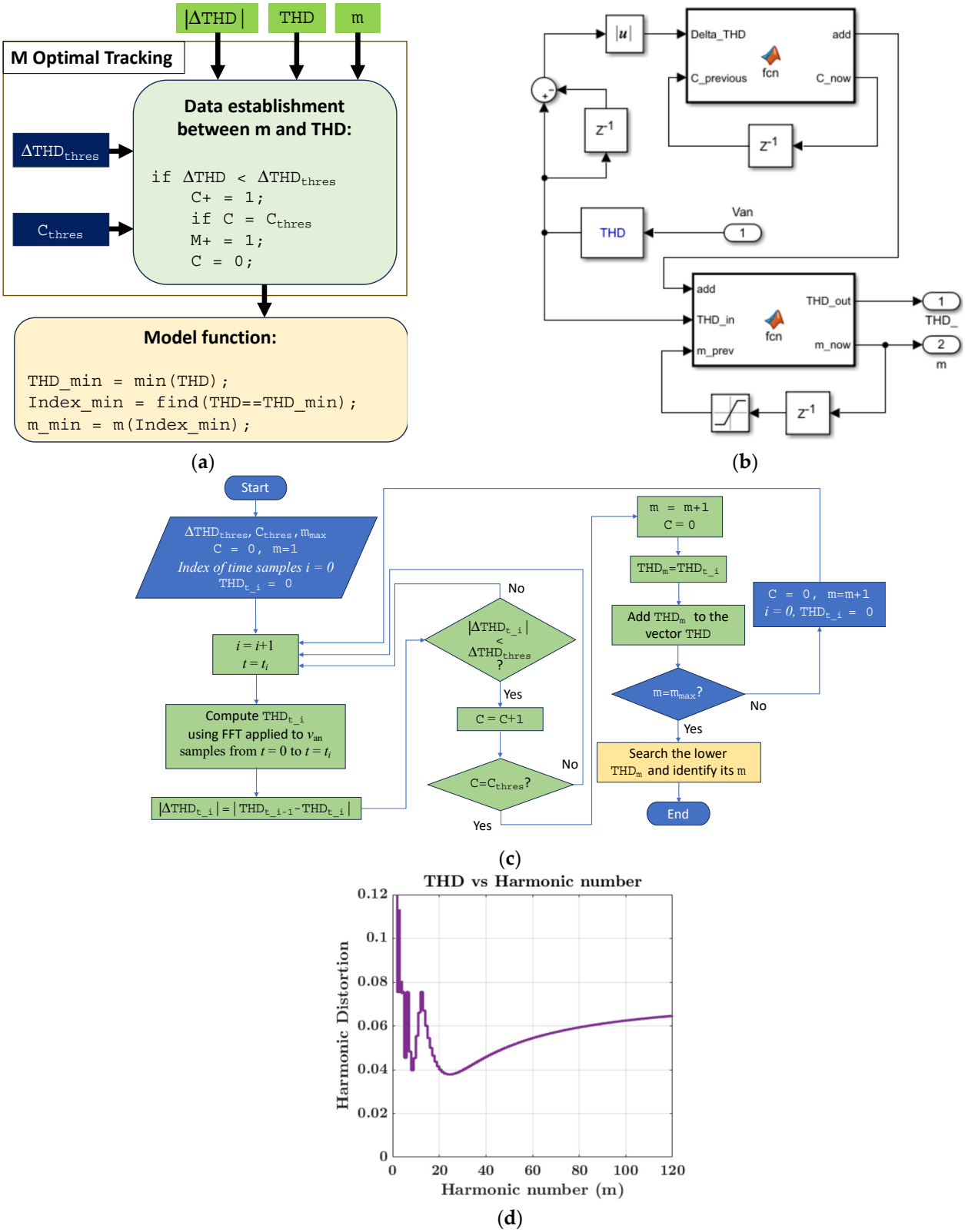


Figure 7. (**a**) Overview of the optimum m-tracking system; (**b**) MATLAB-Simulink model for THD and m-tracking; (**c**) flowchart of the whole optimum m-tracking algorithm; (**d**) evaluated THD vs. *m*.

3. STATCOM Modeling

The parameters used for implementing the UPFC are taken from a real scenario discussed in [20]. They are summarized in Table 1 and used to test the models of the STATCOM and SSSC.

Table 1. UPFC system parameters.

System frequency	60 Hz	Transmission line loading capacity	950 MVA
Grid voltage (V_{LL})	138 kV		
DC-link voltage	24 kV	Load	2000 MW
Transformer turns ratio	138/37 kV		
UPFC rating	±320 MVA	Additional Parameters	
STATCOM rating	±160 MVA	R_{shunt}	6 mΩ
SSSC rating	±160 MVA	L_{shunt}	1 mΩ

3.1. STATCOM Operation

The STATCOM is a piece of shunt-connected reactive compensation equipment that is utilized to generate and/or absorb reactive power and whose output can be varied to maintain control over specific parameters of the electric power system. Its connection with the system to control and the equivalent circuit to study the power flows are shown in Figure 8.

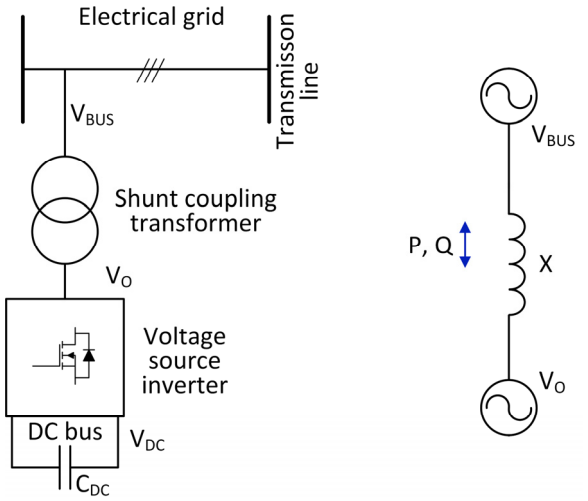


Figure 8. (**Left**) One−line diagram of a STATCOM connected to a line to compensate by the mean of a shunt-coupling transformer; (**Right**) equivalent circuit (lossless transformer and VSI).

The equations of mathematically modeling the system powers are as follows [21]:

$$P = \frac{V_{BUS} V_O \sin \alpha}{X} \tag{3}$$

$$Q = {V_{BUS}}^2 \left(\frac{1 - \frac{V_O}{V_{BUS}} \cos \alpha}{X} \right) \tag{4}$$

where α is the phase angle of V_{BUS} with respect to V_O, and X is the reactance of the coupling transformer.

When the voltage (V_o) generated by the VSI is in phase with V_{BUS} ($\alpha = 0$), only reactive power can flow between the VSI and the grid (P = 0). If V_o is lower than V_{BUS}, Q flows from the grid to the VSI (STATCOM absorbs reactive power). In contrast, if V_o is higher than V_{BUS}, Q flows from the VSI to the grid (STATCOM generates reactive power).

In an ideal lossless power converter, V_o is controlled to be in phase with V_{BUS}; then, the real power does not circulate, and a real power source is not required. Actually, beyond

the one to exchange between the AC line and the DC bus, a small part of real power is also derived from the line to provide the converter losses [17].

When a DC source such as a battery of an energy storage device is connected to the DC side of a STATCOM, it can supply real power to the AC side. This can be carried out by changing the phase angle of the voltage at the AC side of the STATCOM terminal and then the phase angle of the AC power line. When the VSI phase angle is led by one of the AC power lines, the STATCOM absorbs real power from the AC line, whereas when there is a lag between these angles, the STATCOM supplies real power to the AC line.

3.2. STATCOM Model

The model of the STATCOM connected to the grid and the DC bus is shown in Figure 9. Here, a resistance to take into account the power losses is added in series with the reactance related to the leakage inductance of the shunt transformer and the stray inductances of the electrical connections. This model is then implemented in MATLAB-Simulink 2022b.

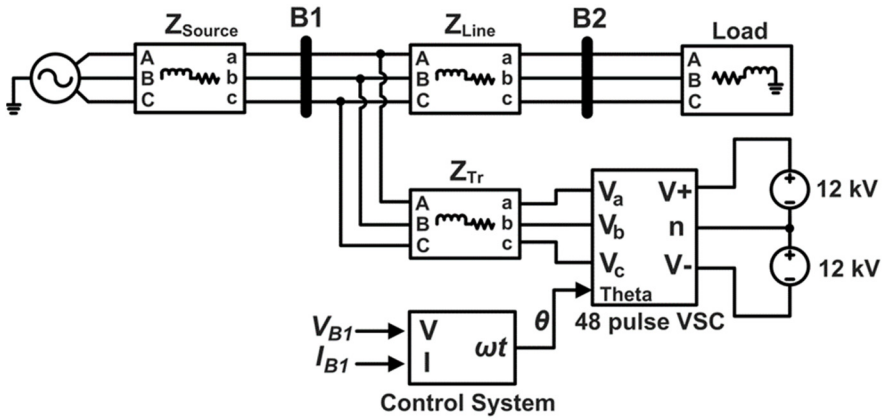


Figure 9. Simulink model of STATCOM connected to the grid.

As mentioned in Section 1, our goal is to implement the STATCOM in voltage control mode. The control approach used here is indirect control. With it, only the phase angle of the output voltage is controllable, and the magnitude remains proportional to the DC-link voltage. However, the DC-link voltage can be varied by regulating the angular position of the output voltage. In this situation, real power is exchanged with the transmission line to charge or discharge the DC-link capacitor to the desired level [22].

The control system is made up of two loops. An inner current loop generates the required converter angle, and an outer voltage loop is meant to regulate the bus voltage and generate the reactive current references for the current loop. The schematic diagram used to implement the current loop control is shown in Figure 10.

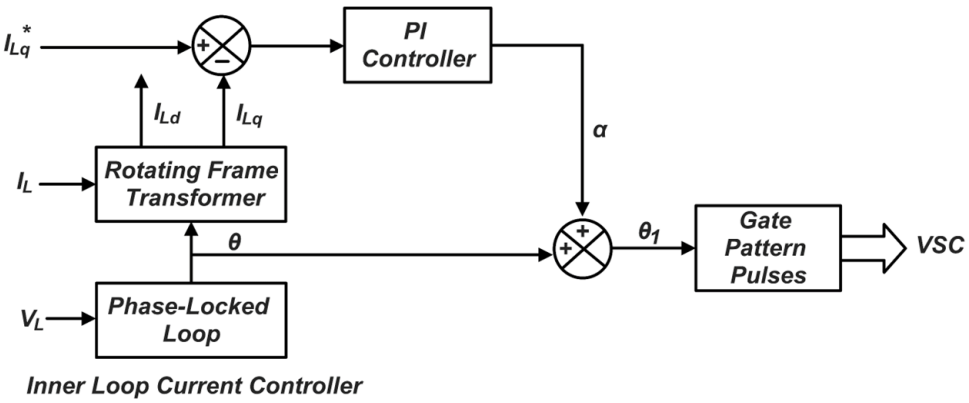


Figure 10. Reactive current control block diagram of the STATCOM.

Considering the Park reference frame, the magnitude of the quadrature current (I_{Lq}) is compared to the reference quadrature current ($I_{Lq}{}^{*}$). Thus, the obtained error signal provides an angle (α), defining the essential phase shift between the converter output and the AC line voltages for changing (by charging or discharging the capacitor) the DC voltage level to the one needed. The phase-locked loop is driven by the AC system voltage, and it generates the fundamental synchronizing signal angle (θ). Angle $\theta_1 = \theta + \alpha$ drives the logic circuit, which generates each gate logic signal to control the power switches of the converter.

It should be noted that the reference quadrature component ($I_{Lq}{}^{*}$) of the current through the VSC could be either positive or negative if the STATCOM is emulating a capacitive or inductive reactance, respectively.

The tuning process of the PI controller in Figure 10 depends on the transfer function linking the output angle to its input reactive current. A small signal analysis carried out in [23] produces the input–output transfer function of Equation (5):

$$\frac{I_{Lq}(s)}{\alpha(s)} = \frac{-V_s\left(L_sCs^2 + R_sCs + m_c^2\right)}{CL_s^2s^3 + 2L_sCR_ss^2 + \left[C\left\{R_s{}^2 + (\omega L_s)^2\right\} + m_c^2L_s\right]s + m_c^2R_s} \tag{5}$$

where m_c is the modulation index of the converter, L_s is the leakage inductance of the coupling transformer, R_s is the resistance related to the converter and coupling inductor losses (effective coupling resistance), and C is the capacitance of the DC-link capacitor. The modulation index can easily be computed from Equation (1) by setting $m = 1$. This is given in Equation (6):

$$m_c = \frac{V_{o1}}{V_{dc}} = \frac{2\sqrt{2}}{\pi}\sin\left(\frac{\sigma}{2}\right) \tag{6}$$

where V_{o1} is the magnitude of the harmonic at the fundamental frequency of the phase voltage at the AC side of the STATCOM.

The DC-link capacitance value can be computed using Equation (7) derived from [24]:

$$C = \frac{0.9I_{rms}}{0.02 \times 4\pi f \times V_{dc}} \tag{7}$$

with I_{rms} given by Equation (8):

$$I_{rms} = \frac{160 \times 10^6}{\sqrt{3}V_{LL}} \tag{8}$$

Using Equations (6)–(8), we obtain $m_c = 0.9$, $I_{rms} \cong 669.4$ A, and $C \cong 1665$ µF. The bandwidth of the PI controller is chosen to be 2 kHz.

Finally, the limiting range of α has to be computed. This is carried out using Equations (9)–(11) obtained from [25]:

$$v_1 = \frac{np\sqrt{6}}{6\pi}V_{dc}\cos\left(\frac{\pi}{24}\right) \tag{9}$$

where p = the pulse number, n = the primary-to-secondary transformer-winding-turns ratio, and v_1 = the fundamental AC output voltage of each set of three-level 24-pulse VSCs. Then, we can write that

$$v_{conv} = 2v_1\cos(\alpha) \tag{10}$$

and

$$Q = \frac{v_s(v_s - v_{conv})}{X} \tag{11}$$

Q is chosen to be ±1.2 pu (leading and lagging), considering a 0.2 pu margin during dynamic conditions.

The tuning of the PI controller is carried out using the SISO Toolbox of MATLAB. The results are shown in Figure 11. We see that when a positive reactive current is demanded, the STATCOM supplies capacitive reactive power to the grid, as observed in the

first 3 s of the responses. When the reactive current demand changes to a negative value, the STATCOM responds to that change and absorbs the reactive power from the grid, acting as an inductor in this case. We also see how insignificant the real power exchange is, at almost 0 W. The small, steady value of 60 W of active power seen in Figure 11 is just that needed by the DC-link capacitor during its charge and discharge process, as was already explained before, and to supply losses in the VSC.

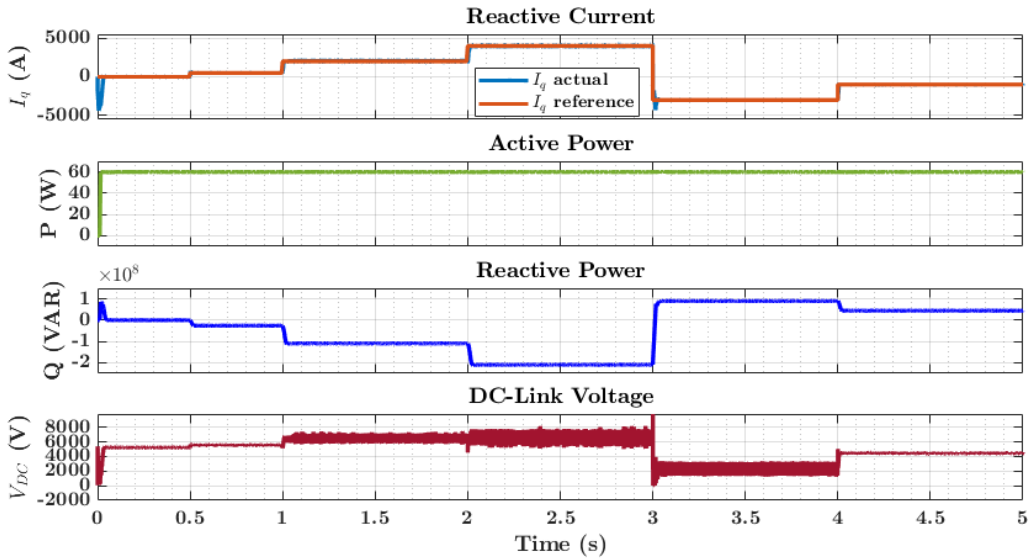


Figure 11. From top to bottom: STATCOM reactive current response for various current references; real power exchange; reactive power exchange between the STATCOM and the grid; DC-link voltage variation of STATCOM VSC.

We also observe from Figure 11 the change in the DC-link voltage of the STATCOM. This is necessary, since we are implementing the indirect control of the STATCOM, and we see from Equation (1) that the unique way to vary the converter output voltage when the zero angle is fixed is for the DC-link voltage to vary.

Next, the outer voltage loop, whose function is to control the bus voltage to a specific reference value and generate the reactive current reference for the power system, is designed. The block diagram used to do this is shown in Figure 12.

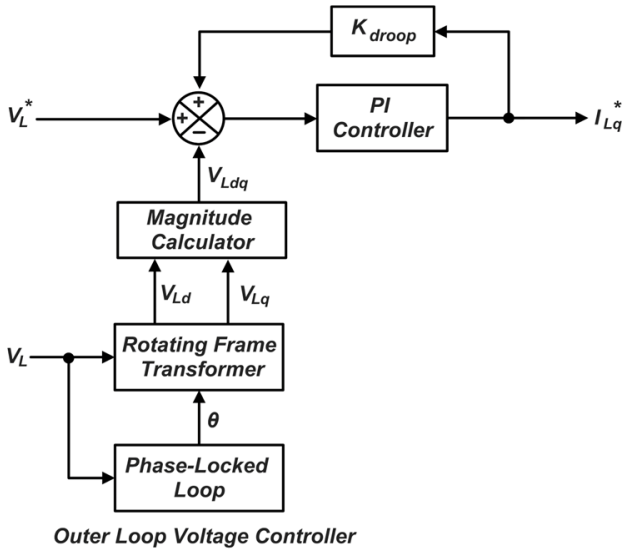


Figure 12. Voltage control block diagram of STATCOM.

The droop factor is chosen to be 0.03. Since the voltage loop is external to the current loop, it has to be slower. Consequently, the PI controller bandwidth chosen is 180 Hz. The transfer function used to represent the plant is defined as follows in Equation (12):

$$\frac{I_q(s)}{V_1(s)} = \frac{1}{Ls + R} \tag{12}$$

The tuning of the controllers is carried out using the zero-pole cancellation technique with different gains defined as $K_P = 2\pi f_o L$ and $K_I = 2\pi f_o R$. A factor of $\sqrt{3/2}\omega L$ is added to the input of the error amplifier of Figure 13. This factor smoothens out the waveform and increases the response time [26].

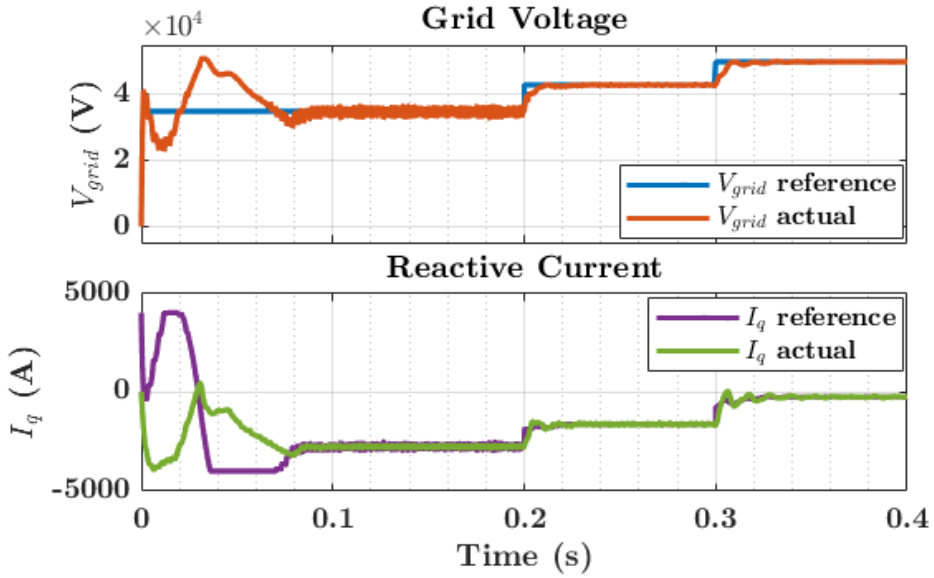


Figure 13. (**top**) STATCOM bus voltage regulation; (**bottom**) STATCOM reactive current flow during bus voltage regulation.

Figure 13 shows the voltage control waveforms (top graph) of the STATCOM as well as the reactive current (bottom graph) being provided by the STATCOM. We observe that the STATCOM can regulate the bus voltage. However, the voltage regulation range is limited. Moreover, Figure 13 shows that the STATCOM current controller can track the required reactive current generated by the voltage loop. As observed, the system possesses some disturbances within the first 0.08 s due to the filters used in the system and the bandwidth of the controllers chosen.

4. SSSC Implementation

4.1. SSSC Operation

The Static Synchronous Series Compensator is a series-connected device consisting of a VSC, a DC-link capacitor, and a coupling transformer, as shown in Figure 14. An SSSC can generate and inject a compensating voltage (V_q) into the transmission line through the coupling transformer and is controllable over the capacitive or inductive range. This voltage is in quadrature with the line current and based on the system requirement; it could be operated in inductive or capacitive mode. Capacitive compensation is used to reduce the series reactance and hence increase the power flow in the line, while inductive compensation increases the line reactance and thus reduces the line power flow. Therefore, by simply changing the injected voltage polarity to be either positive or negative, the SSSC can increase or decrease the power flow of the transmission line [27].

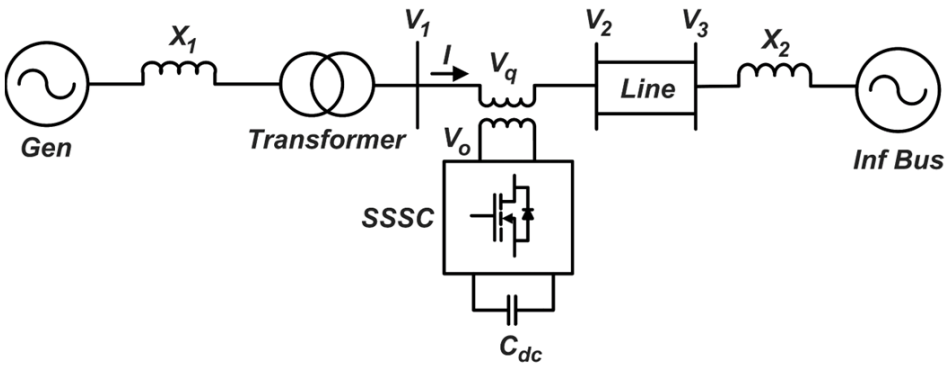


Figure 14. SSSC interface to power system.

The active and reactive power flow equations of an SSSC compensated system are, respectively, given by Equations (13) and (14):

$$P = \frac{V_1 V_2}{X}\sin\alpha + \frac{V_1 V_q}{X}\cos\left(\frac{\alpha}{2}\right) \tag{13}$$

$$Q = \frac{V_1}{X}(V_1 - V_2\cos\alpha) + \frac{V_1 V_q}{X}\sin\left(\frac{\alpha}{2}\right) \tag{14}$$

X is the effective reactance of the line between buses 1 and 2 (X_L + X_q) and α is the phase angle between V_1 and V_2.

4.2. Open-Loop Test of SSSC

The system shown in Figure 14 is implemented in Simulink and the converter's phase angle (α) is slowly varied from 0 to 2π (the phi angle is fixed to 3.75°). We see from the results shown in Figure 15 that as alpha is varied from 0 to 2π, the active and reactive power flow becomes sinusoidal as expected from Equations (13) and (14), thus validating the SSSC open-loop system.

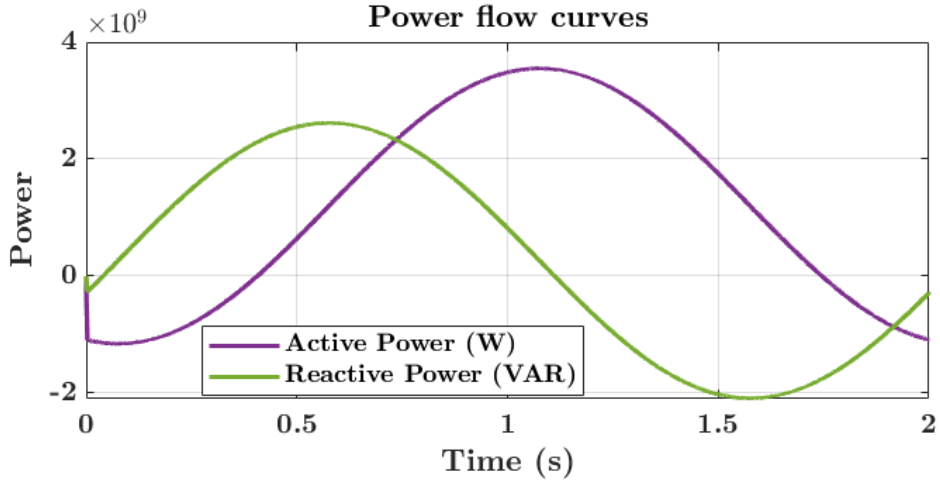


Figure 15. Active and reactive power flow with SSSC in open loop.

5. UPFC Implementation

After having successfully tested the STATCOM in closed loop and the SSSC in open loop, all in standalone mode, now, they can be connected to form the UPFC. The UPFC model shown in Figure 16 is designed and implemented in Simulink.

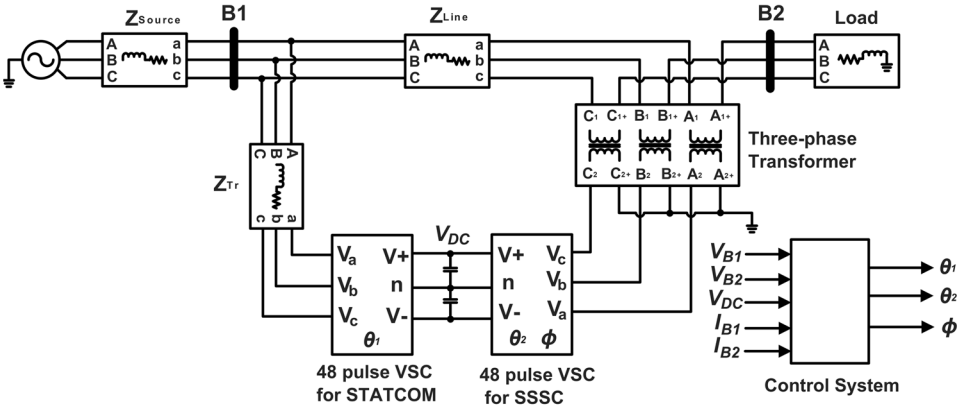


Figure 16. Model of the UPFC implemented in Simulink.

5.1. Open-Loop Operation of the UPFC

Just as was undertaken previously, the STATCOM voltage and current loops are again tested in a closed loop while varying the alpha angle of the SSSC from 0 to 2π. The STATCOM current and voltage loop dynamics as well as the SSSC power flow curves are shown in Figure 17.

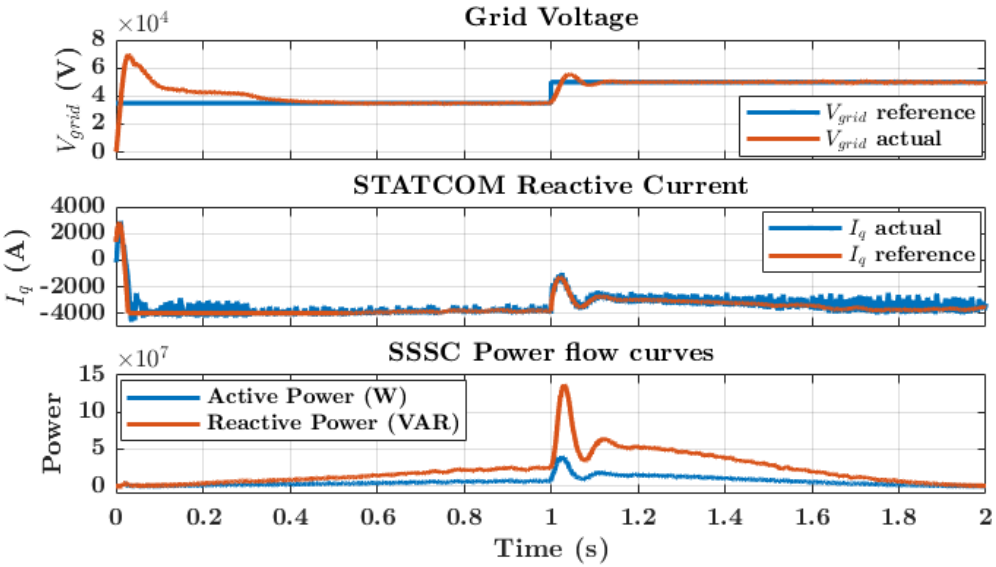


Figure 17. From top to bottom: Voltage control of STATCOM with UPFC in open loop; reactive current control of STATCOM; SSSC power flow in UPFC configuration when STATCOM is in voltage control mode.

It is seen from Figure 17 that connecting both the STATCOM and the SSSC increases the noise in the system. The STATCOM current (reactive power) control loop also works properly. Just like the current, the grid voltage response of Figure 17 shows a better noise rejection at the start of the response compared to that of Figure 13, although this comes at the expense of a slower response and more overshoot in the control system.

The power curves of the SSSC also vary sinusoidally in the open loop when α is varied from 0 to 2π, as depicted by Equations (13) and (14). The sudden increase in the power seen at t = 1 s is due to the change in the grid voltage of the STATCOM at the same time. The results obtained validate the open-loop operation of the UPFC.

5.2. Closed-Loop Operation of UPFC

The closed-loop implementation of the UPFC will be based on the automatic power flow mode of the SSSC. In this mode, the magnitude and angle of the SSSC injected voltage,

V_{pq}, which is determined automatically and continuously by a closed-loop control system, is controlled to produce a line current (I_L) with a magnitude and angle which produces the wanted active and reactive power flow in the line.

Two control approaches are possible: the first one is designing a PI controller to directly control the active and reactive power flow, and the second one is controlling the power flows indirectly by controlling the current flowing in the line. All approaches bring about a completely decoupled *PQ* control. However, the second approach, which is the one used in this work, is much preferable due to its robustness against variations in the parameters of the VSC and AC system, superior dynamic performance, and better control precision [28].

Figure 18 illustrates the control diagram of the utilized approach. We note that with such two degrees of control, the same indirect control scheme that was used in the STATCOM cannot be used. So, the direct control approach is used here.

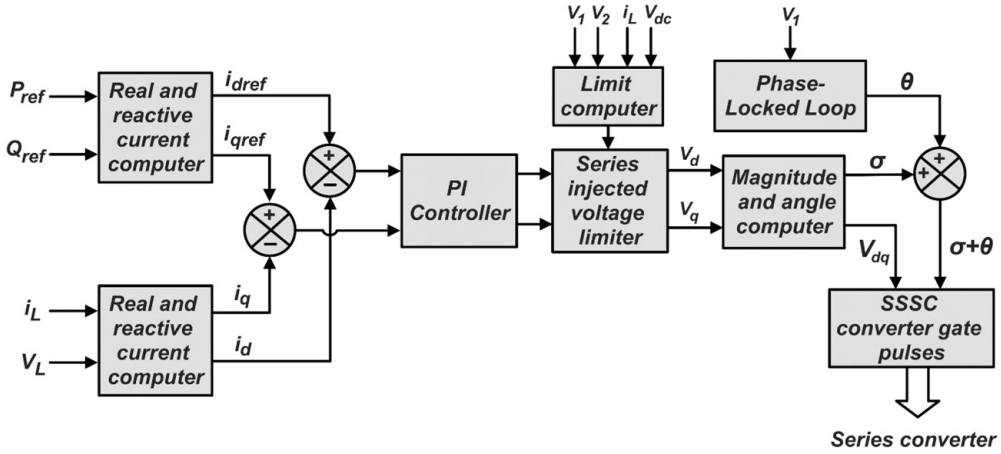


Figure 18. Block diagram of SSSC in automatic PQ control mode.

The small signal transfer function derived from [29] used to design the SSSC current PI controller is given by Equation (15):

$$\frac{i_{dq}(s)}{V_{dq}(s)} = \frac{(L_{se}s + R_{se})/L_{se}^2}{s^2 + 2\left(\frac{R_{se}}{L_{se}}\right)s + \omega^2 + \left(\frac{R_{se}}{L_{se}}\right)^2} \tag{15}$$

The bandwidth of the controller chosen is 800 Hz. The SISO Toolbox of MATLAB 2022b is used to tune the controller to obtain the appropriate response.

The functioning of the SSSC current loop is tested by directly making it work in the four quadrants of the power curve. The results obtained are shown in Figure 19.

We see from Figure 19 that the SSSC current controllers work properly. We also see that the four-quadrant operation of the UPFC is obeyed, which is achieved through the change of sign of the active and reactive currents demanded. This way, the V_{pq} voltage vector rotates, hence changing its magnitude and phase and bringing about the power flow reversals.

For automatic power flow control, the active and reactive current references from the instantaneous power theory are defined, respectively, by Equations (16) and (17):

$$i_{dref}{}^* = \frac{\sqrt{3}}{2}\frac{P_{ref}V_{1d} + Q_{ref}V_{1q}}{V_{1d}{}^2 + V_{1q}{}^2} \tag{16}$$

$$i_{qref}{}^* = \frac{\sqrt{3}}{2}\frac{P_{ref}V_{1q} - Q_{ref}V_{1d}}{V_{1d}{}^2 + V_{1q}{}^2} \tag{17}$$

The factor of $\sqrt{3}/2$ is due to the Δ-Y transformers used in the VSC.

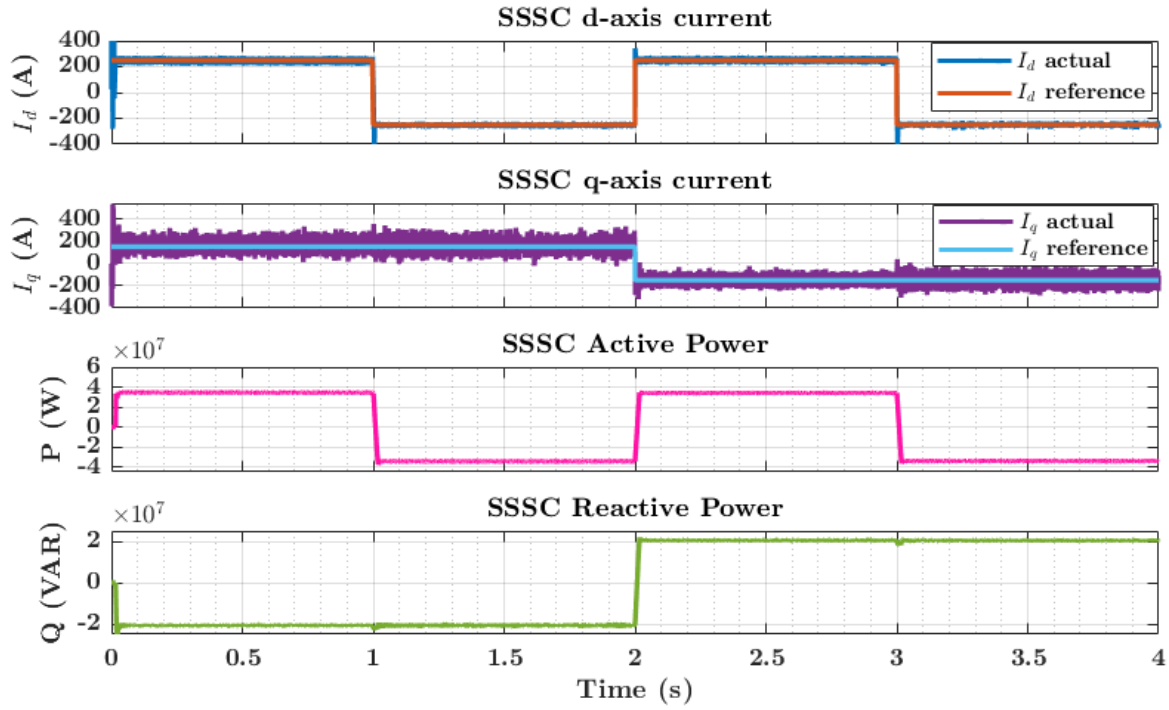


Figure 19. From top to bottom: SSSC *d*-axis current in closed loop; SSSC *q*-axis current in closed loop; active power flow in SSSC; reactive power flow in SSSC.

Figure 20 shows the UPFC power flows, whereby the SSSC operates in automatic power mode and the STATCOM works in voltage control mode. We see that, with the system implemented, we can directly demand the wanted active and reactive powers and the SSSC controller responds to those as demanded. There is some noise in the response, but that can be improved by a better choice of the controller bandwidths as well as cut-off frequencies of the various filters in the system. Figure 20 also shows a step response with the automatic voltage control mode of STATCOM as part of the UPFC. In the simulation, we fixed the reference voltage to 138 kV and the voltage controller responded to that without overshoots within a relatively short time of about 0.4 s.

This brings us to a staggering discovery: in the absence of the UPFC, i.e., when the STATCOM functioned in standalone mode, its range of voltage control was limited and could not control voltages above 70 kV, but with the SSSC, this limit is higher. Furthermore, there were significant disturbances in the transients, leading to a steady state as well as long settling times. These parameters were improved by implementing the UPFC in the open loop. However, the closed-loop implementation of the UPFC made the system even better dynamically. Moreover, the SSSC can provide active and reactive power demands up to values of 95 MW and 108 MVar, respectively.

Moreover, Figure 20 shows the flow of active power through the STATCOM. We see that between t = 0.2 s and t = 1 s, the line active power flow is commanded to increase. As such, the STATCOM absorbs and provides the SSSC with about 9 MW of active power through the DC link. From t = 1 s to t = 1.8 s, the line active power decreases and the shunt device delivers about 31 MW of active power to the node to which it is connected. Finally, Figure 21 shows how the load current THD varies with time when the proposed UPFC is used compared to when it is not used with a theoretical non-linear load connected to bus 2, shown in Figure 16. Without the UPFC, the load current is highly distorted due to the presence of this load. We see how the introduction of the UPFC drastically improves the THD (<5%), showing how it can improve power quality.

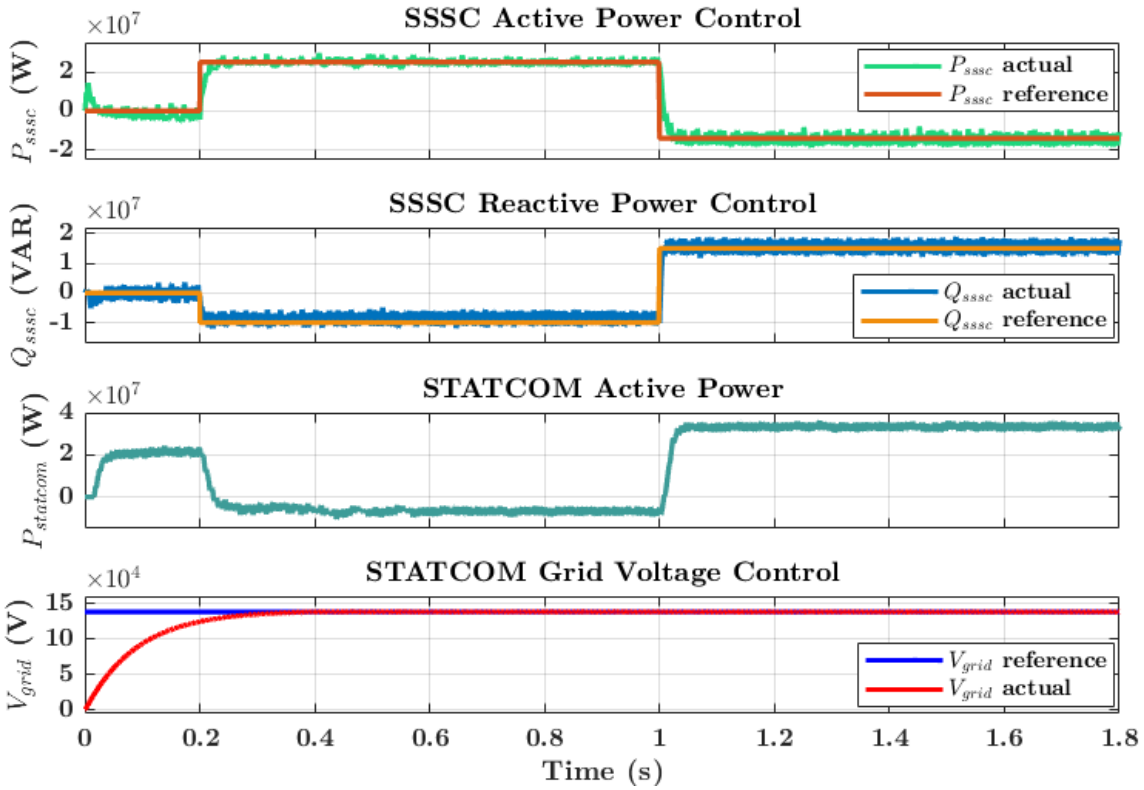


Figure 20. From top to bottom: Active power flow control of SSSC; reactive power flow control of SSSC; automatic voltage control mode of STATCOM; active power exchange of STATCOM.

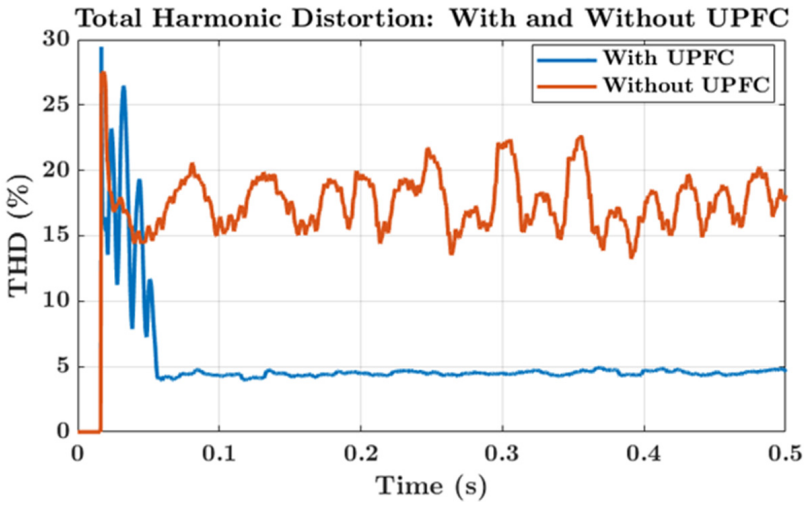


Figure 21. Grid voltage THD analysis with and without UPFC, in presence of a non-linear distorting load.

The THD with the UPFC meets the IEEE 519-2022 standard [30], which defines the voltage and current harmonics distortion criteria for the design of electrical power systems. The THD can be further reduced by using a 96-pulse VSC instead of the one used in this work, albeit at the expense of increased system complexity. An alternative solution to harmonic reduction is to replace the UPFC with a Distributed Power Flow Controller (DPFC), derived from the UPFC by eliminating the DC link between the shunt and series converters. Moreover, the DPFC replaces the large-sized three-phase series converter of the UPFC (SSSC) with multiple line-distributed small-sized single-phase converters to provide redundancy and increase system reliability.

6. Conclusions

In this study, we successfully implemented a UPFC in a closed loop, where we were able to regulate the power flowing in the line using the SSSC and control the node voltage using the STATCOM. A tracking system was established to obtain the best value of the harmonic components, which led to the optimal value of the conduction angle for minimizing the THD. Furthermore, the VSCs of both controllers were built using a combined multilevel–multi-pulse converter, which improved the harmonic distortion of the output voltage waveforms. Finally, as has been seen, the UPFC can improve the voltage quality, power transmission capacity, and stability of the system by suppressing system oscillations. Also, the UPFC gives a quick system response. Furthermore, a harmonic analysis of the system current was performed, and it was found to meet the IEEE 519 standard.

The AC power grid is constantly stressed due to increased load demands, which may cause it to perform beyond its initial capacity. Furthermore, when power system constraints are exceeded due to overload, transient stability concerns might emerge, resulting in system disturbances and grid operators' incapacity to handle daily power demands. Such system disruptions create oscillations, which may result in asynchronous generator operation or even a partial system shutdown. These hazardous effects could be avoided by using FACTS devices that effectively and effortlessly control dynamic power across the AC power network. As a result, the deployment of FACTS devices to the AC grid will result in increased energy efficiency due to better energy utilization.

Future research areas in this field include, but are not limited to, lowering the cost of UPFC equipment, developing new cost-effective UPFC converter topologies and architectures with experimental validation, developing new UPFC control algorithms with reconfigurable architecture, developing wide-area-coordinated control algorithms, and developing new models, methods, and simulation tools for integrating UPFCs into the smart power grid.

The contributions of this study are the methodological approach used in designing and controlling these kinds of systems, which is usually absent in similar papers, and the new algorithm for tracking and determining the optimal conduction angle of the NPC converter, which leads to the least harmonic distortion in the output voltage and current signals. The modeling technique proposed foresees to (i) build open-loop models of each compensator of the UPFC and run simulations varying the parameters to control power flows and/or voltages to verify the dynamics of voltages, currents, and powers; (ii) carry out the numerical study of each compensator with closed-loop controls to expand the testing carried out at step (i); and (iii) execute simulations of the whole UPFC, again in open and closed loops, and compare the results with the ones obtained in the previous steps. The first two steps are needed to verify the models of single parts, while the last step shows the effects of coupling the shunt and series compensators in back-to-back configuration by applying different control strategies. Then, this procedure can be very useful to designers of power flow controllers.

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Data Availability Statement: The data presented in this study are available in this article.

Conflicts of Interest: The authors declare no conflicts of interest.

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