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Design of a 1.2 kV SiC MOSFET with Buried Oxide for Improving Switching Characteristics

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Abstract: The 1.2 kV SiC MOSFET with a buried oxide was verified to be effective in improving switching characteristics. It is crucial to reduce the gate–drain charge (Q_{GD}) of devices to minimize switching loss (E_{total}). The SiC MOSFET with a split gate and device with a buffered oxide have been proposed by previous studies to reduce the Q_{GD} of the devices. However, both devices have a common issue of the concentration of the electric field at the gate oxide. In this paper, we propose the 1.2 kV SiC MOSFET with a buried oxide to reduce the Q_{GD} and suppress the electric field crowding effect at the gate oxide. We analyzed the specific on-resistance ($R_{on,sp}$), Q_{GD} and the maximum electric field at the gate oxide in the off state ($E_{ox,max}$) according to the width (W_{BO}) and thickness of the buried oxides (T_{BO}). The device with the buried oxide, under optimal conditions, showed lower $E_{ox,max}$ and E_{total} without significant increase in $R_{on,sp}$ in comparison to the device with a conventional structure. These results indicate that the buried oxide can improve the switching characteristics of 1.2 kV SiC MOSFETs.

Keywords: SiC; MOSFET; gate charge; electric field crowding effect; switching characteristics

1. Introduction

Silicon carbide (SiC) power semiconductors exhibit superior performance compared to silicon (Si) power semiconductors owing to their wide bandgap energy, high critical electric field and thermal conductivity [1–5]. SiC devices with wide bandgap energy demonstrate reliable operation even at elevated temperatures due to their lower intrinsic carrier density [1,2]. The high critical electric field of SiC enables the design of a thinner N-drift layer with higher doping concentration compared to Si devices operating at the same rated voltage. The resistance of the N-drift layer accounts for the majority of the total resistance, so SiC devices with thin and high-doped N-drift layer exhibit lower on-resistance and conduction loss. Additionally, SiC devices have high thermal conductivity, ensuring stable performance even at high temperatures [3,4].

SiC devices such as SiC Schottky barrier diodes (SBDs) and SiC metal oxide semiconductor field effect transistors (MOSFETs) are widely used in the rated voltage range from 600 V to over 3.3 kV due to their superior breakdown characteristics and low resistance. Particularly, 1.2 kV SiC MOSFETs are extensively utilized as switching components in electric vehicle on-board chargers, inverters and DC–DC converters [4,5]. However, the gate charge of 1.2 kV SiC MOSFETs are required to be minimized because a large portion of the energy loss occurs during the switching operation of the devices. The gate–drain charge (Q_{GD}) is a main parameter that influences the switching characteristics of SiC MOSFETs. High voltage and current are applied simultaneously to the devices when the gate–drain capacitance (C_{GD}) is being charged [5,6]. Several studies to improve the switching characteristics of SiC MOSFETs by reducing the Q_{GD} have been reported [7–17].

Baliga's research group reported the use of a 1.2 kV SiC MOSFET with a split gate to reduce Q_{GD} of the device. The split gate has a split structure of a poly-Si gate over the

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JFET region. The device with the split gate is effective for reducing Q_{GD} because the area overlapped between the gate and the drain is reduced [8–12]. However, the device with the split gate presents the issue that the electric field is concentrated at the gate oxide [8,9]. In subsequent studies, they added a p-type layer of high concentration to the bottom of the p-base region to suppress the electric field crowding effect at the device. This p-type layer of high concentration serves to protect the gate oxide by widening the depletion layer in the p-base junction [10–12].

Buffered oxide is another structure that can reduce the Q_{GD} of SiC MOSFETs. The buffer oxide has the structure where a thick oxide is deposited over the JFET region. The 1.2 kV SiC MOSFET with buffered oxide has lower Q_{GD} compared to the device with a conventional structure due to a decrease in C_{GD} [13,14]. However, the protruding shape of the poly-Si gate leads to the concentration of the electric field at the corners of the buffered oxide. The 1.2 kV SiC MOSFET with a tapered buffer oxide has been introduced to address the issue of electric field crowding effect in the device with the buffered oxide [14]. The tapered buffer oxide is characterized by the addition of an angle to the buffered oxide. The device with tapered buffer oxide has shown the ability to disperse the concentration of the electric field at the corners of the gate oxide [7,14].

The device with the split gate and the p-type layer with high concentration needs an additional step for ion implantation [10–12,15]. In the case of the device with the tapered buffer oxide, the maximum electric field at the gate oxide in the off state ($E_{ox,max}$) of the device is highly dependent on the angle of the tapered buffer oxide [14]. Several studies that have investigating the gate reliability of SiC MOSFETs using an analysis of time dependent dielectric breakdown have reported that SiC MOSFETs have reliable electrical characteristics when the $E_{ox,max}$ has been designed below 3 MV/cm [16–18]. Therefore, it is necessary to develop the devices for low $E_{ox,max}$ as well as for low Q_{GD}.

In this paper, the 1.2 kV SiC MOSFET with buried oxide which has improved switching and electric field characteristics is proposed. We used TCAD simulations to verify the performance of the 1.2 kV SiC MOSFET with the buried oxide. The device with the buried oxide, shown in Figure 1b, has a structure in which the JFET region is etched and filled with oxide. We analyzed the specific on-resistance ($R_{on,sp}$), Q_{GD} and $E_{ox,max}$ of the devices with the buried oxides according to the width (W_{BO}) and thickness of the buried oxide (T_{BO}) to obtain optimal conditions for the buried oxide. In addition, the switching characteristics of the device with the conventional structure and the device with the buried oxide under optimal conditions were compared. The results showed that buried oxide is effective in improving the switching characteristics of 1.2 kV SiC MOSFETs without deteriorating other electrical characteristics.

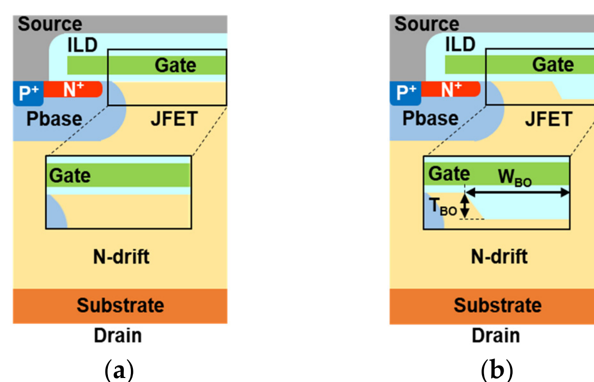

Figure 1. Cross-sectional views of 1.2 kV SiC MOSFETs. (**a**) The device with the conventional structure and (**b**) the device with the buried oxide.

2. Methods of Simulations

Sentaurus TCAD simulations were used to evaluate the performance of the 1.2 kV SiC MOSFET with buried oxide. For comparison, the 1.2 kV SiC MOSFET with the conventional

structure and the 1.2 kV SiC MOSFETs with buried oxides were designed. The simulations were conducted based on the size of a half-cell. The target values for breakdown voltage (BV) and $R_{on,sp}$ were set at 1560 V and 5 mΩ·cm^2, respectively. The cell pitch, channel length, width of the JFET, concentration and thickness of the N-drift layer were designed considering the target BV and $R_{on,sp}$ [19–21]. The width of the JFET from the surface of the N-drift layer, based on the half-cell, is 0.7 μm. The aluminum (Al) concentration of the p-base is highest at a distance of 0.4 μm from the surface of the N-drift layer. At this location of the highest Al concentration in the p-base, the width of the JFET, based on the half-cell, is 0.5 μm. To ensure that the buried oxide does not completely block the JFET region, the W_{BO} was designed to be between 0.1 and 0.5 μm and T_{BO} was designed to be between 0.1 and 0.3 μm. Design parameters of the device with the conventional structure and the device with the buried oxide are summarized in Table 1. To optimize the design conditions for buried oxide, we compared the $R_{on,sp}$, Q_{GD} and $E_{ox,max}$ of the devices with buried oxides according to the W_{BO} and T_{BO}. The switching loss (E_{total}) of the device with the conventional structure and that with the buried oxide under optimal conditions were then compared, revealing that buried oxide is effective in improving the switching characteristics of 1.2 kV SiC MOSFETs.

Table 1. Design parameters of the 1.2 kV SiC MOSFET with the conventional structure and devices with the buried oxides.

Design Parameters [Unit]	Value
Width of the half-cell [μm]	3
Length of the channel [μm]	0.5
Concentration of the N-drift layer [cm^{-3}]	1×10^{16}
Thickness of the N-drift layer [μm]	10
Width of the JFET in half-cell [μm]	0.7
Width of the buried oxide (W_{BO}) [μm]	0.1, 0.2, 0.3, 0.4, 0.5
Thickness of the buried oxide (T_{BO}) [μm]	0.1, 0.2, 0.3

3. Results and Discussion

Figure 2 is the $R_{on,sp}$ of the device with the conventional structure and devices with the buried oxides according to the W_{BO} and T_{BO}.

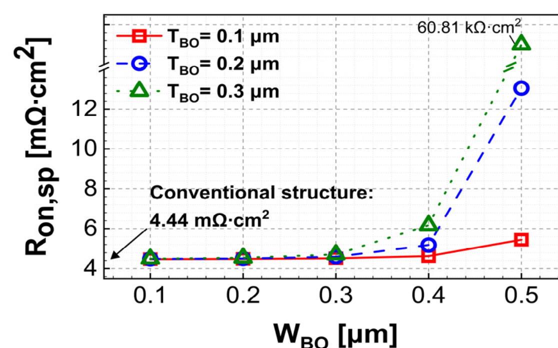

Figure 2. $R_{on,sp}$ of the 1.2 kV SiC MOSFETs with the conventional structure and devices with buried oxides according to the W_{BO} and T_{BO} (V_{GS} = 18 V).

The 1.2 kV SiC MOSFETs with the buried oxides have higher $R_{on,sp}$ than the device with the conventional structure. The $R_{on,sp}$ of the devices with buried oxides increases sharply with the increasing T_{BO} when the W_{BO} is 0.4 μm or higher. To analyze the sharp increase in the $R_{on,sp}$ of the devices with buried oxides when the W_{BO} is 0.4 μm or greater, the total current density of the devices with buried oxides was analyzed.

Figure 3 illustrates the total current density of 1.2 kV SiC MOSFETs with the buried oxides. The total current density was derived when the devices with the buried oxides had

V_{DS} and V_{GS} of 10 and 18 V, respectively. The buried oxide approaches the p-base region as the W_{BO} increases from 0.3 to 0.5 μm, leading to a reduction in the current density flow through the JFET region. For the devices with the T_{BO} of 0.3 μm, it is evident that the buried oxide significantly impedes current flow through the JFET region. This obstruction of the current flow in the JFET region results in an increase in accumulation resistance [19–21]. In the case of the device with the buried oxide, where the W_{BO} is 0.5 and T_{BO} is 0.3 μm, the $R_{on,sp}$ of the device is 60.81 kΩ·cm^2 because the current is rarely flowing through the JFET region. These results indicate that the W_{BO} needs to be 0.4 μm or less to reduce the $R_{on,sp}$.

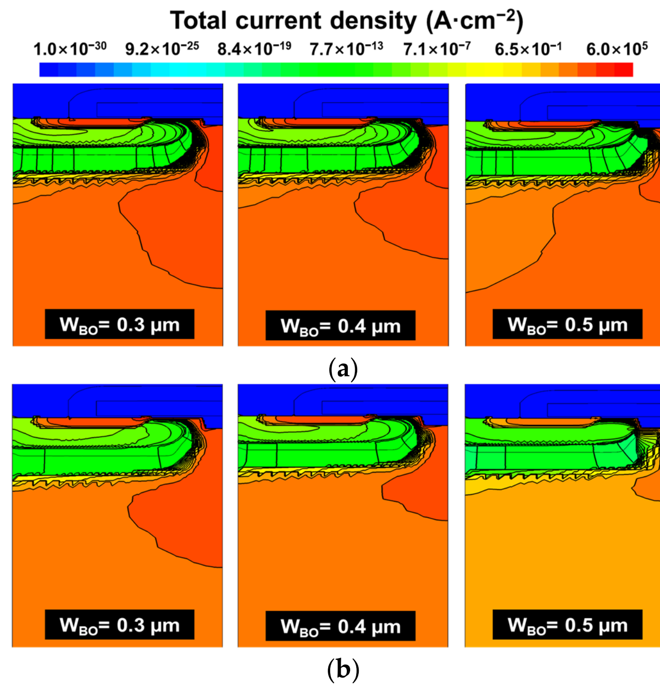

Figure 3. Total current density of the 1.2 kV SiC MOSFETs with the buried oxides (V_{DS}= 10 and V_{GS}= 18 V). The devices with the buried oxide with (**a**) a T_{BO} of 0.2 μm and a W_{BO} from 0.3 to 0.5 μm and (**b**) a T_{BO} of 0.3 μm and a W_{BO} from 0.3 to 0.5 μm.

The Q_{GD} of the 1.2 kV SiC MOSFET with the conventional structure and devices with the buried oxides according to the W_{BO} and T_{BO} are shown in Figure 4.

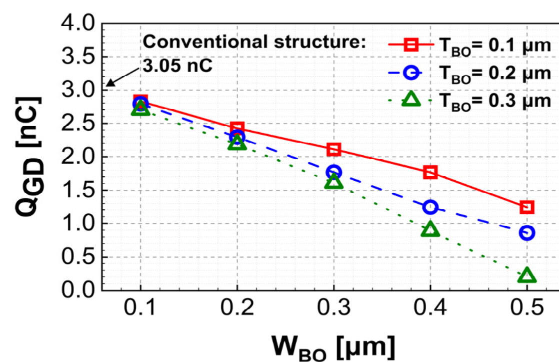

Figure 4. Q_{GD} of the 1.2 kV SiC MOSFETs with the conventional structure and devices with the buried oxides according to the W_{BO} and T_{BO}.

The Q_{GD} was determined by calculating the shift in gate charge between the two points where the slope of the $V_{gs}-Q_G$ curve exhibits the maximum value [13,14]. In contrast to Figure 2, the Q_{GD} of the devices with the buried oxides is lower than that of the device with the conventional structure. This tendency becomes more noticeable as the W_{BO} and T_{BO}

increase. When the devices have buried oxides with larger W_{BO} and T_{BO}, the area where the gate and the drain overlap is reduced, leading to a decrease in C_{GD} between the gate and the drain [5,13,14].

Figure 5 shows the $E_{ox,max}$ of the 1.2 kV SiC MOSFET with the conventional structure and devices with the buried oxides according to the W_{BO} and T_{BO}. The $E_{ox,max}$ of the devices with the buried oxides is lower than that of the device with the conventional structure because the buried oxide is effective in dispersing the electric field at the gate oxide [13,14]. The $E_{ox,max}$ of the devices with buried oxide decreases as the W_{BO} increases from 0.1 to 0.3 µm. However, the $E_{ox,max}$ of the devices with buried oxide increases as the W_{BO} increases from 0.4 to 0.5 µm. The electric field distribution of 1.2 kV SiC MOSFETs with buried oxides according to the W_{BO} and T_{BO} was analyzed to figure out the cause of the increase in the $E_{ox,max}$ of the devices with the buried oxides when the W_{BO} is 0.4 µm or greater.

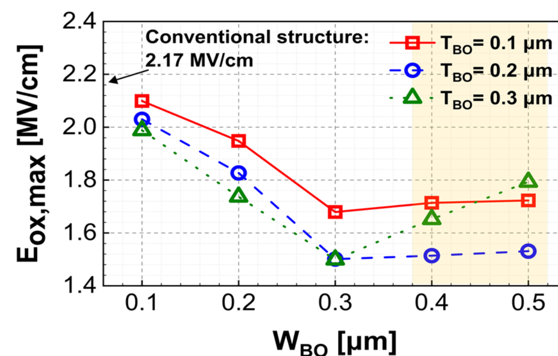

Figure 5. $E_{ox,max}$ of the 1.2 kV SiC MOSFETs with the conventional structure and devices with the buried oxides according to the W_{BO} and T_{BO}.

Figure 6a,b are the electric field distribution of the devices with the T_{BO} of 0.4 and 0.5 µm, respectively. The respective $E_{ox,max}$ and locations where the electric field concentrates at the buried oxide are noted within each figure. The p-base has the highest Al concentration at a distance of 0.4 µm from the surface of the N-drift layer. At this point, the width of the JFET is 0.5 µm based on the half-cell. Therefore, the devices with the buried oxides and with a T_{BO} of 0.3 µm are positioned closer to the junction between the p-base and the JFET than those with a T_{BO} of 0.1 and 0.2 µm. Since the electric field is concentrated at the junction between the p-type and n-type semiconductors, the devices with the buried oxides with a T_{BO} of 0.3 µm have high $E_{ox,max}$ due to the influence of the concentrated electric field at the junction between the p-base and the JFET [5,19,22,23]. When the W_{BO} is 0.3 µm or less, the buried oxide is far enough away from the junction between the p-base and the JFET to prevent this phenomenon. However, when the W_{BO} is 0.4 µm or greater, the buried oxide approaches the junction between the p-base and the JFET, causing an increase in $E_{ox,max}$. This increase in $E_{ox,max}$ is particularly pronounced when the T_{BO} is 0.3 µm.

The devices with buried oxides, where the W_{BO} is greater than 0.4 µm, exhibit a significant increase in $R_{on,sp}$ compared to the other devices with the buried oxides. Among the devices with the buried oxides where the W_{BO} is 0.3 µm or less, the device with the buried oxide with a W_{BO} of 0.3 and a T_{BO} of 0.3 µm has the smallest Q_{GD} and $E_{ox,max}$. Therefore, the optimal conditions for the W_{BO} and T_{BO} were chosen as 0.3 and 0.3 µm, respectively.

We compared the switching characteristics of the device with the conventional structure and the device with the buried oxide under optimal conditions (W_{BO} = 0.3 and T_{BO} = 0.3 µm). The used circuit for switching characteristics is shown in Figure 7. The circuit of Figure 7 was designed based on the settings of the Keysight PD1550A Double Pulse Analyzer. The gate voltage for switching the devices was switched from −5 to 18 V and the drain supply voltage was set to 800 V. Resistance of the gate and the load of the inductor were set to 10 Ω and 120 µH, respectively. The E_{total} was calculated as the integral of the product of I_d and V_{ds} during the time which the device was switched [24].

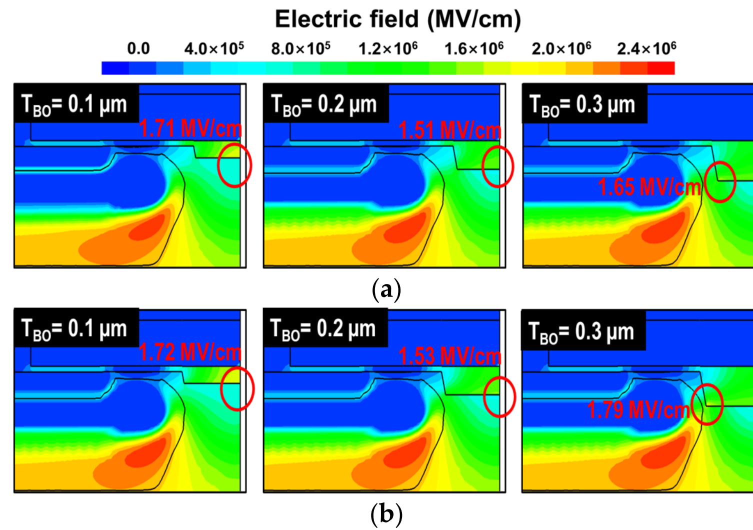

Figure 6. Electric field distribution of the 1.2 kV SiC MOSFETs with the buried oxides in the off state (V_{DS} = 1200 V) with (**a**) a W_{BO} of 0.4 and (**b**) a W_{BO} of 0.5 µm.

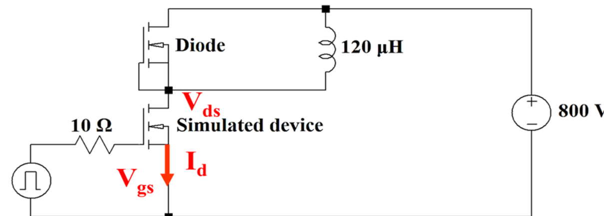

Figure 7. Circuit for switching simulations to compare the E_{total} of the device with the conventional structure and the device with the buried oxide under optimal conditions (W_{BO} = 0.3 and T_{BO} = 0.3 µm).

Figures 8 and 9 are the turn-on and turn-off switching characteristics of the 1.2 kV SiC MOSFETs with the conventional structure and the device with the buried oxide under optimal conditions (W_{BO} = 0.3 and T_{BO} = 0.3 µm), respectively. The V_{gs}, V_{ds} and I_d of the device with the buried oxide (W_{BO} = 0.3 and T_{BO} = 0.3 µm) vary more sharply during the switching process than the device with the conventional structure. Because the device with the buried oxide (W_{BO} = 0.3 and T_{BO} = 0.3 µm) has lower Q_{GD} than the device with the conventional structure, the device with the buried oxide (W_{BO} = 0.3 and T_{BO} = 0.3 µm) has fast rates of charge and discharge [5–7]. The device with the buried oxide (W_{BO} = 0.3 and T_{BO} = 0.3 µm) has lower power dissipated during the switching process than the device with the conventional structure.

The electrical characteristics of the 1.2 kV SiC MOSFETs with the conventional structure and the device with the buried oxide (W_{BO} = 0.3 and T_{BO} = 0.3 µm) are summarized in Table 2. The $R_{on,sp}$, Q_{GD} and $E_{ox,max}$ of the device with the buried oxide (W_{BO} = 0.3 and T_{BO} = 0.3 µm) are 4.71 mΩ·cm^2, 1.61 nC and 1.50 MV/cm, respectively. The device with the buried oxide (W_{BO} = 0.3 and T_{BO} = 0.3 µm) showed a 46.11% decrease in Q_{GD}, a 30.88% decrease in $E_{ox,max}$ and only a 6.10% increase in $R_{on,sp}$ compared to the device with the conventional structure. In addition, the E_{total} of the 1.2 kV SiC MOSFET with the buried oxide (W_{BO} = 0.3 and T_{BO} = 0.3 µm) is lower than the device with the conventional structure. The E_{total} of the device with the buried oxide (W_{BO} = 0.3 and T_{BO} = 0.3 µm) is 39.49 µJ, which is 20.84% lower than that of the device with the conventional structure. These results demonstrate that buried oxide can improve the switching characteristics of 1.2 kV SiC MOSFETs.

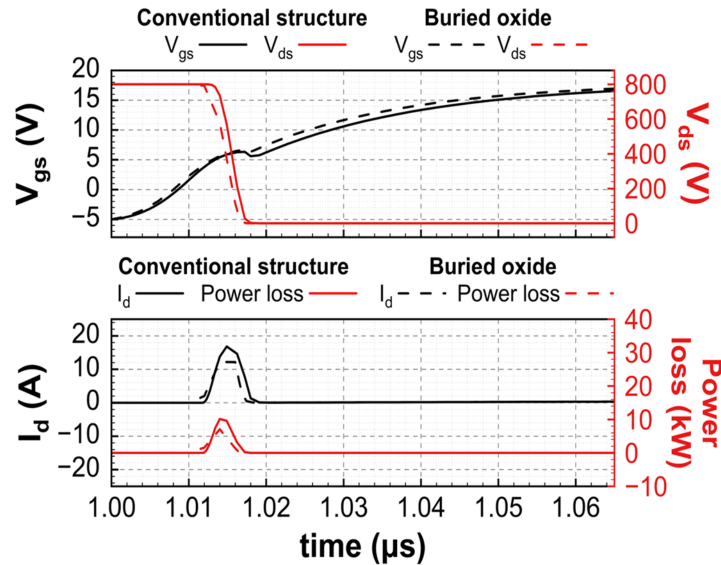

Figure 8. The turn-on switching characteristics of the 1.2 kV SiC MOSFETs with the conventional structure and the device with the buried oxide under optimal conditions (W_{BO} = 0.3 and T_{BO} = 0.3 μm).

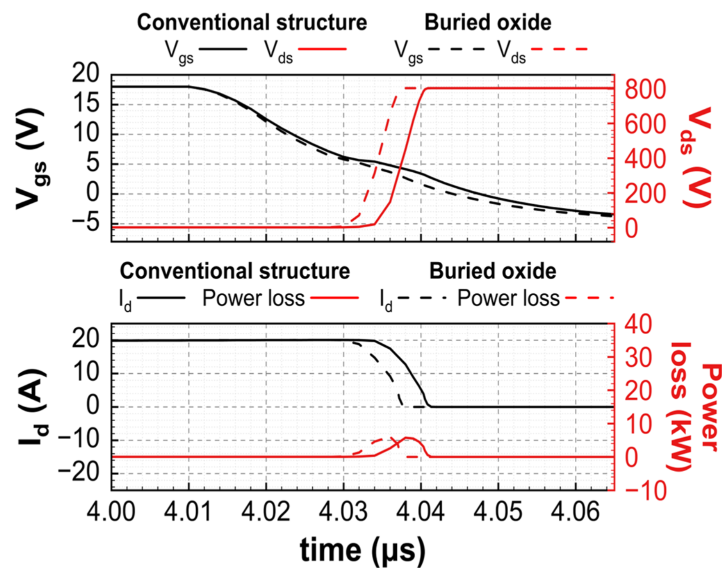

Figure 9. The turn-off switching characteristics of the 1.2 kV SiC MOSFETs with the conventional structure and device with the buried oxide under optimal conditions (W_{BO} = 0.3 and T_{BO} = 0.3 μm).

Table 2. Comparisons of the electrical characteristics of the 1.2 kV SiC MOSFETs with the conventional structure and device with the buried oxide under optimal conditions (W_{BO} = 0.3 and T_{BO} = 0.3 μm).

Electrical Characteristics	The Device with the Conventional Structure	The Device with the Buried Oxide (W_{BO} = 0.3 and T_{BO} = 0.3 μm)
$R_{on,sp}$ [mΩ·cm^2]	4.44	4.71
BV [V]	1677	1688
Q_{GD} [nC]	2.99	1.61
$E_{ox,max}$ [MV/cm]	2.17	1.50
E_{total} [μJ]	49.89	39.49

4. Conclusions

The 1.2 kV SiC MOSFET with the buried oxide was introduced to improve the switching characteristics of the device by reducing the Q_{GD}. By analyzing the $R_{on,sp}$, Q_{GD} and

$E_{ox,max}$ of the devices with the buried oxides according to the W_{BO} and T_{BO}, it was shown that the device with the buried oxide has the best performance when the W_{BO} and T_{BO} are 0.3 and 0.3 μm, respectively. The $E_{ox,max}$ and E_{total} of the device with the buried oxide (W_{BO} = 0.3 and T_{BO} = 0.3 μm) were 1.50 MV/cm and 39.49 μJ, resulting in 30.88% and 20.84% reductions compared to those with the conventional structure. The $R_{on,sp}$ of the device with the buried oxide (W_{BO} = 0.3 and T_{BO} = 0.3 μm) increased by only 6.10% compared to that of the device with the conventional structure.

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