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An All-Digital Timing Mismatch Calibration Algorithm Based on Reference Channel for TIADC

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Abstract: This paper proposes an all-digital calibration algorithm that utilizes a reference channel to suppress the timing mismatch in the Time-Interleaved Analog-to-Digital Converter (TIADC). The output of the reference channel is aligned with each sub-channel in turn, therefore enabling the simultaneous sampling and conversion of the same input signal. First, the statistical characteristics across the channels are employed for estimating the timing mismatch; then, by comparing the output difference between the reference channel and the sub-channels that are sampled simultaneously, the deviation of the derivator can be calibrated. Finally, combining both calibration results yields an accurate final output. This proposed algorithm provides an effective solution to improve TIADC performance in high-speed data acquisition systems. The proposed architecture is applied to a 12-bit 2.4 GS/s four-channel TIADC model, and then its effectiveness is verified. The simulation results exhibit that the Effective Number Of Bits (ENOB) at an input signal frequency of 984 MHz shows a remarkable improvement from 6.88 bits to 11.92 bits. The effectiveness of this technique is also demonstrated through the off-chip calibration of a commercial 12-bit four-channel 2 GS/s TIADC using a 680 MHz input signal that is based on the actual chip results.

Keywords: all-digital calibration; time-interleaved analog-to-digital converter; timing mismatch; reference channel; derivator

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1. Introduction

The analog-to-digital converter is a bridge that is applied to convert analog signals into discrete signals [1]. It is widely used in various fields, such as wireless communication, electronic radar, medical equipment, etc. With the progress of the time, the demand for ADC is growing. The essential criteria for ADC are higher precision, higher speed, lower power consumption, etc. It is difficult for a single-structure ADC to incorporate all these three factors in the existing technologies. Fortunately, TIADC can solve this problem effectively [2]. The TIADC can double the sampling rate of the whole ADC, and it can easily reach the sampling rate of 1 GS/s [3].

The TIADC is composed of M sub-channels. Due to the manufacturing process, layout routing, temperature, voltage, and other such factors, mismatches between the sub-channels will occur, such as offset mismatch, gain mismatch, and timing mismatch [3]. Indeed, the degradation of the Signal-to-Noise Ratio (SNR) and Spurious Free Dynamic Range (SFDR) of the output signal are most probably connected to these mismatches. The system as a whole cannot satisfy the demands for high precision and high speed unless these errors

are calibrated accurately. The common calibrations for offset and gain mismatches involve the accumulation and averaging of the input signal, and this is followed by its subtraction from the original signal. This approach is both straightforward and efficient [4]. The calibration of timing mismatch is the most challenging compared to other mismatches [2]. Therefore, the architecture proposed in this paper was mainly designed to solve the timing mismatch problem.

The calibration of timing mismatches can be accomplished through methodologies that are akin to those employed in analog loop calibration. The analog loop calibration method primarily involves filtering the TIADC sampling clock, and it is coupled with the adjustment of clock phases through the observation of output discrepancies in the digital domain for each sub-ADC channel. This procedure serves to effectively eliminate sampling timing mismatches [5,6]. Ref. [5] introduced a kind of foreground calibration technology based on an analog auxiliary circuit, which predominantly depended on the filtration efficacy of the analog domain filter circuit with respect to the clock signal. However, this method exhibited significant limitations, and its calibration performance was greatly influenced by temperature variations, process variations, and voltage fluctuations. Ref. [6] introduced a coarse adjustment technique for an analog variable delay line. Nonetheless, the fixed and coarse step sizes in this method imposed limitations on its effective adjustment range, as discerned from experimental analysis.

In contrast, all-digital calibration technology offers high reliability and powerful portability advantages, therefore effectively addressing the aforementioned issues. Several methodologies have been developed to address timing mismatch calibration within an all-digital domain. The investigations of all-digital calibration structures are mainly focused on two parts: the estimation method and the compensation method.

Thereinto, the predominant error estimation methodologies entail the utilization of the cross-correlations among sub-channels [2,3,7–12], or the introduction of a reference channel [13–16]. Based on the correlations among sub-channels, a complex computational matrix is commonly constructed. For example, Ref. [9] introduced an estimation methodology that employs signal modulation for the construction of an error coefficient matrix. Nevertheless, a notable limitation was observed in terms of the sluggish convergence rates (110 k) and constraints associated with finite input bandwidths. Please note that these methods that are predicated on signal modulation or Hadamard matrix operations are infrequently employed in practical applications due to their elevated computational intricacy. Calibration structures that are predicated on reference channels commonly exhibit relative simplicity. The estimation process can be construed as the assessment between a designated sub-channel and the reference channel. The calibration procedure can be delineated as a specialized form of a dual-channel calibration structure, i.e., one that is impervious to the influence of channel count expansion. Notably, this configuration is frequently characterized by diminished hardware consumption. In the paradigm of sub-channel cross-correlation, the escalation in the number of channels engenders an exponential amplification in the complexity of the formulated system of error functions. This not only augments the intricacy of design but also imparts a substantial inefficiency in terms of hardware utilization. Ref. [14] proposed an estimation methodology, one which entailed the application of a high-pass filter for the processing of input slopes that pertained to both the sub-ADC and the reference ADC. However, the reference channel necessitated a significant degree of precision, thus resulting in substantial hardware consumption with many multiplication–addition units in the usage of a high-precision filter case. Additionally, the calibration performance gradually deteriorates with increasing frequency, which is a common issue faced by most calibration structures [3,13–15]. Typically, increasing the order of the filter and parallel correlation derivative [6] was employed to mitigate this deterioration, but it inevitably led to an increase in hardware consumption. Ref. [16] proposed an innovative split-based structure. This design segregated an M-channel TIADC into two segments that featured mutually co-prime operating frequencies. At each sampling instance, each segment actively provides a sub-ADC channel as a reference for the other. The utilization

of the difference in the outputs from the dual paths serves as a new thought for actively extracting the temporal misalignment information between channels. Ref. [17] proposed a methodology for error computation based on the detection of the monotonic trends in the sampled data from sub-channels and reference channels, whereby they then subsequently applied cumulative difference accumulation. It is noteworthy that this structural approach eliminates the necessity for any multiplication or division operations. However, there have only been a few reports about timing mismatch calibration techniques based on reference channels, and their effectiveness needs further verification and improvement.

Most compensation methods rely on either filtering techniques [18–21] or Taylor expansion [11,22,23]. Numerous structures of the commonly employed filter are subjects of the study, with a substantial portion of researchers directing their investigations toward fractional-delay filters and perfect-reconstruction filters. Ref. [19] introduced a methodology that employed fractional filters for the phase adjustment in the input signal. Ref. [20] introduced a methodology that utilized the perfect reconstruction filters to efficaciously rectify errors in reconstructed signals. However, this approach consumed high hardware and substantial power. In addition, the structures based on Taylor series expansion are highly regarded for their low complexity, rapid convergence, and notable efficacy, which make them equally popular. Ref. [11] utilized a Taylor series expansion to approximate the error terms within the output signal. The calibration of the errors in the output signal was achieved through the consideration of the time misalignment errors and the derivatives of the input signal. The conventional approach to optimizing the output performance and the input signal bandwidth in calibration algorithms typically relies on the degree of differentiation or the second-order differential term. However, the exponential increase in the hardware consumption has not been positively linked to the commensurate improvements in the input bandwidth.

In this paper, an all-digital calibration structure is proposed to address the aforementioned issues. A reference channel is used to extract the timing mismatch of each sub-channel. The compensation structure is formulated based on the expansion of the first-order Taylor series. The derivator which is optimized with the Richardson extrapolation is based on the first-order numerical differential of the Lagrange interpolation polynomial of the 5-point formula. The optimization of the derivator circuit's structure, as is outlined in this paper, aims to minimize the hardware consumption and the overall resource utilization. In addition, an auxiliary circuit is introduced to further enhance the output precision and performance, which improves the overall accuracy and efficiency. This design manifests attributes including the expeditious convergence, the compact hardware footprint, and the straightforward architectural framework. This paper is organized as follows. Section 2 describes the construction of the TIADC module and the merits of the proposed calibration technique. Section 3 shows the simulation results which verify the effectiveness of the technique. Section 4 is mainly used to discuss the advantages and disadvantages of the proposed algorithm as well as the direction of the future work. Finally, the conclusions are drawn in Section 5.

2. Timing Mismatch Model and Proposed Timing Mismatch Calibration Structure

Assuming that the prior calibrations with the help of a reference ADC [24] have been made for other mismatches (i.e., offset and gain mismatches), we only need to focus on the calibration of the timing mismatch. Figure 1 shows the structure of the M-channel TIADC with the reference channel. The output of the optimal M-channel TIADC system can be expressed as

$$y_i(n) = x(n \cdot MT_s + iT_s + \Delta t_i), i = 0, \cdots, M-1. \quad (1)$$

In (1), $y_i(n)$ is the sampled value of the input signal $x(n)$ at the time $t = n \cdot MT_s + iT_s + \Delta t_i$, where Δt_i represents the timing mismatch of the i^{th} sub-channel and T_s represents the sampling period. The signal $y(n)$ of the entire TIADC can be expressed as

$$y(n) = \sum_{i=0}^{M-1} y_i(n) = \sum_{i=0}^{M-1} x(n \cdot MT_s + iT_s + \Delta t_i). \tag{2}$$

In the actual circuit, the timing mismatch is much smaller than T_s, $\Delta t_i = r_i T_s, r_i \ll 1\%$. r_i represents the timing mismatch coefficient of the i^{th} sub-channel.

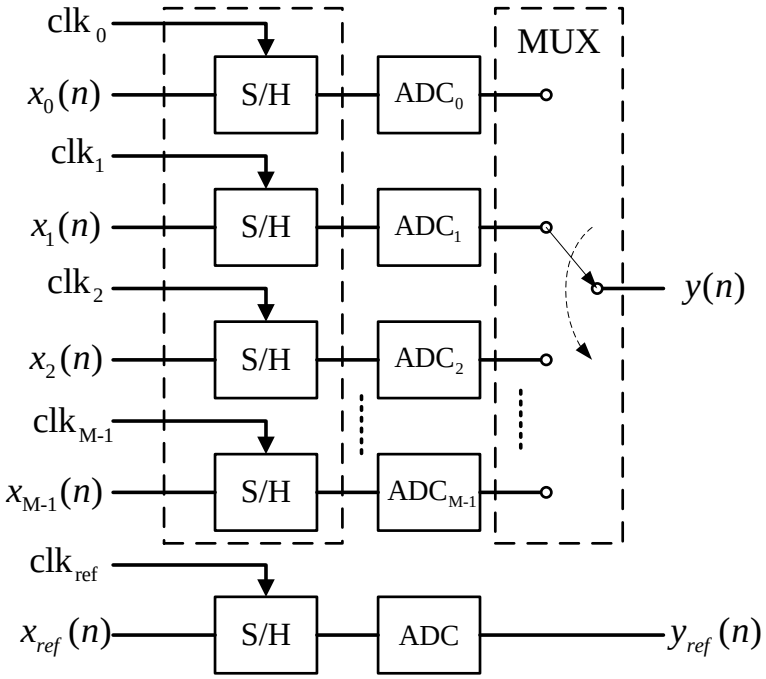


Figure 1. The structure of the M channel TIADC. clk_{M-1} is the sample clock of the sub-ADC. clk_{ref} is the sample clock of the reference ADC. S/H stands for the sample holder.

2.1. Timing Mismatch Compensation

In practice, the timing mismatch is typically negligible in comparison to the sampling period. As a result, the first-order Taylor series is employed for approximation [6]. The function of the timing mismatch compensation $\hat{y}_i(n)$ on the i^{th} sub-channel is expressed as

$$\hat{y}_i(n) \approx y_i(n) - \Delta t_i y_i'(n), \tag{3}$$

where $y_i'(n)$ represents the differential value of the output from the i^{th} sub-channel. The deviation coefficients of the derivator exhibit frequency-dependent variations during the execution of the differentiation operation [25]. Therefore, the relationship between the output of the derivator ($D_i(n)$) and the ideal derivative ($y_i'(n)$) can be mathematically expressed as

$$D_i(n) = g_D \cdot y_i'(n), \tag{4}$$

where g_D represents the deviation coefficient of the derivator. (3) is rewritten as

$$\hat{y}_i(n) \approx y_i(n) - \frac{1}{g_D} \cdot \Delta t_i \cdot D_i(n). \tag{5}$$

The deviation coefficient of the derivator is solely dependent on the frequency. Figure 2 shows the implementation architecture of the timing mismatch calibrations.

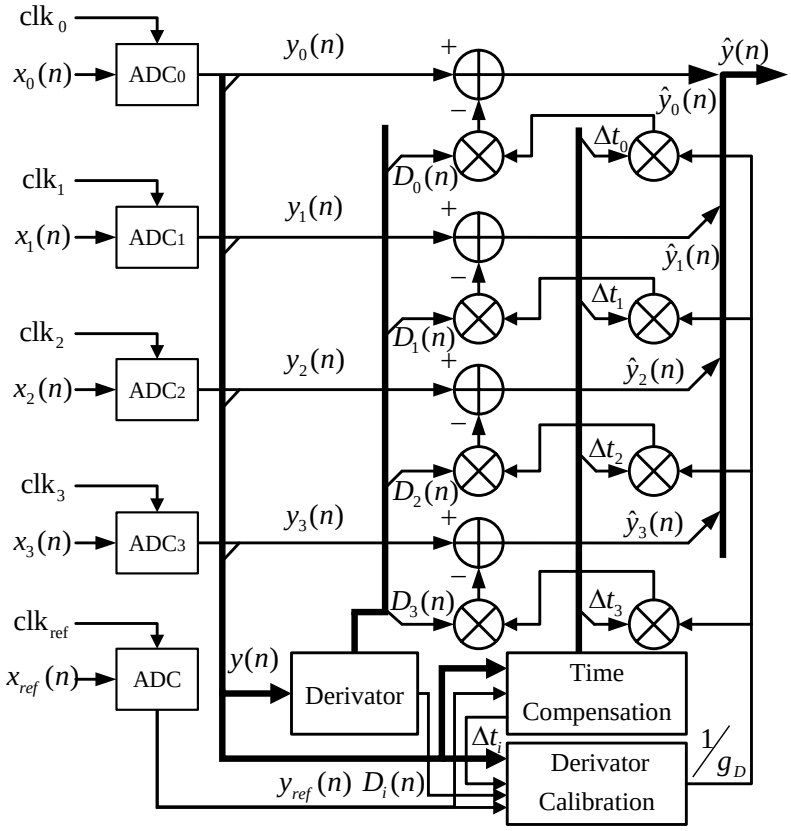


Figure 2. Proposed calibration system of the timing mismatch and the derivator deviation coefficient with the reference channel.

2.2. Estimation Architecture

In this sub-section, this paper presents an adaptive estimation method that utilizes the first-order statistics to address the timing mismatches. The estimation model is based on a four-channel model with an additional channel for reference. The sampling frequency of TIADC is f_s. The sampling frequency of the sub-channel is $f_s/4$. The sampling frequency of the reference channel is $f_s/5$. The sampling values of the reference channel are aligned with each sub-channel in turn. The sampling timing of each sub-channel ADC and the reference channel ADC is illustrated in Figure 3.

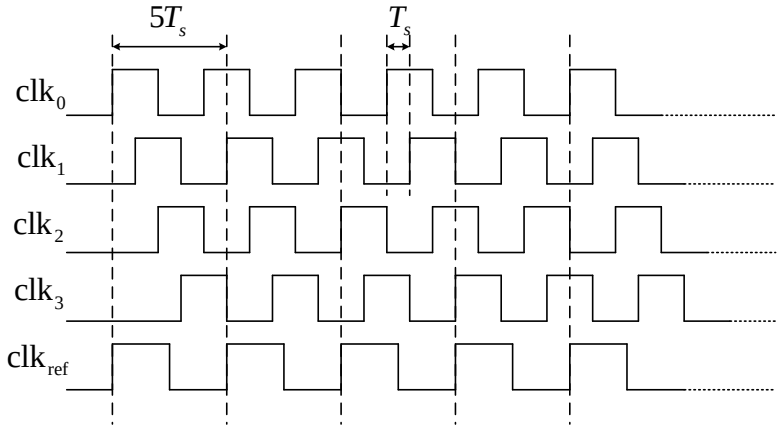


Figure 3. TIADC calibration sampling timing.

The specific sampling sequences are extracted through down-sampling. The output sequence $y_{i\_d}(n)$ of the i^{th} sub-channel after down-sampling is expressed as

$$\begin{aligned} y_{i\_d}(n) &= y_i(5n-5+i) \\ &= x(n \cdot 20T_s - (20-5i)T_s + \Delta t_i). \end{aligned} \tag{6}$$

The corresponding output sequence $y_{ref\_di}(n)$ of the reference channel needs to be extracted accordingly, which can be formulated as

$$\begin{aligned} y_{ref\_di}(n) &= y_{ref}(4n-4+i) \\ &= x(n \cdot 20T_s - (20-5i)T_s), \end{aligned} \tag{7}$$

where $y_{ref}(n)$ represents the output of the reference channel, which can be expressed as

$$y_{ref}(n) = x(n \cdot 5T_s). \tag{8}$$

The estimation of the timing mismatch requires the utilization of the cross-correlation function between the sub-channel and the reference channel. The reference channel output sequence $y_{ref\_dk}(n)$ ($k = mod(i+2, 4)$ for $i = 0, \cdots, 3$, $mod()$ stands for modulus function) of the corresponding sub-channel can be denoted as

$$y_{ref\_dk}(n) = \begin{cases} y_{ref\_d\{mod(i+2,4)\}}(n-1), i = 0, 1 \\ y_{ref\_d\{mod(i+2,4)\}}(n-0), i = 2, 3, \end{cases} \tag{9}$$

the cross-correlation function $R_{y_{i\_d}(n-1)y_{ref\_dk}(n-1)}$ between the sub-channel and the reference channels after down-sampling, i.e., $y_{i\_d}(n-1)$ and $y_{ref\_dk}(n-1)$, respectively, is expressed as

$$\begin{aligned} R_{y_{i\_d}(n-1)y_{ref\_dk}(n-1)} &= E(y_{i\_d}(n-1) \cdot y_{ref\_dk}(n-1)) \\ &= R_{xx}(10T_s - \Delta t_i), \end{aligned} \tag{10}$$

where $E(\cdot)$ expresses the mathematical expectation. It is realized through Modified Moving Average (MMA) [23], which is shown in Figure 4. It is expressed as

$$y[n] = (1-\mu)y[n-1] + \mu x[n], \tag{11}$$

where $y[n]$ and $x[n]$ are the output and the input, and μ represents a constant smoothing factor. The recursive calculation of the average output $y[n]$ relies on both the preceding result $y[n-1]$ and the current input term $x[n]$. The (11) is commonly utilized in Digital Signal Processing (DSP), and the recursive calculation of the computing moving averages. In terms of the hardware implementation, opting for a 2^{-k} sample period—with k being any positive integer is proved to be advantageous since multiplying the signal by μ can be efficiently accomplished via the proper arithmetic shifting by k bits instead of employing a hardware multiplier. $R_{xx}(10T_s - \Delta t_i)$ expresses the cross-correlation of $x(n + \Delta t_i)$ and $x(n + 10T_s)$. By the first-order Taylor series approximation, it could be approximately expressed as

$$R_{xx}(10T_s - \Delta t_i) \approx R_{xx}(10T_s) - \Delta t_i \cdot R'_{xx}(10T_s), \tag{12}$$

where $R'_{xx}(10T_s)$ is the derivative of the autocorrelation of the input signal. It could be expressed as

$$\begin{aligned} R'_{xx}(10T_s) &= E(x'(n)x(n-10T_s)) \\ &= E(y'_{ref}(n)y_{ref}(n-2)), \end{aligned} \tag{13}$$

where $y'_{ref}(n)$ is the derivative of the reference signal. From (10) and (12), the cross-correlation value between $y_{i\_d}(n-1)$ and $y_{ref\_dk}(n-1)$ is expressed as

$$R_{y_{i\_d}(n-1)y_{ref\_dk}(n-1)} \approx R_{xx}(10T_s) - \Delta t_i \cdot R'_{xx}(10T_s). \tag{14}$$

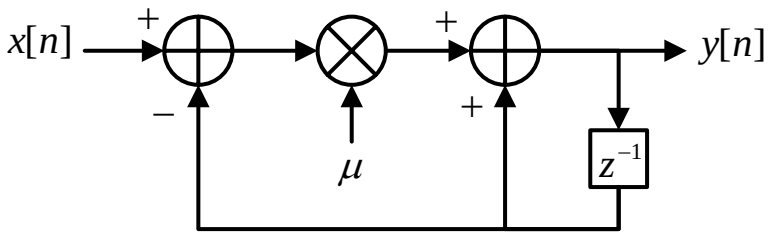


Figure 4. The Modified Moving Average (MMA) filter. z^{-1} stands for the D flip-flop.

Obviously, the cross-correlation value $R_{y_{i\_d}(n-1)y_{ref\_dk}(n)}$ between $y_{i\_d}(n-1)$ and $y_{ref\_dk}(n)$ is expressed as

$$R_{y_{i\_d}(n-1)y_{ref\_dk}(n)} \approx R_{xx}(10T_s) + \Delta t_i \cdot R'_{xx}(10T_s). \tag{15}$$

To obtain the timing mismatch, the difference of the cross-correlation values λ_{cor_i} can be derived by subtracting the two equations that is mentioned above (i.e., (14) and (15)):

$$\lambda_{cor\_i} = 2\Delta t_i \cdot R'_{xx}(10T_s), \tag{16}$$

which is in direct proportion to Δt_i.

Approximately, the timing mismatch Δt_i can be represented as

$$\Delta t_i = \frac{\lambda_{cor\_i}}{2R'_{xx}(10T_s)}. \tag{17}$$

The implementation architecture of (17) is shown in Figure 5.

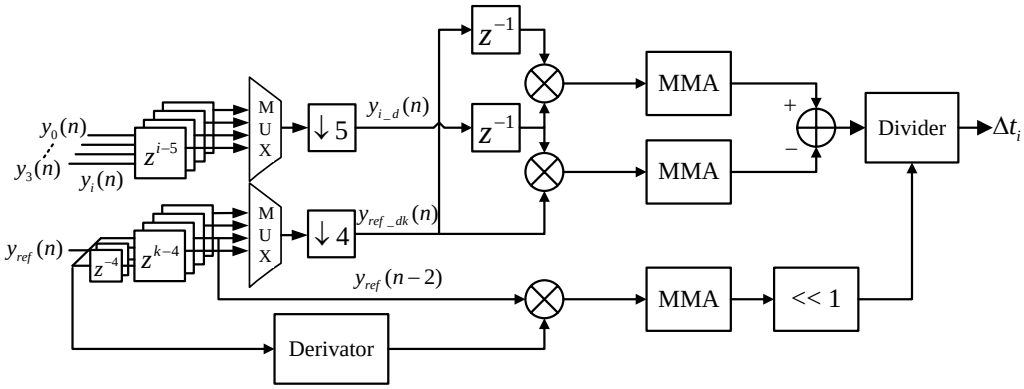


Figure 5. Proposed architecture of the timing mismatch.

2.3. Derivator Architecture

The traditional derivator is essentially a filter, which consists of the multiplier and the delay register units. Considering that the differentiation effect of the derivator increases with its order, it inevitably consumes a large amount of the aforementioned filters to obtain a sufficiently high order (e.g., [2,6]) and meet the requirements of the design. This paper

proposes a simplified structure of the derivator. According to the Lagrange interpolation polynomial, the first-order numerical differentiation can be expressed as [26]

$$D_0(n,1) = \frac{y(n-2) - 8y(n-1) + 8y(n+1) - y(n+2)}{12}, \tag{18}$$

where $D_0(n,1)$ represents the output of the derivator. By the usage of the Taylor series expansion, the terms $y(n-2)$, $y(n-1)$, $y(n+1)$, and $y(n+2)$ can be effectively expanded. Consequently, (18) can be elegantly reformulated as

$$D_0(n,1) \approx y'(n) - \frac{3}{5!}y^{(5)}(n) - \frac{15}{7!}y^{(7)}(n) + \cdots, \tag{19}$$

where $y'(n)$ is the derivative of $y(n)$, similarly, $y^{(5)}(n)$ and $y^{(7)}(n)$ are the fifth-order and seventh-order derivative of $y(n)$, respectively. To enhance the differentiation effect of the derivator, the Richardson extrapolation is employed to construct the higher-order approximation formulas [27]. It estimates the value of the target function by approximation with different step lengths. The first order numerical differential formula $D_m(n,h)$ from a higher-precision extrapolation can be expressed as

$$D_m(n,h) = \frac{4^{m+1}D_{m-1}(n,\frac{h}{2}) - D_{m-1}(n,h)}{4^{m+1}-1}, \tag{20}$$

where h represents the sampling step and m represents the number of the iterations. As the number of the iterations increases, the output of the derivator gradually converges to the ideal derivative value. The following expression for the output of the derivator $D_1(n,2)$ can be derived by the single iteration:

$$D_1(n,2) = \frac{16D_0(n,1) - D_0(n,2)}{15}, \tag{21}$$

where $D_0(n,2)$ is expressed as [26]

$$D_0(n,2) = \frac{y(n-4) - 8y(n-2) + 8y(n+2) - y(n+4)}{24}. \tag{22}$$

Subsequently, $D_1(n,2)$ can be obtained from the Taylor series expansions of $D_0(n,1)$ and $D_0(n,2)$, as is described below.

$$D_1(n,2) \approx y'(n) + \frac{3}{7!}y^{(7)}(n) + ... \tag{23}$$

By comparing (19) and (23), the application of the Richardson extrapolation formula eliminates a certain amount of higher-order derivatives (e.g., $y^{(5)}(n)$) and enhances the accuracy of the derivator so that the compensation performance can be improved effectively. By substituting (18) and (22) into (21), the expression can be derived as follows:

$$\begin{aligned} D_1(n,2) = &\{2^4 \cdot [(y(n-2) - y(n+2)) \\ &- 2^3 \cdot (y(n-1) - y(n+1))] \\ &- [y(n-4) - y(n+4)) \\ &- 2^3 \cdot (y(n-2) - y(n+2))]\} \cdot \frac{1}{180}. \end{aligned} \tag{24}$$

The implementation architecture of (24) is shown in Figure 6.

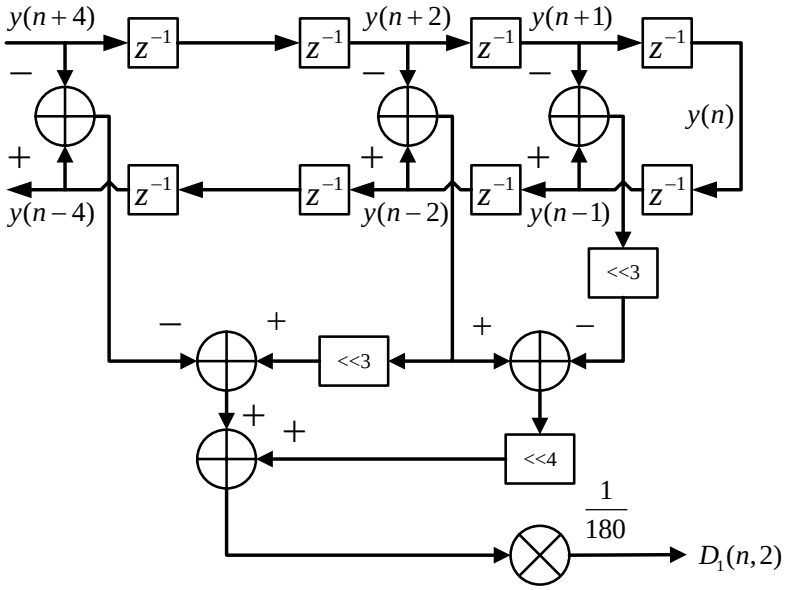


Figure 6. Proposed architecture of the derivator.

2.4. Derivator Calibration

The linearity of the derivator gradually deteriorates with the increase of the frequency. The non-negligible deviation between the actual and ideal output of the derivative significantly impacts the accuracy of the final compensation and calibration. To compensate for the output deviation at the high-frequency cases, this paper presents a straightforward structure for the calibration of the derivator.

The deviation coefficient of the derivator is solely dependent on the frequency and is unrelated to any channel. Take Channel 3, for example. The sequence $y_{ref\_d3}(n)$ after down-sampling is selected. It is aligned with Channel 3, which is written as

$$y_{ref\_d3}(n) = y_{ref}(4n-1) = x(n \cdot 20T_s - 5T_s). \tag{25}$$

Similarly, the sampling sequence $y_{3\_d}(n)$ that is corresponding to Channel 3 is expressed as

$$y_{3\_d}(n) = y_3(5n-2) = x(n \cdot 20T_s - 5T_s + \Delta t_3). \tag{26}$$

The timing mismatch has been rectified after the compensation with the Taylor series, whereas the derivator still exhibits a frequency-dependent bias coefficient. The corresponding output of the derivator $D_{3\_d}(n)$ is written as

$$D_{3\_d}(n) = g_D \cdot y'_{3\_d}(n) = g_D \cdot x'(n \cdot 20T_s - 5T_s + \Delta t_3). \tag{27}$$

Using Taylor series expansion and combining (25) and (27), the following results can be derived as

$$y_{ref\_d3}(n) = y_{3\_d}(n) - \Delta t_3 \cdot \frac{D_{3\_d}(n)}{g_D}. \tag{28}$$

The expectation of the deviation coefficient can be expressed as

$$\begin{aligned} \frac{1}{g_D} &= \frac{1}{N} \cdot \sum_{n=1}^{N} \left(\frac{y_{3\_d}(n) - y_{ref\_d3}(n)}{\Delta t_3 \cdot D_{3\_d}(n)}\right) \\ &= \frac{E(y_{3\_d}(n)) - E(y_{ref\_d3}(n))}{E(\Delta t_3 \cdot D_{3\_d}(n))}, \end{aligned} \tag{29}$$

where the expectation of $E(y_{3\_d}(n))$, $E(y_{ref\_d3}(n))$ and $E(\Delta t_3 \cdot D_{3\_d}(n))$ are constants on account of the input signal $x(n)$ that is band-limited. The calibration architecture of the derivator's deviation according to (29) is shown in Figure 7.

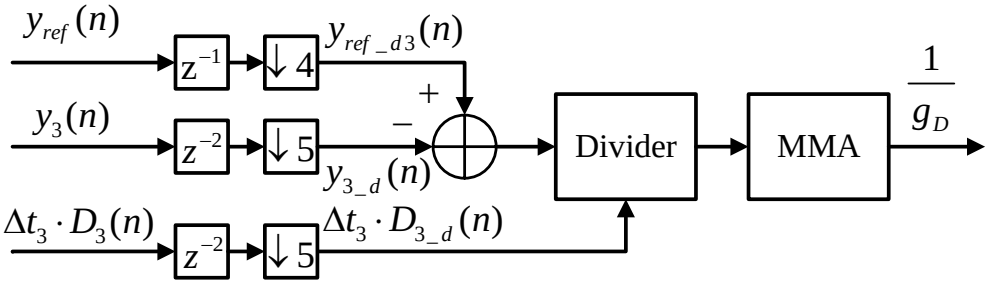


Figure 7. Proposed architecture of the derivator calibration.

3. Performance Verification

To verify the validity of the technology, the ideal output of the TIADC is systematically generated through the MATLAB. Different timing mismatches are deliberately introduced to the outputs of each channel, and conventional simulations are strictly conducted using the MATLAB environment. The TIADC output signals, deviations across all channels, and the comprehensive calibration architecture are synthesized through the MATLAB 2023a software (Section 3.1). To enhance the validation of the algorithm's reliability, this paper employs a commercial TIADC from our company as the data source for evaluating the proposed calibration algorithm (Section 3.2). The design of this TIADC is accomplished through the Cadence Virtuoso ic617 software. The effective calibration results also serve to illustrate the reliability of the algorithm.

3.1. Simulation

In this section, a 12-bit 2.4 GS/s four-channel TIADC model with the timing mismatches is constructed to verify the effectiveness of the proposed estimation and the compensation architecture. The sampling frequency of each subchannel is 600 MS/s and the reference channel is 480 MS/s.

Figure 8 shows the spectra of a single-tone signal with a frequency of $0.41f\_s$. The timing mismatches of the four channels $[\Delta t\_0, \Delta t\_1, \Delta t\_2, \Delta t\_3]$ are set as [1‰, −2‰, 3‰, −4‰]. After calibration, the harmonics that are caused by the timing mismatches decrease substantially. The SFDR and SNR increase from 43.81 dB and 43.17 dB to 89.39 dB and 73.50 dB, respectively.

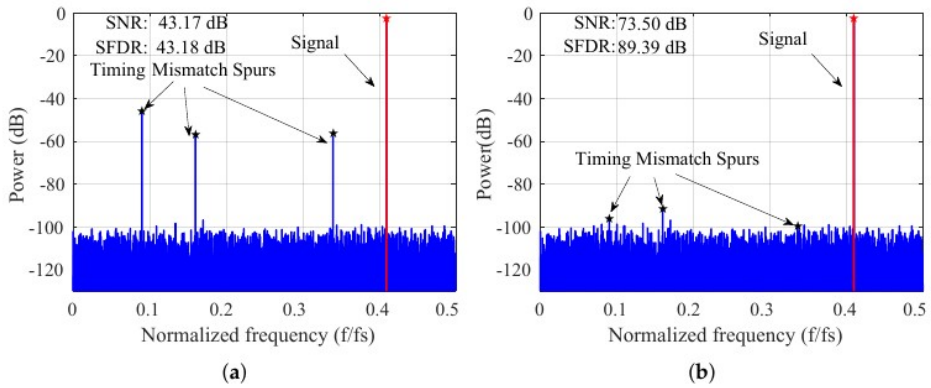


Figure 8. The spectra of four-channel TIADC output for a single-tone signal input of $0.41f_s$ (**a**) before calibration and (**b**) after calibration.

Near the boundary of the Nyquist frequency band, the performance of the derivator significantly decreases, which contributes to a substantial drop in the output efficiency

(Figure 9a). Compared to the uncalibrated case, the SFDR (SNR) after all-digital timing mismatch calibration without the derivator calibration module increased from 42.85 dB (42.21 dB) to 64.08 dB (62.93 dB), indicating a modest improvement. In contrast, the circuit that introduces the derivator-assisted calibration (Figure 9) raises the SFDR and SNR to 86.96 dB and 73.67 dB, as illustrated in Figure 9b. This brings substantial improvements to derivative calibration.

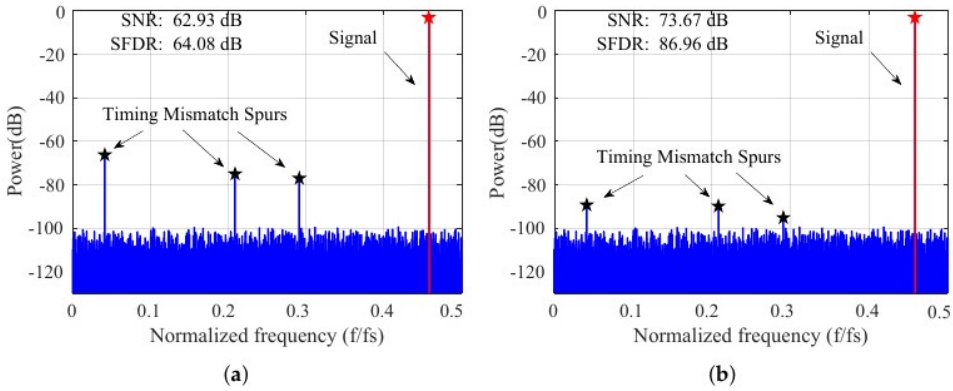


Figure 9. The spectra of four-channel TIADC output for a single-tone signal input of $0.45f_s$ (**a**) without the derivator calibration and (**b**) with the derivator calibration.

Figure 10a shows the convergence rate of the timing mismatches. In the actual simulation, the channel rotation method is used to estimate the timing mismatch of each channel. It can be observed that the typical channel switches after approximately 300 samples. The convergence rate of the derivator's deviation coefficient is shown in Figure 10b, and the convergence samples are approximately 2000. The entire system reaches convergence at approximately 3200 samples. The deviation value $1/g_D$ is around 1.075 when the f_{in} is $0.41f_s$.

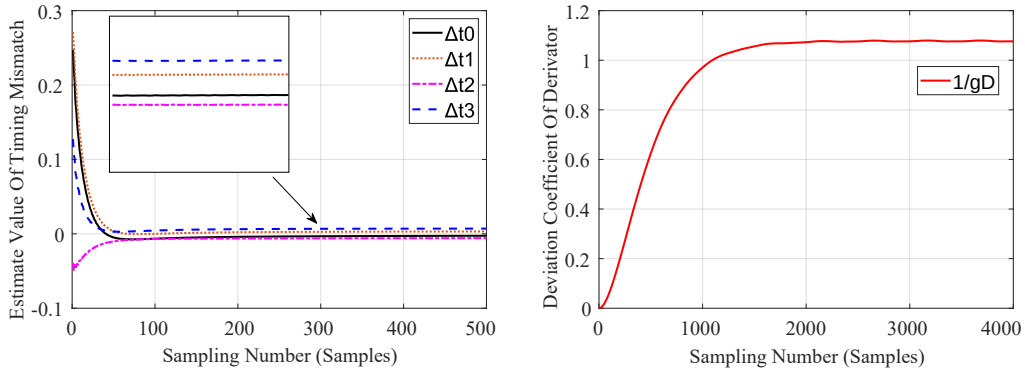
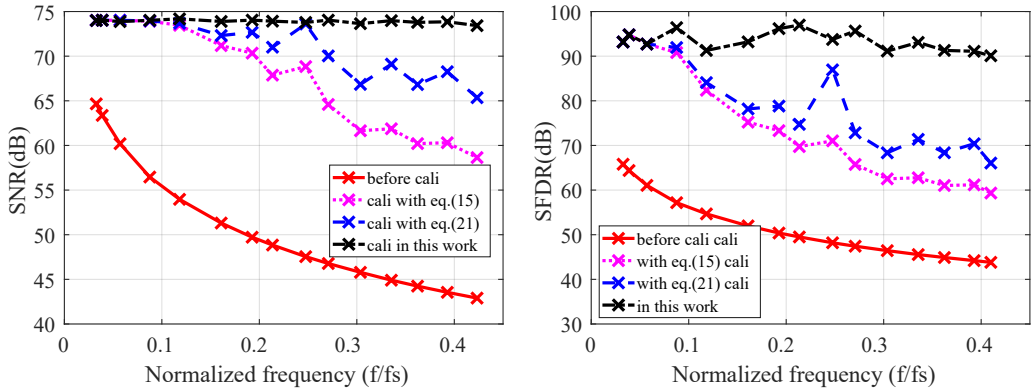


Figure 10. (**a**) The convergence rate of the time mismatch error. (**b**) The convergence rate of the derivator's deviation coefficient.

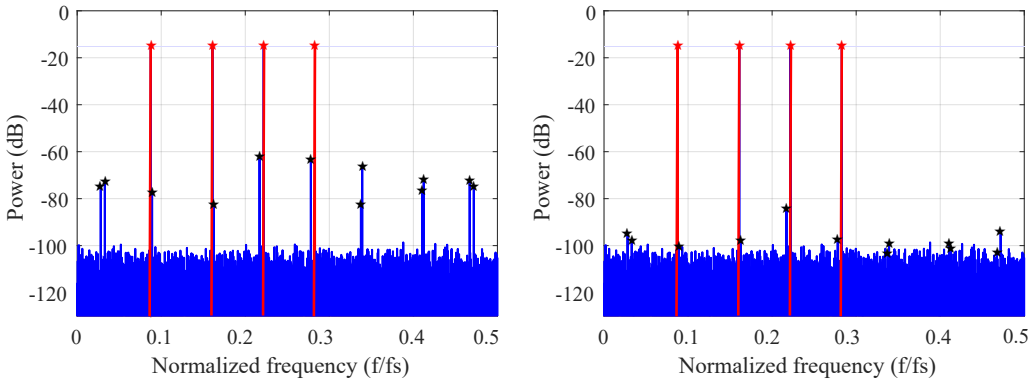
Figure 11 shows a significant improvement of the SNR and SFDR under different frequencies. The output performance shows little difference at the low frequencies, but the unmodified structure exhibits a noticeable decrease in performance at the higher frequencies. Moreover, the proposed calibration architecture effectively maintains a stable and high level of the SNR and SFDR in almost the entire Nyquist domain.



(**a**) (**b**)

Figure 11. (**a**) The SNR and (**b**) SFDR performance versus different input frequencies.

Figure 12 shows the spectra of the four-channel TIADC output for the multi-tone signal input. The frequencies in Figure 12 are $[0.088f_s, 0.161f_s, 0.222f_s, 0.283f_s]$. As can be seen, the spurs from the timing mismatches are effectively suppressed.



(**a**) (**b**)

Figure 12. The spectra of four-channel TIADC output for multi-tone signal input (**a**) before calibration and (**b**) after calibration. (The red line signifies the signal, and the blue line signifies the spur).

3.2. Hardware Implementation and Validation

The Verilog design is synthesized to a gate-level netlist by Synopsys Design Compiler (DC) tool that targets the 28 nm technology. The design target of Application Specific Integrated Circuit (ASIC) for the calibration structure is a 12-bit 2.4 GS/s four-channel TIADC. The synthesis result shows that the area of the proposed structure is 0.03 mm^2.

The off-chip calibration of a commercial four-channel 12-bit TIADC is performed on the Field Programmable Gate Array (FPGA). The JESD204B interface is also applied for the high-speed signal transmission between the TIADC and the FPGA (VCU108 from Xilinx). The input signal is a 680 MHz sine wave sampled at the frequency of 2 GS/s. Figure 13 shows the test platform that is comprised of the TIADC chip, the clock chip, the Serial Peripheral Interface (SPI) controller, and the FPGA circuit board.

Based on the measured data from the 2 GS/s four-channel 12-bits TIADC, the proposed method is used for the off-chip calibration. The input is a single-tone signal with a frequency of 680 MHz (=0.34f_s). Figure 14 shows the off-chip calibration results of the commercial TIADC. It can be seen that the spurs caused by the timing mismatch at the frequencies of $0.09f_s$, $0.16f_s$ and $0.41f_s$ are reduced by 15.09 dB, 26.67 dB, and 12.65 dB, respectively.

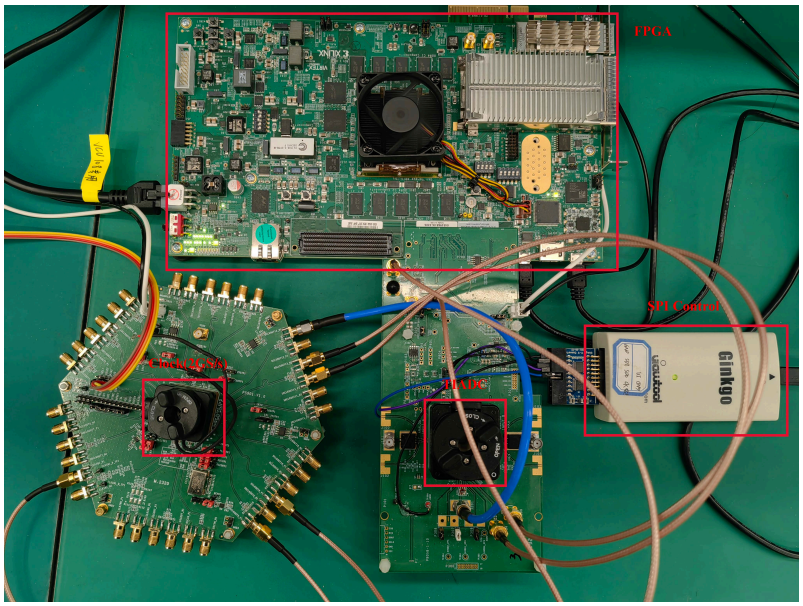


Figure 13. Experimental setup for the off-chip timing mismatch calibration of the four-channel 2 GS/s TIADC .

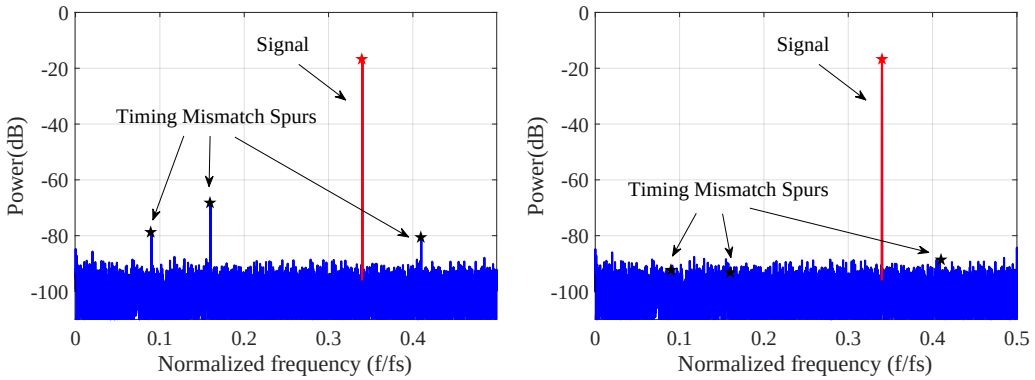


Figure 14. The off-chip calibration results of the commercial TIADC with the input signal being 680 MHz and the sampling rate being 2 GS/s (**a**) before calibration and (**b**) after calibration.

4. Discussion

Table 1 presents the other four works on the all-digital calibration techniques that have been proposed in recent years. Compared to the works of other groups [9,12], this paper presents several significant advantages over the structure with the reference channel, especially in the area consumption and the convergence speed. Compared to Ref. [28], it achieves superior calibration results while maintaining the same level of the accuracy. A significant improvement in calibration performance for the multi-frequency signals is also observed. Compared to Ref. [9], this paper presents a faster convergence speed and wider effective bandwidth. As mentioned, the techniques in Refs. [9,28,29] fail to maintain high-precision output at the high frequencies, which result in a noticeable degradation in the calibration performance. By contrast, the proposed technique solves this issue.

Relative to the calibration methodologies that have been recently reported by our group, the algorithm in this article shows significant advantages [30,31]. In contrast to the approach in Ref. [30], the feedback architecture is employed to approximate the parameters to the actual values, despite inherent stability concerns. By utilizing a feedforward calibration structure, this paper systematically enhances the stability and improves the entire performance of the calibration process. Relative to the framework in Ref. [31],

the proposed structure is characterized by its simplicity, low computational complexity, rapid convergence, and superior performance. The calibration structures in Refs. [30,31] present limited efficacy in the multi-frequency signals calibration, therefore imposing significant constraints on their practical applications. In contrast, the calibration architecture in this paper demonstrates the superior effectiveness in the context of the multi-frequency signals calibration.

Table 1. Simulation Performance Comparison.

	[9]	[28]	[29]	[30]	[31]	**This Work**
Channels	4	4	4	4	4	4
Resolution	12 bits	12 bits	6 bits	12 bits	14 bits	12 bits
Timing mismatch	$-0.012 \cdot T_s$	$-0.025 \cdot T_s$	$-0.018 \cdot T_s$	$-0.031 \cdot T_s$	$-0.015 \cdot T_s$	$-0.004 \cdot T_s$
Sample frequency	3 GS/s	\	32 GS/s	2 GS/s	3 GS/s	2.4 GS/s
Input frequency	$0.282 \cdot f_s$	$0.410 \cdot f_s$	$0.495 \cdot f_s$	$0.437 \cdot f_s$	$0.435 \cdot f_s$	$0.459 \cdot f_s$
Multi-tone input	Yes	No	No	No	No	Yes
Convergence time (samples)	15 k	110 k	24 k	1.2 k	600	3.2 k
SFDR	77.69 dB	64.10 dB	37.24 dB	85.69 dB	109.30 dB	86.96 dB
SNR	71.00 dB	62.21 dB	31.28 dB	67.96 dB	79.95 dB	73.63 dB
ENOB	11.50 bits	10.04 bits	5.44 bits	11.00 bits	12.98 bits	11.93 bits
Area	0.047 mm^2	\	0.695 mm^2	0.02 mm^2	\	0.03 mm^2

Although the inclusion of the reference channel is a notable drawback in comparison to the structure without one, it has been demonstrated to be a strong-expansible and straight structure. The application of the method from Ref. [2] to systems with more than 8 channels generates an exponential increase in hardware resource consumption at both the estimation module for derivative poly-phase filters and the matrix processing unit. However, the proposed structure in this paper can be expanded to accommodate additional channels without incurring any extra hardware consumption within the estimation module.

Given all that, this paper sufficiently validates the effectiveness of the algorithm by the co-simulation of the MATLAB and off-chip measured data. Compared with other literature [9,28,29], the all-digital calibration framework in this paper demonstrates the notable advantages in terms of convergence speed, SFDR, SNR, hardware resource efficiency, and multi-frequency signals calibration. However, the approaches involve additional channels, necessitating a more complex layout, especially concerning the clock tree. In the context of the future endeavors, the forthcoming work will involve the refinement of the existing algorithmic framework, with a particular emphasis on optimizing both the area utilization and the performance. Our calibration methodology is slated for the implementation leveraging an ASIC library.

5. Conclusions

This paper has proposed an all-digital calibration structure of the four-channel TIADC. It effectively addresses the frequency-dependent challenges in compensating for the timing mismatch calibration. Herein, we present a novel estimation method that exploits statistical regularities among individual sub-channels and a reference channel to accurately determine time mismatches. This methodology presents a streamlined architecture with swift convergence rates and robust stability, rendering it exceptionally well-suited for integration into the commercial TIADC. Additionally, an innovative compensation framework we proposed is grounded in the first-order Taylor series expansion. The derivator is refined through the utilization of the Richardson extrapolation, employing the first-order numerical differentiation of the Lagrange interpolation polynomial. The derivator auxiliary circuit is incorporated to improve the accuracy of the derivator and optimize hardware consumption. The simulation that is applied to the 12-bits 2.4 GS/s TIADC demonstrates its effective calibration performance at both the single and the multiple frequencies. The SFDR and

SNR at a specific frequency ($0.41 f_s$) present an increase of 45.58 dB and 30.33 dB, respectively. Furthermore, the effectiveness of this approach is further substantiated through the off-chip calibration based on the actual TIADC. Moreover, its versatility is manifested in having freedom from the objective restraints, such as the number of channels, input signal amplitude, input frequency, etc. The system possesses the remarkable ability to consistently maintain optimal performance even at high frequencies.

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