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A 96 dB DR Second-Order CIFF Delta-Sigma Modulator with Rail-to-Rail Input Voltage Range

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Abstract: A second-order delta-sigma modulator (DSM) is proposed for readout integrated circuits of sensor applications requiring a small area and low-power consumption. The proposed second-order CIFF DSM with the architecture of cascaded-of-integrator feedforward (CIFF) basically consists of two integrators, a 3-bit quantizer, data-weighted averaging (DWA) circuit, and clock generator. The use of the 3-bit quantizer instead of the single-bit quantizer reduces the size of the feedback capacitor in the first integrator. The 3-bit quantizer is designed based on a successive approximation register analog-to-digital converter for small area and low power implementation. Furthermore, the proposed second-order CIFF DSM has a single supply without an additional reference driver while having a wide analog input voltage range with rail to rail. The proposed second-order CIFF DSM, implemented using a 130 nm 1-poly 6-metal CMOS process with a supply of 1.5 V, has an area of 0.096 mm^2. It has a sampling frequency of 500 kHz for the implementation of an input bandwidth of 2 kHz and an oversampling ratio of 125. The measured peak signal-to-noise and distortion ratio is approximately 90 dB when the differential analog input signal has a frequency of 353 Hz and an amplitude of 1.2 Vpp. The measured dynamic range is approximately 96.3 dB.

Keywords: delta-sigma modulator; cascaded-of-integrator feedforward; 3-bit quantizer; integrator; reference driver; single supply

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1. Introduction

Recently, various sensors have been used in biomedical applications and internet-of-things (IoT) devices [1–3]. Among the various signals in the natural world, sensor devices that acquire signals such as temperature, pressure, and geometers require the acquisition of low-frequency signals, including DC signals [4–6]. As the characteristics of these sensor devices continue to be advanced, their analog output signals have high dynamic characteristics. Therefore, high-resolution analog-to-digital converters (ADCs) are required for the implementation of readout integrated circuits (ROICs) for these sensors. To reduce the power and area of the ROIC for sensors while having high resolution characteristics, successive approximation register (SAR) ADCs and delta-sigma ADCs can be used. SAR ADCs use a minimal number of analog blocks, which is advantageous for implementing low-power, small-area ADCs [7,8]. However, the area and mismatch of the digital-to-analog converter (DAC) makes it difficult to achieve high-resolution characteristics. SAR ADCs using noise shaping (NS) have been proposed as an alternative to the resolution enhancement limitations of SAR ADCs [9,10], but there are still structural difficulties in implementing resolutions above 14–16 bits. Delta-sigma ADCs typically use analog integrators with op amps, which have the disadvantage of relatively increased power consumption and area, but they have been widely used in high-performance sensor interfaces because they have

a suitable structure to achieve high resolution [1–6,11,12]. In particular, noise shaping by delta-sigma modulation (DSM) and oversampling schemes enable the implementation of high resolution.

In general, a variable gain amplifier (VGA) located between the sensor and the ADC increases the voltage range of the analog signal supplied by the sensor [13–15]. As a result, the ADC may be required to have a rail-to-rail input voltage range to improve the dynamic performance of the ADC. On the other hand, a DSM has a feedback loop that includes an integrator, where the range of the reference voltage used in the feedback path of the DSM determines the range of the analog input voltage of the DSM. Due to the structural characteristics of the DSM, when an analog input voltage corresponding to the full range of the reference is input to the DSM, the output of the integrator of the DSM is saturated and its stability deteriorates. This causes the dynamic characteristics of the DSM to deteriorate rapidly. Considering this, when the reference used in the DSM has a rail-to-rail range, the delta-sigma ADC will be able to perform stable data conversion even if the VGA using the same supply voltage as the delta-sigma ADC supplies an analog signal with a maximum voltage range. However, the generation of a reference voltage with a rail-to-rail range may increase the design complexity of the reference driver.

In this work, a DSM is proposed that has a wide analog input voltage range of rail-to-rail while using a single supply without any additional reference driver. The proposed DSM has a second-order cascaded-of-integrator feedforward (CIFF) structure, which allows the two stages of integrators to have a small output range. In addition, the 3-bit quantizer used in the proposed DSM reduces the size of the capacitors used in the integrators, which reduces the overall area and power consumption of the DSM.

2. Behavioral Model of Second-Order CIFF DSM with 3-Bit Quantizer

In general, since DSMs have a feedback structure unlike Nyquist ADCs, it is necessary to verify the characteristics of the overall structure, including the stability of the DSM structure, and the design specification of each block. Therefore, the structure of the DSM is designed through a behavioral model to implement the design specification. Figure 1a shows the block diagram using the MATLAB Simulink version R2015b for behavioral simulation of the proposed second-order CIFF DSM. The behavioral model of the proposed second-order CIFF DSM basically consists of two integrators, a 3-bit quantizer, and a data-weighted averaging (DWA) block. Each integrator can be implemented using the Add, Unit Delay, and Gain blocks. The gain error of each integrator due to the finite voltage gain of the operational amplifier is set by the parameters $K1$ and $K2$ in the Gain block, respectively. Thus, the behavioral model of the first integrator is derived as Equation (1). If the operational amplifier used in the first integrator has a voltage gain at low frequencies of 60 dB, then $K1$ is set to $1 - 1/1000$ in the behavioral model.

$$\frac{V_{INT1}[n]}{V_S[n]} = \frac{Z^{-1}}{1 - K1 \cdot Z^{-1}} \tag{1}$$

The CIFF architecture for the DSM reduces the design complexity of the operational amplifier by making the output voltage range of the integrator smaller [16–19]. Furthermore, the use of the 3-bit quantizer instead of the single-bit quantizer reduces the size of the integration capacitor in the first integrator. The two structural design techniques mentioned above can simultaneously reduce the power consumption of the operational amplifier and the area of the capacitor used for the integrator. However, the use of the 3-bit quantizer requires a 3-bit DAC in the feedback path of the DSM. The nonlinearity of the 3-bit DAC causes distortion noise at the output of the DSM by the signal transfer function. Typically, capacitor-based DACs (CDACs) use $2^N - 1$ unit capacitors to achieve N-bit resolution, and the mismatch between these unit capacitors degrades the linearity of the CDAC. In this work, the DWA block is used as a feedback path to the first integrator to reduce the effect of mismatch in the 3-bit DAC [20–22].

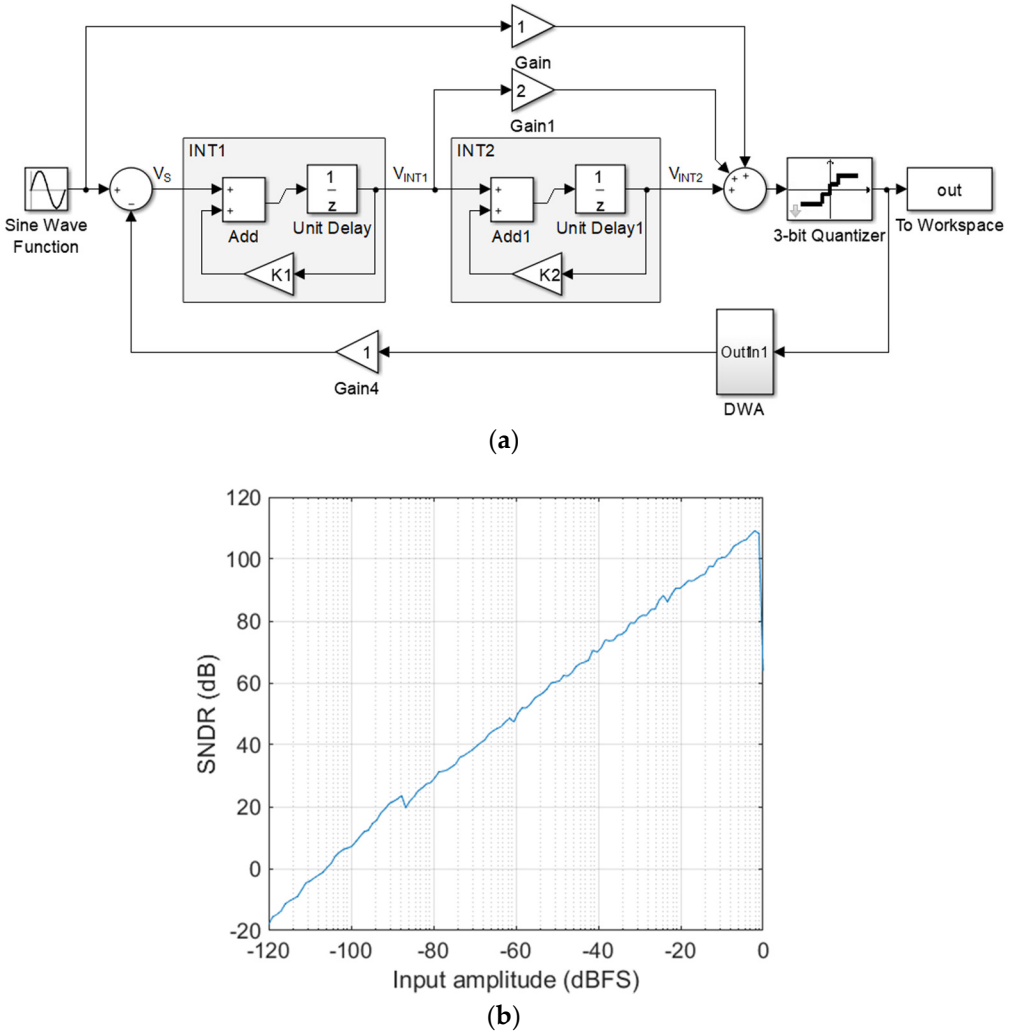

Figure 1. Behavioral design of second-order CIFF DSM: (**a**) block diagram; (**b**) simulated dynamic performance.

Figure 1b shows the simulated dynamic performance about the behavioral model of the second-order CIFF DSM with 3-bit quantizer shown in Figure 1a. The simulation was performed for an analog input signal with a frequency of 100 Hz and an oversampling ratio of 125. The signal-to-noise and distortion ratio (SNDR) of the output signal of the proposed DSM as a function of the magnitude of the analog input signal was plotted. When both operational amplifiers used in the two integrators have a voltage gain of 60 dB, the maximum SNDR is 110.5 dB. Although this is a simple model that does not include the modeling of various noises, it is verified that the proposed second-order CIFF DSM structure with a 3-bit quantizer is a suitable structure for monitoring the DC voltage.

The DWA used in this work consists of a 3-bit full adder, a 3-to-7 binary to thermometer decoder, and a logarithmic shifter, as shown in Figure 2. The DWA is designed to sequentially rotate and select all the unit elements of the 3-bit DAC. For example, when the 3-bit quantizer of the DSM outputs 3b'001 in the first timing, the DWA selects one unit element of the 3-bit DAC, and when the 3-bit quantizer of the DSM outputs 3b'101 in the second timing, the DWA selects the next five unit-elements of the 3-bit DAC selected in the previous timing. If the 3-bit quantizer of the DSM continues to output 3b'110 at the next timing, the DWA selects the last six unit-elements of the 3-bit DAC selected at the previous timing, starting with the last unit element. Figure 3 shows the simulated SNDR performances of the DSM according to applying the DWA for the mismatches between each unit element that occur randomly in the 3-bit DAC. To investigate the change in the dynamic characteristics of the DSM with respect

to the mismatch of the 3-bit DAC, the simulation was performed by using the behavioral model designed in the MATLAB Simulink shown in Figure 1a. The mismatch between the unit elements of the 3-bit DAC is designed to be determined by a random function with a specified maximum mismatch value. Mismatches of 0.1%, 1%, and 5% between the unit elements of the 3-bit DAC worsen the average SNDR of the DSM to 77.37 dB, 56.25 dB, and 42.40 dB. The standard deviations in these cases are 5.25, 5.84, and 5.29, respectively, as shown in Figure 3a. The DWA improves the dynamic performances of the DSM, which are worsened by the mismatch of the 3-bit DAC, and Figure 3b shows the improved SNDR of the DSM when the DWA is applied for a 3-bit DAC with mismatches. When the mismatch between the unit elements of the 3-bit DAC is 0.1% and 1%, the average SNDR of the DSM is 108.74 dB and 108.37 dB, respectively. Even when the mismatch between the unit elements of the 3-bit DAC is 5%, the average SNDR of the DSM remains at 104.57 dB. The use of DWA also improves the deviation to 0.84, 1.2, and 1.76 in each case.

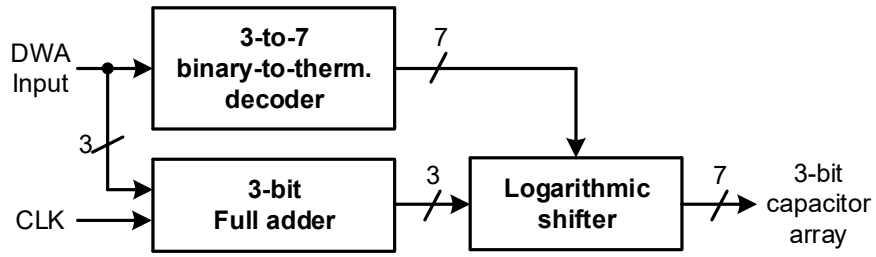

Figure 2. Block diagram of DWA.

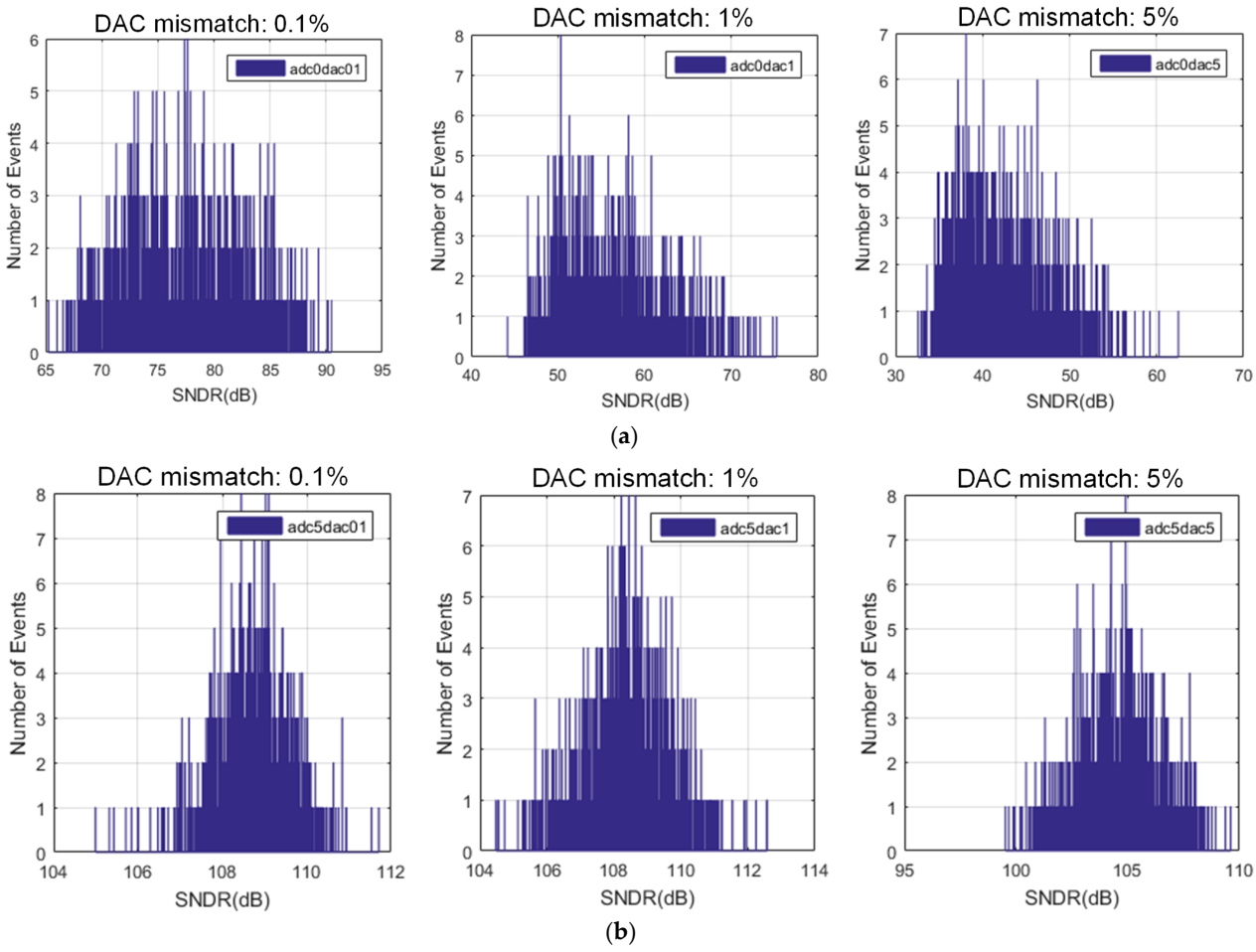

Figure 3. SNDR performances of DSM for DAC mismatch: (**a**) w/o DWA; (**b**) w/ DWA.

3. Transistor-Level Design of Second-Order CIFF DSM with 3-Bit Quantizer

The proposed second-order CIFF DSM with a 3-bit quantizer, shown in Figure 4a, consists of a first integrator including a 3-bit capacitor array, a second integrator, and a 3-bit successive approximation register (SAR) ADC for the 3-bit quantizer [23–25]. The CDAC capacitor array used for the operation of the 3-bit SAR ADC also performs the summation operations required by the CIFF structure. This can reduce the area of the DSM using the CIFF structure. The 3-bit capacitor array in the first integrator is used as a sampling capacitor for sampling an analog input signal and a CDAC for feedback corresponding to the 3-bit quantization. Therefore, it consists of seven unit capacitors, which are connected in parallel and controlled equally when used as sampling capacitors, and act as a 3-bit CDAC for the feedback operation of the DSM. The mismatch between the seven unit capacitors causes distortion in the output of the DSM when the 3-bit capacitor array operates as a 3-bit CDAC. To reduce this effect, a DWA circuit is used in this work for dynamic element matching of the capacitors of the seven units. On the other hand, the proposed second-order CIFF DSM has a full rail-to-rail range of analog input signals. For its implementation, the reference voltage of the full rail-to-rail input is typically supplied to a 3-bit capacitor array used as a 3-bit CDAC. If the full rail-to-rail reference voltage is generated via a reference driver, the implementation of the reference driver requires a supply voltage range that is larger than the range of the reference voltage, i.e., an additional supply voltage separate from the supply voltage for the DSM must be supplied to the reference driver. This can be a burden in system designs that use DSMs. Therefore, this design does not use a separate reference driver and uses the supply voltage used for the second-order CIFF DSM as the reference voltage for the 3-bit capacitor array. The output voltage of the first integrator is defined as shown in Equation (2), where C_{S1} and C_{I1} have the same value, and k is the decimal value of the digital output of the 3-bit SAR ADC, from 0 to 7. Therefore, the proposed CIFF DSM has a full rail-to-rail input range.

$$V_{INT1}[n] = V_{INT1}[n-1] + \frac{C_{S1}}{C_{I1}} \cdot V_{IN}[n] + \frac{C_{S1}}{C_{I1}} \cdot \left\{ \left(\frac{7-2k}{7} \right) \cdot (V_{DD} - V_{SS}) \right\} \quad (2)$$

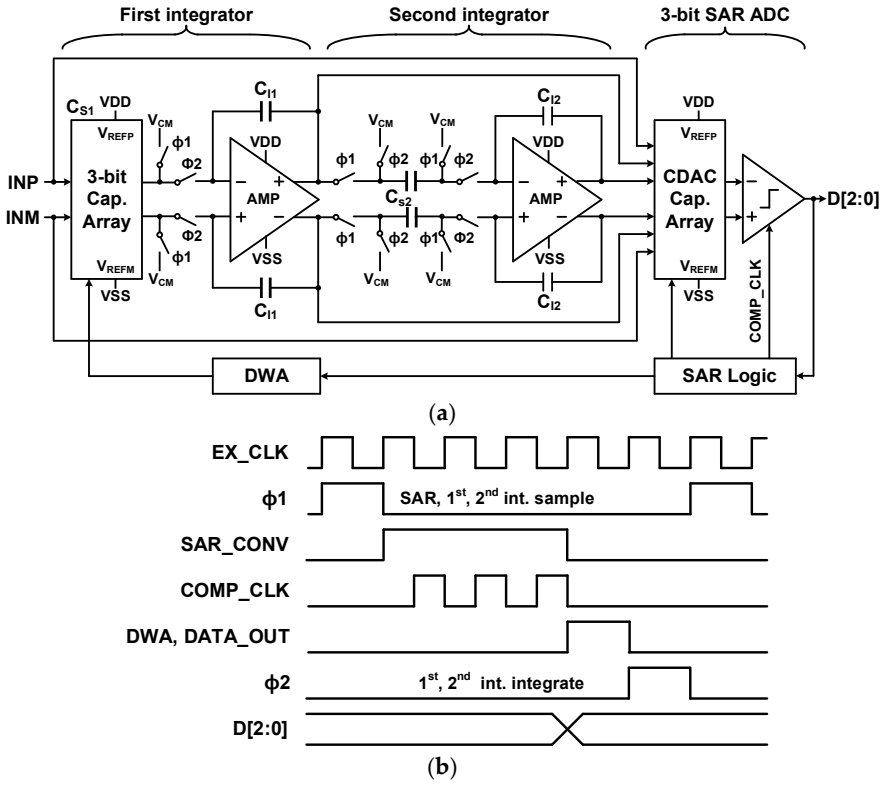

Figure 4. Transistor-level design of second-order CIFF DSM: (**a**) block diagram; (**b**) timing diagram.

The second-order CIFF DSM using the proposed 3-bit quantizer performs the sampling of the differential analog input signal (INP and INM) and its quantization into a 3-bit digital signal every six cycles of the external clock (EX_CLK), as shown in Figure 4b. The differential analog input signal is sampled into the 3-bit capacitor array and the CDAC capacitor array during one cycle of EX_CLK, and then the signal sampled into the CDAC capacitor array is quantized through the operation of the SAR ADC for three cycles of EX_CLK and output as a 3-bit digital code. The 3-bit digital code is supplied to the 3-bit capacitor array during the Φ2 section through the DWA operation performed during one cycle of EX_CLK to perform the feedback operation of the DSM with the 3-bit quantizer.

3.1. CDAC Capacitor Array

The CDAC capacitor array consists of a total of 16 unit capacitors to achieve a voltage gain of 1:2:1 for the analog input signal, the first integrator output, and the second integrator output. For sampling the analog input signal, 4 C_Us of capacitors C_{A2}, C_{A1}, and C_{A0} are used. Overall, $8{\cdot}C_U$ of C_B and $4{\cdot}C_U$ of C_C are used to sum the first integrator output signal and the second integrator output signal to perform the operation of the DSM with CIFF structure. Figure 5a shows the circuit connections of the CDAC capacitor array for the sampling operation as a first step to proceed with the quantization along with the summation of the three analog signals. During the Φ1 interval shown in Figure 4b, the tops of all capacitors of the CDAC capacitor array are connected to the V_{CM}, while the bottoms of C_{A2}, C_{A1}, and C_{A0} are connected to the analog input signal, the bottom of C_B is connected to the first integrator output signal, and the bottom of C_C is connected to the second integrator output signal. This results in a summed sampling of the three analog signals with a voltage gain of 1:2:1. Through this process, the summation behavior required by the CIFF structure of the DSM is performed. The operation of the SAR ADC for 3-bit quantization is performed using 4 C_Us of the 16 C_Us of the CDAC capacitor array, which are the capacitors of C_{A1} to C_{A3}. The operation of the SAR ADC utilizes a V_{CM}-based CDAC [26], where all 16 C_Us are switched to V_{CM} voltage, as shown in Figure 5b, after the sampling operation of the analog signals shown in Figure 5a. Figure 5c shows the VREF switching for the operation of a 3-bit SAR ADC. C_{A2} is then connected to V_{REFP} or V_{REFM} depending on the value of the D [2], which is the result of the comparator for the values of V_{DACP} and V_{DACM}. D [1], the result of the comparison of the values of V_{DACP} and V_{DACM}, updated by the previous CDAC operation, determines the reference value that drives C_{A1}. Finally, after the CDAC is converted a second time, the comparator determines D [0], the value of the LSB of the final 3-bit quantizer. In this 3-bit quantization operation, C_{A0} is still connected to the voltage of the V_{CM}.

3.2. Operational Amplifier for Integrator

Figure 6 shows the circuit diagram of the operational amplifier for the first and second integrators, the basic architecture of a two-stage operational amplifier. In the two-stage operational amplifier, R_Z and C_Z are added for frequency compensation to improve the stability of the frequency response due to the operation of the two-stage amplification. The CMFB voltage generated by the common-mode feedback circuit of the switching capacitor structure controls the output common-mode voltage of the fully differential structure operational amp to be half VDD. Furthermore, to reduce the input referred noise, the transistors used for the first stage in the operational amplifier have a length of 2 μm, which is approximately 15 times larger than the minimum length of the CMOS process used in this work. The two-stage operational amplifier is designed at 70 dB to achieve an open-loop voltage gain of over 60 dB, determined by behavioral simulation, and has a phase margin of over 60 degrees with frequency compensation.

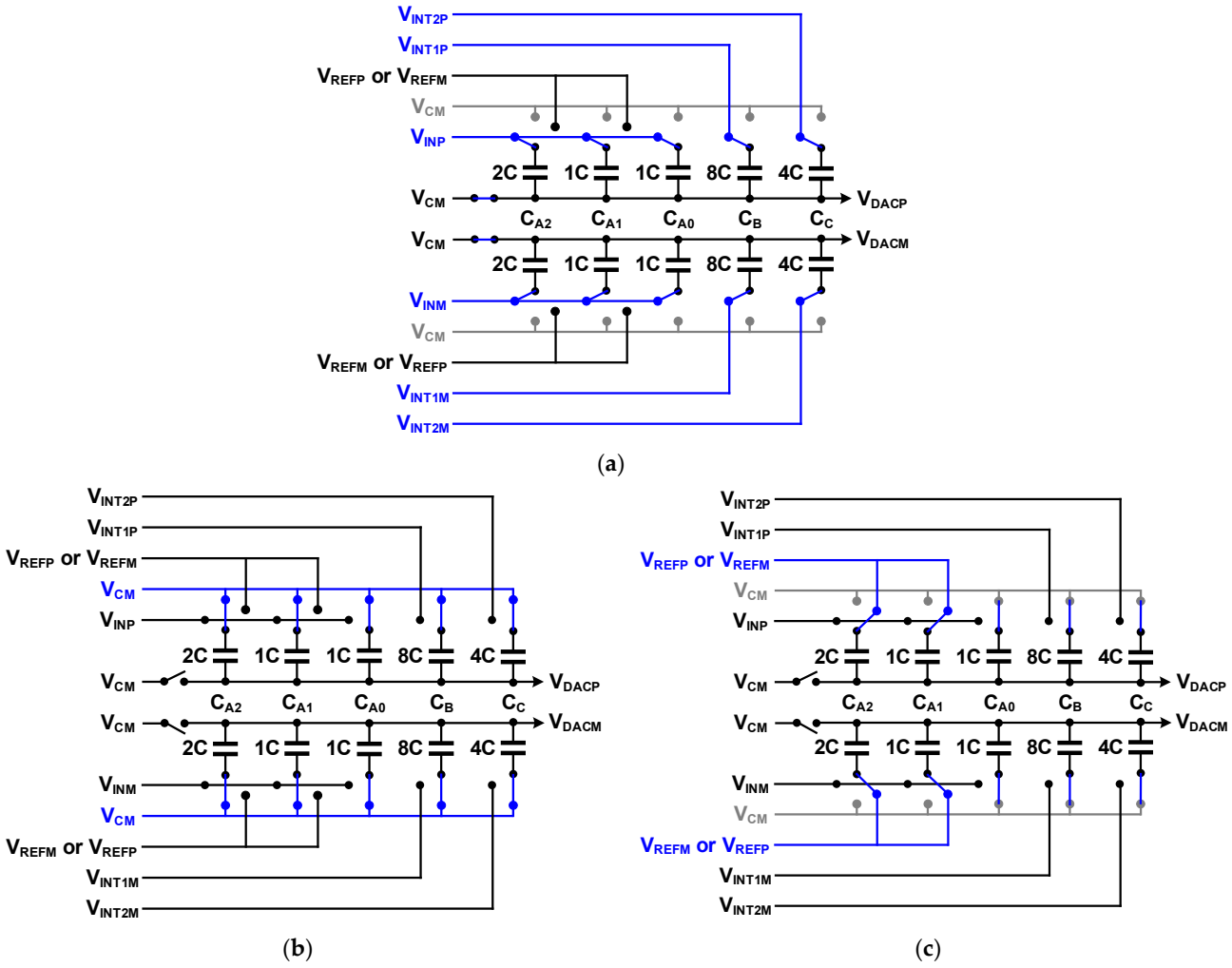

Figure 5. Configuration and behavior of CDAC capacitor array: (**a**) sampling mode; (**b**) V_{CM} switching for 3-bit quantization; (**c**) VREF switching for 3-bit quantization.

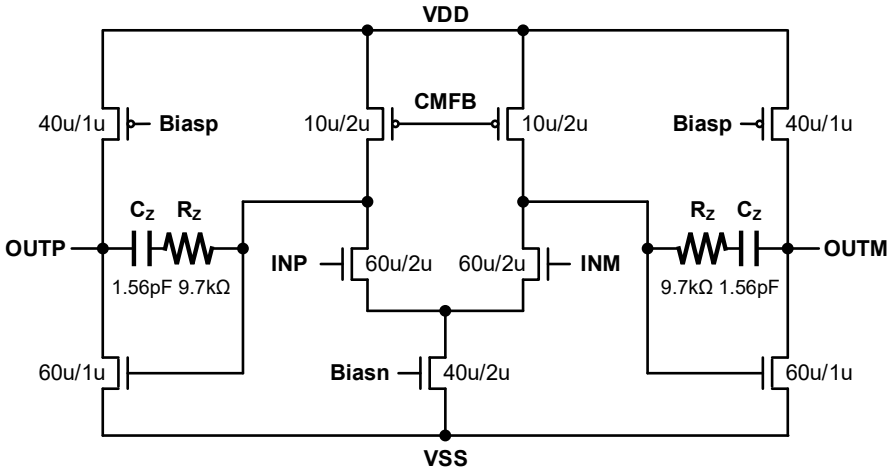

Figure 6. Circuit diagram of operational amplifier for integrator.

4. Chip Implement and Measurement Results

The proposed second-order CIFF DSM with 3-bit quantizer was fabricated using a 130 nm 1-poly 6-metal CMOS process with a 1.5 V supply voltage. The sampling frequency of the proposed second-order CIFF DSM is 500 kHz to implement an input bandwidth of

2 kHz and an oversampling ratio of 125. To implement this, the EX_CLK signal with a frequency of 3 MHz is fed to the implemented second-order CIFF DSM.

The proposed second-order CIFF DSM has an active area of 359 µm × 267 µm, as shown in Figure 7a. The first integrator, including the 3-bit capacitor array, occupies an area of 22,320 µm^2, making it the largest area in the implemented second-order CIFF DSM. The second integrator has an area of 18,600 µm^2, and the CDAC capacitor array and comparator have an area of 7800 µm^2. Finally, the digital blocks of the SAR logic and DWA are implemented using an area of 20,300 µm^2. The digital blocks were separated from the two integrators to reduce the impact of digital noise. Figure 7b through Figure 7d show the layout of the first integrator, second integrator, and CDAC capacitor array and comparator for the 3-bit SAR ADC, respectively. The same operational amplifier with an area of 183 µm × 50 µm was used for both integrators. The capacitors for the first integrator including the 3-bit capacitor array and the second integrator including the second sampling capacitor were designed using stacked metal–insulator–metal capacitors (MIMs) as unit capacitors to reduce the possible area, as shown in Figure 7b,c. The unit stacked MIM capacitor realized by the 4 µm × 4 µm area, the smallest size supported by the process used in this work, has a capacitance of 66 fF. On the other hand, the CDAC capacitor array used for the operation of the 3-bit SAR ADC and the summation operation of the CIFF uses a conventional MIM shown in Figure 7d instead of a stacked MIM to reduce power consumption, reducing the capacity of the unit capacitor to 33 fF.

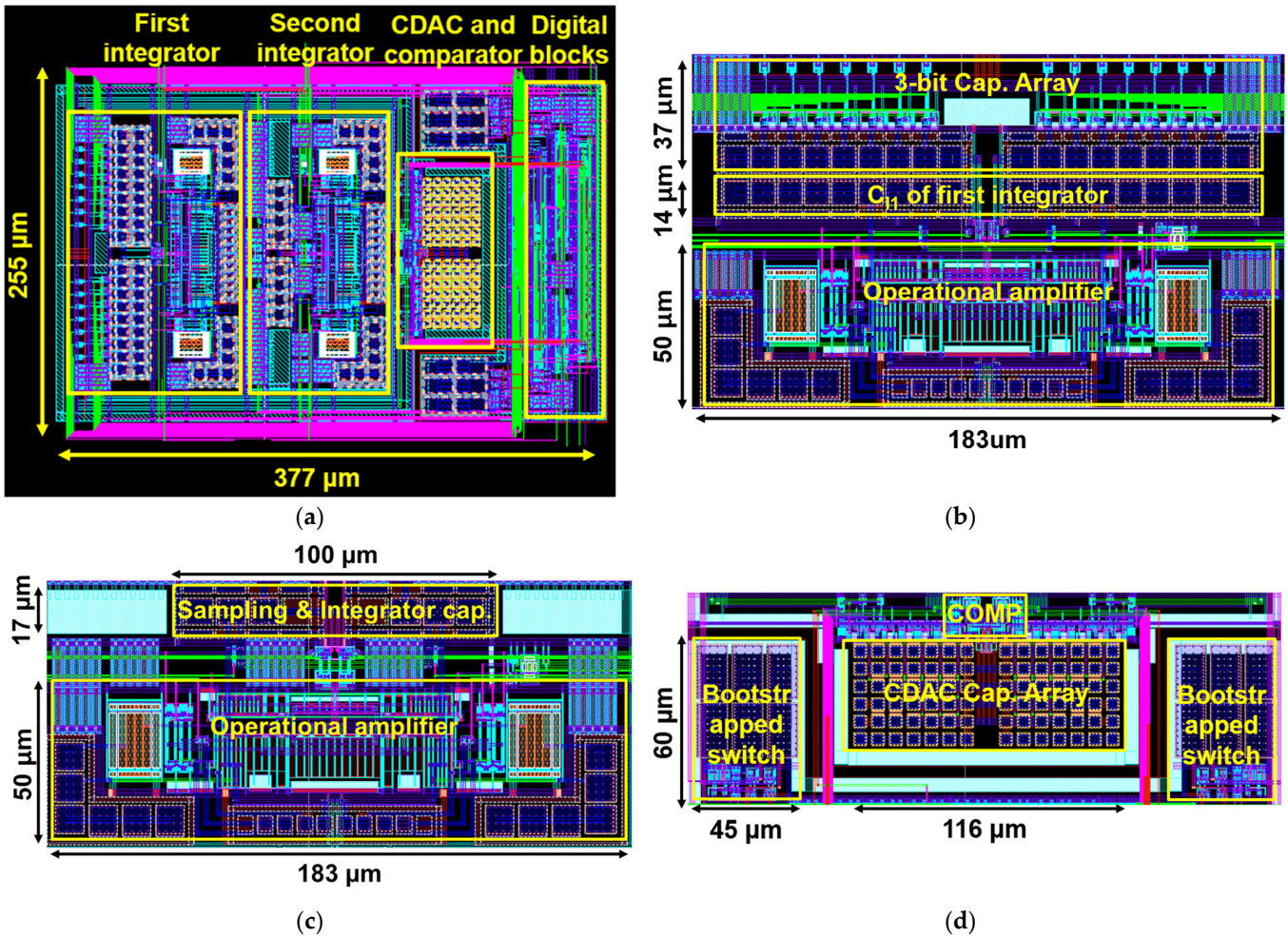

Figure 7. Layout of implemented second-order CIFF DSM (**a**) entire block; (**b**) first integrator; (**c**) second integrator; (**d**) CDAC capacitor array and comparator for 3-bit SAR ADC.

As shown in Table 1, the power consumption of the proposed second-order CIFF DSM is 304.6 µW. The analog block, including the two integrators, consumes 294.8 µW, accounting for 96.8% of the total. In this work, the proposed second-order CIFF DSM did not use a reference driver separately although having the range of a full rail-to-rail analog input signal. Instead, decoupling capacitors between the two power voltages were placed in the empty space between the circuits and under the power lines to stabilize VDD and VSS, which are used as reference voltages. Therefore, the area and power consumption due to the reference driver are not increased.

Table 1. Measured digital output of second-order CIFF DSM.

Block		Power Consumption
Analog	First integrator	147.9 µW
	Second integrator	146.7 µW
	3-bit SAR ADC (w/o SAR Logic)	227.5 nW
Digital blocks (w/SAR Logic)		9.741 µW
Total		304.6 µW

Figure 8 shows the test environment for the implemented second-order CIFF DSM with 3-bit quantizer. The analog differential input signal was sourced from Audio Precision equipment (Beaverton, OR, USA). The NI PXIe-5451 was used to supply the external clock signal (EX_CLK) for the second-order CIFF DSM with a 3-bit quantizer and acquire the 3-bit output digital code. The performance of the implemented second-order CIFF DSM was analyzed through signal processing using LabVIEW 2021 software for the acquired digital output code.

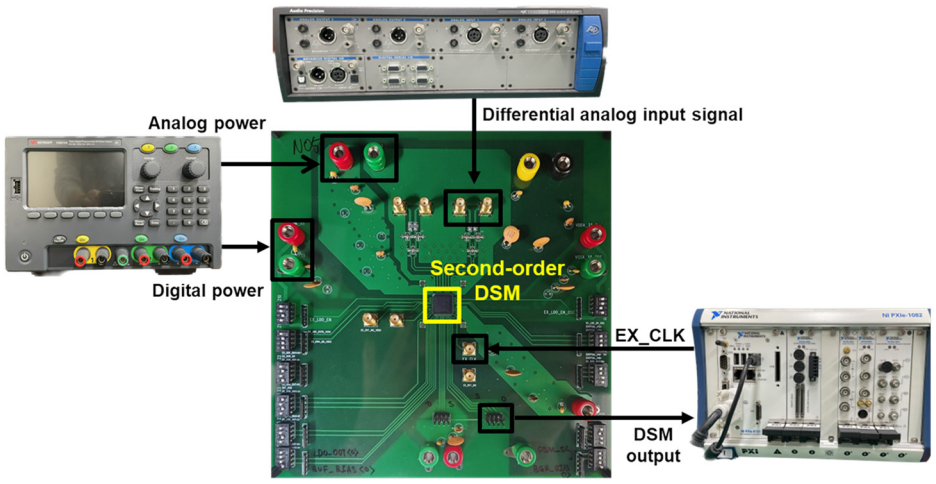

Figure 8. Test environment of implemented second-order CIFF DSM.

Figures 9 and 10 show the measured results of the proposed second-order CIFF DSM with 3-bit quantizer. The measurements of the fabricated second-order CIFF DSM were performed with a sampling rate of 500 kHz to realize an oversampling ratio of 125 for an input bandwidth of 2 kHz. For this evaluation, the frequency of EX_CLK was determined to be 3 MHz. In addition, a differential analog input signal with a frequency of 353 Hz and an amplitude of 1.2 Vpp was supplied for evaluation. Figure 9 shows the real-time waveform of the measured 3-bit output of the proposed second-order CIFF DSM, expressed as a decimal value. The digital output of the second-order CIFF DSM is a PWM signal with eight voltage levels, ranging from 0 to 7, as decimal values for a sinusoidal analog input signal. The measured dynamic performances of the implemented second-order CIFF DSM are shown in Figure 10. Figure 10a is the power spectral density obtained by

performing a fast Fourier transform on the measured 3-bit output of the second-order CIFF DSM. The spectral density increased with increasing frequency after 2 kHz with a slope of 40 dB/dec. This validates the behavioral of noise shaping by the second-order structure of the proposed DSM. The measured peak SNDR for a bandwidth of 2 kHz is approximately 90 dB. Figure 10b shows the power spectrum density for the measured output code of the second-order CIFF DSM when the two signals for the differential analog inputs are shorted to a voltage in common mode. This measurement shows the noise of the implemented second-order CIFF DSM itself, without the influence of the differential analog input signal. The measured power spectrum density for the noise of the 3-bit output of the second-order CIFF DSM is the same as in Figure 10a, showing that noise shaping is performed as the frequency increases. However, within a bandwidth of 2 kHz, the harmonic components for the analog input signal do not appear. Also, the measured noise floor over the frequency range of DC to 2 kHz is approximately 120 dB. In addition, the measured dynamic range (DR) over a bandwidth of 2 kHz is approximately 96.3 dB.

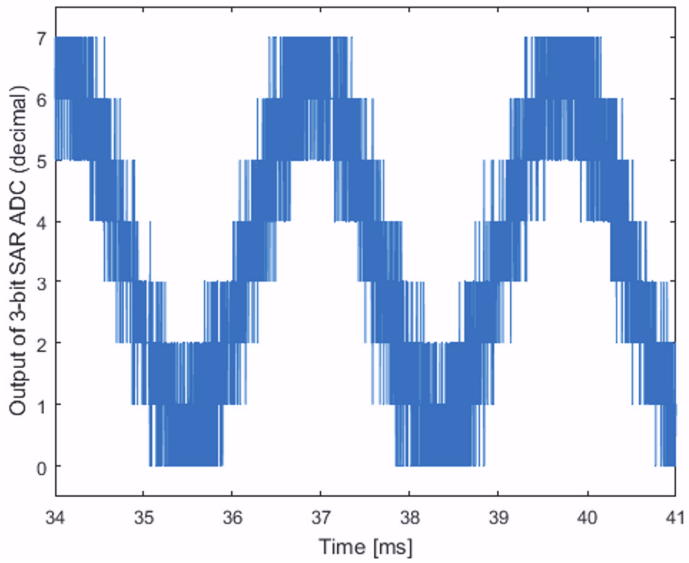

Figure 9. Measured digital output of second-order CIFF DSM.

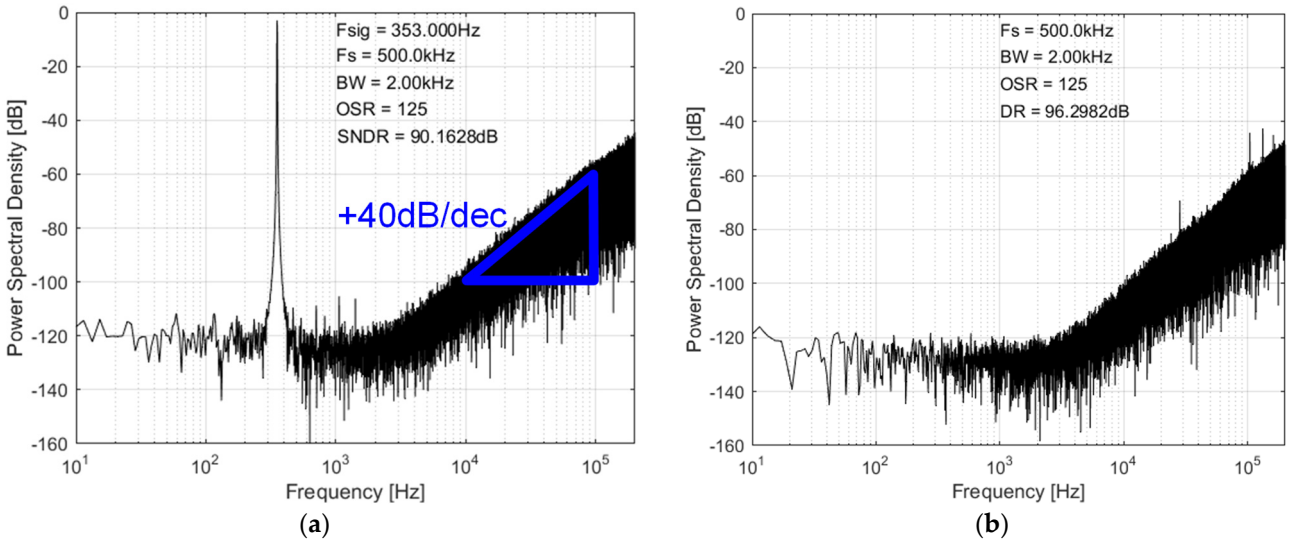

Figure 10. Measured dynamic performances of second-order CIFF DSM: (**a**) differential analog input signal with frequency of 353 Hz and amplitude of 1.2 Vpp; (**b**) no differential analog input signal.

Figure 11 shows the dynamic performance as a function of the amplitude of the analog input signal. From the results shown in Figure 10b, when an analog signal of −96.3 dB is supplied, the implemented second-order CIFF DSM has a SNDR of 0 dB. As the magnitude of the analog signal increases, the dynamic performance of the second-order CIFF DSM increases, with a maximum SNDR of 90.16 dB when the analog signal is −1.94 dB, as shown in Figure 10a. In this case, the analog input signal of the second-order CIFF DSM has a voltage range of 0.15 V to 1.35 V. If an analog input voltage greater than this was fed to the second-order CIFF DSM, the two integrator outputs of the DSM would saturate and the SNDR characteristics of the second-order CIFF DSM would deteriorate rapidly.

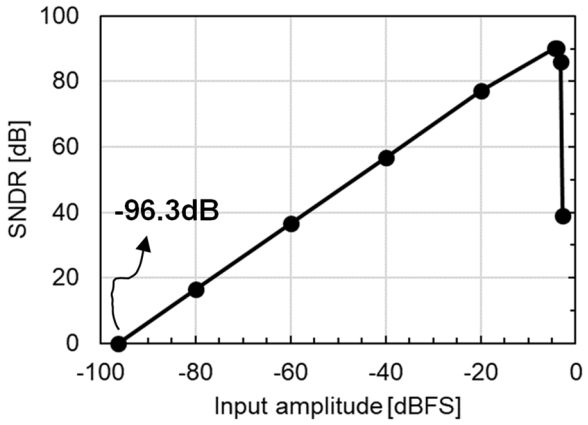

Figure 11. Dynamic performance according to amplitude of analog input signal.

Table 2 compares the performance of the proposed second-order CIFF DSM with reported CIFF DSMs implemented using a similar process. The CIFF DSMs presented in [27] and [28] have large bandwidths above 20 kHz and SNDR characteristics above 90 dB. The large bandwidth implementation results in relatively high-power consumption. The CIFF DSMs presented in [29,30] have small bandwidths of less than 1 kHz while consuming less power. These CIFF DSMs also utilize a third-order CIFF structure, similar to the structure of the CIFF DSM in [28], and have an area at least four times larger than the area of the second-order CIFF DSM proposed in this work. The CIFF DSM reported in [31] has a similar second-order structure and multi-bit quantizer to the CIFF DSM proposed in this work, with comparable design specifications. It is characterized by an SNDR of up to 93.9 dB with smaller power consumption than the proposed second-order CIFF DSM, but with a relatively large area.

Table 2. Performance comparison of CIFF DSMs.

Item	[27]	[28]	[29]	[30]	[31]	This Work
Process [nm]	180	180	90	180	110	130
Supply voltage [V]	1.8	1.8	1.2	1.5	1.5	1.5
Order of CIFF DSM	Second	Third	Third	Third	Second	Second
Power [μW]	800	340	30	4	62.43	304.6
Sampling frequency [MHz]	12.8	3.072	0.25	0.2	0.512	0.5
Oversampling ratio	128	64	500	125	128	125
Bandwidth [kHz]	50	24	0.25	0.8	2	2
DR [dB]	-	98	95.6	94.1	96.3	94.36
SNDR [dB]	94.6	96.2	91	89.3	93.9	90.16
Area [mm^2]	0.2	0.8	0.39	0.75	0.165	0.096

5. Conclusions

The second-order CIFF DSM with 3-bit quantizer was implemented using a 130 nm 1-poly 6-metal CMOS process with a supply of 1.5 V. It was designed using the two integrators, the 3-bit quantizer, the DWA circuit, and the clock generator to have a small area and low power characteristics to be suitable for ROICs in sensor applications. The SAR ADC-based 3-bit quantizer was used to reduce the integration capacitor size of the first integrator to implement a small area and low power second-order CIFF DSM. The CDAC capacitor array used for the operation of the 3-bit SAR ADC also performs the summing operation. This eliminates the additional circuit for summation required by the DSM in the CIFF structure. An additional 3-bit CDAC was used to feedback the results of the 3-bit quantizer to the first integrator. On the other hand, while the nonlinearity of the 3-bit CDAC within the SAR ADC does not significantly affect the overall characteristics of the DSM, the nonlinearity of the 3-bit DAC for feedback to the first integrator on the output of the 3-bit quantizer significantly worsens the dynamic characteristics of the DSM. In this work, the DWA circuit was used to prevent the deterioration of the characteristics of the proposed second-order CIFF DSM due to the nonlinearity of the 3-bit DAC. In addition, the proposed second-order CIFF DSM does not use an additional reference driver despite having a full rail-to-rail analog input range. As a result, the proposed second-order CIFF DSM further reduces area and power consumption due to the elimination of the reference driver. The proposed second-order CIFF DSM has an area of 0.096 mm^2. Its input bandwidth and OSR are 2 kHz and 125, respectively. The DR and peak SNDR of the implemented second-order CIFF DSM were measured to be approximately 96.3 dB and 90 dB, respectively, when of the differential analog input signal has a frequency of 353 Hz. The proposed second-order CIFF DSM, implemented with digital filters, can be used as a high-resolution ADC for small areas and low power ROIC.

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