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Heat Dissipation Capability of Stagger-Stacked Double Data Rate Module

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Abstract: In this study, we introduce a stagger-stacked DDR module that comprises one IPD chip (top die) along with four memory chips initially. The steady-state thermal characteristics of this configuration were empirically assessed using a dedicated thermal test vehicle. The purpose of this research is to investigate the module's junction temperature by adjusting four factors: the thermal conductivity of the molding plastic, chip thickness, chip misalignment length, and the thermal conductivity of the adhesive film. We observed that the junction temperature decreases with an increase in the chip staggered length. An improved orthogonal experimental method was utilized to achieve the optimal design of the module. The optimal junction temperature has decreased by 4.74% compared to the initial value. Additionally, three alternative packaging technologies—cantilever, pyramid, and a combination of cantilever and pyramid—were evaluated for the benchmarking of the thermal performance. Ultimately, the stagger-stacked package demonstrated a reduction in the junction temperature by 3.62%, 7.95%, and 5.63%, respectively, when compared to the three traditional stacked packages.

Keywords: stagger-stacked DDR module; thermal resistance; junction temperature optimization; improved orthogonal experiment

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1. Introduction

The substantial increase in packaging density necessitates the advancement of both technological innovations and architectural designs within the packaging domain. In order to achieve the development goals of light, thin, small, high-performance, and high-reliability chips, engineers have explored the satisfactory method—SiP (System-in-Package). Stacked chips are commonly used for packaging memory chips. However, as the power consumption of the chip continues to increase, the heat generation increases accordingly and brings about heat dissipation challenges. Thermal crosstalk among internal dies in the vertical dimension intensifies the thermal management challenge, necessitating a reduced power budget to ensure that memory chips function below the temperature threshold of 85 °C [1,2]. In addition, an innovative integrated fanout packaging technology was proposed in [3] for developing state-of-the-art mobile applications. The thermal performance of the advanced packaging technologies was analyzed and compared with two typical technologies. The results showed that the proposed packaging technology had a 12% and 17% lower junction to ambient thermal resistance than FC PoP and 3D IC. In [4], a novel 3D flip chip fanout packaging approach (FC-FOWLP) incorporating Si bridges was introduced. When compared to the 3D FOWLP and 3D stacked IC package, the FC-FOWLP demonstrates the lowest thermal resistance across all the components. In [5], an orthogonal experiment was conducted to investigate the reliability of a four-tier die-stacked SiP structure. Through optimal design, it was possible to reduce maximum thermal stress by more than 21.2%. Paper [6–8] optimizes the structure and materials of the heat sink

to improve the heat dissipation capacity of the packaging system. With the development of chemical technology and material technology, new thermal switches [9] and thermal transistors [10] become the next generation of future thermal management technologies.

In this paper, we initially present the stagger-stacked DDR module, which contains five layer chips: the top die is one IPD chip and the other dies are memory chips. Subsequently, a finite element model is developed to simulate the steady-state thermal performance of the structure. The thermal conductivity of the molding compound, chip thickness, chip staggered length, and thermal conductivity of the adhesive film are selected, respectively, to analyze and to enhance the stagger-stacked DDR module. The results demonstrate that an increase in the chip staggered length effectively mitigates the junction temperature. These four factors are also employed as variable factors for enhanced orthogonal experiments. Specifically, two consecutive rounds of orthogonal experimentation are conducted to optimize the overall module's heat dissipation performance, resulting in an optimal design. After combining the optimal values of various factors and performing simulation again, the optimal junction temperature can be determined. Compared with the initial junction temperature, the optimal junction temperature has experienced a reduction of 4.74%. Subsequently, the thermal performance of the proposed package is benchmarked with three kinds of traditional stacked packaging configurations, and the result reveals that the stagger-stacked DDR module has the best thermal performance. When compared to the three traditional stacked packages (cantilever, pyramid, and cantilever–pyramid combination), our proposed stagger-stacked package demonstrates reductions in junction temperature by 3.62%, 7.95%, and 5.63%, respectively. The findings indicate that the staggered-stacked DDR module proposed in this paper possesses superior thermal performance.

2. Finite Element Model of the Stagger-Stacked DDR Module

The simulation model of the stagger-stacked DDR module is created by using ANSYS 2023 R2. Figure 1 illustrates the complete structure of the module, encompassing one IPD chip (die 5), four memory chips (die1~die4), adhesive film, a molding compound, a substrate, and a pin. The structure has been simplified (excluding bonding wires, etc.) to facilitate more efficient simulation calculations. Important thermal parameters are presented in Table 1. The dimensions of the molding compound and substrate are 14 mm × 15.5 mm in length and width, respectively. The substrate has a thickness of 0.25 mm, while the molding compound is 0.9 mm thick, which exceeds the top chip by 0.3 mm. Two sets of adhesive films with dimensions of 5 mm × 10 mm × 0.02 mm and 4.5 × 10 × 0.02 mm are utilized. Based on the data tabulated in Table 1, a chip staggered length of 0.5 mm is determined. We will evaluate the thermal characteristics of the stagger-stacked DDR module mounted on a PCB, where the model is built following the JEDEC 51-2 standard [11]. The IPD chip is set to 0.1 W, and the other memory chips are set to 0.5 W, respectively. An ambient temperature of 25 °C is considered. The initial junction temperature is 74.87 °C, which is shown in Figure 2. The picture also demonstrates that the junction temperature rises by about 50 °C. Therefore, it is necessary to optimize the thermal performance of the module.

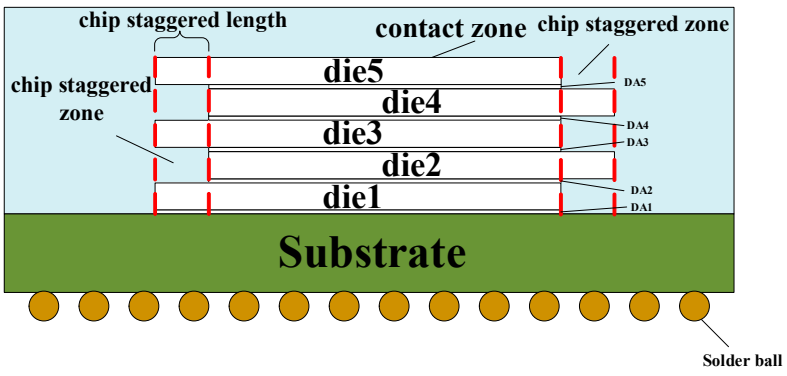

Figure 1. The whole structure of the stagger-stacked DDR module.

Table 1. Dimensional and thermal parameters of the stagger-stacked DDR module.

Components	Dimension (mm)	Thermal Conductivity (W/mK)
die	5 × 10 × 0.1	124
DA1	5 × 10 × 0.02	3
2	D51	2.3 × 2.3
3	D52	2.3 × 2.3
DA2~DA5	4.5 × 10 × 0.02	3
Substrate	14 × 15.5 × 0.25	x, y: 20 z: 0.8
Molding compound	14 × 15.5 × 0.9	0.8
pin	0.25 × 0.25 × 0.25	50
PCB	114.3 × 76.2 × 1.6	x, y: 25.76 z: 0.38

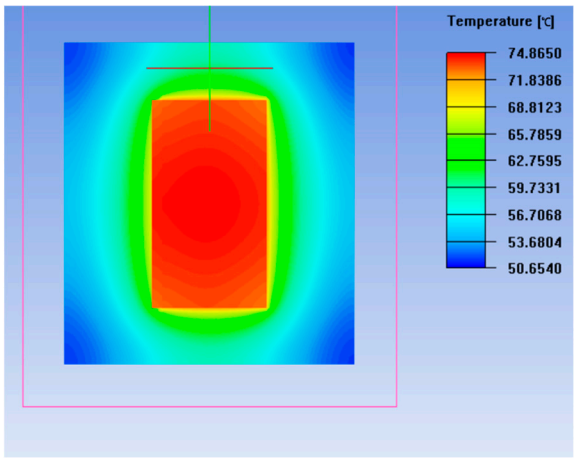

Figure 2. The initial temperature distribution of the stagger-stacked DDR module.

3. Optimize Thermal Performance Based on Single Factor

For multi-chips, the heat generated by the chips in each layer will be coupled to each other, which will easily cause the chip to overheat and fail. As a result, research on the optimization of the junction temperature of the stacked package is significant. In this paper, four different factors, including the thermal conductivity of the molding compound, the chip thickness, the chip staggered length, and the thermal conductivity of the adhesive film, are selected to analyze and improve the thermal performance of the stagger-stacked DDR module. The following section will discuss the effect of the factors on the junction temperature.

3.1. Effect of Thermal Conductivity of Molding Compound

In order to study the influence of the thermal conductivity of the molding compound on the junction temperature, the thermal conductivity of the molding compound is set to range from 0.5 W/m K to 25 W/m K. It can be inferred from Figure 3 that with an increase in the thermal conductivity of the molding compound, there is a continuous decrease in the junction temperature of the module. Moreover, for high values of thermal conductivity, the curve tends to flatten out. When the thermal conductivity of the molding compound is 0.5 W/m K, the junction temperature of the DDR module is 75.77 °C, which is the highest value. When the thermal conductivity of the molding compound exceeds 20 W/m K, the junction temperature of the module is 65.57 °C, which is the lowest value of the junction temperature, and no longer changes with the increase in thermal conductivity. This is because the ratio of the thermal resistance of the molding compound to the total thermal resistance tends to be stable, and the effect of the thermal conductivity of the molding compound on the junction temperature is no longer obvious.

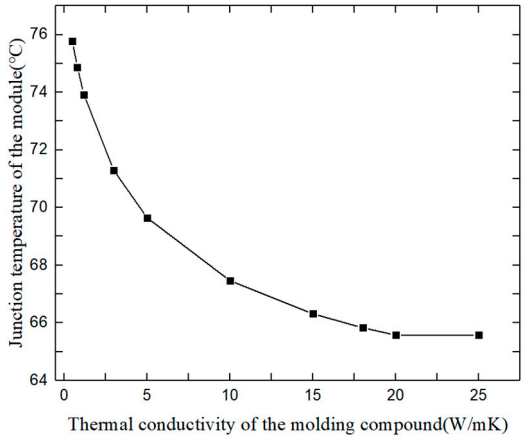

Figure 3. Junction temperature versus thermal conductivity of the molding compound.

3.2. Effect of Chip Thickness

As seen in Figure 4., the junction temperature of the module decreases continuously with an increase in die thickness. The maximum value of the module junction temperature appears at a die thickness of 0.06 mm, measuring 75.84 °C. The minimum value appears at a die thickness of 0.2 mm, and the temperature is 73.2 °C. This is because as the thickness of the die increases, the volume of the die increases, and its heat generation rate decreases.

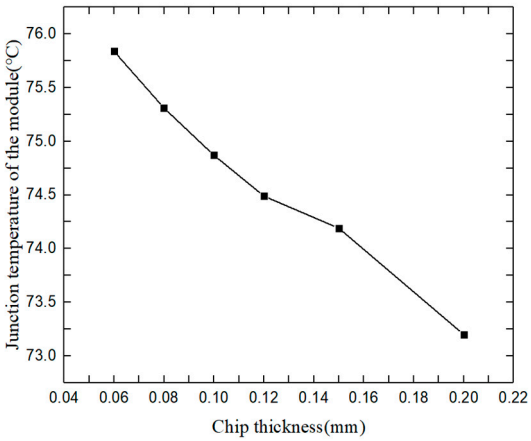

Figure 4. Junction temperature vs. chip thickness.

3.3. Effect of Chip Staggered Length

The change in the chip staggered length between the chips will not only change the thermal resistance of the molding compound in the chip staggered zone but also the thermal resistance of the contact zone. Therefore, we only change the value of the chip staggered length to ensure that other factors remain unchanged and to then observe the change in the junction temperature. For this analysis, a parameterized simulation model has been regenerated for chip staggered length values in a range from 0.5 mm to 2.5 mm. The result is given in Figure 5. It can be observed from Figure 5 that when the chip staggered length increases from 0.5 mm to 2.5 mm, the junction temperature of the module continues to decrease, and the lowest temperature is 72.17 °C. As a result, increasing the chip staggered length is beneficial to dissipate heat. This is because when adding the chip staggered length, more power is allocated to the chip staggered zone, and the heat flow concentration in the contact zone is alleviated. Therefore, the effect of thermal coupling between the chips is reduced. On the other hand, this phenomenon can be explained from the perspective of thermal resistance. We divided the components above the module substrate into four regions, which is shown in Figure 6. As shown in the picture, the top molding compound is set to region 1 (yellow slash area), the central part is set to region 2 (green slash area), and

the left and right sides are set to region 3 (brown slash area) and region 4 (red slant area), respectively. Assuming that the chip staggered length is x (mm), the length in region 2 is 5 − x (mm). According to the thermal resistance calculation formula, the overall thermal resistance of the component can be calculated. Regions 1 to 4 have been marked in Figure 6

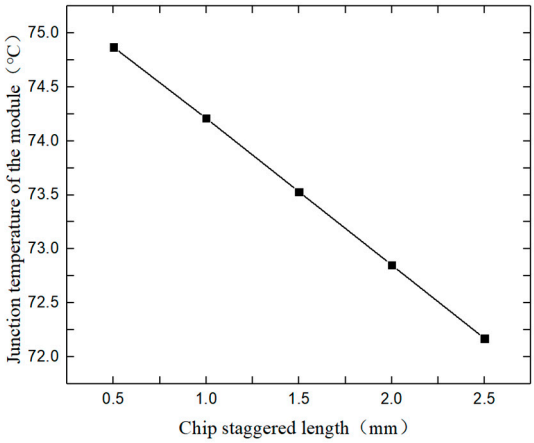

Figure 5. Junction temperature vs. chip staggered length.

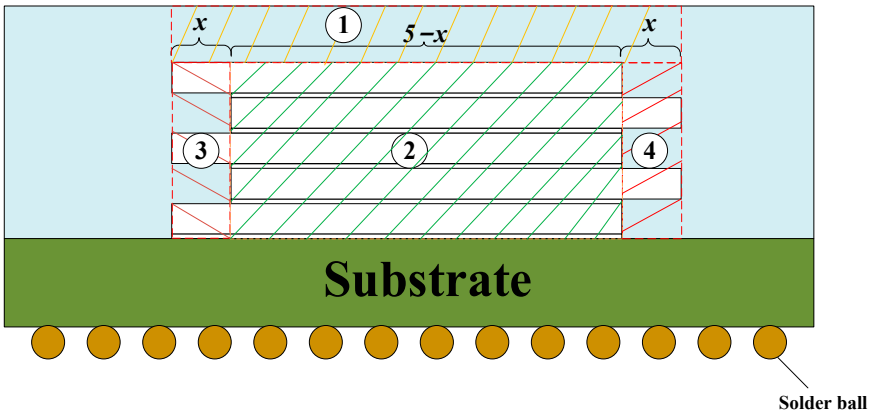

Figure 6. Schematic diagram of zone division.

Taking the calculation process of the conduct thermal resistance of region 1 and region 2 as an example:

$$R_{\text{region1}} = \frac{0.3 \times 10^{-3}}{(5+x) \times 10 \times 10^{-6} \times 0.8} = \frac{37.5}{5+x}$$

$$R_{\text{region 2}} = 5 \cdot \frac{0.1 \times 10^{-3}}{(5-x) \times 10 \times 10^{-6} \times 124} + 5 \cdot \frac{0.02 \times 10^{-3}}{(5-x) \times 10 \times 10^{-6} \times 3} = \frac{3.733}{5-x}$$

The computing method of region 3 and 4 is similar to region 1 and 2, so the calculation results are given directly:

$$R_{\text{region 3}} = \frac{35.912}{x}$$

$$R_{\text{region 4}} = \frac{50.161}{x}$$

When heat is transferred from region 1 to the substrate, regions 2~4 will transfer heat at the same time. Therefore, the expression of total thermal resistance can be written as follows:

$$R_{\text{total}} = R_{\text{region 1}} + R_{\text{region 2}} // R_{\text{region 3}} // R_{\text{region 4}}$$

Therefore, the function expression of the total thermal resistance is as follows:

$$R_{\text{total}} = \frac{78.128}{104.645 - 17.196 \cdot x} + \frac{37.5}{5 + x}$$

In order to observe the changing process of thermal resistance clearly, when converting function expressions into graph form, which is shown in Figure 7, it can be concluded that when the chip staggered length increases from 0.5 mm to 2.5 mm, the total thermal resistance continues to decrease. Therefore, the junction temperature of the module continues to decrease.

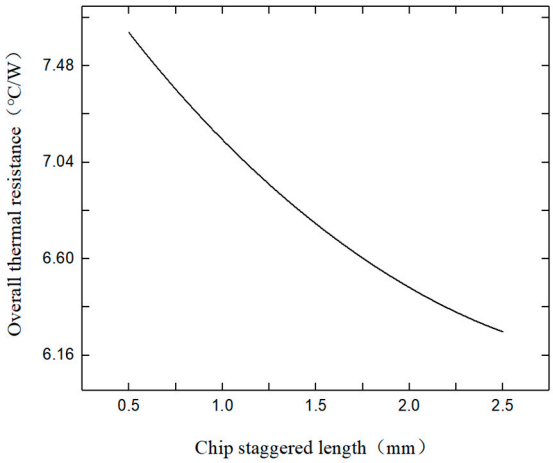

Figure 7. Overall thermal resistance vs. chip staggered length.

3.4. Effect of Thermal Conductivity of Adhesive Film

Figure 8 illustrates the trend of junction temperature changes with the thermal conductivity of adhesive film. As the thermal conductivity of the adhesive film changes from 0.5 W/m K to 3 W/m K, there is a significant decrease in the module's junction temperature. And when the thermal conductivity of the adhesive film increases from 3 W/m K to 18 W/m K, the change in the junction temperature is not obvious. This is because the ratio of the thermal resistance of the adhesive film to the total thermal resistance tends to be constant, and continuing to increase the thermal conductivity of the adhesive film has little effect on the junction temperature.

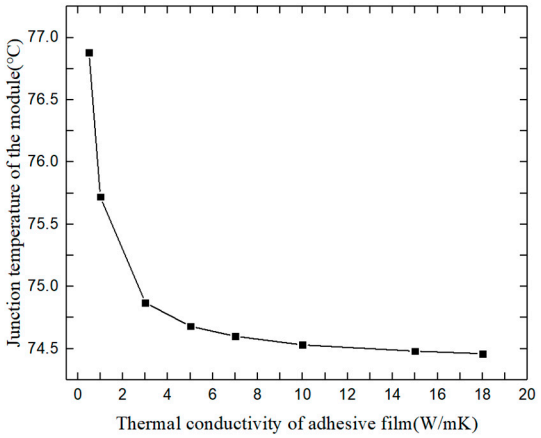

Figure 8. Junction temperature vs. thermal conductivity of adhesive film.

4. Orthogonal Experimental Design

A multi-factor test usually contains many factors and levels, which will cause a large number of tests and waste time. The orthogonal experimental method is an efficient

method for designing processes that operate consistently under a variety of conditions. The method determines the most important factor and the best design when experiments are completed [12–14]. Four selected control factors and their levels are applied in this work, and these are tabulated in Table 2. The L16 (45) orthogonal array is chosen as the main experiment to minimize the junction temperature. The junction temperature of the module is used as the quality factor [15]. The orthogonal test combination and simulation results are listed in Table 3.

Table 2. Control factors and levels.

Control Factors	Levels			
	1	**2**	**3**	**4**
Thermal conductivity of molding compound (W/m K) (A)	0.3	0.5	0.8	1.2
Chip thickness (mm) (B)	0.06	0.08	0.1	0.12
Chip staggered length (mm) (C)	0.5	1	1.5	2
Thermal conductivity of adhesive film (W/m K) (D)	0.5	1	3	5

Table 3. Test combination and simulation results.

Test Number	A (W/m K)	B (mm)	C (mm)	D (W/m K)	E (Errors)	Junction Temperature (°C)
1	0.3	0.06	0.5	0.5	1	79.9858
2	0.3	0.08	1	1	2	77.6081
3	0.3	0.1	1.5	3	3	76.0275
4	0.3	0.12	2	5	4	75.3698
5	0.5	0.06	1	3	4	76.0407
6	0.5	0.08	0.5	5	3	75.9295
7	0.5	0.1	2	0.5	2	75.8257
8	0.5	0.12	1.5	1	1	75.2676
9	0.8	0.06	1.5	5	2	74.3284
10	0.8	0.08	2	3	1	73.2505
11	0.8	0.1	0.5	1	4	75.7211
12	0.8	0.12	1	0.5	3	75.6339
13	1.2	0.06	2	1	3	73.4334
14	1.2	0.08	1.5	0.5	4	74.2441
15	1.2	0.1	1	5	1	73.0833
16	1.2	0.12	0.5	3	2	73.4868

After obtaining the experimental results of the first orthogonal table, it is necessary to perform a range analysis on the orthogonal table to obtain the key factors affecting the junction temperature and the optimal value of each factor. The range analysis results of the first orthogonal experiment are listed in Table 4; the error is an absolute value.

Table 4. Test combination and simulation results.

	A (W/m K)	B (mm)	C (mm)	D (W/m K)	E (Errors)
K1	308.9911	303.7883	305.1232	305.6895	301.5872
K2	303.0635	301.0321	302.3659	302.0301	301.2489
K3	298.9339	300.6576	299.8676	298.8055	301.0243
K4	294.2476	299.7581	297.8794	298.711	301.3757
k1	77.24778	75.94708	76.2808	76.42238	75.3968
k2	75.76588	75.25803	75.59148	75.50753	75.3122
k3	74.73348	75.1644	74.9669	74.70138	75.2561
k4	73.5619	74.93953	74.46985	74.67775	75.3439
R	3.68588	1.00755	1.81095	1.74463	0.1407
Range analysis's order	1	4	2	3	5

Range analysis determines the order of the discussed factor and the optimized level combination. Consequently, the thermal conductivity of the molding compound has the greatest impact on the junction temperature of the module, followed by chip staggered length and the thermal conductivity of the adhesive film, and chip thickness has the smallest effect on junction temperature. After that, the range values of the various factors are sorted from large to small, and the level values of the various factors are sorted from small to large,

forming the optimized control factors and levels of the improved orthogonal experiment, as shown in Tables 5 and 6. The range analysis results of the improved orthogonal experiment are shown in Table 7.

Table 5. Control factors and levels of the improved orthogonal experiment.

	A (W/m K)	B (mm)	C (mm)	D (W/m K)	E (Errors)
Level 1	0.3	0.5	0.5	0.06	1
Level 2	0.5	1	1	0.08	2
Level 3	0.8	1.5	3	0.1	3
Level 4	1.2	2	5	0.12	4

Table 6. Test combination and simulation results of the improved orthogonal experiment.

Test Number	A (W/m K)	B (mm)	C (mm)	D (W/m K)	E (Errors)	Junction Temperature (°C)
1	0.3	0.5	0.5	0.06	1	79.9858
2	0.3	1	1	0.08	2	77.6081
3	0.3	1.5	3	0.1	3	76.0275
4	0.3	2	5	0.12	4	75.3698
5	0.5	0.5	1	0.1	4	76.7808
6	0.5	1	0.5	0.12	3	77.1581
7	0.5	1.5	5	0.06	2	75.2461
8	0.5	2	3	0.08	1	74.3507
9	0.8	0.5	3	0.12	2	74.4886
10	0.8	1	5	0.1	1	74.0475
11	0.8	1.5	0.5	0.08	4	75.4599
12	0.8	2	1	0.06	3	74.3482
13	1.2	0.5	5	0.08	3	74.2745
14	1.2	1	3	0.06	4	74.3382
15	1.2	1.5	1	0.12	1	72.6562
16	1.2	2	0.5	0.1	2	72.9218

Table 7. Range analysis results of the improved orthogonal experiment.

	A (W/m K)	B (mm)	C (mm)	D (W/m K)	E (Errors)
K1	308.9911	305.5297	305.5256	303.9183	301.0402
K2	303.5357	303.1518	301.3932	301.6931	300.2645
K3	298.3442	299.3897	299.205	299.7776	301.8083
K4	294.1907	296.9905	298.9379	299.6727	301.9487
k1	77.2478	76.3824	76.3814	75.9796	75.2601
k2	75.8839	75.7880	75.3483	75.4233	75.0661
k3	74.5861	74.8474	74.8013	74.9444	75.4521
k4	73.5477	74.2476	74.7345	74.9182	75.4872
R	3.7001	2.1348	1.6469	1.0614	0.4211
Range analysis's order	1	2	3	4	5

According to Table 7, the order in which the various factors affecting the junction temperature is the thermal conductivity of the molding compound (A) > chip staggered length (B) > the thermal conductivity of the adhesive film (C) > chip thickness (D). After the second range analysis, the range of the chip staggered length is significantly greater than the range of the thermal conductivity of the adhesive film. Thus, compared with conducting only one orthogonal experiment, although conducting orthogonal experiments twice continuously cannot improve the final effect of the optimization, it can more accurately obtain the ranking results of the degree of influence on the junction temperature. It is necessary to minimize the junction temperature of the module to obtain the optimal design of the parameters and thereby enhance the thermal reliability of the module. The results listed in Table 7 indicate that the optimal design is the A4B4C4D4 combination, and the optimal temperature distribution is shown in Figure 9. It can be observed that the optimal junction temperature of the module is 71.32 °C. Compared with the initial junction temperature of 74.87 °C, the optimal junction temperature has decreased by 4.74%, and the heat dissipation performance of the module has been improved.

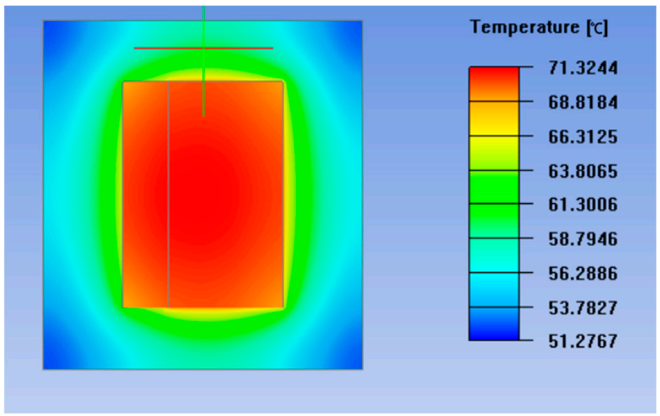

Figure 9. The optimal temperature distribution of the module.

5. Thermal Performance Benchmarking

In this section, the thermal characteristics of the six-layer stagger-stacked DDR module will be first compared with the performance of a cantilever package for the same six chips with the same power dissipation. The internal chips are set to 0.5 W, respectively. Next, the thermal performance of the three-layer stagger-stacked DDR module will be compared to the three-layer pyramid, cantilever, and pyramid combination package.

5.1. Benchmarking with Six-Layer Cantilever Package

Figures 10 and 11 compare the schematic diagram of a six-layer cantilever stacked package and a six-layer stagger-stacked DDR module. Except for the different stacking methods, the other conditions remain the same. Each chip is set to 0.5 W, and the ambient temperature is 25 °C. Both of the two types of packages are built in a natural convection environment of opening boundaries. The results of the steady-state thermal simulation are shown as temperature contours in Figures 12 and 13.

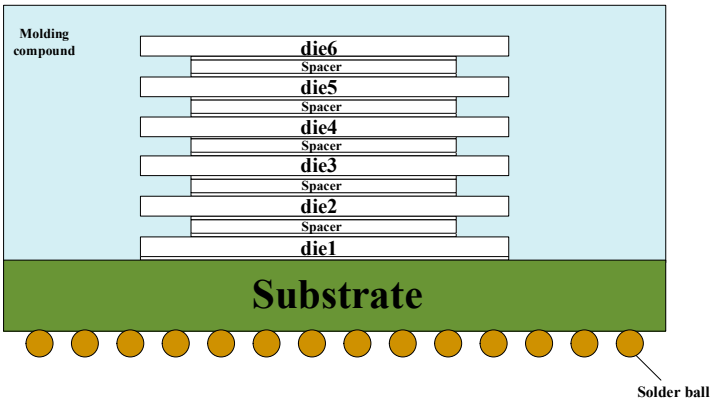

Figure 10. Schematic diagram of a six-layer cantilever stacked package.

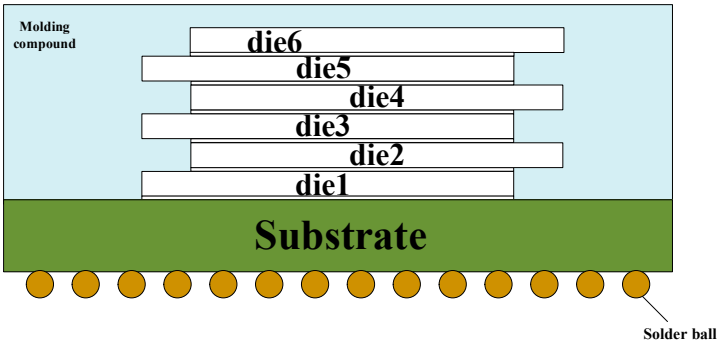

Figure 11. Schematic diagram of a six-layer stagger-stacked DDR module.

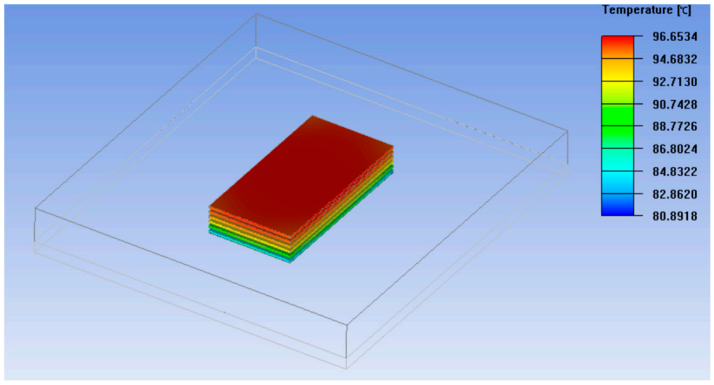

Figure 12. Initial temperature distribution of six-layer cantilever package.

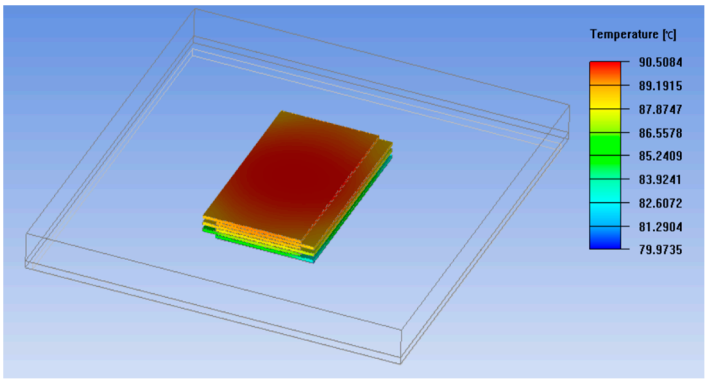

Figure 13. Initial temperature distribution of six-layer stagger-stacked DDR module.

It is observed that the six-layer cantilever package reaches a maximum temperature of 96.65 °C, and the value is 90.51 °C for the six-layer stagger-stacked DDR module. The junction temperature of the two types of packages exceeds the operation limit (85 °C). Therefore, it is necessary to optimize the heat dissipation of the two types of packages. By using the conclusions of the orthogonal experiment design, the thermal conductivity of the molding compound and adhesive film is increasing, and the thickness of the chip and chip staggered length is increasing to 2 mm. Figures 14 and 15 show the optimal temperature distribution of the two types of packages. As a result, an optimized six-layer stagger-stacked DDR module is approximately 3.62% lower in junction temperature than an optimized six-layer cantilever package.

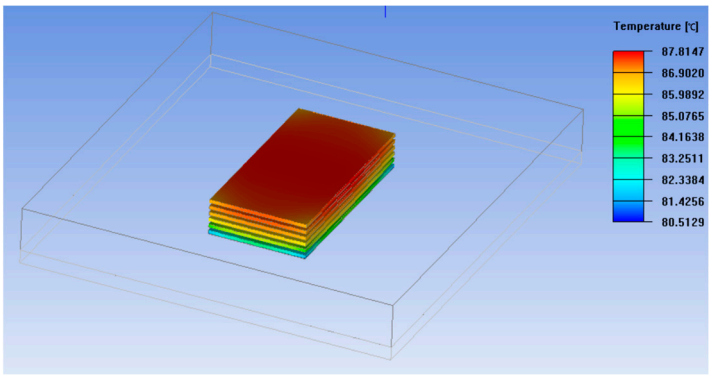

Figure 14. Optimal temperature distribution of six-layer cantilever package.

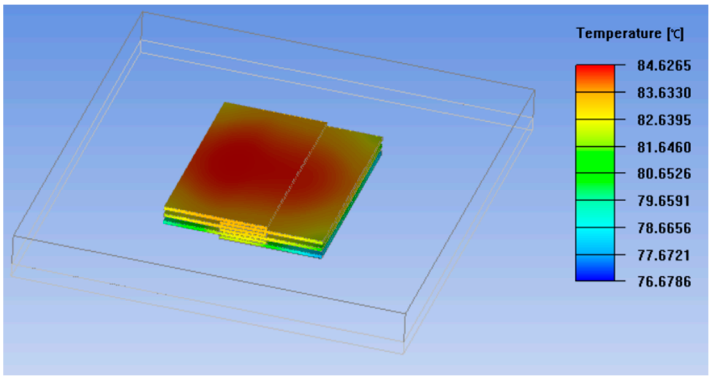

Figure 15. Optimal temperature distribution of six-layer stagger-stacked DDR module.

5.2. Benchmarking with Three-Layer Cantilever Package

In this section, we compare the thermal performance of the three-layer pyramid package and the three-layer cantilever and pyramid combination package with the thermal performance of the three-layer stagger-stacked DDR module. The schematic diagrams of the three types of packages are shown in Figures 16–18. Each chip is set to 0.4 W. The ambient temperature is set to 25 °C, and the three structures are optimized by the orthogonal experiment method. The junction temperature comparison of the three structures is shown in Table 8.

Table 8. Comparison of heat dissipation characteristics of three different structures.

	Initial Junction Temperature (°C)	Optimal Junction Temperature (°C)
Three-layer pyramid package	75.59	70.54
Three-layer cantilever and pyramid combination package	74.18	68.81
Three-layer stagger-stacked DDR module	70.72	64.93

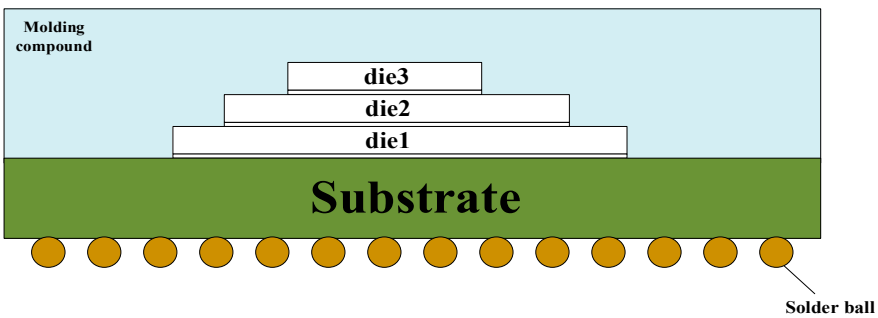

Figure 16. Schematic diagram of a three-layer pyramid package.

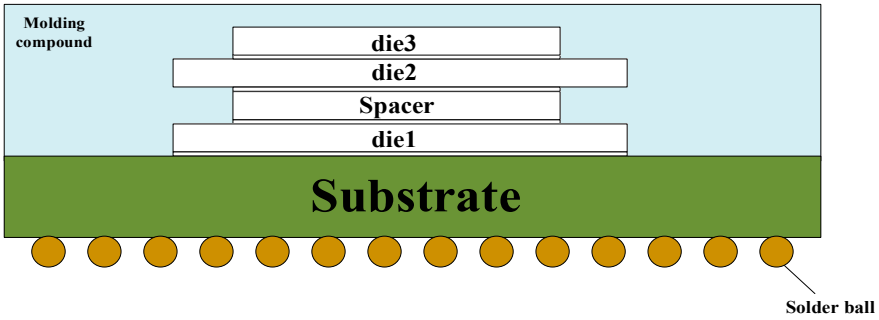

Figure 17. Schematic diagram of a three-layer cantilever and pyramid combination package.

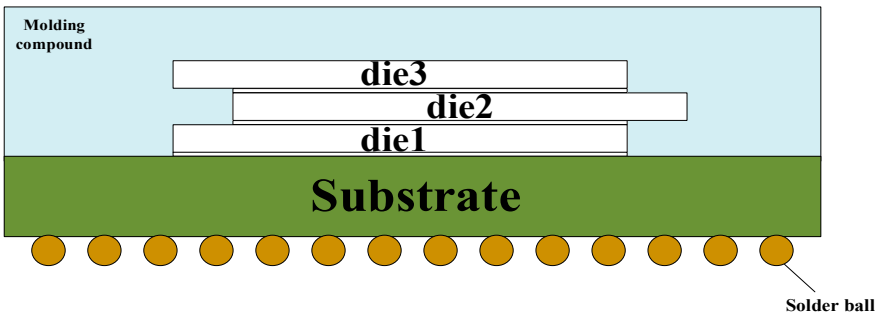

Figure 18. Schematic diagram of a three-layer stagger-stacked DDR module.

It can be observed from Table 8 that the heat dissipation performance of the stagger-stacked DDR module is the best. After optimization by the orthogonal experiment method, the junction temperature of the stagger-stacked DDR module is 7.95% lower than that of the pyramid package and 5.63% lower than that of the cantilever and pyramid combination package.

6. Conclusions and Prospects

In this paper, we firstly present the stagger-stacked DDR module, which contains five layer chips: the top die is one IPD chip and the other dies are memory chips. The thermal simulation structure of the module is built, and the initial temperature distribution is obtained. The result demonstrates that the junction temperature rises by about 50 °C; hence, this paper studies the thermal performance of the module from four aspects: the thermal conductivity of the molding compound, chip thickness, chip staggered length, and the thermal conductivity of the adhesive film. It is found that increasing the chip staggered length is beneficial to dissipating heat. Subsequently, the orthogonal experiment is used twice continuously to optimize the overall heat dissipation performance of the module, and an optimal design is gained. Compared with the initial junction temperature, the optimal junction temperature has decreased by 4.74%. Benchmarking of the package thermal characteristics reveals the proposed module to show good thermal performance compared to the other three types of packages. The research presented in this paper offers valuable reference significance for the thermal design studies of staggered-stacked DDR module packaging. However, there are still aspects that warrant further exploration. In this paper, we are only looking at the thermal design of staggered stacked DDR module packages in the case of wire bonding. In the future, we can study the heat dissipation of a stacked DDR module with TSV (Through Silicon Via). In addition, this paper is studying the thermal performance of staggered-stacked DDR modules, but it lacks actual measurement results. Further research will concentrate on related content, striving to make improvements in the next phase.

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Conflicts of Interest: The authors declare no conflicts of interest.

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