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Analysis of a Multilevel Dual Active Bridge (ML-DAB) DC-DC Converter Using Symmetric Modulation

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Abstract: Dual active bridge (DAB) converters have been popular in high voltage, low and medium power DC-DC applications, as well as an intermediate high frequency link in solid state transformers. In this paper, a multilevel DAB (ML-DAB) has been proposed in which two active bridges produce two-level (2L)-5L, 5L-2L and 3L-5L voltage waveforms across the high frequency transformer. The proposed ML-DAB has the advantage of being used in high step-up/down converters, which deal with higher voltages, as compared to conventional two-level DABs. A three-level neutral point diode clamped (NPC) topology has been used in the high voltage bridge, which enables the semiconductor switches to be operated within a higher voltage range without the need for cascaded bridges or multiple two-level DAB converters. A symmetric modulation scheme, based on the least number of angular parameters rather than the duty-ratio, has been proposed for a different combination of bridge voltages. This ML-DAB is also suitable for maximum power point tracking (MPPT) control in photovoltaic applications. Steady-state analysis of the converter with symmetric phase-shift modulation is presented and verified using simulation and hardware experiments.

1. Introduction

Because of various advantages, such as high power density, buck and boost conversion, high frequency operation, bi-directional power flow and galvanic isolation, the dual active bridge (DAB) has been widely used since the concept was first introduced in [1]. Conventionally, the DAB is a dc-dc power converter, though it has many applications in DC-AC, AC-DC [2], AC-AC [3] conversion, solid state transformers (SST) [3,4] and automotive power converters [5,6]. Most converters use the full-bridge DAB, which produces two-level (2L) square waves across the high frequency transformer. For medium and high voltage applications, DAB converters are usually cascaded [4,7] to achieve the desired high voltages due to the voltage limitation of the commercially available semiconductor switches. Experimental results, using 15-kV silicon carbide (SiC) based insulated-gate bipolar transistor (IGBT), have been reported in [8]. The multilevel DAB (ML-DAB) can overcome this voltage constraint of semiconductor switches to a great extent. The ML-DAB can be used in medium voltage (generally 2.3 kV to 6.6 kV [9]) applications without cascading or, if cascaded, can reduce the number of cascading modules in high voltage power conversion, such as high voltage direct current (HVDC) [7] applications.

Power converters synthesizing more than two voltage levels, such as the neutral point clamped (NPC), cascaded H-bridge (CHB) and flying capacitor (FC), are traditionally known as multilevel converters. Usually, the multilevel topology is used in medium or high voltage inverter applications [9,10]. The CHB topology is typically used with multiple cascaded DABs to achieve higher voltages. In the CHB topology, a DAB module itself does not synthesize multilevel (e.g., 3L, 5L, 7L, and so on) voltages, like NPC or FC. Because of the simple control and modulation scheme along with the simpler circuit structure, the 3L NPC is ahead of others in various industrial applications [9]. Very few works have been published on ML-DAB. A silicon carbide junction gate field-effect transistor (SiC-JFET) based 25-kW, high switching frequency DAB has been proposed in [11], where both primary and secondary bridges produce two-level voltages, although the secondary side bridge is formed in the NPC configuration. A detailed analysis on a semi-dual active bridge (S-DAB) has been presented in [12], where the primary and secondary bridges produce 2L and 3L voltage waveforms, respectively, which are phase-shifted to control the power flow. The concept of symmetric modulation for 2L-to-5L bridge voltages with an NPC-based secondary bridge has been introduced by the authors in [13], which has the advantage of having simple mathematical representation and a minimum number of parameters to define the voltage waveforms and to control the power flow through the ML-DAB. In [14], an NPC-based multilevel DAB is reported with capacitor voltage balancing.

This paper will analyze the design, modulation and power flow control of 3L NPC-based ML-DAB configurations for different cases where two active bridges produce 2L-5L, 5L-2L and 3L-5L voltage waveforms across the high frequency transformer. Section 2 discusses 3L NPC-based ML-DAB configurations with a symmetric modulation and switching scheme. Power flow equations for various ML-DAB configurations with soft-switching analysis are shown in Section 3. Section 4 discusses the applications of ML-DAB, such as maximum power point tracking (MPPT) for photovoltaic (PV) applications. Sections 5 and 6 present the simulation results and conclusions, respectively.

2. ML-DAB Topologies with Symmetric Phase-Shift Modulation

In this ML-DAB configuration, two bridges are assumed to have different dc voltage levels (*i.e.*, V_S and V_P, where $V_P > V_S$) where V_P and V_S are high and low dc bus voltages, respectively. Figures 1 and 2 show voltage step-up and step-down schematics of NPC-based 2L-5L DAB, respectively. Most DAB-based power electronic converters deal with different voltage levels at the two ends of the converter, and this ML-DAB is very suitable for such applications. If the required voltage level is much higher than the dc bus voltage V_P, a higher voltage may be achieved by cascading multiple ML-DABs, which, in turn, facilitates conversion of large-scale (in the order of megawatts) power with a fewer number of ML-DAB modules. This methodology improves the overall efficiency and increases the power density.
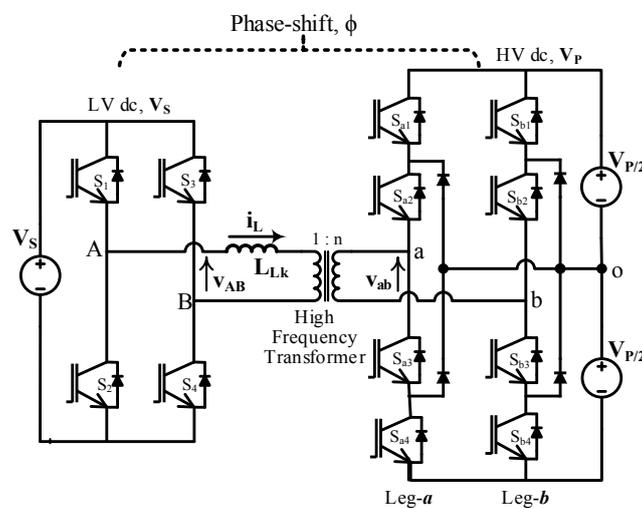
Figure 1. Boost configuration ($V_P > V_s$) of a multilevel dual active bridge (ML-DAB), where the transformer primary voltage (v_{AB}) is two-level (2L) and the secondary (v_{ab}) is of 5L.
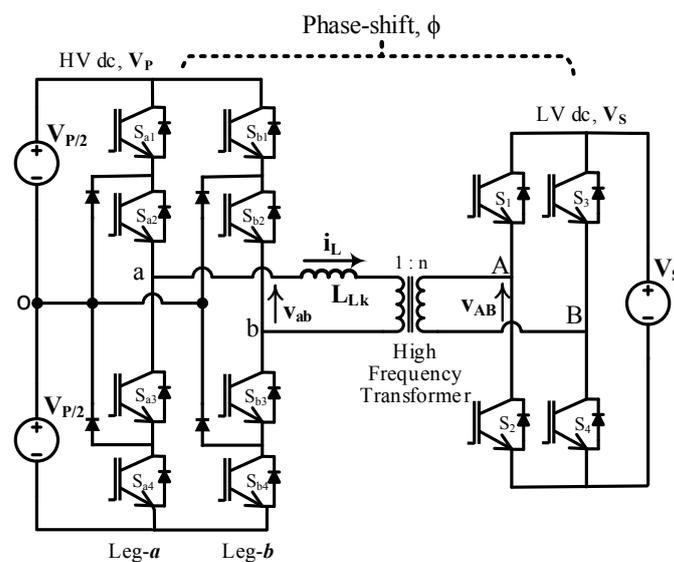
Figure 2. Buck configuration ($V_s < V_P$) of the ML-DAB where the transformer primary voltage (v_{ab}) is of 5L and the secondary (v_{AB}) is of 2L.

2.1. Neutral Point Diode Clamped Configuration

The neutral point diode clamp (NPC) is one of the most popular and widely-used multilevel topologies in medium and high voltage industrial applications. In this ML-DAB, three-level (3L) diode clamped legs (leg-*a*, *b* in Figures 1 and 2) are used to produce a leg-to-leg five-level (5L) voltage waveform v_{ab}. The low voltage bridge is switched so as to produce a two-level (2L) square waveform v_{AB} across the transformer. Compared to the 2L voltage source converter, the 3L-NPC configuration employs clamping diodes to connect the phase output to the neutral point "*o*", as shown in Figures 1 and 2, which produces a 3L voltage at each NPC leg. The voltage sources (*i.e.*, $V_s, \frac{V_P}{2}$) shown in Figures 1 and 2 are practically replaced by bulk capacitors, and the input and/or the output of the ML-DAB usually are followed by a source, a load or other converters in real applications. This ML-DAB can be configured for single phase or three phases with bi-directional power-flow capability by using current bi-directional switches and a suitable modulation scheme. In this paper, we are analyzing different cases of ML-DAB assuming a single-phase transformer with unidirectional power flow from the 2L bridge to the 5L bridge. The bi-directional power flow can easily be controlled with the phase-shift angle (ϕ) between the active bridges. Power always flows from the voltage-leading bridge to the voltage-lagging bridge.
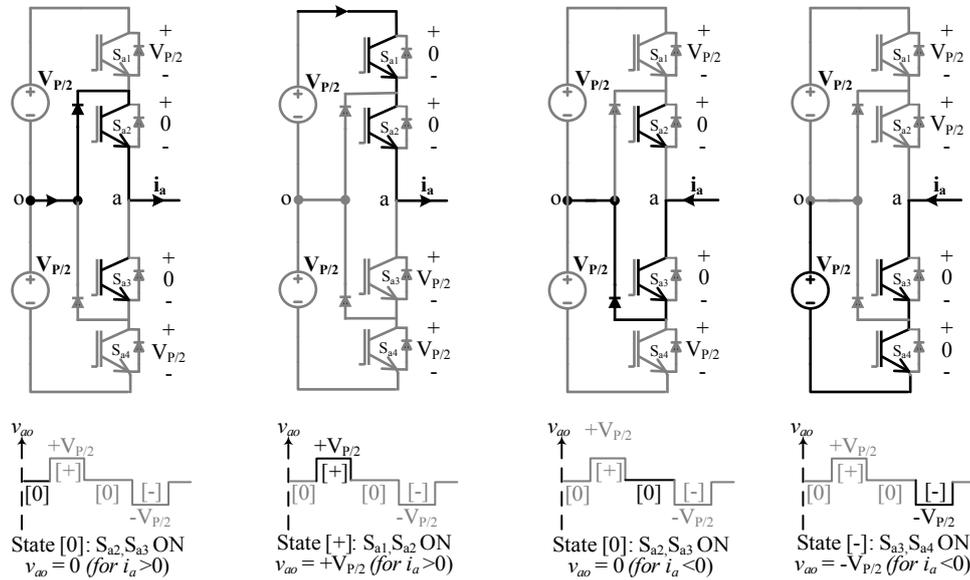
2.2. Switching States of the 3L-NPC Bridge

The NPC inverter concept was first proposed in 1980 [15]. Since then, researchers have contributed to several aspects of this converter, such as various modulation schemes, the number of voltage levels, capacitor voltage balancing, harmonics mitigation and active clamping instead of diodes. Switching and modulation details of a 3L-NPC as a three-phase inverter are studied in detail in [16]. In ML-DAB operation, the switching pattern of NPC is slightly different from that in conventional inverters. Unlike 3L-NPC line frequency (*i.e.*, 50 or 60 Hz) inverters, the switching frequency is considered the fundamental frequency in an ML-DAB. Table 1 shows how a three-level voltage is synthesized in a 3L-NPC leg for both positive ($i_a > 0$) and negative ($i_a < 0$) current flow.

Table 1. Switching states in a 3L-NPC leg.

Switching States	Status of the Switches in 3L-NPC Leg-*a*				3-Level LEG Voltage, v_{ao}
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	
+	ON	ON	OFF	OFF	$+\frac{V_P}{2}$
0	OFF	ON	ON	OFF	0
−	OFF	OFF	ON	ON	$-\frac{V_P}{2}$

Figure 3 shows some major switching states to form a 3L (*i.e.*, $+\frac{V_P}{2}, 0, -\frac{V_P}{2}$) voltage waveform v_{ao}. The main advantage of the 3L-NPC is that all of the switching devices in a leg withstand only half (*i.e.*, $\frac{V_P}{2}$) of the dc bus voltage (*i.e.*, V_P) during commutation between states, which also yields lower $\frac{dv}{dt}$ in comparison to the two-level inverter. Switching between "+" and "−" states are not considered, because this scheme involves all four switches (S_{a1} to S_{a4}) in a leg, two being turned on and the other two being commutated off, during which dynamic voltage on each switch may not be kept the same [16]. This also causes double the switching losses. A small dead time is allowed between different states. The leg-*b* is

also switched in a similar pattern to create a 3L voltage waveform v_{bo}. In this proposed modulation scheme, v_{bo} is phase-shifted from v_{ao} by an amount $(\alpha + \beta)$ to produce a leg-to-leg 5L voltage waveform waveform v_{ab} across the transformer (Figure 4).

**Figure 3.** Switching states and corresponding 3L voltage (v_{ao}) synthesized from leg-*a* of a 3L-NPC bridge.
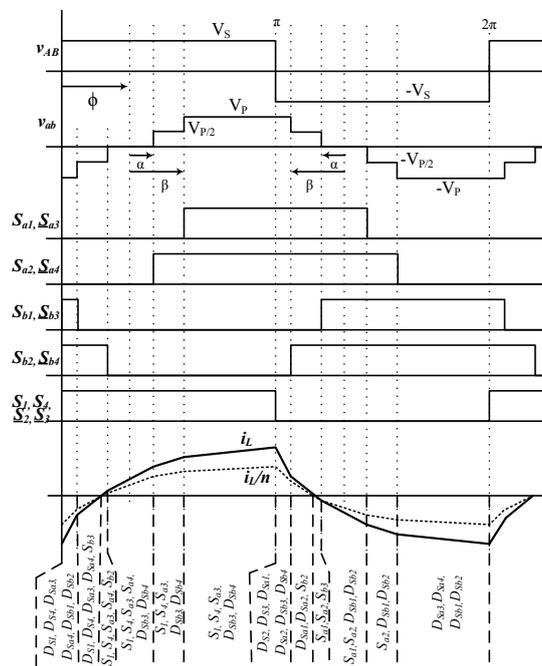
Figure 4. Switch pulses and corresponding voltage waveforms and primary current in a 2L-5L DAB boost topology.

The two-level bridge has two legs, each having two complementary switches operating with a 50% duty cycle. When S_1, S_4 are turned on, the leg-to-leg square wave voltage $v_{AB} = +V_s$, and when S_2, S_3 are turned on, $v_{AB} = -V_s$. Gate pulses for all twelve switches (*i.e.*, S_1 to S_4 and S_{a1} to S_{a4}, S_{b1} to S_{b4}) for

both 2L and 5L bridges in a boost topology are shown in Figure 4 with the resulting voltage waveforms (v_{AB}, v_{ab}) across the high frequency transformer and the current (i_L and $\frac{i_L}{n}$) through the leakage inductor.

2.3. Symmetric Modulation

In order to synthesize the 5L voltage v_{ab}, the switching pulses and the resulting voltage waveform are defined with respect to angular distances (*i.e.*, α, β) instead of the duty cycle. These angles α, β are measured symmetrically at zero, π and 2π within a switching period (Figure 5). The zero and π are considered at the mid-point of the zero voltage level of the 5L voltage v_{ab}. Defining v_{ab} in such a symmetrical way is advantageous in terms of the minimum numbers of parameters (α, β) required, which, in turn, easily describe and derive a simple mathematical expression for power flow in the ML-DAB. These parameters α and β shape the multilevel voltage waveform and can be utilized in the improvement of the total harmonic distortion (THD) and voltage balancing of the capacitors [14]. The phase-shift angle ϕ is independent of α, β and acts as the control parameter to control the power flow in the ML-DAB.
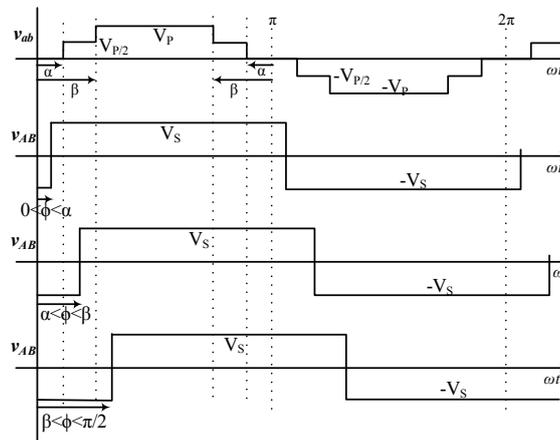
Figure 5. Voltage waveforms in a 5L-2L DAB for three different cases of buck topology when v_{AB} is formed using $D = 0.5$.

In order to produce a zero-average symmetric alternating waveform, the low-voltage (V_S) bridge legs should be switched complementarily at the duty cycle (D) in a range of zero to 50% ($0 < D \leq 0.5$). If $D = 0.5$, a 2L ($v_{AB} \equiv +V_S, -V_S$) voltage v_{AB} will be formed, and if $D < 0.5$, a 3L ($v_{AB} \equiv +V_S, 0, -V_S$) voltage will be produced (Figure 6). This 3L voltage at the low voltage bridge is also generated symmetrically, equally spaced from zero and π by an angle γ. This single parameter γ can define the 3L v_{AB} for the whole range of $D < 0.5$.
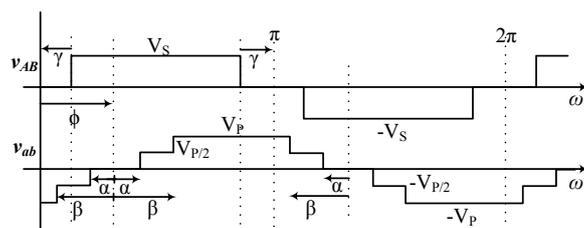
Figure 6. Voltage waveforms in a 3L-5L DAB boost topology when v_{AB} is formed using $D < 0.5$.

3. Power Flow Equations and Soft Switching in ML-DAB

In ML-DAB, power flow is controlled by the phase-shift angle (ϕ) between v_{AB} and v_{ab}, like conventional DAB. The leakage inductance of the high frequency transformer acts as the main energy transfer element. This primary referred leakage inductance is assumed externally as L_{Lk} in Figures 1 and 2. In order to analyze the power flow through each type of ML-DAB shown in Figures 4–6, we will analyze the current i_L through the leakage inductor for each topology.

3.1. 2L-5L DAB Boost Topology

The switching and modulation for a 2L-5L DAB boost topology is shown in Figure 4. The 2L v_{AB} is assumed to start at angle zero, and 5L v_{ab} is lagging v_{AB} by the phase-shift angle $\phi, \left(0 < \phi < \frac{\pi}{2}\right)$. From the basic inductor voltage relation we get,

$$v_L = L.\frac{di_L}{dt}$$
$$or, i_L(t) = \frac{1}{L}.\int_{t_1}^{t_2} v_L.dt$$
$$or, i_L(\theta) = \frac{1}{\omega L}.\int_{\theta_1}^{\theta_2} v_L.d\theta; \text{ where, } \theta = \omega t$$

$$(1)$$

One switching cycle time period has been converted to 2π radians in the following equations. Now, writing this $i_L(\theta)$ equation for each segment of v_L from zero to π as shown in Figure 4, we get, for $0 < \theta < (\phi - \beta)$:

$$i_L(\theta) = \frac{V_s + \frac{V_P}{n}}{\omega L}.\theta + i_L(0); \ i_L(\phi - \beta) = \frac{V_s + \frac{V_P}{n}}{\omega L}.(\phi - \beta) + i_L(0),$$

$$(2)$$

for $(\phi - \beta) < \theta < (\phi - \alpha)$:

$$i_L(\phi - \alpha) = \frac{V_s + \frac{V_P}{2n}}{\omega L}.(\phi - \alpha - \phi + \beta) + i_L(\phi - \beta),$$

$$(3)$$

for $(\phi - \alpha) < \theta < (\phi + \alpha)$:

$$i_L(\phi + \alpha) = \frac{V_s}{\omega L}.(\phi + \alpha - \phi + \alpha) + i_L(\phi - \alpha),$$

$$(4)$$

for $(\phi + \alpha) < \theta < (\phi + \beta)$:

$$i_L(\phi + \beta) = \frac{V_s - \frac{V_P}{2n}}{\omega L}.(\phi + \beta - \phi - \alpha) + i_L(\phi + \alpha),$$

$$(5)$$

for $(\phi + \beta) < \theta < \pi$:

$$i_L(\pi) = \frac{V_s - \frac{V_P}{n}}{\omega L}.(\pi - \phi - \beta) + \frac{V_s - \frac{V_P}{2n}}{\omega L}.(\beta - \alpha) + \frac{V_s}{\omega L}.(2\alpha) + \frac{V_s + \frac{V_P}{2n}}{\omega L}.(\beta - \alpha) + \frac{V_s + \frac{V_P}{n}}{\omega L}.(\phi - \beta) + i_L(0),$$

$$(6)$$

Assuming zero average current through the transformer, $i_L(0) = -i_L(\pi)$:

$$or, -2i_L(0) = \frac{V_s}{\omega L}.(\pi) - \frac{V_P}{2n\omega L}.(2\pi - 4\phi)$$
$$or, i_L(0) = \frac{V_P}{n\omega L}.\left(\frac{\pi}{2} - \phi\right) - \frac{V_s}{\omega L}.\left(\frac{\pi}{2}\right)$$

$$(7)$$

Putting this expression of i_L(zero) in the above equations, we can get the $i_L(\theta)$ at different points,

$$i_L(\phi - \beta) = \frac{V_s}{\omega L} \cdot \left(\phi - \beta - \frac{\pi}{2}\right) + \frac{V_P}{n\omega L} \cdot \left(\frac{\pi}{2} - \beta\right),$$
$$i_L(\phi - \alpha) = \frac{V_s}{\omega L} \cdot \left(\phi - \alpha - \frac{\pi}{2}\right) + \frac{V_P}{n\omega L} \cdot \left(\frac{\pi}{2} - \frac{\alpha}{2} - \frac{\beta}{2}\right),$$
$$i_L(\phi + \alpha) = \frac{V_s}{\omega L} \cdot \left(\phi + \alpha - \frac{\pi}{2}\right) + \frac{V_P}{n\omega L} \cdot \left(\frac{\pi}{2} - \frac{\alpha}{2} - \frac{\beta}{2}\right),$$
$$i_L(\phi + \beta) = \frac{V_s}{\omega L} \cdot \left(\phi + \beta - \frac{\pi}{2}\right) + \frac{V_P}{n\omega L} \cdot \left(\frac{\pi}{2} - \beta\right).$$

$$(8)$$

The average power flow expression from the primary to secondary bridge through the leakage inductance can be written as follows:

$$P_o = \frac{1}{\pi} \int_0^\pi v_{AB}(\theta) \cdot i_L(\theta) \cdot d\theta$$

$$or, P_o = \frac{V_s}{2\pi} [\{i_L(0) + i_L(\phi - \beta)\} \cdot (\phi - \beta) + \{i_L(\phi - \beta) + i_L(\phi - \alpha)\} \cdot (\beta - \alpha) + \{i_L(\phi - \alpha) + i_L(\phi + \alpha)\} \cdot (2\alpha)$$

$$+ \{i_L(\phi + \beta) + i_L(\phi + \alpha)\} \cdot (\beta - \alpha) + \{i_L(\phi + \beta) + i_L(\pi)\} \cdot (\pi - \phi - \beta)]$$

$$(9)$$

After calculating the above power equation using (3), we get the simplified power equation as follows,

$$P_o = \frac{V_P V_s}{n\omega L} \cdot \left(\phi - \frac{\phi^2}{\pi} - \frac{\alpha^2}{2\pi} - \frac{\beta^2}{2\pi}\right)$$

$$(10)$$

$$or, P_{o_{p.u.}} = m\left(\phi - \frac{\phi^2}{\pi} - \frac{\alpha^2}{2\pi} - \frac{\beta^2}{2\pi}\right); \; where \; m = \frac{V_P}{nV_s}, P_{base} = \frac{V_s^2}{\omega L}$$

$$(11)$$

where P_o is the average power ($P_{o_{p.u.}}$ is the per unit power) measured at the output of the converter with the variables defined as, $\omega = 2\pi f_s$, where f_s is the switching frequency, n is the transformer turns ratio, m is the voltage conversion ratio defined as $m = \frac{V_P}{nV_s}$ and L is the primary referred inductance (L_{Lk}) used at the high frequency link. The per unit power *vs.* ϕ and β, while α is chosen to be fixed at 10^0, is shown in Figure 7 for different m values. Power *vs.* ϕ and β planes with different m-values for a 2L-5L DAB boost topology are shown in Figure 7.
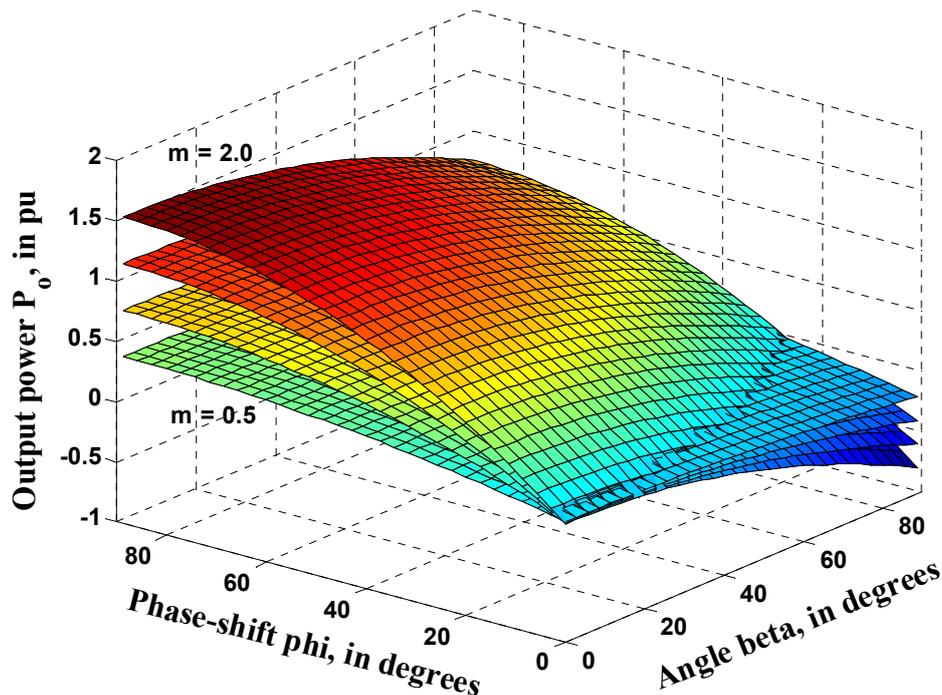

Figure 7. ML-DAB output power $P_{o_{p.u}}$ *vs.* ϕ and β with $\alpha = 10^0$ for $m = 0.5, 1, 1.5$ and 2.

3.2. 5L-2L DAB Buck Topology

The voltage waveforms for a 5L-2L DAB buck topology are shown in Figure 5. The 5L v_{ab} is assumed to start at angle zero, and 2L v_{AB} is lagging by the phase-shift angle ϕ. In this topology, based on the value of ϕ, there may be three cases, such as Case I: $0 < \phi < \alpha$, Case II: $\alpha < \phi < \beta$ and Case III: $\beta < \phi < \frac{\pi}{2}$. Each case has been analyzed to formulate a power flow equation using the same procedure described from (1) to (11).

$$\text{Case I: } P_o = \frac{V_P V_S}{n \omega L} \phi \left(1 - \frac{\alpha}{\pi} - \frac{\beta}{\pi}\right) ; \ 0 < \phi \leq \alpha \tag{12}$$

$$\text{Case II: } P_o = \frac{V_P V_S}{n \omega L} \left(\phi - \frac{\phi^2}{\pi} - \frac{\alpha^2}{2\pi} - \frac{\phi\beta}{\pi}\right) ; \ \alpha < \phi \leq \beta \tag{13}$$

$$\text{Case III: } P_o = \frac{V_P V_S}{n \omega L} \left(\phi - \frac{\phi^2}{\pi} - \frac{\alpha^2}{2\pi} - \frac{\beta^2}{2\pi}\right) ; \ \beta < \phi \leq \frac{\pi}{2} \tag{14}$$

Equation (14) may be considered as the generalized one and can be rewritten as follows,

$$P_o = m \frac{V_S^2}{\omega L} \left(\phi - \frac{\phi^2}{\pi} - \frac{\alpha^2}{2\pi} - \frac{\beta^2}{2\pi}\right); \text{ where } m = \frac{V_P}{n V_S} \tag{15}$$

Equations (10) and (15) are the same, which also validates the bi-directional power-flow capability of this ML-DAB converter only based on the phase-shift between primary and secondary side bridge voltages. Figure 8 shows the power flow from the 5L to 2L bridge for the three different cases described above.
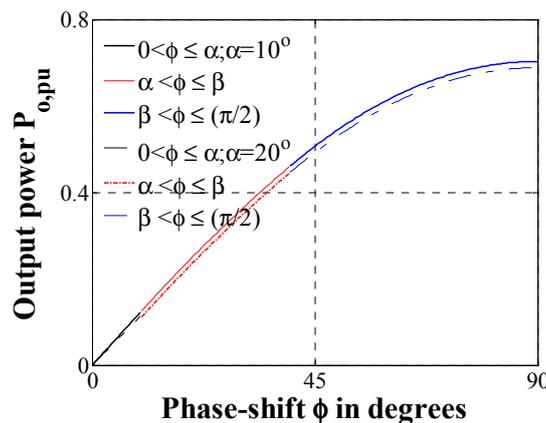

Figure 8. Power flow through DAB for all three cases (12) to (14), with respect to phase-shift ϕ; here, $\alpha = 10^0$ and 20^0, $\beta = 40^0$ are assumed for calculation.

3.3. 3L-5L DAB Boost Topology

The primary and secondary voltage waveforms for a 3L-5L DAB boost topology are shown in Figure 9. The 3L v_{AB} is assumed to start at angle γ after the zero, and 5L v_{ab} is lagging v_{AB} by the phase-shift angle ϕ. The pulse-width of 3L waveform is assumed symmetrically reduced by an angle of γ, which actually results from switch duty cycles $D < 0.5$. Using the same sector-wise inductor current analysis, as shown in (1) to (10), the power flow equation for this topology has been derived as,

$$P_{o_{p.u}} = \left[m\left\{\left(\phi - \frac{\phi^2}{\pi} + \frac{\beta\gamma}{\pi} + \frac{\gamma}{2} - \frac{\beta^2}{2\pi} - \frac{\alpha^2}{2\pi}\right)\right\} + \gamma\left\{\frac{\pi + \beta - \phi - \gamma}{2\pi}\right\}\right] \tag{16}$$

If we put $\gamma = 0$ in (16), it reduces to the 2L-5L power equation in (11). Similarly, if the condition is such that $\alpha = \beta = 0$, Equations (11) and (16) reduce to the conventional two-level DAB onverter equations [1].
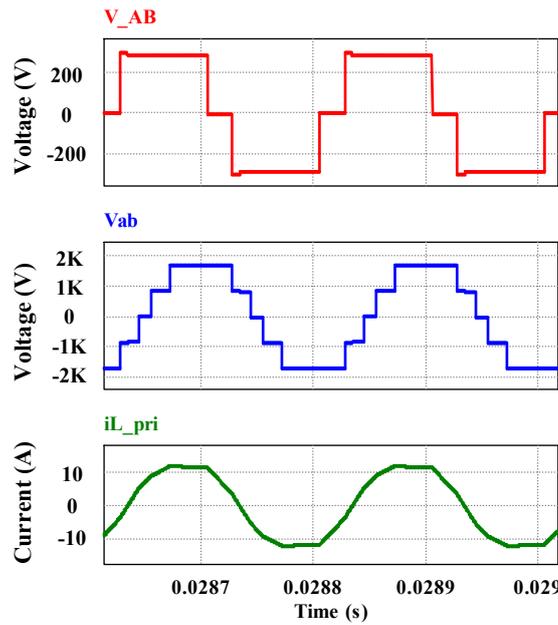
Figure 9. Primary 3L voltage v_{AB}, secondary 5L voltage v_{ab} and current through the primary primary referred leakage inductance i_L; where $V_s = 290$ V, $V_P = 1{,}868$ V, $\alpha = 10^0$, $\beta = 40^0$, $\gamma = 20^0$ and $\phi = 60^0$.

3.4. Soft Switching

The per unit output power *vs.* ϕ - β characteristics is shown in Figures 10 (15), where α is chosen as 15^0, as this value gives the minimum THD in five-level v_{ab} [14]. In Figure 11, the two-dimensional view of ϕ - β planes ease the visualization of the boundary values of $\phi > 55^0$ and $\beta \geq 46^0$ for achieving soft-switching both in primary (2L) and secondary (5L) bridges, as described in the following subsections.
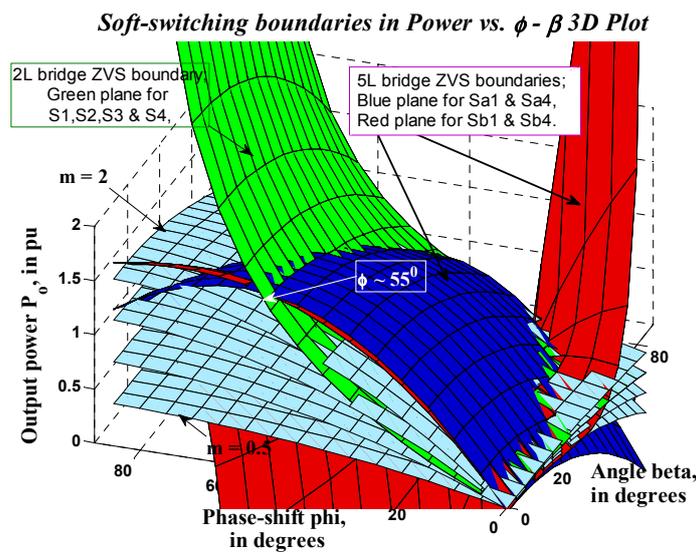
Figure 10. Soft switching boundaries shown in three-dimensional power *vs.* ϕ - β planes (where $\alpha = 15^0, 0 < \beta < 90^0$ and $0 < \phi < 90^0$); the grey planes (15) show the power *vs.* phi-beta relations for *m* = 0.5, 1, 1.5, 2; the green plane (17) is for two-level bridge, and the zero voltage switching (ZVS) is possible while operating under this plane; the blue (18) and red (19) planes are for five-level bridge leg-*a* and leg-*b*, respectively.
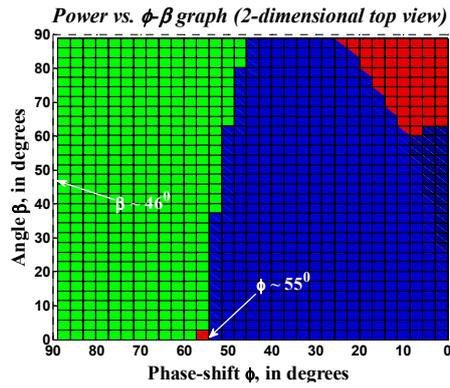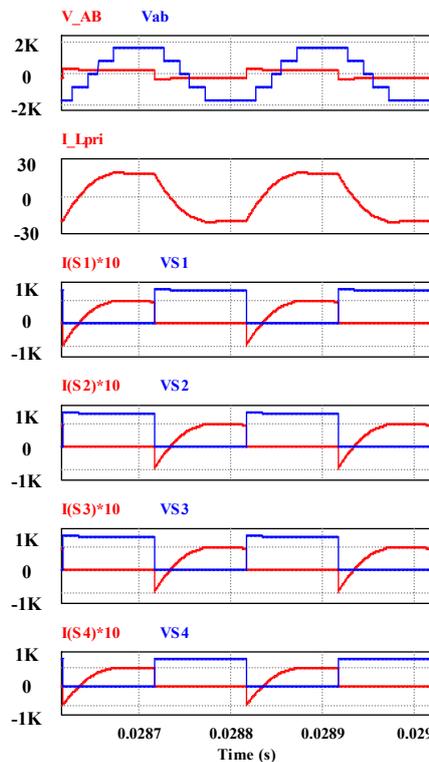
Figure 11. Two-dimensional view of Figure 10 showing the ZVS boundaries of ϕ and β.

The conventional 2L DAB topology can achieve zero voltage switching (ZVS) for all switches in the entire power range when m is equal to unity. The switching pulses for the 2L-5L DAB switches are shown in Figure 4. It is possible to achieve the same in the primary bridge (S_1 to S_4) with the condition of $i_L(0) < 0$ as shown in Figure 12.

3.4.1. Soft-Switching Conditions for the Two-Level (V_s) Bridge

From the current and voltage waveform of the switches in the primary two-level (V_s) bridge (Figure 12), we can say that the condition for soft-switching in the primary bridge should be,

$$i_L(0) < 0$$
$$or, \frac{V_P}{n\omega L}.\left(\frac{\pi}{2} - \phi\right) - \frac{V_s}{\omega L}.\left(\frac{\pi}{2}\right) < 0 \qquad (17)$$
$$or, \frac{V_P}{nV_s} \equiv m < \frac{\left(\frac{\pi}{2}\right)}{\left(\frac{\pi}{2} - \phi\right)}$$

Figure 12. Voltage across the transformer v_{AB} and v_{ab}, inductor current i_L and switch currents and voltages for S_1 to S_4.

### 3.4.2. Soft-Switching Conditions for the Leg-*a* of NPC (Five-Level) Bridge

Condition for S_{a1} and S_{a4} to be turned-on at ZVS: $i_L(\phi + \beta) > 0$

$$or, m > \frac{\{\pi - 2(\phi + \beta)\}}{(\pi - 2\beta)} \tag{18}$$

Boundary condition for S_{b1} and S_{b4} to be turned-on at ZVS: $i_L(\phi - \alpha) = 0$

$$or, m = \frac{\{\pi - 2(\phi - \alpha)\}}{\{\pi - (\alpha + \beta)\}} \tag{19}$$

In the NPC bridge, ZVS happens in the switches S_{a1}, S_{a4}, S_{b1}, S_{b4} during turn-on at $m = 1$. The rest of the switches (S_{a2}, S_{a3}, S_{b2}, S_{b3}) are also turned on at a favorable condition when the current through the switch is already zero, as shown in Figures 13 and 14.
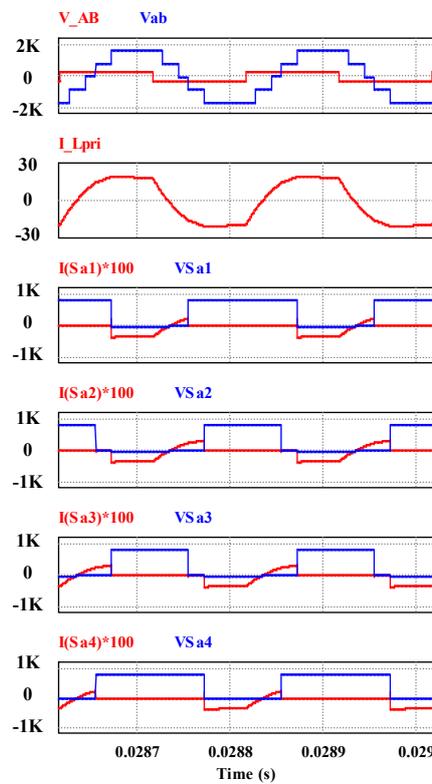
Figure 13. Voltage across the transformer v_{AB} and v_{ab}, inductor current i_L and switch currents and voltages for S_{a1} to S_{a4}.
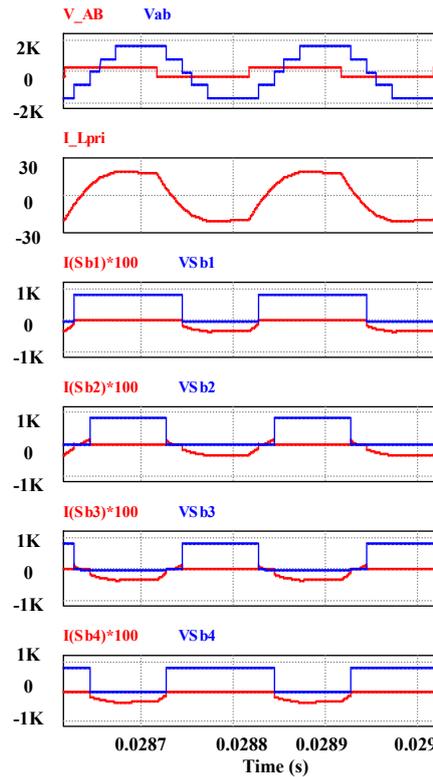
Figure 14. Voltage across the transformer v_{AB} and v_{ab}, inductor current i_L and switch currents and voltages for S_{b1} to S_{b4}.

3.5. Transformer Design

Considering the operating frequency and loss profile, various core materials, such as silicon steel, amorphous alloy and nano-crystalline, are used as the transformer core. For frequencies less than 10 kHz, the amorphous metglas material shows better performance. For this ML-DAB converter, amorphous metglas alloy 2605SA1 material has been chosen in the transformer core, because of its high permeability, low core losses, high saturation flux density and narrow hysteresis curve. The design of a 3.4-kVA transformer core and winding wires has been calculated using the area-product method as shown below:

The transformer core area product is defined as,

$$A_p = A_{core}A_{window} = \frac{k_{conv}(V_1 I_{1_{rms}} + V_2 I_{2_{rms}})}{k_w B_{mx} J_{mx} f_s} \tag{20}$$

where,

$V_1 \approx V_s = 292\,V, V_2 \approx V_P = 1{,}667\,V$, switching frequency $f_s = 5\,kHz$,

$I_{1_{rms}} = 16.2\,A, I_{2_{rms}} = 2.9\,A$ (RMS values calculated from simulation results),

$k_{conv} = 0.5$ (this factor value is chosen based on the converter topology),

$k_w = 0.4$ (this is the fill-factor having values usually within range of 0.3 to 0.6),

$B_{mx} = 1\,T$ (chosen based on the maximum saturation flux density being 1.56 T),

$J_{mx} = 6\,A/mm^2$ (peak current density with the use of litz wire).

From Equation (20), we get $A_p = 398{,}650\,mm^4$. By using metglass 2605SA1 AMCC-50 core specification, we get, $A_p = 462{,}000\,mm^4, A_{core} = 330\,mm^2, A_w = 1{,}400\,mm^2$.

The conductor cross-section can be found as $A_{cond_1} = \frac{I_{1_{rms}}}{J_{mx}} = 2.7\,mm^2, and\ A_{cond_2} = 0.48\,mm^2$.

The number of turns in the transformer is calculated as,

$$N_1 = \frac{k_{conv}V_1}{A_{core}f_sB_{mx}} = 89 \; turns,$$ and similarly $N_2 = 509 \; turns$. AWG 12 259/36 and AWG 20 38/30 Type 2 litz wire have been chosen for transformer primary and secondary windings, respectively.

4. Applications for ML-DAB

The proposed ML-DAB could find some suitable applications in a solid state transformer (SST), a front-end DC-DC converter in a photovoltaic (PV) system, a high step-up voltage DC-DC or an intermediate stage in ac-ac applications. Figure 15 shows a block diagram of the ML-DAB in a grid-connected large-scale PV system. The ML-DAB module along with inverter stage can act as a building block to be cascaded in order to achieve the 13.8-kV distribution voltage requirement.
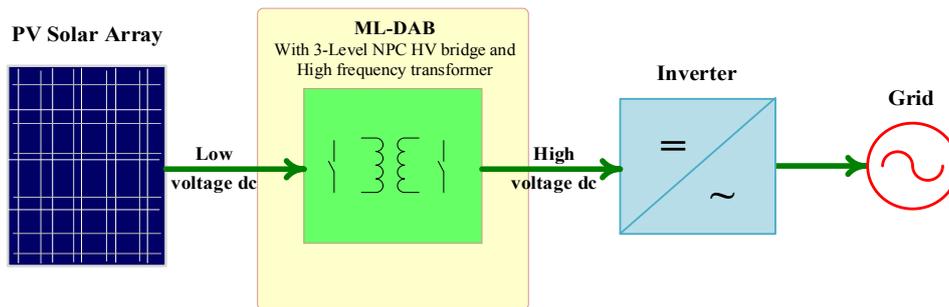

Figure 15. ML-DAB module in a grid-connected photovoltaic (PV) power converter.

This ML-DAB can control maximum power point tracking (MPPT) by controlling the phase-shift (ϕ) between two active bridges. This topology has the advantage of being modular and replacing the bulky line frequency transformer at the grid-end with a smaller high frequency power electronic transformer. Figures 16 and 17 show the MPPT performance in an ML-DAB in PV applications.
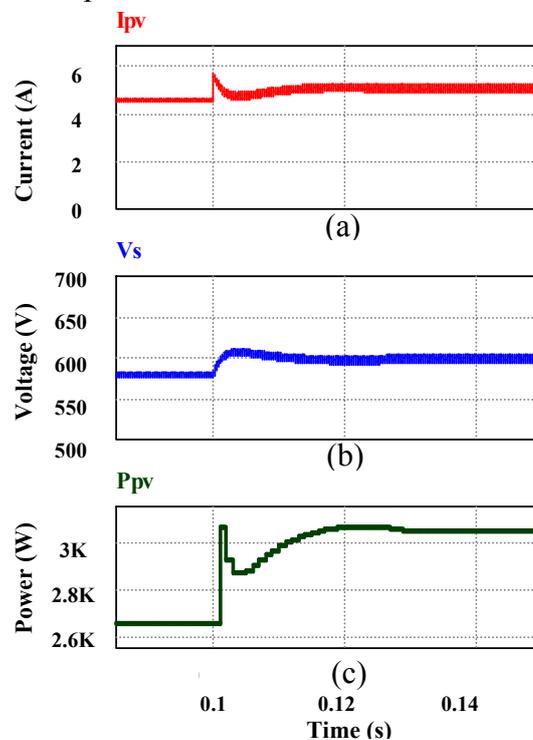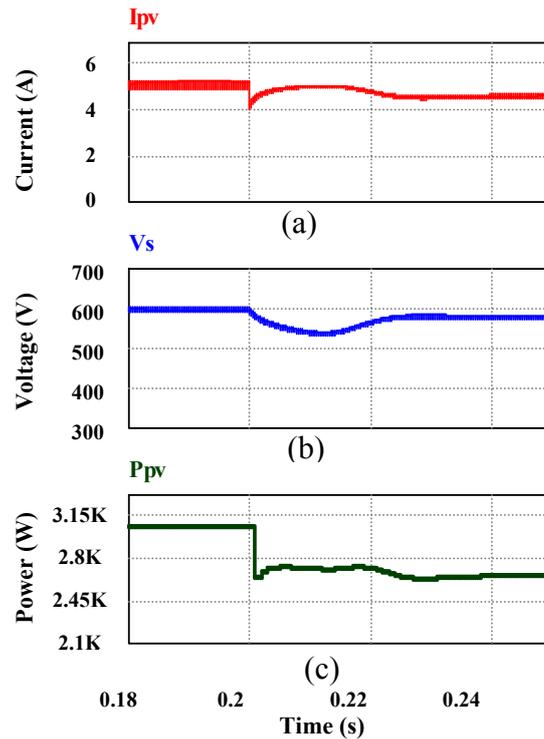

Figure 16. (From top to bottom) (**a**) Change in PV output current I_{pv} due to the change in light intensity from 800 W/m² to 1,000 W/m²; (**b**) corresponding change in voltage V_{pv} because of maximum power point tracking (MPPT) and (**c**) power P_{pv}.

Figure 17. (From top to bottom) (**a**) Change in PV output current I_{pv} due to the change in light intensity from 1,000 W/m^2 to 800 W/m^2; (**b**) corresponding change in voltage V_{pv} because of MPPT and (**c**) power P_{pv}.

## 5. Simulation and Experimental Results

A 3.34-kW ML-DAB module with a single phase high frequency transformer has been simulated in PSIM$^®$. The design parameters of the ML-DAB are listed in Table 2. Based on the soft-switching constraints for the ML-DAB switches, as shown in (16) to (19), a good choice for modulation parameters is used for simulation, which are $\alpha = 10$, $\beta = 30^0$ and $\phi = 70^0$. For the PV application explained in Section 4, 1,200-V or 1,700-V rated IGBTs are needed for ML-DAB. There are limitations in the switching characteristics of commercially available IGBTs when operated above 20 kHz. Hence, we have chosen 5 kHz for the proposed ML-DAB. The minimum input capacitor value has been theoretically calculated as 39 uF based on the ML-DAB parameters in Table 2. In the prototype, we have used a 100-uF polypropylene capacitor with a high ripple current carrying capacity.

As per (10) and Table 2, the key simulation results are shown in Figures 18 and 19 for a 2L-5L DAB in the steady state. The corresponding voltage and current waveforms for the 3L-5L ML-DAB have been shown in Figure 9 for the same input, output dc voltage and power rating as shown in Table 2. The phase-shift ϕ is actually the control parameter that is controlled by a proportional-integral (PI) controller sensing the variation in input (e.g., the PV panel's output) or output (e.g., the input voltage of an inverter) dc voltages of the ML-DAB. Figures 18 and 19 show the input and output voltage, current and average power of the ML-DAB obtained from simulation.

Table 2. Parameter values for a 3.34-kW ML-DAB based on the 2L-5L topology.

Item Description	Nominal Value
Power rating of a ML-DAB module, P_o	3.34 kW
$V_s = V_{dc(2L)}$	292 V
$V_P = V_{dc(5L)}$	1,668 V
ML-DAB high frequency transformer's turns ratio, $n = \dfrac{V_P}{V_s}$	5.716
$I_{L_{2L}}$	11.4 A
$I_{L_{5L}}$	2 A
$I_{L_{2L(rms)}}$	17 A
Switching frequency, f_s	5 kHz
Leakage Inductance for ML-DAB transformer, L (value calculated as per Equation 14)	0.5 mH
2-level PV side bridge IGBT's V_{CE}	600 V (49% of V_s)
3-level NPC bridge IGBT's V_{CE}	1,200 V (70% of $\frac{V_P}{2}$)

Soft-switching results for semiconductor switches in the converter are shown in Figures 12–14 showing zero voltage switching (ZVS) and zero current switching (ZCS) performance. Infineon 1,200-V IGBT modules FF100R12YT3 are modeled in the simulation to estimate the losses and efficiency. In the simulation, the conduction losses have been modelled based on the IGBT datasheet parameters and assuming linear switching characteristics. The efficiency is 96.42%, as seen in the simulation.
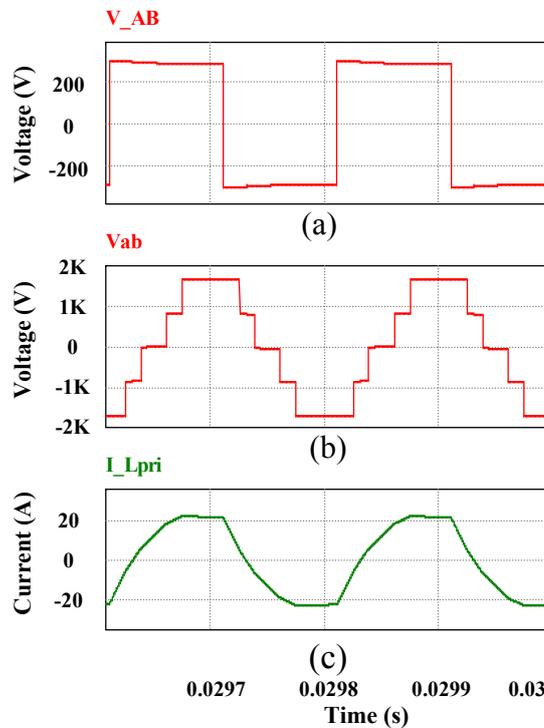

Figure 18. (From top to bottom) (**a**) Primary 2L voltage v_{AB}; (**b**) secondary 5L voltage v_{ab}; and (**c**) current through the primary referred leakage inductor i_L.
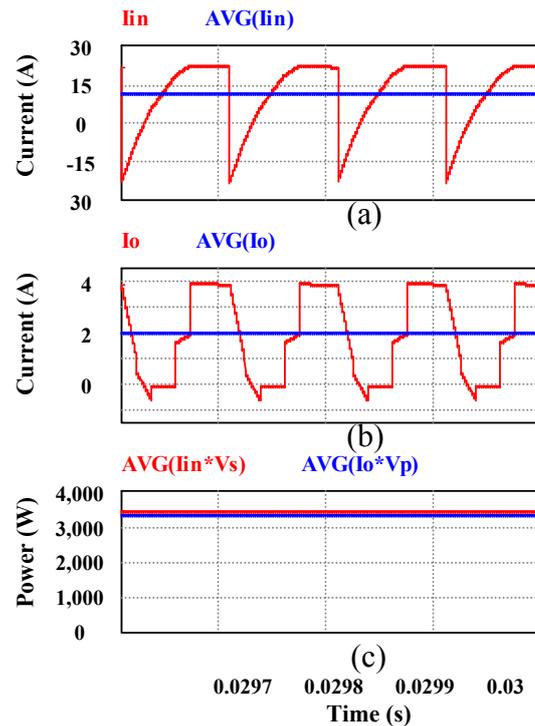
Figure 19. (From top to bottom) (**a**) ML-DAB input current I_{in} and its average; (**b**) output current I_{out} and its average; and (**c**) average input and output power $P_{in} = AVG(I_{in} * V_s)$ and $P_{out} = AVG(I_o * V_P)$.

Simulation and experimental results also verify the functionality of the proposed ML-DAB and the symmetric modulation technique. A hardware prototype (Figure 20) has been built and tested with a scaled-down input voltage ($V_s = 120$ V, $f_s = 5$ kHz) to verify the power flow and open-loop control. The gate signal for all the twelve IGBTs used in the ML-DAB is shown in Figure 21.The experimental voltage and current waveforms shown in Figures 22 and 23 have a close match with the simulation results shown in Figures 18 and 19. Figure 24 shows the output voltage and current waveforms when the ML-DAB is connected to a full-bridge inverter and a resistive-inductive (R-L) load. In the hardware prototype, an overall efficiency of 88% (Figure 25) has been observed for a 120-V input voltage and 638 W (which is 20% of the rated power of the converter) of input power (Table 3). At full rated power, it is expected that the observed efficiency will closely match with the theoretical and simulated efficiency figures.
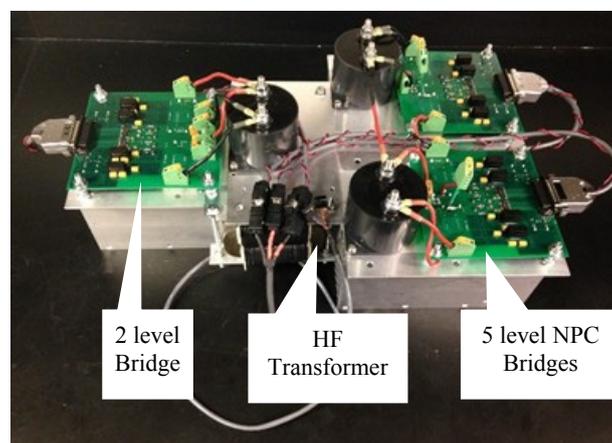

Figure 20. ML-DAB prototype hardware setup for laboratory testing.
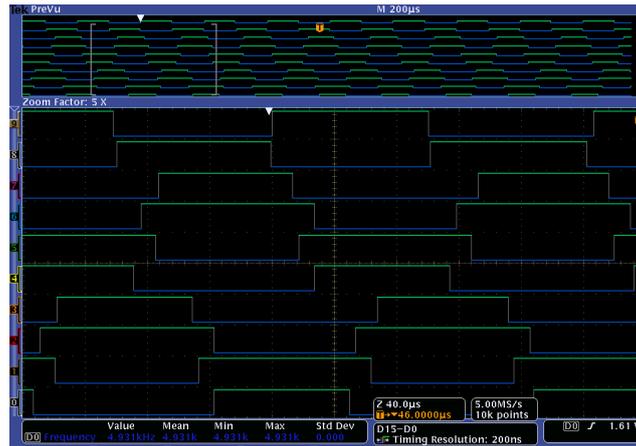
Figure 21. Gate pulses for the ML-DAB IGBTs (from top to bottom: $S_{1,4}, S_{2,3}$ and $S_{a1}, S_{a2}, S_{a3}, S_{a4}$ and $S_{b1}, S_{b2}, S_{b3}, S_{b4}$).

Table 3. Experimental efficiency and losses for the prototype ML-DAB.

V_S (V)	V_P (V)	P_{in} (w)	P_{out} (w)	$P_{loss_{trans}}$ (w)	$P_{loss_{total}}$ (w)	Eff_{trans} (%)	Eff_{total} (%)
60	310	161	133	14	28	90	83
80	416	284	239	27	45	90	84
100	521	443	373	45	70	89	84
120	626	638	561	42	77	93	88
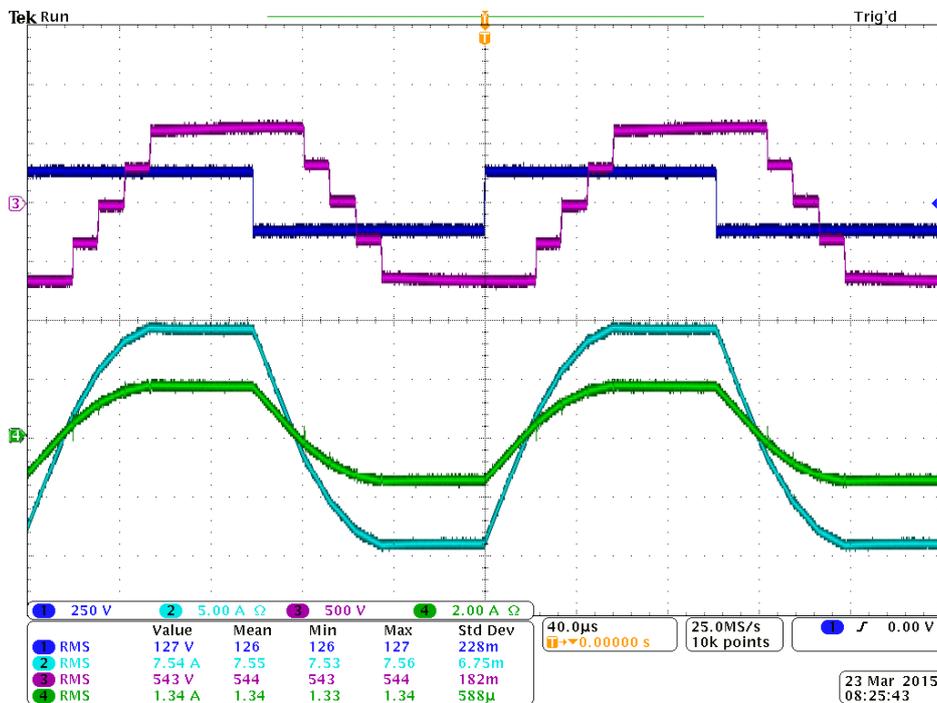
Figure 22. ML-DAB 2L voltage v_{AB}, 5L voltage v_{ab} and current through the 2L and 5L side of the transformers $i_{L_{pri}}$ and $i_{L_{sec}}$; where $V_s = 125$ V, $V_P = 650$ V, $n = 5.71$, $\alpha = 10^0$, $\beta = 30^0$ and $\phi = 70^0$.
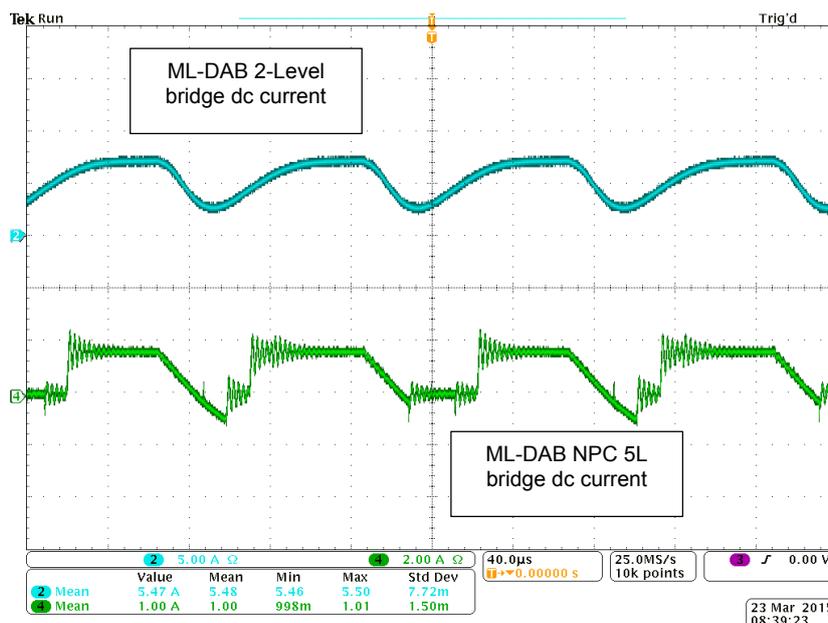
Figure 23. ML-DAB input (2L bridge) and output (5L bridge) dc current waveforms $I_{dc_{2L}}$ and $I_{dc_{5L}}$.
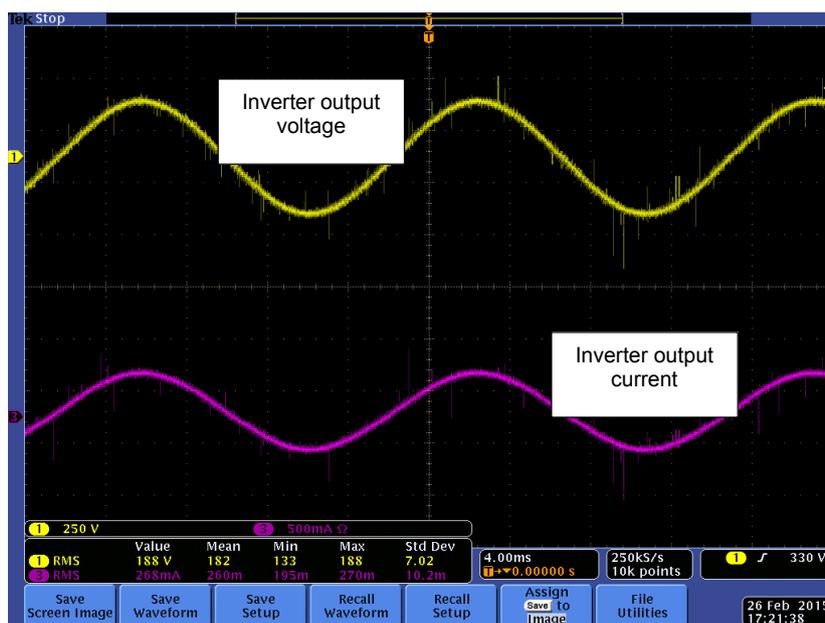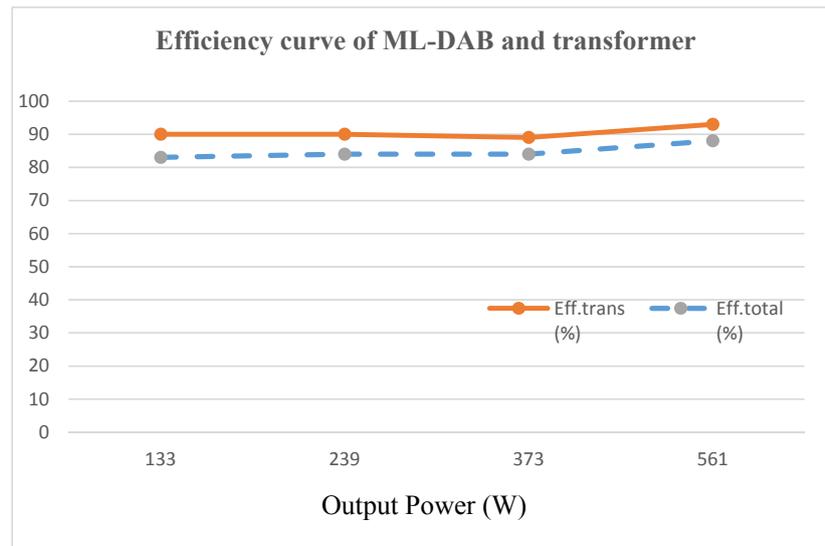

Figure 24. Output voltage and current waveforms when the ML-DAB is connected to a full-bridge inverter and a resistive-inductive (R-L) load.

Figure 25. Efficiency curve of the transformer and ML-DAB with output power variation.

6. Conclusions

In this paper, a multilevel DAB (ML-DAB) dc-dc converter has been proposed for its use in high step-up/down, high-voltage applications. The boost and buck configurations of the ML-DAB have been explained in detail. A symmetric modulation technique has been proposed, which allows for independent control of the phase-shift from the control parameters that shape the multilevel voltage waveforms. The paper analyzes in detail the 2L-5L, 5L-2L and 3L-5L voltage waveforms across the high frequency transformer and derives expressions for the power flow. A soft-switching analysis along with boundary conditions is presented. The converter is designed and simulated in PSIM®. A hardware prototype is built and tested to verify the proposed ML-DAB performance with the symmetric modulation scheme. Experimental results have been presented to validate the proposed modulation and power flow in the ML-DAB.

Acknowledgments

Author Contributions

M.A. Moonem and H. Krishnaswami conceived the concept, performed the analysis and designed the experiments. R. Hernandez and C. Pechacek designed the prototype and performed the experiments; R. Hernandez and H. Krishnaswami analyzed the data; M.A. Moonem wrote the paper; All authors approved the final manuscript.

Conflicts of Interest

The authors declare no conflict of interest.

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