electronics

Review

Flexible Electronics: Integration Processes for Organic and Inorganic Semiconductor-Based Thin-Film Transistors

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Abstract: Flexible and transparent electronics have been studied intensively during the last few decades. The technique establishes the possibility of fabricating innovative products, from flexible displays to radio-frequency identification tags. Typically, large-area polymeric substrates such as polypropylene (PP) or polyethylene terephthalate (PET) are used, which produces new requirements for the integration processes. A key element for flexible and transparent electronics is the thin-film transistor (TFT), as it is responsible for the driving current in memory cells, digital circuits or organic light-emitting devices (OLEDs). In this paper, we discuss some fundamental concepts of TFT technology. Additionally, we present a comparison between the use of the semiconducting organic small-molecule pentacene and inorganic nanoparticle semiconductors in order to integrate TFTs suitable for flexible electronics. Moreover, a technique for integration with a submicron resolution suitable for glass and foil substrates is presented.

1. Introduction

Nowadays, transparent and flexible electronics are one of the technologies with the widest range for innovative products, so they are the focus of several research groups and enterprises. One reason for this interest is the chance to integrate identification tags, smart cards or flexible displays using almost the

same integration processes. Moreover, the cost of these devices is kept low due to the innovative use of newly created or adapted processes for large-area and flexible substrates. Thin-film transistors (TFT) are an essential element of this technology. They are responsible for the driving current in memory cells, digital circuits or for light-emitting diodes (LEDs). Another characteristic of this technology is the opportunity to introduce new materials, which improve the electrical performance, simplify the integration process or even add new mechanical properties to the final product.

Organic and inorganic semiconductors have been used to integrate TFTs for more than 20 years [1,2]. They exhibit better characteristics in comparison to amorphous silicon-based transistors due to the achieved performance and low production cost. Nevertheless, when pursuing a cost-efficient production with a high reliability and restrained mechanical characteristics, there are new requirements. Most of them are related to the fact that flexible substrates can only be handled at low temperatures, due to their flexibility, *i.e.*, all deposited materials suffer from mechanical stress during their fabrication or use. For instance, the use of non-malleable metal connections or dielectrics may induce a failure after bending the substrate. For this sake, all components (materials and integration processes) have to be selected carefully to fulfill these requirements.

In this review paper, we concisely address the fundamental concept, electrical analysis and limitations of the flexible electronic technology. Additionally, we present a comparison between organic and inorganic based TFTs, as well as an integration routine in order to fabricate submicron structures on foil at reduced costs.

2. Thin-Film Transistor Fundamentals

Thin-film transistors basically consist of three elements: the active semiconductor, the electrical connections (source, drain and gate) and the dielectric layer. The dielectric layer separates the gate electrode from the active semiconducting film, whereas the source and drain contacts are directly connected to the semiconductor, determining the transistor's dimensions. As a voltage is applied to the gate electrode, the majority charge carriers are attracted by the electric field and form a conducting channel (accumulation mode). In general, the electrical connections consist of thermally evaporated or sputtered metal layers. The choice of the drain/source contact material is crucial, as it determines whether electron or hole injection is preferred. This depends on the position of its Fermi level with respect to the frontier molecular orbitals (highest occupied molecular orbital, HOMO, and lowest unoccupied molecular orbital, LUMO) and the valence/conduction band in the case of organic and inorganic semiconductors, respectively. Considering the metal-semiconductor interface, a Schottky barrier will be formed (Figure 1), which has poor blocking properties in comparison to a pn-junction. As a voltage is applied between drain and source contacts, an off-current occurs due to the tunneling of charge carriers across the formed potential barrier (Figure 1b). The potential barrier width can be reduced by applying a voltage to the gate electrode and, as a result, the drain current increases (Figure 1c).

In general, TFT operation is expressed using the same models as for the metal-insulator-semiconductor field-effect transistor (MISFET). Although it may not provide quantitative agreement with the device, it represents the transistor's basic operation.
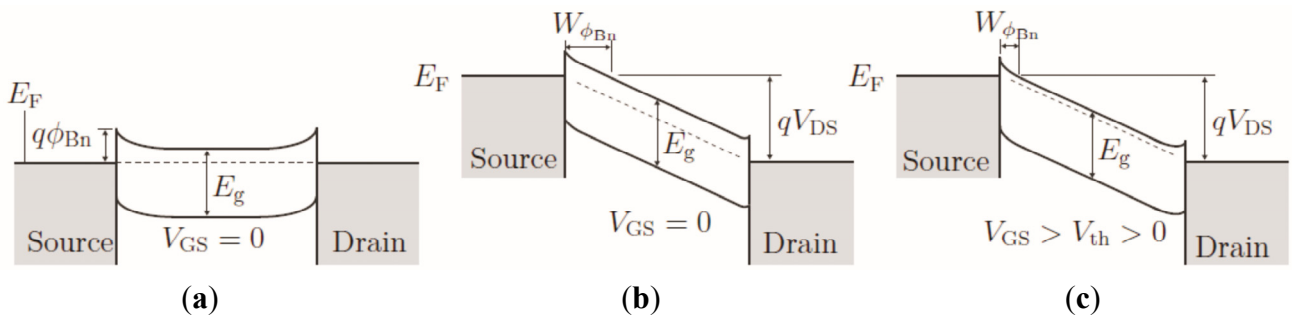
Figure 1. Band diagram of the Schottky contacts to an n-type semiconductor with metal contacts: (**a**) without applied voltages; (**b**) with drain voltage and (**c**) with drain and gate voltages. © 2015 IEEE. Reprinted, with permission, from [3].

2.1. Integration

As discussed above, the three elements, *i.e.*, semiconductor, dielectric and metal contacts, are the main components of a TFT. The arrangement of these elements has a strong influence on both the device performance and the integration process itself. The devices are divided into two main groups, the staggered and the coplanar setup. The position of the drain/source electrodes and the gate dielectric in relation to the channel area defines the transistor configuration. In coplanar structures (Figure 2b,d), the drain/source electrodes and the dielectric are located at the same side of the channel, whereas in staggered structures (Figure 2a,c) the drain/source electrodes and the dielectric are placed at opposite sides. The position of the gate electrode is also used to classify the setups as either bottom-gate (Figure 2a,b) or top-gate devices (Figure 2c,d). Usually, bottom-gate devices are referred as an inverted structure.
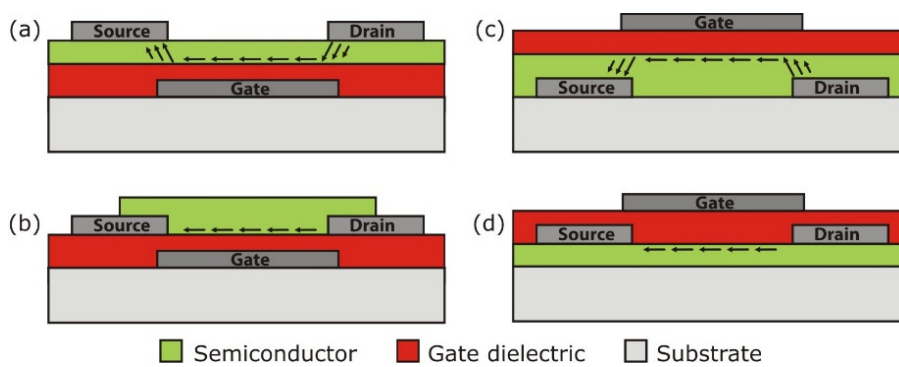
Figure 2. General thin-film transistor configurations: (**a**) staggered bottom-gate; (**b**) coplanar bottom-gate; (**c**) staggered top-gate and (**d**) coplanar top-gate.

The contact resistances between the metal (drain and source) electrodes and the semiconductor reduce the maximum current that will flow through the device in the on-state. Nevertheless, as a Schottky barrier is formed at those contacts, the contact resistance during the transistor off-state should be high enough to prevent a high leakage current. For staggered structures, a major contribution to the contact resistance is related to access resistance. This mainly occurs because the charge carriers have to travel through the semiconducting layer thickness before reaching the gate dielectric/semiconductor interface. In the case of coplanar setups, the drain and source electrodes are already in contact with the formed accumulation

layer, which results in a low access resistance. However, results show that if drain/source electrodes are deposited on the active semiconductor, the access resistance is reduced due to valleys in the semiconducting film [4]. An additional reduction of the contact resistance is observed due to the increased contact area when the drain/source metal is deposited on the semiconductor layer [5].

Moreover, the integration process has to be adapted for the different setups. The inverted coplanar layout permits the semiconducting layer to be deposited in the last step. For this reason, the semiconducting film will not suffer from chemical impacts and other integration process steps. For other layouts, the semiconductor has to withstand different processes, as for example lithography, etching or annealing steps.

Deposition methods for metals, dielectrics, semiconductors and all materials used in the integration process should be also entirely suitable for flexible electronics. However, there are variations, either in the quality of the material, temperature or production costs. For the deposition of the semiconductor, commonly vacuum techniques produce a denser film with higher charge carrier mobilities [6,7].

During the last few decades, pentacene seems to be the most promising candidate for organic semiconductor applications. Typically, pentacene layers are deposited by evaporation under high- or ultra-high-vacuum conditions [8], whereby the substrate temperature can be vary between room temperature and 80 °C to improve the self-ordering of the semiconductor molecules [9–11]. Here, charge carrier mobilities up to 3 cm^2/Vs could be achieved [12]. Furthermore, deposition under low vacuum conditions assisted by an inert gas stream is possible [8].

Nowadays, new materials promising good environmental stability and higher mobilities have been synthesized. Various research groups focus on materials such as dinaphtho(2,3-b:2′,3′-f)thieno (3,2-b)thiophene (C_n-DNTT) and 2,7-dioctyl(1)benzothieno(3,2-b)(1)benzothiophene (C_8-BTBT), which can be deposit by thermal evaporation or from solutions, respectively [13–16]. Currently, the highest achieved field-effect mobility is about 43 cm^2/Vs for C_8-BTBT deposited by a special off-centered spin-coating technique [17].

For inorganic semiconducting films, the highest mobilities and denser films are commonly achieved using sputtering techniques [2,18]. With this technique it is possible to deposit binary compounds such as ZnO, In_2O_3, and semiconductor compositions with different ratio between elements, such as IZO, IGO, ZTO, GIZO [19–21]. In 2003, Hoffman *et al.* have demonstrated a fully functional transparent ZnO TFT. Even using high annealing temperatures of around 600 °C–800 °C, the device mobility was found to be 0.35–0.45 cm^2/Vs [22]. Using RF magnetron sputtering, Fortunato *et al.* reported a high mobility (70 cm^2/Vs) ZnO based TFT [23]. The transistor performance can be further improved by using a GIZO target [24] or co-sputtering techniques [25]. Additionally, adjusting the pressure in the chamber and the power during the process, the defect concentration as well as the film density can be controlled [26,27]. When oxygen is added, a reactive process occurs and the amount of oxygen in the film can be adjusted [28,29]. Atomic layer deposition (ALD) is another method to achieve high-density layers as demonstrated by [30,31]. Nevertheless, these films are deposited under vacuum conditions, increasing the production cost. Conjointly, when large area substrates are used, the equipment size will limit the template size.

For this reason, methods using solutions have greater potential to fulfill the requirements imposed for large-area and flexible substrates. They can be divided into two main groups, *i.e.*, molecular precursors and nanoparticle suspensions. For molecular precursors, the temperature in which the semiconductor

film will be synthesized depends on the type of precursor [32]. Commonly nitrate precursors require lower annealing temperatures than acetate or chloride precursors, and greater performance is achieved [33]. In the case of nanoparticle suspensions, the semiconductor is already synthesized in the form of nanoparticles being dispersed in a solution, either water or other solvents, like ethanol, isopropanol and butyl acetate. That means it is possible to fabricate high-quality nanoparticles in mass production, using high temperature and vacuum processes. It maintains an attractive cost base and has almost no influence on the transistor integration process. After the nanoparticle deposition, an annealing process removes the solvent [34–36].

One of the main advantages of using a solution based process is the variety in coating methods. Most of the literature refers to spin-coating methods; however, methods like inkjet printing, spray coating, doctor blade and Meyer rods have attracted the interest of research groups, due to the opportunity to integrate low-cost devices on large area and flexible substrates either using organic or inorganic semiconductors [17,37–40].

2.2. Submicron Structures Suitable for Foil Substrates

To investigate and integrate thin-film transistors at submicron scales, a suitable process is required. In general, nanostructures are established using expensive equipment, like high-resolution lithography [41] or electron beam lithography [42]. Nonetheless, these methods are not entirely suitable for large area and flexible substrates. The side-wall deposition and etch-back (SWEB) technique is a cheap method to fabricate nanostructures applying only conventional lithography.

The SWEB technique can be used to integrate nanoscaled field-effect transistors in bulk silicon. Figure 3 depicts the schematic integration process of this method on silicon. Since silicon is stable at high temperatures, a process temperatures of around 800 °C are used for the nanostructure formation. The main advantage of the SWEB technique is that the transistor size is not defined by the lithography itself, but by the deposition of a sacrificial layer in combination with an etching process. After the thermal oxidation of the wafer or the deposition of SiO_2 by plasma-enhanced chemical vapor deposition (PECVD), the position of the nanostructure is defined by a standard photolithography step and a subsequent anisotropic etching (Figure 3a–c). As a result, a rectangular edge, perpendicular to the wafer surface, is formed in the oxide film. After the photoresist removal, silicon nitride (Si_3N_4) is deposited conformably by low pressure chemical vapor deposition (LPCVD). Due to the very high uniformity of this deposition (better than +/−1%), the thickness of the deposited film, which defines the transistor channel length afterwards, can be controlled carefully. Subsequently, the Si_3N_4 is etched back by a directional dry etching process. After removing of SiO_2 by selective wet etching, a Si_3N_4 spacer stays on the surface, as shown in Figure 3d,e. As the structure size is defined by the thickness of the deposited silicon nitride film, it is possible to achieve nanostructures using standard lithography. Applying the spacers as a mask, the structure can be transferred to the underneath layer (Figure 3f). An example of nanostructures fabricated using the SWEB technique is shown in Figure 4a. Nanoscaled MOSFETs can be integrated by structuring polysilicon. Figure 4b depicts the output characteristics of a 70 nm channel length transistor using μm resolution photolithography. Additional information and discussion about this technique can be found in [43].
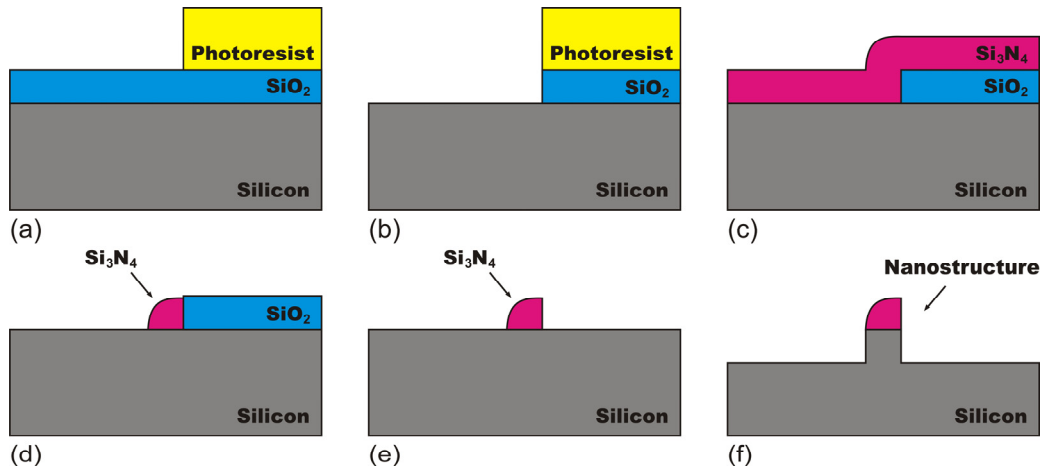
Figure 3. Schematic process of the side wall deposition and etch-back technique. (**a**) The photoresist is structured by conventional photolithography and (**b**) transferred to the underneath SiO_2 layer. (**c**) Subsequent to the photoresist removal, Si_3N_4 is deposited conformably and (**d**) etched back by a directional dry etching process. (**e**) The SiO_2 layer is removed by selective wet etching and a Si_3N_4 spacer stays on the surface. (**f**) Applying the spacers as a mask, the structure can be transferred to the underneath layer.
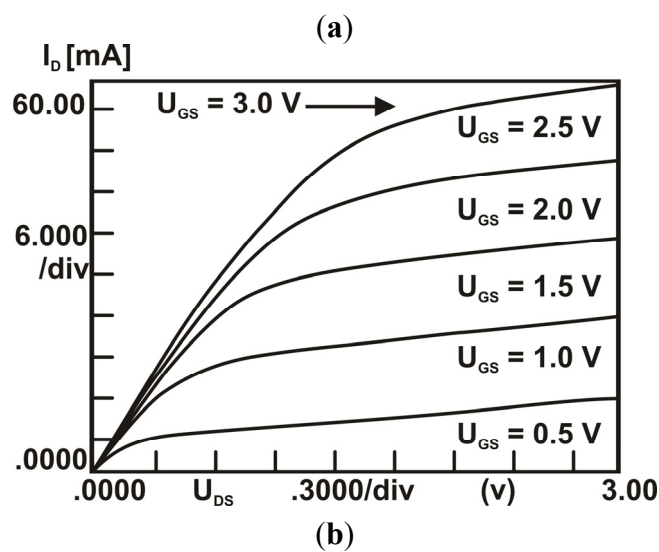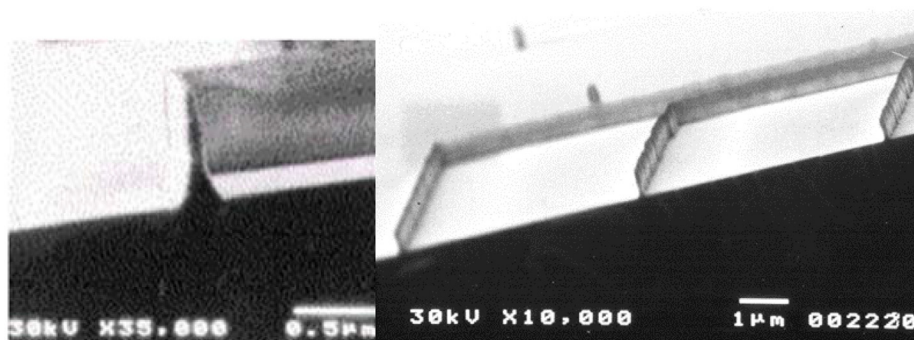
Figure 4. (**a**) Example of structures fabricated using the SWEB technique on silicon bulk and polycrystalline Si on SiO_2; (**b**) electrical characteristic of a MOSFET integrated by SWEB with L = 70 nm and W = 300 μm. © 2015 IEEE. Reprinted, with permission, from [43].

In the MOSFET technology, the creation of a nanoline acting as the gate electrode is sufficient as the source and drain contact areas are defined subsequent to the ion implantation. In contrast, to integrate nanoscaled TFTs on glass and flexible substrates an additional step is required to define the channel length of the transistor by a nanogap. Figure 5 shows the adaptation of the SWEB technique to avail the process to flexible substrates. First, the position of the structure is defined by conventional photolithography, where the sacrificial layer is the photoresist itself (Figure 5a). A PECVD-SiO_2 layer is deposited at low temperature and etched anisotropically (Figure 5b,c). After the photoresist removal, the nanostructure (nanoline) stays back (Figure 5d). In order to achieve a nanogap from a nanoline, a metal is evaporated anisotropically (Figure 5e). By using a selective etching process, the PECVD-SiO_2 is removed creating a nanogap (transistor channel) as shown in Figure 5f. Depending on the integrated setup (staggered/coplanar or inverted/noninverted), the SWEB is done directly on the substrate or after the integration of the gate electrode and dielectric. Nevertheless, when the technique is performed over the gate dielectric, the anisotropic etching of the PECVD-SiO_2 can damage the dielectric layer, if the etching time is not defined carefully. Furthermore, all processes should be selected to fulfill the substrate requirements; for instance, the process temperature is limited to 150 °C.
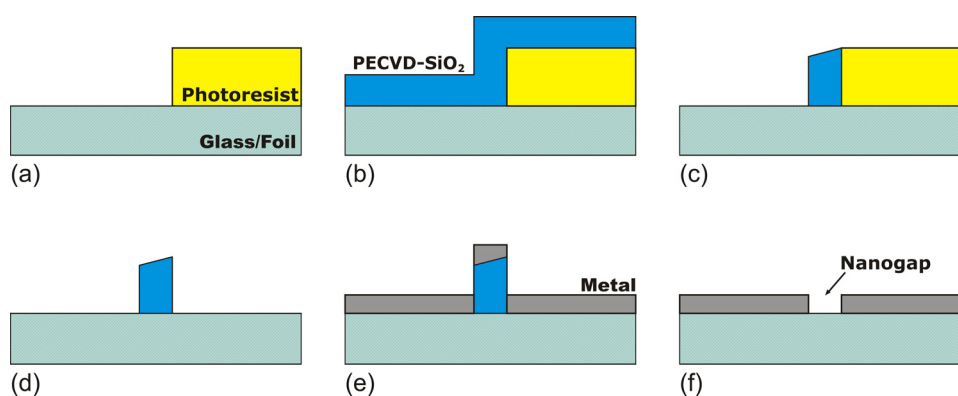

Figure 5. Process flow for integrating nanoscaled gaps on glass or foils. (**a**) The photoresist is structured by conventional photolithography. (**b**) A SiO_2 layer is deposited at low temperature and (**c**) etched anisotropically. (**d**) Subsequent to the photoresist removal, a nanoline stays back. (**e**) A metal is evaporated anisotroically and (**f**) the SiO2 is removed by a selective etching process.

3. Organic Based TFT

The properties of the gate dielectric are essential for the performance of OFET-devices. Roughness and polarity of the insulating layer surface are crucial for the morphology and distribution of the electronic states of the grown organic semiconductor. The first OFET-devices were developed using silicon dioxide, a standard dielectric material in MOSFET technology. The growth process of SiO_2 can be well-controlled, providing a low defect density and a smooth surface to produce well-oriented organic semiconducting films [44–46]. Besides the high electrical stability, thermally grown SiO_2 on a heavily doped Si wafer acts as template to evaluate new synthesized organic semiconducting materials. As a first investigation, 30 nm pentacene were evaporated under high-vacuum conditions as an active semiconducting layer, in which the drain and source contacts consist of gold. The transistor exhibits a

threshold voltage of about 1.5 V and an on-off ratio of 10^3 at a drain-source voltage of $V_{DS} = -40$ V [47]. Notwithstanding of the high gate voltage, no electrical breakdown could be observed. In order to improve the growth process of the pentacene film, an oxygen plasma surface treatment of the dielectric material was performed before the evaporation. Figure 6 shows the electrical characteristics of OFET-devices using thermally grown SiO_2 as insulating layer (a) without and (b) with prior treatment by an oxygen plasma. Evidently, the surface treatment leads to a threshold voltage shift to 17.2 V [47] regarding the polarization of the dielectric due to the generation of free bonds at its surface [48]. Furthermore, the electrical strength diminished, resulting in an increasing leakage current at off-state. Nevertheless, the surface treatment leads to higher drain currents at lower gate voltages, regarding the increased pentacene crystallites at the dielectric surface. AFM studies found a crystallite diameter of 250 nm at untreated and 1 μm at treated SiO_2 surfaces, respectively [47].
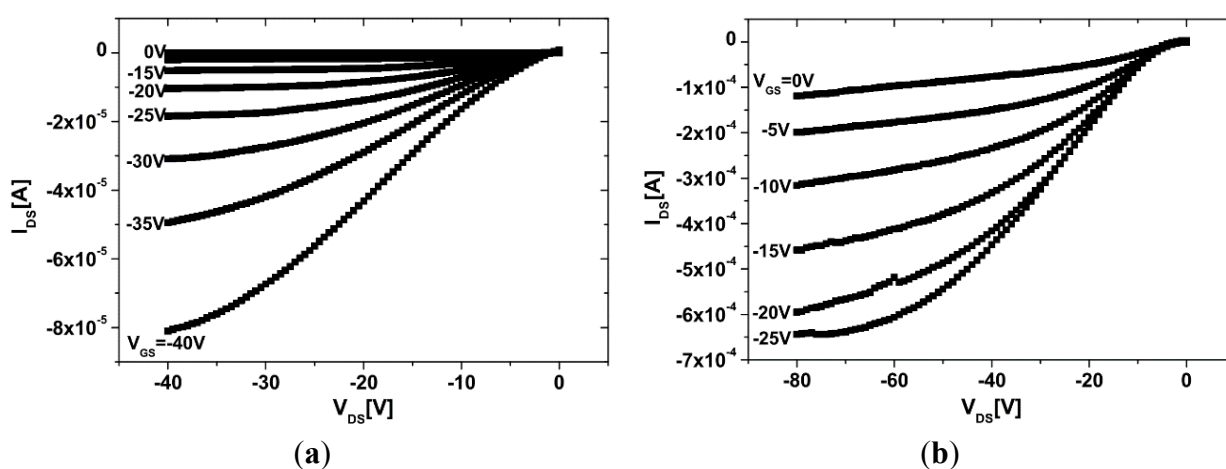
Figure 6. Output characteristics of an inverted coplanar pentacene OTFT using SiO_2 as gate dielectric (L = 1 μm, W = 1000 μm). (**a**) Without oxygen plasma treatment (t_{ox} = 150 nm); (**b**) with oxygen plasma treatment in a parallel-plate reactor (t_{ox} = 100 nm). Reprinted from [47], with permission from John Wiley and Sons.

As the thermal growth of SiO_2 cannot occur on other substrate materials with individual gate contacts, other deposition techniques for the gate dielectric are required for the realization of digital circuits. A low-temperature-oxide (LTO) can be deposit by CVD techniques. Triethylsilane forms silicon dioxide by the separation of ethyl groups from the residual silane under low pressure and continuous oxygen flow. Due to the process temperatures of 550 °C, titanium can be used as a gate material. To avoid the oxidation of the gate metal during the LTO-deposition, an additional step to nitrify the titanium can be performed. Nevertheless, large leakage currents and a low on-off ratio that are related to carbon atoms from ethyl groups prevent the building of digital circuits. Even after an additional thermal treatment, just a slightly better breakdown voltage can be observed [47].

By using PECVD-deposition techniques, a further decrease of the process temperature can be achieved. At typical process temperatures between 130 °C and 300 °C, silicon dioxide is formed by a chemical reaction of silane and oxygen. Due to the low temperatures, the nitridation of the titanium gate electrode is not necessary, but a high defect density and low electrical stability restrain the exclusive use of PECVD-oxide for OTFT [49]. Nevertheless, PECVD-oxide can be used as an oxidation barrier for

the metal gate electrode, replacing the time-consuming step of nitrifying titanium. Admittedly, a reduction of the leakage current can be observed compared to the above mentioned LTO-process, but a rather low on-off ratio exhibits the impossibility of building digital circuits [47].

Flexible electronic devices using polymeric substrates such as polyethylene terephthalate (PET) or polypropylene (PP) are sensitive to thermal treatments. High process temperatures, electrical instability and the low dielectric constant of SiO_2 ($k = 3.9$) create a demand for other deposition techniques and materials. Reactive sputtering techniques provide process temperatures down to room temperature, but it should be mentioned that sputtering of the gate dielectric leads to a high surface roughness. Experiments using tantalum pentoxide Ta_2O_5 ($k = 23$) as dielectric material show a rather low mobility of 8.2×10^{-5} cm^2/Vs of the OFET-device regarding to an amorphous growth of the pentacene film [47]. Furthermore, it is shown that the stoichiometric ratio of oxygen and tantalum is important to control. An excessive amount of tantalum leads to a metallic character in the insulating layer [50,51].

Inorganic dielectric materials have in common that they lack mechanical elasticity, hence they are partly usable in flexible electronic devices. However, polymeric dielectrics are featured with high mechanical flexibility and rather low processing temperatures. A commercially available coating varnish, Bectron, which is based on modified alkyd chemistry, was used for initial investigations. Its low curing temperatures of 80 °C and deposition by spin-coating show possible application for flexible electronics. Limited stability against solvents that are part of optical lithography and insufficient control of the deposited layer thickness led to efforts being discontinued [47].

Organic-inorganic nanocomposites are intertwining the advantages of inorganic and polymeric dielectrics. While the polymeric matrix leads to the flexible attributes of the nanocomposite material, the permittivity can be adjusted by the involved inorganic component. Therefore, a high-*k*-resist based on hydrolyzed and partially condensed ethyl silicates was used. The high-*k*-resist contains different amounts of zirconium dioxide or titanium dioxide resulting in dielectric constants between 9 and 12 [47]. The deposition of the resist can be done by spin-coating. The curing process consists of a soft-bake step at temperatures of 80 °C, followed by an UV-curing step for cross-linking of the polymeric matrix material. The resulting layers exhibit a thickness in the range of 200 nm and 400 nm and a sufficient stability against the common solvents used in optical lithography.

Figure 7 shows the electrical characteristics of an OFET-device using a 200 nm thick high-*k*-resist layer as dielectric material. A 150 nm thick aluminum layer serves as the gate electrode. As active semiconducting material, 30 nm of pentacene was thermally evaporated under high-vacuum conditions. The transistor exhibited a threshold voltage of about 7.4 V, an on-off ratio greater than 10^2 and a saturation regime mobility of 0.022 cm^2/Vs [47].

In general, organic materials are influenced by environmental conditions such as ambient humidity and oxygen. As organic semiconductors act as active layers in OTFT, the device's performance is directly affected. Water vapor and oxygen lead to modifications in the charge carrier field-effect mobility and in the threshold voltage [52–54]. To investigate the impact of ambient humidity and oxygen, long-term experiments were executed. Therefore, an OFET-device using 110 nm of thermally grown SiO_2, as insulating layer, on a heavily doped Si substrate was prepared. A 58 nm thick pentacene layer was evaporated under high-vacuum conditions. The long-term experiments were performed over a period of 9 months at intervals of 3 months. The device was stored under ambient dark atmosphere conditions in a shielded metal box. The measurements were performed under ambient conditions.
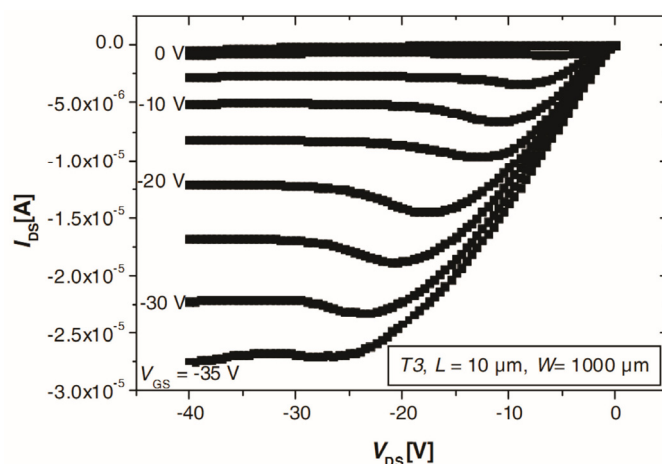
Figure 7. Output characteristics of an inverted coplanar pentacene OTFT using a high-*k* dielectric (L = 10 μm, W = 1000 μm and t_{ins} = 200 nm). Reprinted from [47], with permission from John Wiley and Sons.

Figure 8 shows the electrical characteristics of the device during the long-term experiment. Over the 9 months interval, the drain current decreases from −61 μA to −187 nA, the charge carrier mobility in the linear regime diminishes from $2 \times 10^{-3} cm^2/Vs$ to $1.2 \times 10^{-5} cm^2/Vs$, and the threshold voltage shifts from 4.8 V to −8 V [55]. Table 1 shows an overview of the results. Further experiments specify the dominating agent in the device's degradation. Therefore, a chip carrying a proceeded OTFT template was bonded and connected to the measurement setup, followed by placement in a vacuum chamber. A 30 nm thick layer of pentacene was evaporated under high-vacuum conditions. Subsequent to the measurement under high-vacuum conditions, the chamber was flooded with pure technical oxygen before repeating the measurement. The relevant transfer characteristics are shown in Figure 9.
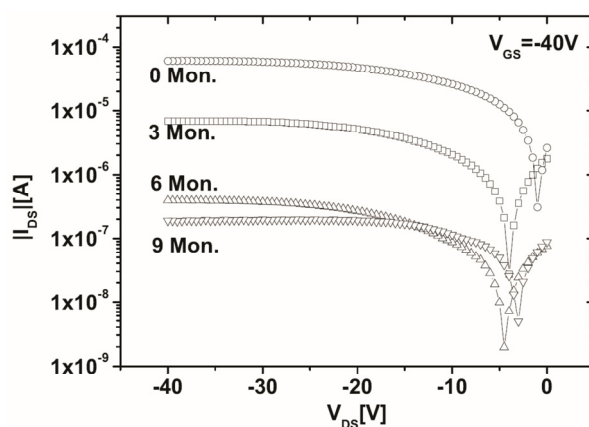
Figure 8. V_{DS}—I_{DS} characteristics of an inverted coplanar pentacene OTFT at V_{GS} = −40 V using SiO_2 as gate dielectric after 0, 3, 6 and 9 months (L = 1 μm, W = 1000 μm and t_{ox} = 110 nm). Reprinted from [55], with permission from Cambridge University Press.

Table 1. Behavior of the electrical parameter of an inverted coplanar pentacene OFET-device after 9 months of investigation. Reprinted from [55], with permission from Cambridge University Press.

Time	I_{DS} (µA)	V_{th} (V)	µ (cm²/Vs)
0 months	−60.9	4.8	2.0×10^{-3}
3 months	−6.8	2.3	2.4×10^{-4}
6 months	−0.457	−3.4	2.2×10^{-5}
9 months	−0.187	−8	1.2×10^{-5}
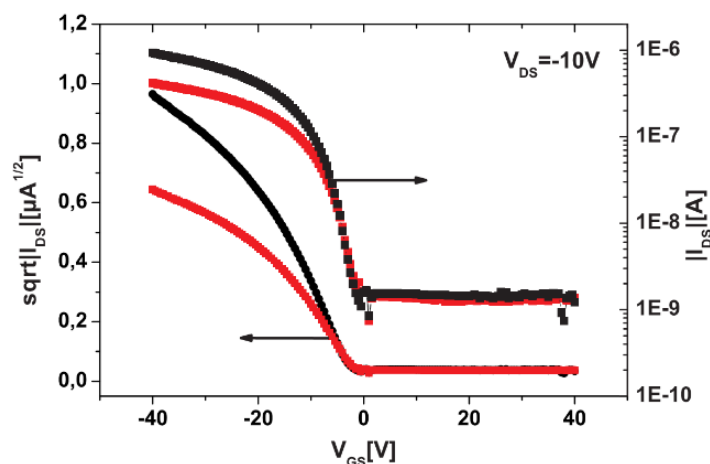
Figure 9. Transfer characteristics of an inverted coplanar pentacene OTFT using SiO_2 as gate dielectric (L = 1 µm, W = 1000 µm and t_{ox} = 110 nm). Measurement under vacuum conditions (black curves) and after the impact of oxygen (red curves). © 2015 IEEE. Reprinted, with permission, from [56].

Subsequent to the flooding of the chamber, the drain current in the saturation regime decreases from −15.9 µA to −6.4 µA, whereas the threshold voltage shifts from −2.6 V to −0.7 V [56]. This threshold voltage shift is related to the influence of oxygen on the molecular structure of pentacene. Oxygen is connected to the middle benzene ring of the pentacene molecule, creating acceptor states for electrons [57]. As a result, negative charges at grain boundaries and at the dielectric surface were introduced [58]. It should be mentioned that the threshold voltage shifted in the opposite direction as observed in the long term degradation experiments. From the literature it is well-known that water molecules can diffuse into the organic semiconducting material and dissociate under the impact of an electric field [57]. The formed H^+ and OH^- ions create defects in the pentacene crystal, acting as traps for positive charge carriers. Therefore, the current decreases, the interface between the gate dielectric and the semiconductor becomes polarized and a threshold voltage shift in the negative direction can be observed. It should be mentioned that the sign of the permanent bias stress has an impact on the direction of the threshold voltage shift [59]. Nevertheless, regarding both experiments, the influence of water seems to dominate the degradation of pentacene OTFT devices. As a result, an efficient encapsulation of pentacene OTFT devices is needed to ensure long term stability. As oxygen also diffuses through polymeric substrates, a flexible encapsulation of the completed device is required.

4. Inorganic-Based TFT

Inorganic semiconductors are commonly more stable than organic semiconductors. For this sake, we investigated the integration of a high-quality inorganic semiconducting layer using low temperature processes for realization of TFTs. For this reason, the use of nanoparticles is a suitable approach to address these issues.

In order to investigate the nanoparticle properties, an oxidized silicon wafer was used as a back contact gate electrode and gate dielectric. Drain and source electrodes were integrated using aluminum. Afterwards, silicon nanoparticles dispersed in ethanol were spin-coated on the substrate. Due to the poor contact between the metal electrodes and the nanoparticles, an annealing step at 500 °C was performed. However, the electrical characteristics of the transistors were poor, and field-effect mobilities of only about 10^{-7} cm^2/Vs were extracted [3]. The main reason for the low performance of these transistors is related to the inter particle connections. Considering that the transistor has a channel length of 8 μm and the Si nanoparticles have an average size of 60 nm, there are at least 130 particles connecting the drain to the source. As a nature oxide is built on the Si nanoparticle surface, the contact resistance between nanoparticles will increase, diminishing the transistor current level even when high voltages are applied. Due to a reoxidation process, the application of a passivation layer or even the removal of the oxide layer by using hydrofluoric acid will not enhance the transistor performance [60]. Hence, TFTs based on Si nanoparticles are not suitable for device integration on flexible substrates, mainly because of the poor quality of the contacts between the nanoparticles and the high annealing temperatures.

In order to reduce the number of inter-particle connections and to improve transistor performance, a smaller transistor is required. For this sake, the side-wall deposition etch-back technique can be used even with μm-resolution photolithography, as previously discussed. The best performance will be achieved when the transistor channel length perfectly matches the nanoparticle size. In this case, a single nanoparticle acts as the active semiconductor connecting drain and source [61]. An inverted coplanar setup with L = 60 nm and W = 100 μm was integrated to electrically characterize the transistor. Figure 10 shows the transistor characteristics. The extracted field-effect mobility, considering the whole transistor width, is about 10^{-2} cm^2/Vs [3]. Nevertheless, due to the low yield of operating devices, the assumption that the entire channel is filled with nanoparticles is not realistic and the mobility is strongly underestimated. A more realistic value, considering that only one nanoparticle is active, is in the range of 100–200 cm^2/Vs [43].

To improve the yield, an inverted staggered setup is used. After the nanoparticle deposition, drain and source electrodes are structured. Even integrating a 70-nm-channel-transistor, the yield is higher and the devices show mobilities of around 10^{-3} cm^2/Vs [3]. Figure 11 depicts a typical output characteristic of these devices. The effect of dopants in the nanoparticle were also investigated, and phosphorous and boron doped nanoparticles were used. On one hand, the influence of phosphorous is weakly observed, because just a few dopants are electrically active. On the other hand, boron doped particles strongly affect the transistor's behavior, as the aluminum, used as drain and source electrodes, and the p-doped silicon built an ohmic contact [3].
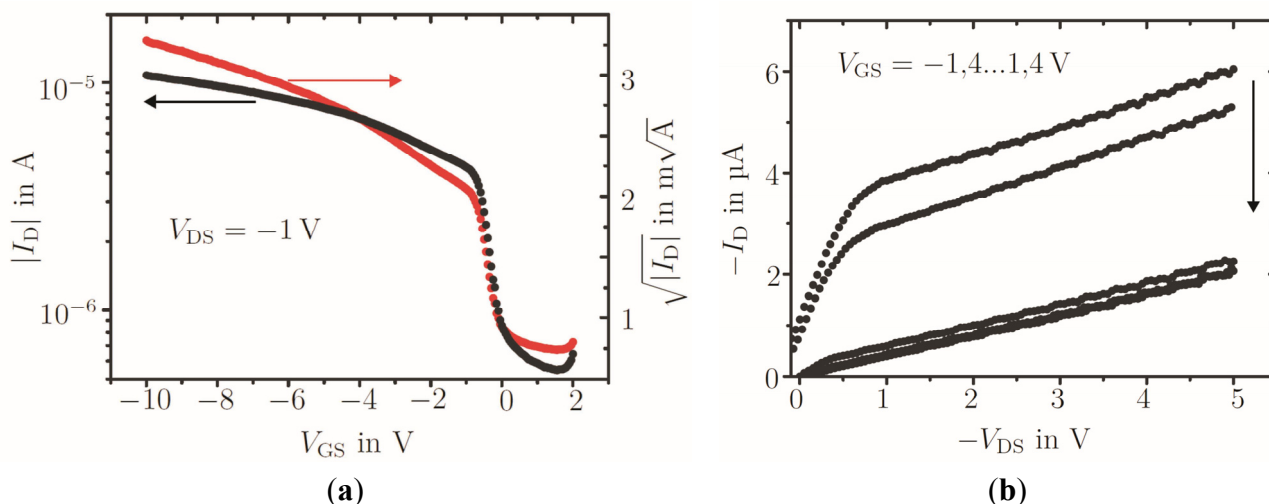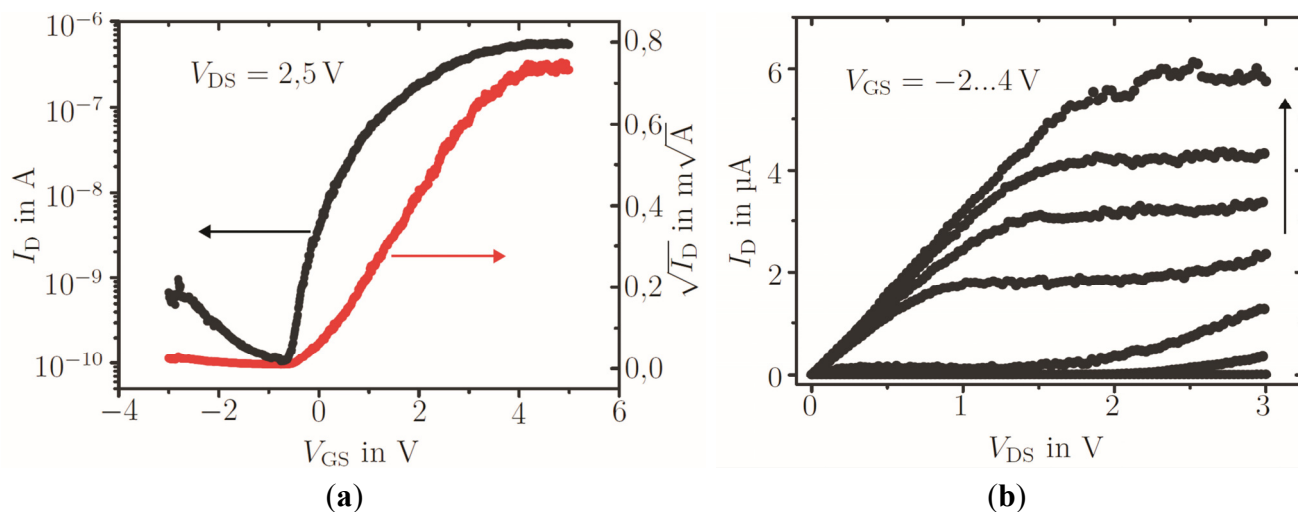
Figure 10. (**a**) Transfer and (**b**) output characteristics of an inverted coplanar single particle TFT integrated by SWEB technique using Si nanoparticles (L = 60 nm, W = 100 μm and t$_{ox}$ = 15 nm). © 2015 IEEE. Reprinted, with permission, from [3].
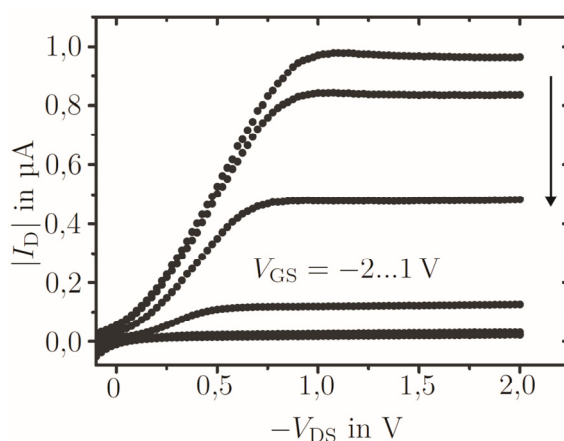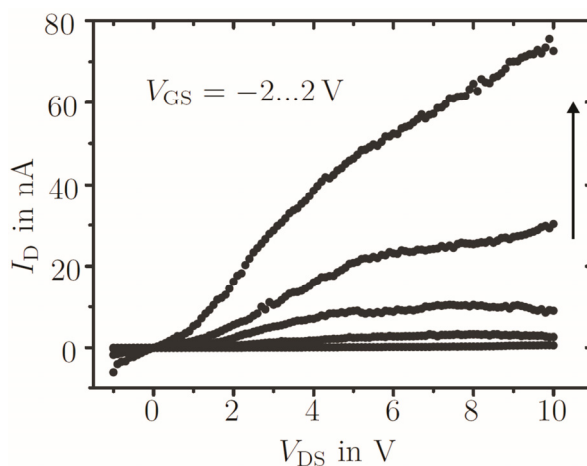

Figure 11. Output characteristics of an inverted staggered single particle TFT integrated by the SWEB technique with a Si nanoparticle (L = 70 nm, W = 800 μm and t$_{ox}$ = 30 nm). © 2015 IEEE. Reprinted, with permission, from [3].

On account of the oxide shell, the performance of TFTs using Si nanoparticles is limited. For this reason, the utilization of a material that does not present an insulating shell is required, for instance a metal oxide. Zinc oxide is a well-researched material, has outstanding electrical, sensory and chemical properties and is transparent to the visible light spectrum. A water-based solution containing ZnO nanoparticles (mean particle size: 80–100 nm) was deposited on templates with metal trenches integrated by the SWEB technique [62,63]. As already observed with the single Si nanoparticle TFT, the yield of the operating device is low, mainly because the nanoparticle must perfectly fit the metal gap between the drain and source electrodes. The transfer and output characteristics are depicted in Figure 12, in which the extracted mobility is around 10^{-2} cm^2/Vs considering the whole transistor width. However, due to the low yield of operating devices, it is possible to assume that one or two nanoparticles are responsible for the transistor operation; hence, the mobility would be in the range of 10 to 20 cm^2/Vs [3,43].

The yield of operating devices can be improved by increasing the metal gap size. Figure 13 shows a non-inverted staggered setup with channel length of 300 nm. Considering that the mean nanoparticle size is around 80–100 nm, the electron flow will take place through multiple particles. As a result, the maximal on current will be reduced [43]. Additionally, as a consequence of the top gate structure, the interface between the nanoparticles and the gate dielectric is rough, and a non-uniform accumulation layer in the semiconducting film is formed, reducing the drain current.
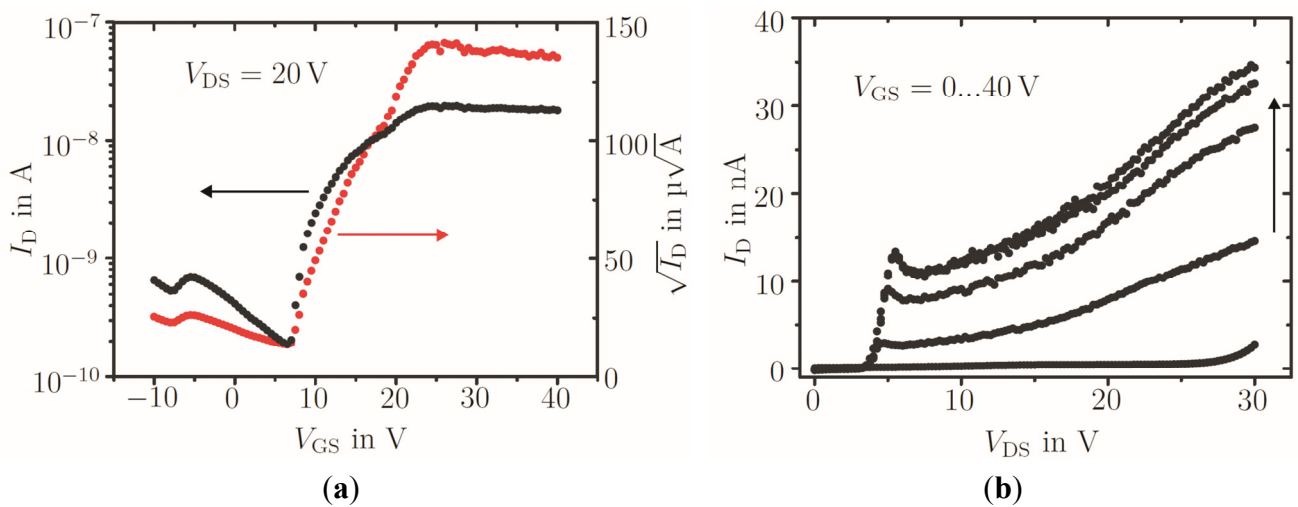

Figure 12. (**a**) Transfer and (**b**) output characteristics of an inverted coplanar single particle TFT integrated using the SWEB technique with ZnO nanoparticle (L = 80 nm, W = 100 μm and t_{ox} = 31 nm). © 2015 IEEE. Reprinted, with permission, from [3].
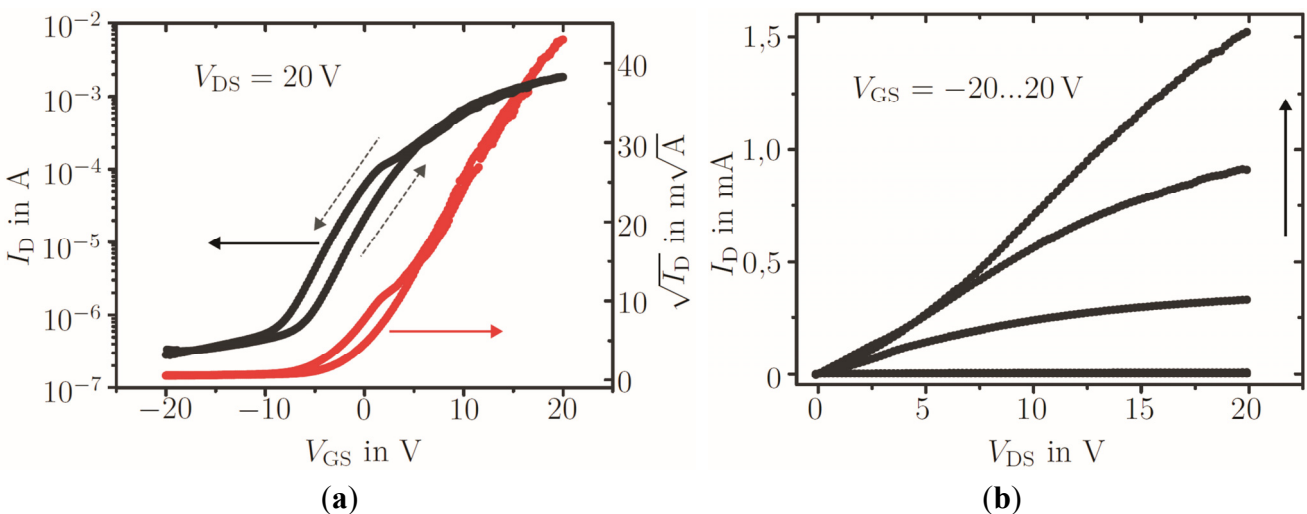

Figure 13. Output characteristics of a noninverted staggered ZnO nanoparticle TFT integrated by SWEB technique (L = 300 nm, W = 20 μm and t_{ox} = 120 nm). © 2015 IEEE. Reprinted, with permission, from [43].

As the ZnO nanoparticle-based devices showed reasonable electric characteristics and the yield of well-operating devices was higher, the ZnO nanoparticle dispersion was spin-coated on a similar inverted coplanar template as that used for Si nanoparticles. After an annealing step of 430 °C in an oxygen atmosphere to saturate the oxygen vacancies in the lattice, the transistors were characterized. As shown in Figure 14, the transistors depict improved performance in comparison to the Si nanoparticle

transistor. Nonetheless, due to the poor contact between the nanoparticles and the drain/source metal electrodes, the on-current is limited and a field-effect mobility about 10^{-5} cm^2/Vs was produced [3]. As discussed previously, the contact between the semiconductor and the metal electrode can be improved by an inverted staggered setup. However, because of the limited adhesion between the nanoparticulated film and the silicon oxide (gate dielectric), an additional thermal treatment is required. The annealing step was performed at 600 °C in an oxygen atmosphere, where a sintering process in the nanoparticulated film was observed and the adhesion was improved [3,64]. Figure 15 shows the typical transfer and output characteristics of a ZnO TFT when a staggered setup is used. The expected increase of the on-current is observed and a mobility in the order of 10^{-3} cm^2/Vs was extracted, as well as an improved on-off ratio of around 10^4 [3]. Due to the high process temperature used during the fabrication of this device, they are not suitable for flexible electronics.


Figure 14. (**a**) Transfer and (**b**) output characteristics of an inverted coplanar ZnO nanoparticle TFT (L = 8 μm, W = 16000 μm and t$_{ox}$ = 300 nm). © 2015 IEEE. Reprinted, with permission, from [3].

Figure 15. (**a**) Transfer and (**b**) output characteristics of an inverted staggered ZnO nanoparticle TFT (L = 8 μm, W = 16000 μm and t$_{ox}$ = 53 nm). © 2015 IEEE. Reprinted, with permission, from [3].

The integration of TFTs using a silicon substrate as a gate back contact is adequate to investigate the transistor performance and characteristics of the semiconductor/metal interface. However, for the integration of electronic circuits, the definition of the gate electrode is required. Aiming a later fabrication on foils, a flexible gate dielectric must be used. For this reason, a polymeric dielectric, *i.e.*, a 5:1:51 PVP:PMCF:PGMEA mixture, was evaluated [65,66]. An annealing step at 200 °C is required to initiate the polymer cross-linking reaction. Figure 16 depicts the transistor transfer curve, where a highly pronounced hysteresis is observed when the gate voltage is swept forward and backward. The hysteresis is mainly attributed to the dipoles which are present in the gate dielectric, and to the interaction with the ambient. A partial cross-linked process, which increases the effect of the hydroxyl groups in the gate dielectric layer, gives rise to these dipoles [67,68]. Conjointly, molecular oxygen and adsorbed water at the nanoparticle surface may induce variation in the film carrier concentration [69,70]. A more precise and detailed explanation regarding this hysteretic behavior is given in our previous work [71].
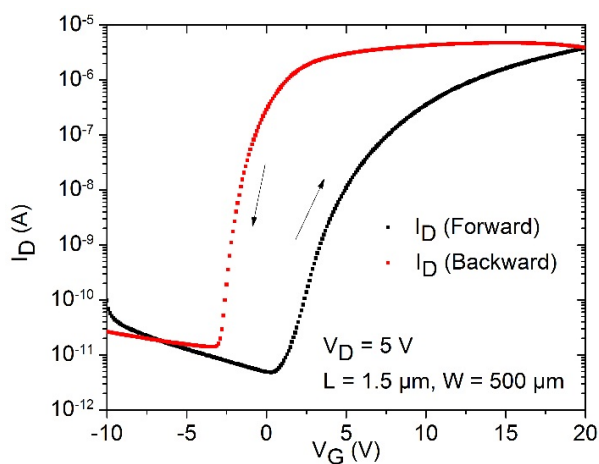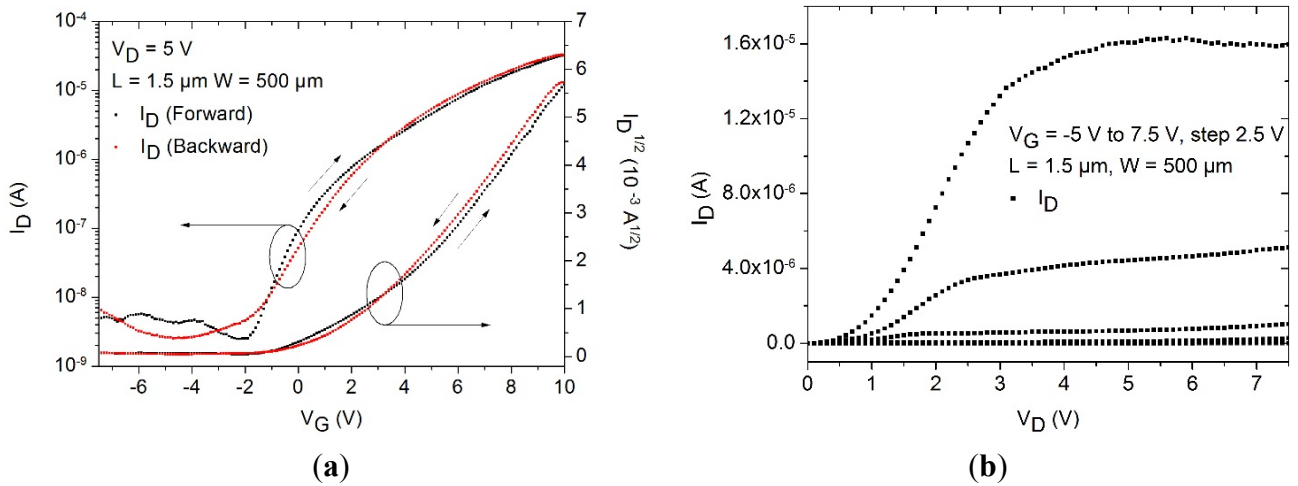

Figure 16. Transfer characteristics of an inverted staggered ZnO nanoparticle TFT using PVP as gate dielectric (L = 1.5 µm, W = 500 µm and t_{ins} = 200 nm).

To achieve better performance and reduction of hysteresis, a high-*k* dielectric containing TiO_2 nanoparticles can be used. An improved device is achieved, as shown in Figure 17. A field-effect mobility of around 0.1 cm^2/Vs and a threshold voltage of around 2.2 V were produced [72]. This integration process is fully compatible with flexible substrates, and the maximum temperature for these devices was only 150 °C.

In order to investigate a later integration on large area foils, a spray coating technique was evaluated for the deposition of the semiconducting film. For this study, an inverted coplanar setup was tested with the maximal processing temperature limited to 150 °C. Due to a capillary effect, the solution containing the ZnO nanoparticles was deposited preferably within the channel area, which improves the yield of devices operating well in comparison to spin-coated devices. A typical transfer and output curve of one of these devices is depicted in Figure 18. Additionally, oxygen plasma treatment prior to the spray coating deposition and heating up the substrate during the spray step improve the semiconducting film morphology [73]. This shows that the spray coating technique has good potential for later integration in large-area and flexible substrates.

Figure 17. (**a**) Transfer and (**b**) output characteristics of an inverted staggered ZnO nanoparticle TFT using a high-*k* dielectric (L = 1.5 μm, W = 500 μm and t$_{ins}$ = 200 nm). Reprinted from [72], with permission from Elsevier.
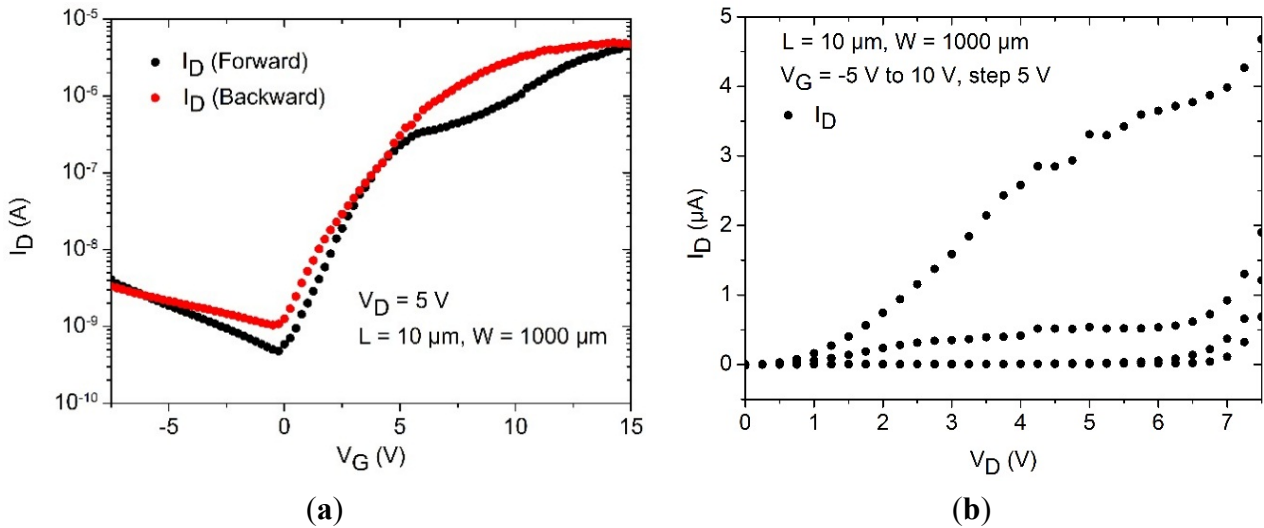

Figure 18. (**a**) Transfer and (**b**) output characteristics of an inverted coplanar ZnO nanoparticle TFT using spray coating technique and a high-*k* dielectric (L = 10 μm, W = 1000 μm and t$_{ins}$ = 200 nm).

As the electron flow through a ZnO nanoparticulated film is based on percolation paths [74], traps located at determined current paths will induce a discrete current fluctuation. For this sake, it is possible to observe non-continuities in the I-V curve presented in this study. Additional information about this effect can be found in [72]. The large surface area present in nanocompounds highlights the effect of the traps [75], but the same effect may occur for polycrystalline and amorphous films.

5. First Applications

The electrical characteristics of the integrated TFTs enable the integration of inverter circuits. Additionally, since the integration process was carefully selected to be compatible with flexible substrates, it is possible to transfer the integration process to different kinds of substrates. Glass substrate

is commonly used as an intermediate substrate, allowing a smooth transition from an oxidized Si wafer to foils. For the circuit, an enhancement-load inverter was designed. Figure 19a depicts a 3D schematic graph of a ZnO based inverter, as well as its electrical representation. Figure 19b depicts an optical microscope image of this element. The electrical characteristics of the inverter are presented in Figure 20. It is possible to observe that the inverter shows maximum peak gains of about 4 V/V and the power dissipation density is less than 26 nW/μm^2 [76]. The voltage transfer characteristics are affected by the hysteretic behavior when PVP is used as the gate dielectric. Nonetheless, it is demonstrated that ZnO nanoparticles have the potential for digital circuit integration, even when low annealing temperatures are used [66,76].
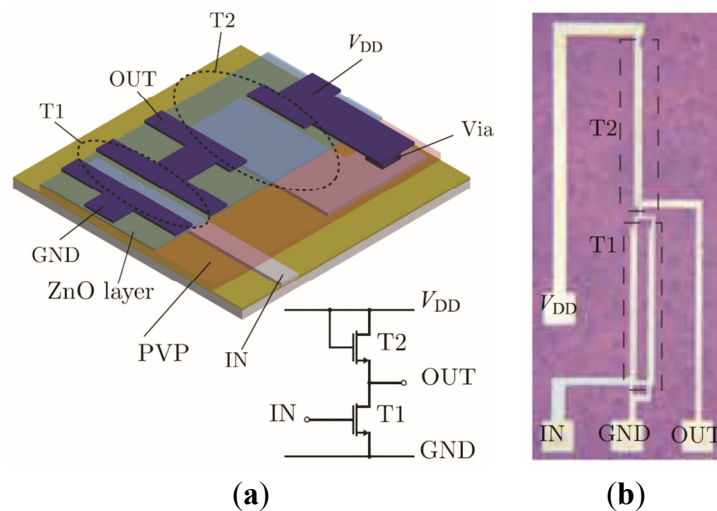

Figure 19. (**a**) Schematic graph, electrical representation and (**b**) an optical microscope picture of the inverter. Reprinted from [66], with permission from Elsevier.
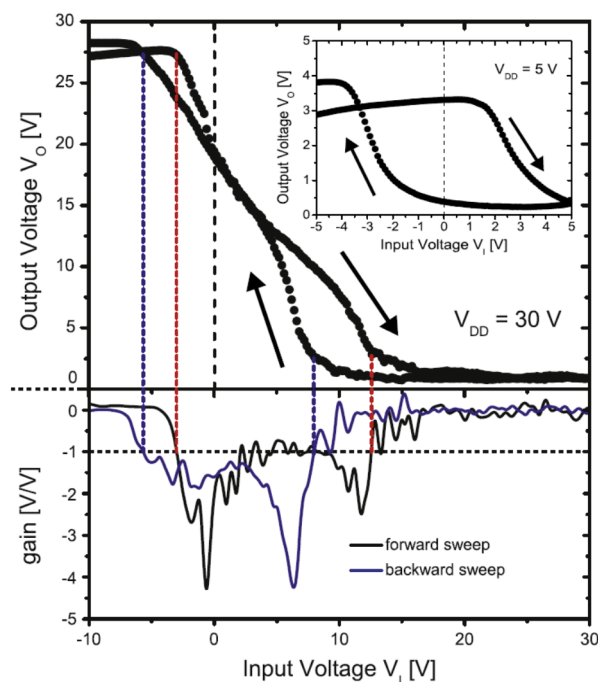
Figure 20. Voltage transfer characteristics of a ZnO based inverter. Reprinted from [76], with permission from Elsevier.

The optical properties of the inverter structure were also investigated. Figure 21 depicts the optical transmittance of the inverter device in the visible light spectrum. The minimum transmittance at a wavelength of about 370 nm is typical for the ZnO nanoparticles [77]. Because aluminum was used as contact electrodes (gate, drain and source), the transmittance is furthermore reduced. However, the integrated transistors and circuits are sufficiently transparent.
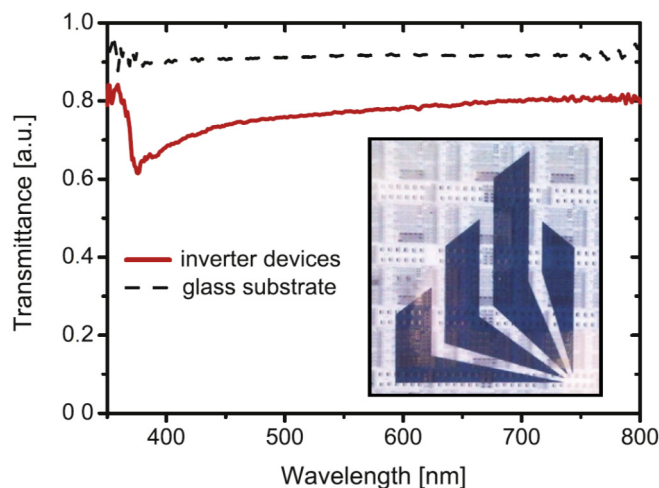
Figure 21. Optical transmittance of ZnO based inverter on a glass substrate. Reprinted from [76], with permission from Elsevier.

Beside the above exhibit inverter structures, inverters based on pentacene were realized. For the gate electrode 50 nm of gold was evaporated on a silicon substrate. A high-*k*-resist containing TiO_2 as inorganic component ($k = 9.5$) was deposited by spin-coating, resulting in a layer thickness of 300 nm for the gate dielectric. Gold was used for drain and source contacts. As an active semiconducting layer, 40 nm pentacene was thermal evaporated under high-vacuum conditions.

Figure 22 shows the electrical characteristics of the resulting inverter. Stable high- and low-level and peak gains of about 5.5 V/V demonstrate its applicability in digital circuits [78].
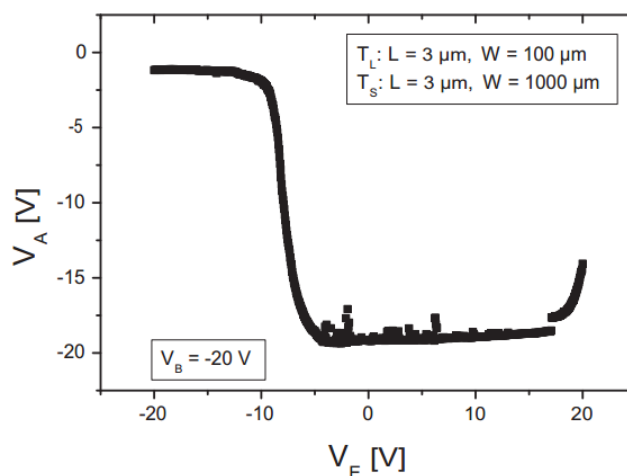
Figure 22. Voltage characteristics of a pentacene based inverter using a high-*k* dielectric (t_{ins} = 300 nm) with the output voltage V_A, input voltage V_E and operating voltage V_B. Adapted from [78].

The previous results related to the high-*k* dielectric, as well as low-temperature processing, led to the investigation of OTFTs on foil substrates, as shown in Figure 23. For the gate electrode, 150 nm of aluminum was evaporated onto a 23 μm PET substrate. The high-*k*-resist containing TiO_2 nanoparticles and gold were used as gate dielectric and drain/source contacts, respectively. Before the deposition of the semiconducting layer, the completed template was treated by an oxygen plasma step to improve the molecular order of the growing pentacene film. A 30 nm thick layer of pentacene was deposited under high-vacuum conditions.
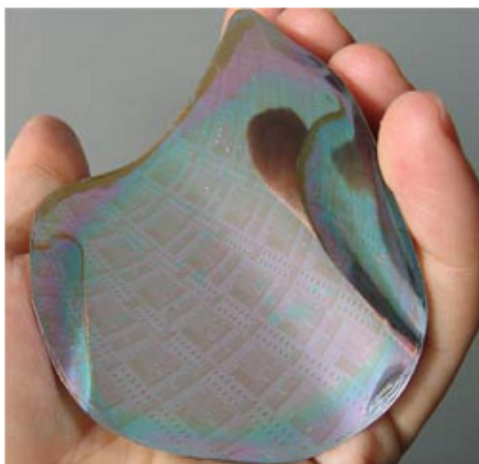
Figure 23. OFET on a PET substrate using a high-*k* dielectric. Reprinted from [47], with permission from John Wiley and Sons.

Electrical characteristics of the resulting transistor device are shown in Figure 24. The maximum drain current is about −36.7 μA at $V_{DS} = −40$ V and $V_{GS} = −40$ V, whereas the on-off ratio is in the order of 10^3. The threshold voltage is −7.5 V and the charge carrier mobility in the saturation regime is 0.35 cm²/Vs [47]. Finally, it should be mentioned that the preparation process can be adjusted to the requirements of ZnO-nanoparticles easily.
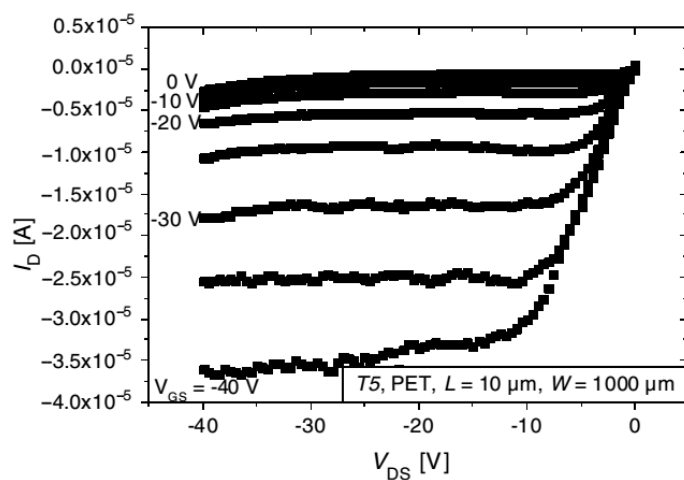
Figure 24. Output characteristics of an inverted coplanar pentacene OTFT using a high-*k* dielectric on a PET substrate (L = 10 μm, W = 1000 μm and t_{ins} = 400 nm). Reprinted from [47], with permission from John Wiley and Sons.

Although the chosen materials and processes are essential to achieve the integration of flexible electronics, flexibility tests are also required to evaluate the effects on device performance. To determine the influence of compression or tensile strain on the electrical properties of TFTs, a systematic change of the bending radius during the electrical characterization has to be carried out. In general, compression or tensile strain causes reversible variations in the channel conductivity until a critical bending radius is reached, and the device is damaged by crack formation in the dielectric layer and delamination of the electrodes [79,80]. An enhancement of the flexibility properties can be achieved either by reducing the substrate thickness or an encapsulation of the TFTs in a sandwich construction between a sealant and the substrate [80]. Recently, Sekitani *et al.* showed a low-voltage organic transistor fabricated on a 12.5 μm thick polymeric substrate covered with an encapsulation stack. The device operated without degradation even at a bending radius of 100 μm [81]. In addition, the gate dielectric influences the device performance as the induced strain modifies the capacitances of the dielectric due to changes in the layers thickness (Poisson-effect) and permittivity.

The electrical properties of materials such as ZnO with a high piezoelectric tensor are influenced when subjected to mechanical stress. Kim *et al.* reported a flexible ZnO transistor using atomic layer deposition. Additionally, the variation in the electrical characteristics in different bending states was discussed and attributed to the ZnO piezoelectric properties [82]. Using a nanoparticular ZnO dispersion, the mechanical stress endured by the transistor during bending states is not transferred to individual nanoparticles. The deformation is instead released through the nanoparticle network. Therefore, the TFT threshold voltage is constant during the bending test; however, the deformation of the ZnO film causes a variation of the physical distance between nanoparticles, which influences the transistor current level, as reported by Jun *et al.* [35].

For organic materials, several results indicate that the electrical properties are influenced by morphological changes in the organic film. Recently, Cosseddu *et al.* showed, by a systematical variation of the pentacene crystal domain size, a modification of the hopping energy barrier for the charge carriers [83]. For instance, as the compression strain shortens the distance between nearby crystal domains, the field-effect mobility is increased.

6. Conclusions

In this article, we discussed the integration processes of (in)organic-based TFTs on foil substrates. As foil substrates are only partially resistant against chemicals and have strict thermic restrictions, the choice of the process parameter is essential. In order to integrate submicron structures on transparent substrates, such as glass or foils, the SWEB technique is a good approach.

For inorganic semiconducting material, Si and ZnO nanoparticle dispersions were evaluated. On the one hand, Si nanoparticulated films are unsuitable for flexible electronics. A low maximum current and a low carrier mobility due to the surrounding oxide shell at the nanoparticle surface were observed. To improve transistor performance, inter-particle connections can be minimized by reducing the transistor's channel length. On the other hand, ZnO nanoparticles are a promising candidate for integration in low-cost devices. Additionally, they are suitable for large-area substrates when applied using spray-coating techniques.

For the organic semiconductor, evaporated pentacene was the main material used to evaluate the performance of OTFTs. Compared with inorganic semiconductors, pentacene suffers from environmental influences such as ambient humidity and oxygen. Both impacts lead to a reduction of the charge carrier mobility and a threshold voltage shift depending on the specific influencing agent. Long-term experiments show that the dominating effect of the pentacene degradation is related to water vapor.

Furthermore, possible dielectric materials were investigated. Inorganic dielectric materials exhibit either high processing temperatures or insufficient mechanical flexibility. Therefore, polymeric and inorganic-organic nanocomposite (high-*k*) dielectrics were established. As the used polymeric dielectrics either suffer from solvents used by optical lithography or introduce instabilities during transistor operation, future research efforts will focus on the use of the high-*k*-resist as dielectric material.

Inverters based on ZnO nanoparticles integrated on a glass substrate were realized. Peak gains of about 4 V/V and a low power consumption were observed. Nevertheless, they are affected by the hysteretic behavior when PVP is used as a gate dielectric. Pentacene and the high-*k*-resist were used for realization of inverters on Si-substrates and integration of TFTs on PET substrates. For the inverters, a stable low- and high-level as well as a peak gain of 5 V/V were observed. The OTFTs exhibited a threshold voltage of -7.5 V and an on-off ratio in the order of 10^3. The charge carrier mobility in the saturation regime was found to be 0.35 cm^2/Vs.

Future works will focus on two main parts, the improvement of the active semiconducting layer and the reduction of parasitic capacitances. To minimize degradation processes for long term applications, organic semiconductors, as C$_n$-DNTT or C$_8$-BTBT, promising good environmental stability, will be used, as well as a combination of humidity and UV-irradiation treatment for stabilization and performance enhancement of the ZnO films. Furthermore, the reduction of the overlap of the drain/source contacts with the gate electrode will lead to a diminution of parasitic capacitances increasing the operation frequency. Additional improvement could be achieved when the semiconductor material is limited to the active transistor areas.

Acknowledgments

Conflicts of Interest

The authors declare no conflict of interest.

References

1. Sirringhaus, H. 25th Anniversary Article: Organic Field-Effect Transistors: The Path Beyond Amorphous Silicon. *Adv. Mater.* **2014**, *26*, 1319–1335.

2. Fortunato, E.; Barquinha, P.; Martins, R. Oxide Semiconductor Thin-Film Transistors: A Review of Recent Advances. *Adv. Mater.* **2012**, *24*, 2945–2986.

3. Hilleringmann, U.; Wolff, K.; Assion, F.; Vidor, F.F.; Wirth, G.I. Semiconductor nanoparticles for electronic device integration on foils. In *AFRICON* Proceeding of the IEEE Africon Conference, Livingstone, Zambia, 13–15 September 2011.

4. Pesavento, P.V.; Chesterfield, R.J.; Newman, C.R.; Frisbie, C.D. Gated four-probe measurements on pentacene thin-film transistors: Contact resistance as a function of gate voltage and temperature. *J. Appl. Phys.* **2004**, *96*, 7312.

5. Hong, D.; Yerubandi, G.; Chiang, H.Q.; Spiegelberg, M.C.; Wager, J.F. Electrical Modeling of Thin-Film Transistors. *Crit. Rev. Solid State Mater. Sci.* **2008**, *33*, 101–132.

6. Youssef, S.; Combette, P.; Podlecki, J.; Asmar, R.A.; Foucaran, A. Structural and Optical Characterization of ZnO Thin Films Deposited by Reactive RF Magnetron Sputtering. *Cryst. Growth Des.* **2009**, *9*, 1088–1094.

7. Gao, W.; Li, Z. ZnO thin films produced by magnetron sputtering. *Ceram. Int.* **2004**, *30*, 1155–1159.

8. Ling, M.M.; Bao, Z. Thin Film Deposition, Patterning, and Printing in Organic Thin Film Transistors. *Chem. Mater.* **2004**, *16*, 4824–4840.

9. Bouchoms, I.; Schoonveld, W.A.; Vrijmoeth, J.; Klapwijk, T.M. Morphology identification of the thin film phases of vacuum evaporated pentacene on SIO2 substrates. *Synth. Metals* **1999**, *104*, 175–178.

10. Scharnberg, M.; Zaporojtchenko, V.; Adelung, R.; Faupel, F.; Pannemann, C.; Diekmann, T.; Hilleringmann, U. Tuning the threshold voltage of organic field-effect transistors by an electret encapsulating layer. *Appl. Phys. Lett.* **2007**, *90*, 13501.

11. Pannemann, C.; Diekmann, T.; Hilleringmann, U. Nanometer scale organic thin film transistors with Pentacene. *Microelectron. Eng.* **2003**, *67–68*, 845–852.

12. Klauk, H.; Halik, M.; Zschieschang, U.; Schmid, G.; Radlik, W.; Weber, W. High-mobility polymer gate dielectric pentacene thin film transistors. *J. Appl. Phys.* **2002**, *92*, 5259.

13. Zschieschang, U.; Ante, F.; Kälblein, D.; Yamamoto, T.; Takimiya, K.; Kuwabara, H.; Ikeda, M.; Sekitani, T.; Someya, T.; Nimoth, J.B.; *et al.* Dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT) thin-film transistors with improved performance and stability. *Org. Electron.* **2011**, *12*, 1370–1375.

14. Xie, W.; Willa, K.; Wu, Y.; Häusermann, R.; Takimiya, K.; Batlogg, B.; Frisbie, C.D. Temperature-Independent Transport in High-Mobility Dinaphtho-Thieno-Thiophene (DNTT) Single Crystal Transistors. *Adv. Mater.* **2013**, *25*, 3478–3484.

15. Kano, M.; Minari, T.; Tsukagoshi, K. Improvement of subthreshold current transport by contact interface modification in p-type organic field-effect transistors. *Appl. Phys. Lett.* **2009**, *94*, 143304.

16. Liu, C.; Minari, T.; Lu, X.; Kumatani, A.; Takimiya, K.; Tsukagoshi, K. Solution-Processable Organic Single Crystals with Bandlike Transport in Field-Effect Transistors. *Adv. Mater.* **2011**, *23*, 523–526.

17. Yuan, Y.; Giri, G.; Ayzner, A.L.; Zoombelt, A.P.; Mannsfeld, Stefan C.B.; Chen, J.; Nordlund, D.; Toney, M.F.; Huang, J.; Bao, Z. Ultra-high mobility transparent organic thin film transistors grown by an off-centre spin-coating method. *Nat. Commun.* **2014**, *5*, doi:10.1038/ncomms4005.

18. Carcia, P.F.; McLean, R.S.; Reilly, M.H.; Nunes, G. Transparent ZnO thin-film transistor fabricated by RF magnetron sputtering. *Appl. Phys. Lett.* **2003**, *82*, 1117.

19. Fortunato, E.M.C.; Barquinha, P.M.C.; Pimentel, A.C.M.B.G.; Gonçalves, Al.M.F.; Marques, A.J.S.; Martins, R.F.P.; Pereira, L.M. Wide-bandgap high-mobility ZnO thin-film transistors produced at room temperature. *Appl. Phys. Lett.* **2004**, *85*, 2541.

20. Nomura, K.; Takagi, A.; Kamiya, T.; Ohta, H.; Hirano, M.; Hosono, H. Amorphous Oxide Semiconductors for High-Performance Flexible Thin-Film Transistors. *Jpn. J. Appl. Phys.* **2006**, *45*, 4303–4308.

21. Joo, H.N.; Seung, Y.R.; Sung, J.J.; Chang, S.K.; Sung-Woo, S.; Rack, P.D.; Dong-Joo, K.; Hong, K.B. Indium Oxide Thin-Film Transistors Fabricated by RF Sputtering at Room Temperature. *IEEE Electron Device Lett.* **2010**, *31*, 567–569.

22. Hoffman, R.L.; Norris, B.J.; Wager, J.F. ZnO-based transparent thin-film transistors. *Appl. Phys. Lett.* **2003**, *82*, 733.

23. Fortunato, E.; Pimentel, A.; Pereira, L.; Gonçalves, A.; Lavareda, G.; Águas, H.; Ferreira, I.; Carvalho, C.N.; Martins, R. High field-effect mobility zinc oxide thin film transistors produced at room temperature. *J. Non-Cryst. Solids* **2004**, *338–340*, 806–809.

24. Barquinha, P.; Pereira, L.; Gonçalves, G.; Martins, R.; Fortunato, E. Toward High-Performance Amorphous GIZO TFTs. *J. Electrochem. Soc.* **2009**, *156*, H161, doi:10.1149/1.3049819.

25. Iwasaki, T.; Itagaki, N.; Den, T.; Kumomi, H.; Nomura, K.; Kamiya, T.; Hosono, H. Combinatorial approach to thin-film transistors using multicomponent semiconductor channels: An application to amorphous oxide semiconductors in In–Ga–Zn–O system. *Appl. Phys. Lett.* **2007**, *90*, 242114, doi:10.1063/1.2749177.

26. Fortunato, E.; Barquinha, P.; Pimentel, A.; Gonçalves, A.; Marques, A.; Pereira, L.; Martins, R. Recent advances in ZnO transparent thin film transistors. *Thin Solid Films* **2005**, *487*, 205–211.

27. Barquinha, P.; Pereira, L.; Gonçalves, G.; Martins, R.; Fortunato, E. The Effect of Deposition Conditions and Annealing on the Performance of High-Mobility GIZO TFTs. *Electrochem. Solid-State Lett.* **2008**, *11*, H248, doi:10.1149/1.2945869.

28. Tominaga, K.; Murayama, T.; Sato, Y.; Mori, I. Energetic oxygen particles in the reactive sputtering of Zn targets in Ar/O2 atmospheres. *Thin Solid Films* **1999**, *343–344*, 81–84.

29. Hong, R.; Qi, H.; Huang, J.; He, H.; Fan, Z.; Shao, J. Influence of oxygen partial pressure on the structure and photoluminescence of direct current reactive magnetron sputtering ZnO thin films. *Thin Solid Films* **2005**, *473*, 58–62.

30. Lim, S.J.; Kwon, S.J.; Kim, H.; Park, J.S. High performance thin film transistor with low temperature atomic layer deposition nitrogen-doped ZnO. *Appl. Phys. Lett.* **2007**, *91*, 183517.

31. Park, S.-H.K.; Hwang, C.-S.; Jeong, H.Y.; Chu, H.Y.; Cho, K.I. Transparent ZnO-TFT Arrays Fabricated by Atomic Layer Deposition. *Electrochem. Solid-State Lett.* **2008**, *11*, H10, doi:10.1149/1.2801017.

32. Kim, S.J.; Yoon, S.; Kim, H.J. Review of solution-processed oxide thin-film transistors. *Jpn. J. Appl. Phys.* **2014**, *53*, 02BA02, doi:10.7567/JJAP.53.02BA02.

33. Jeong, W.H.; Bae, J.H.; Kim, H.J. High-Performance Oxide Thin-Film Transistors Using a Volatile Nitrate Precursor for Low-Temperature Solution Process. *IEEE Electron Device Lett.* **2012**, *33*, 68–70.

34. Faber, H.; Burkhardt, M.; Jedaa, A.; Kälblein, D.; Klauk, H.; Halik, M. Low-Temperature Solution-Processed Memory Transistors Based on Zinc Oxide Nanoparticles. *Adv. Mater.* **2009**, *21*, 3099–3104.

35. Jun, J.H.; Park, B.; Cho, K.; Kim, S. Flexible TFTs based on solution-processed ZnO nanoparticles. *Nanotechnology* **2009**, *20*, 505201, doi:10.1088/0957-4484/20/50/505201.

36. Lee, S.; Jeong, S.; Kim, D.; Park, B.K.; Moon, J. Fabrication of a solution-processed thin-film transistor using zinc oxide nanoparticles and zinc acetate. *Superlattices Microstruct.* **2007**, *42*, 361–368.

37. Myny, K.; Smout, S.; Rockelé, M.; Bhoolokam, A.; Ke, T.H.; Steudel, S.; Cobb, B.; Gulati, A.; Rodriguez, F.G.; Obata, K.; *et al.* A thin-film microprocessor with inkjet print-programmable memory. *Sci. Rep.* **2014**, *4*, 7398.

38. Meyers, S.T.; Anderson, J.T.; Hung, C.M.; Thompson, J.; Wager, J.F.; Keszler, D.A. Aqueous Inorganic Inks for Low-Temperature Fabrication of ZnO TFTs. *J. Am. Chem. Soc.* **2008**, *130*, 17603–17609.

39. Diao, Y.; Tee, B.C.-K.; Giri, G.; Xu, J.; Kim, D.H.; Becerril, H.A.; Stoltenberg, R.M.; Lee, T.H.; Xue, G.; Mannsfeld, Stefan C.B.; *et al.* Solution coating of large-area organic semiconductor thin films with aligned single-crystalline domains. *Nat. Mater.* **2013**, *12*, 665–671.

40. Yoo, S.-H.; Park, M.-K.; Park, J.-S.; Kim, H.-R. Enhanced Adhesion and Transmittance Uniformity in Laminated Polymer-Dispersed Liquid Crystal Films. *J. Opt. Soc. Korea* **2014**, *18*, 753–761.

41. Kim, R.-H.; Holmes, S.; Halle, S.; Dai, V.; Meiring, J.; Dave, A.; Colburn, M.E.; Levinson, H.J. 22-nm-node technology active-layer patterning for planar transistor devices. *J. Micro/Nanolith. MEMS MOEMS* **2010**, *9*, 13001, doi:10.1117/1.3302125.

42. Manfrinato, V.R.; Wen, J.; Zhang, L.; Yang, Y.; Hobbs, R.G.; Baker, B.; Su, D.; Zakharov, D.; Zaluzec, N.J.; Miller, D.J.; *et al.* Determining the Resolution Limits of Electron-Beam Lithography: Direct Measurement of the Point-Spread Function. *Nano Lett.* **2014**, *14*, 4406–4412.

43. Hilleringmann, U.; Vidor, F.F.; Assion, F. Application of side-wall deposition and etch-back technology for nanometer scale device integration. In Proceedings of the Pan African Conference on Science, Computing and Telecommunications (PACT), Arusha, Tanzania, 14–18 July 2014; pp. 98–103.

44. Knipp, D.; Street, R.; Krusor, B.; Apte, R.; Ho, J. Polycrystalline pentacene thin films for large area electronic applications. *J. Non-Cryst. Solids* **2002**, *299–302*, 1042–1046.

45. Steudel, S.; de Vusser, S.; de Jonge, S.; Janssen, D.; Verlaak, S.; Genoe, J.; Heremans, P. Influence of the dielectric roughness on the performance of pentacene transistors. *Appl. Phys. Lett.* **2004**, *85*, 4400, doi:10.1063/1.1815042.

46. Klauk, H.; Gundlach, D.J.; Nichols, J.A.; Jackson, T.N. Pentacene organic thin-film transistors for circuit and display applications. *IEEE Trans. Electron Devices* **1999**, *46*, 1258–1263.

47. Diekmann, T.; Pannemann, C.; Hilleringmann, U. Dielectric layers for organic field effect transistors as gate dielectric and surface passivation. *Phys. Stat. Sol. (A)* **2008**, *205*, 564–577.

48. Lee, M.W.; Song, C.K. Oxygen Plasma Effects on Performance of Pentacene Thin Film Transistor. *Jpn. J. Appl. Phys.* **2003**, *42*, 4218–4221.

49. Pannemannn, C.; Diekmann, T.; Hilleringmann, U. Organic Field-Effect-Transistors with Pentacene for radio-controlled-price-tag applications. *Adv. Radio Sci.* **2003**, *1*, 219–221.

50. Liang, Y.; Dong, G.; Hu, Y.; Wang, L.; Qiu, Y. Low-voltage pentacene thin-film transistors with Ta2O5 gate insulators and their reversible light-induced threshold voltage shift. *Appl. Phys. Lett.* **2005**, *86*, 132101.

51. Iino, Y.; Inoue, Y.; Fujisaki, Y.; Fujikake, H.; Sato, H.; Kawakita, M.; Tokito, S.; Kikuchi, H. Organic Thin-Film Transistors on a Plastic Substrate with Anodically Oxidized High-Dielectric-Constant Insulators. *Jpn. J. Appl. Phys.* **2003**, *42*, 299–304.

52. Cipolloni, S.; Mariucci, L.; Valletta, A.; Simeone, D.; de Angelis, F.; Fortunato, G. Aging effects and electrical stability in pentacene thin film transistors. *Thin Solid Films* **2007**, *515*, 7546–7550.

53. Jackson, T.N.; Yen-Yi Lin; Gundlach, D.J.; Klauk, H. Organic thin-film transistors for organic light-emitting flat-panel display backplanes. *IEEE J. Select. Top. Quantum Electron.* **1998**, *4*, 100–104.

54. Jurchescu, O.D.; Baas, J.; Palstra, Thomas T.M. Effect of impurities on the mobility of single crystal pentacene. *Appl. Phys. Lett.* **2004**, *84*, 3061.

55. Pannemann, C.; Diekmann, T.; Hilleringmann, U. Degradation of organic field-effect transistors made of pentacene. *J. Mater. Res.* **2004**, *19*, 1999–2002, doi:10.1557/JMR.2004.0267.

56. Pannemann, C.; Diekmann, T.; Hilleringmann, U. On the degradation of organic field-effect transistors. In Proceedings of the 16th International Conference on Microelectronics (ICM), Tunis, Tunisia, 6–8 December 2004; pp. 76–79.

57. Northrup, J.E.; Chabinyc, M.L. Gap states in organic semiconductors: Hydrogen- and oxygen-induced states in pentacene. *Phys. Rev. B* **2003**, doi:10.1103/PhysRevB.68.041202.

58. Verlaak, S.; Arkhipov, V.; Heremans, P. Modeling of transport in polycrystalline organic semiconductor films. *Appl. Phys. Lett.* **2003**, *82*, 745.

59. Knipp, D.; Street, R.A.; Völkel, A.; Ho, J. Pentacene thin film transistors on inorganic dielectrics: Morphology, structural properties, and electronic transport. *J. Appl. Phys.* **2003**, *93*, 347.

60. Pi, X.D.; Mangolini, L.; Campbell, S.A.; Kortshagen, U. Room-temperature atmospheric oxidation of Si nanocrystals after HF etching. *Phys. Rev. B* **2007**, doi:10.1103/PhysRevB.75.085423.

61. Wolff, K.; U. Hilleringmann. Silicon Nanoparticles contacted by metal nanogaps for FET applications. In *Technical Proceedings of the 2007 Nanotechnology Conference and Trade Show*; NSTI Nanotech: Boca Raton, FL, USA, 2007; Volume 1, pp. 185–188.

62. Wolff, K.; Hilleringmann, U. N-type single nanoparticle ZnO transistors processed at low temperature. In Proceedings of the European Solid State Device Research Conference (ESSDERC), Athens, Greece, 14–18 September 2009; pp. 460–463.

63. Assion, F.; Wolff, K.; Hilleringmann, U. Low-Temperature Integration of Nanoparticulate Zinc Oxide FETs on Glass Substrate. In Proceedings of the European Solid State Device Research Conference (ESSDERC), Seville, Spain, 14–16 September 2010; p. 17.

64. Wolff, K.; Hilleringmann, U. Analysis and modeling of pseudo-short-channel effects in ZnO-nanoparticle thin-film transistors. In Proceedings of the European Solid State Device Research Conference (ESSDERC), Seville, Spain, 14–16 September 2010; pp. 226–229.

65. Vidor, F.F.; Wirth, G.I.; Wolff, K.; Hilleringmann, U. Study on the Performance Enhancement of ZnO Nanoparticles Thin-Film Transistors. *ECS Trans. (ECST)* **2011**, *39*, 109–115.

66. Wolff, K.; Hilleringmann, U. Solution processed inverter based on zinc oxide nanoparticle thin-film transistors with poly(4-vinylphenol) gate dielectric. *Solid-State Electron.* **2011**, *62*, 110–114.

67. Veres, J.; Ogier, S.; Lloyd, G.; Leeuw, D. de. Gate Insulators in Organic Field-Effect Transistors. *Chem. Mater.* **2004**, *16*, 4543–4555.

68. Lim, S.C.; Kim, S.H.; Koo, J.B.; Lee, J.H.; Ku, C.H.; Yang, Y.S.; Zyung, T. Hysteresis of pentacene thin-film transistors and inverters with cross-linked poly(4-vinylphenol) gate dielectrics. *Appl. Phys. Lett.* **2007**, *90*, 173512.

69. Hirschwald, W.H. Zinc oxide: an outstanding example of a binary compound semiconductor. *Acc. Chem. Res.* **1985**, *18*, 228–234.

70. Morrison, S. Semiconductor gas sensors. *Sens. Actuat.* **1981**, *2*, 329–341.

71. Vidor, F.F.; Wirth, G.; Assion, F.; Wolff, K.; Hilleringmann, U. Characterization and Analysis of the Hysteresis in a ZnO Nanoparticle Thin-Film Transistor. *IEEE Trans. Nanotechnol.* **2013**, *12*, 296–303.

72. Vidor, F.F.; Wirth, G.I.; Hilleringmann, U. Low temperature fabrication of a ZnO nanoparticle thin-film transistor suitable for flexible electronics. *Microelectron. Reliab.* **2014**, *54*, 2760–2765.

73. Vidor, F.F.; Ulrich Hilleringmann. Integration von ZnO Nanopartikel Dünnschicht-Transistoren durch Sprühbeschichtung. In *GMM-Fachbericht-Mikro-Nano-Integration*; VDE-Verlag: Berlin, Germany, 2014.

74. Meulenkamp, E.A. Electron Transport in Nanoparticulate ZnO Films. *J. Phys. Chem. B* **1999**, *103*, 7831–7838.

75. Xu, J.; Pan, Q.; Shun, Y.; Tian, Z. Grain size control and gas sensing properties of ZnO gas sensor. *Sens. Actuat. B: Chem.* **2000**, *66*, 277–279.

76. Wolff, K.; Hilleringmann, U. Inverter circuits on glass substrates based on ZnO-nanoparticle thin-film transistors. *Solid State Electron.* **2012**, *67*, 11–16.

77. Degussa AG. *Advanced Nanomaterials*; Datasheet "AdNano Zinc Oxide": Hanau, Germany, 2011.

78. Diekmann, T. Polymere Dielektrika für Organische Feldeffekt-Transistoren Mit Pentacen auf Foliensubstraten. Ph.D. Thesis, University of Paderborn, Paderborn, Germany, 20 December 2007.

79. Song, K.; Noh, J.; Jun, T.; Jung, Y.; Kang, H.-Y.; Moon, J. Fully Flexible Solution-Deposited ZnO Thin-Film Transistors. *Adv. Mater.* **2010**, *22*, 4308–4312.

80. Sekitani, T.; Kato, Y.; Iba, S.; Shinaoka, H.; Someya, T.; Sakurai, T.; Takagi, S. Bending experiment on pentacene field-effect transistors on plastic films. *Appl. Phys. Lett.* **2005**, *86*, 73511.

81. Sekitani, T.; Zschieschang, U.; Klauk, H.; Someya, T. Flexible organic transistors and circuits with extreme bending stability. *Nat. Mater.* **2010**, *9*, 1015–1022.

82. Kim, J.-M.; Nam, T.; Lim, S.J.; Seol, Y.G.; Lee, N.-E.; Kim, D.; Kim, H. Atomic layer deposition ZnO:N flexible thin film transistors and the effects of bending on device properties. *Appl. Phys. Lett.* **2011**, *98*, 142113.

83. Cosseddu, P.; Tiddia, G.; Milita, S.; Bonfiglio, A. Continuous tuning of the mechanical sensitivity of Pentacene OTFTs on flexible substrates: From strain sensors to deformable transistors. *Org. Electron.* **2013**, *14*, 206–211.