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A Novel Single-switch Phase Controlled Wireless Power Transfer System

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Abstract: Battery charging is a fundamental application of Wireless Power Transfer (WPT) systems that requires effective implementation of Constant Current (CC) and Constant Voltage (CV) power conduction modes. DC-DC converters used in WPT systems utilize large inductors and capacitors that increase the size and volume of the system in addition to causing higher DC losses. This work proposes a novel single-switch active rectifier for phase controlled WPT systems that is smaller in volume and weight as compared to conventional WPT topologies. The proposed method simplifies the control scheme using improved Digital Phase Control (DPC) and Analog Phase Control (APC) to realize the CC and CV power transfer modes. Furthermore, it prevents forward voltage losses in Silicon Carbide (SiC) switches and shoot through states with improved switching patterns. Simulation studies and experimental results are added to verify the effectiveness of the proposed methodology.

Keywords: active rectifiers; single-switch; analog phase control; digital phase control; wireless power transfer

1. Introduction

WPT techniques can realize energy conversion without physical connections. It has gained tremendous attention in both research and industry. Recently, wireless charging is the focus of study. To improve battery life time, the system has special requirements for the charging current and voltage profiles. WPT systems can realize both CC and CV power transfer modes through either primary or secondary side control. However, primary side control requires an additional communication channel [1,2]. It is more simplified and straightforward to directly achieve the CC and CV power transfer modes through secondary side control. Therefore, various DC-DC converters [3–8] are installed on the receiver side for power regulation, including buck converter [4], boost converter [5,9,10], and buck-boost converter [6,11]. Although DC-DC converters have simpler controls, they require additional capacitors and inductors that increase the weight, volume, and cost of the receiver. In addition, more cascaded circuits result in more losses on the DC side. To address these drawbacks, researchers propose active rectifiers on the receiver side. Active rectifiers are initially put forward to reduce the conduction losses of the diode rectifier and transfer the power bi-directionally [12–19]. Recently, Phase Control (PC) method is introduced to regulate resonant currents [20–25], which can further reduce the energy consumed by parasitic resistances.

Active rectifiers proposed for WPT systems can be classified into three categories: (i) full bridge rectifier with four switches; (ii) semi-bridgeless rectifier with two switches; and (iii) single- switch rectifier. Full active bridge rectifiers are used in various applications [12–25]. Four Metal-Oxide-

Semiconductor Field Effect Transistors (MOSFETs) and four isolated driver circuits are installed on the receiver side. Short circuit may appear in the full bridge topology due to faulty operation. Such a characteristic reduces the reliability of the WPT systems, especially battery charging systems where short circuit can lead to fire and explosion. It is desirable to investigate a more cost-effective and reliable approach to achieve secondary PC. Therefore, researchers in [26–28] develop two-switch rectifiers for WPT systems. In [26,27], a semi-bridgeless topology with two MOSFETs is proposed, where two switches are installed on the lower side of the rectifier. Secondary PC can be achieved as well. In [28], two MOSFETs are in reverse connection and controlled by one signal. Duty ratio control is applied to regulate the power. Furthermore, researchers in [29–36] investigate single-switch rectifiers. In [29], a switch is connected in parallel with a resonant compensation capacitor. Power regulation can be achieved by tuning/detuning through this variable capacitor. However, this method makes the system deviate from optimal resonant point, which may cause an efficiency drop. In [30–32], a switch is connected in series with parallel resonant tank. When the switch is turned off, the receiver transfers the power only in half the period. In addition, it is difficult to obtain a stable DC voltage. In [33], an active switch is inserted into the lower phase leg of a full diode bridge. When the switch is turned on, the resonant tank is shorted in half the period and the power can be regulated by duty ratio control. In [34–36], a boost converter is directly connected after the diode bridge which reduces one filter capacitor.

Active rectifiers with two or four switches can realize PC [12–27], whereas previous single-switch rectifiers can only adopt duty ratio control [29–36]. Although duty ratio control is easier to implement, it can cause resonant current oscillations when the power transfer path is chopped. It requires larger filter capacitors to maintain the desired DC voltage. In addition, single-switch receivers in [29–33] are half-controlled, i.e., their power regulation abilities are restricted, which may fail to meet the CC and CV power transfer requirements.

This paper proposes a novel single-switch phase controlled receiver for WPT systems for the first time. With this method, the secondary side inductor is removed and only a small filter capacitor is added, thereby reducing the size of the receiver and lessening the number of switches used. The salient contributions of this work are:

(1) The proposed methodology reduces the number of active switches and isolated driver circuits as compared to conventional phase controlled receivers.
(2) An APC method is applied to this improved receiver that circumvents synchronization algorithms and additional programming. APC method regulates the power automatically, which reduces the difficulty in design and implementation.
(3) Most previously discussed single-switch methods are half-controlled and use duty ratio variation. In this work, the receiver is fully controlled and has a stronger power regulation ability as compared to conventional single-switch receivers.
(4) The proposed receiver fully utilizes the SiC MOSFET to reduce switching losses while avoiding high forward voltage losses through its intrinsic diode.

This paper is divided as follows: Section 2 shows the proposed single-switch receiver and illustrates its operating modes. Then, it presents the derivations for the CC and CV power transfer modes. Section 3 elaborates the detailed implementation techniques of the proposed DPC and APC methods. In Section 4, simulations and experiments are added to validate the feasibility and effectiveness of the proposed topology and control methods. Finally, Section 5 concludes this paper.

2. Modeling and Analysis

This section presents mathematical modeling and analysis for the proposed WPT system.

2.1. Proposed Topology

A WPT system with the proposed single-switch receiver is shown in Figure 1. U_i and U_o are the DC voltages, whereas v_p and v_s are the primary and secondary resonant voltages. L_p and L_s are the

primary and secondary coil inductances, which are compensated by C_p and C_s, respectively. S_1–S_5 are the SiC MOSFETs, and D_1–D_5 are the diodes. C_i and C_o are the filter capacitors, and R_L is the load. i_1 and i_2 are the currents flowing through S_5 and D_5, respectively. I_i and I_o denote the input and output DC currents.

The typical waveforms of the proposed topology are shown in Figure 2, where 2β presents the phase angle of v_s. According to the current directions and paths, the receiver has six operating modes as depicted in Figure 3.

Mode 1: $i_s > 0$, and S_5 is on. There exist two current loops on the receiver side: L_s–D_1–S_5–D_4–C_s and C_o–R_L. The diode bridge is short-circuited by S_5, and I_o is supplied by C_o. Thus, v_s is zero.

Mode 2: $i_s > 0$, and S_5 is turned off at the beginning of Mode 2. C_o charges, and U_o increases. Thus, the current loop is L_s–D_1–D_5–U_o–D_4–C_s. v_s is basically equal to U_o.

Mode 3: $i_s > 0$, and S_5 is turned on at the beginning of Mode 3. Then, i_s flows through S_5 and v_s becomes zero. U_o is supplied by C_o, and it begins to decrease. The current loops are: L_s–D_1–S_5–D_4–C_s and C_o–R_L.

Mode 4: S_5 remains on and v_s. remains zero, whereas i_s changes its direction. U_o continues to decrease. The current loop of i_s becomes L_s–C_s–D_3–S_5–D_2.

Mode 5: $i_s < 0$, and S_5 is turned off at the beginning of Mode 5. C_o charges via i_s, and U_o begins to increase. The current loop is L_s–C_s–D_3–D_5–U_o–D_2. v_s is basically equal to $-U_o$.

Mode 6: $i_s < 0$, and S_5 is turned on at the beginning of Mode 6. The current loop of i_s becomes L_s–C_s–D_3–S_5–D_2, and U_o is supplied by C_o again.

To minimize switching losses, a SiC MOSFET can be used. Since the forward voltage of the intrinsic diode of the SiC MOSFET is high, a SiC diode is connected in parallel to overcome the high forward voltage loss of the intrinsic diode. However, no current freewheels through S_5 in the proposed receiver, which means the SiC diode is not necessary in this application. Therefore, the proposed receiver can fully utilize the SiC MOSFET to reduce switching losses while avoiding its drawback of high forward voltage losses through its intrinsic diode.

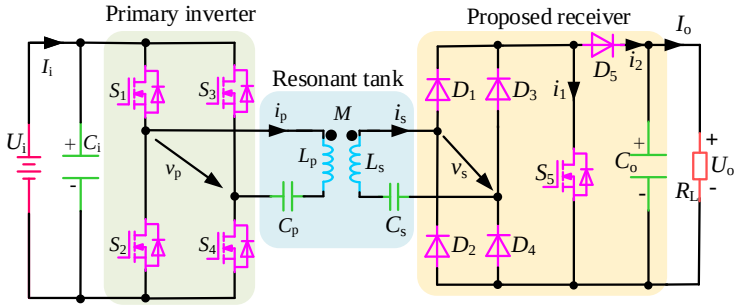

Figure 1. WPT system with proposed single-switch receiver.

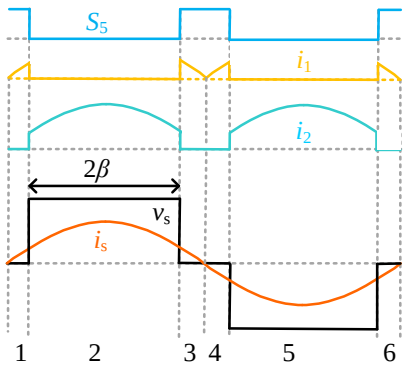

Figure 2. Typical waveforms of proposed receiver. S_5, gate drive signal (blue line); i_1, current flowing through MOSFET (yellow line); i_2, current flowing through D_5 (light green line); i_s, secondary resonant current (orange line); v_s, secondary resonant voltage (black line).

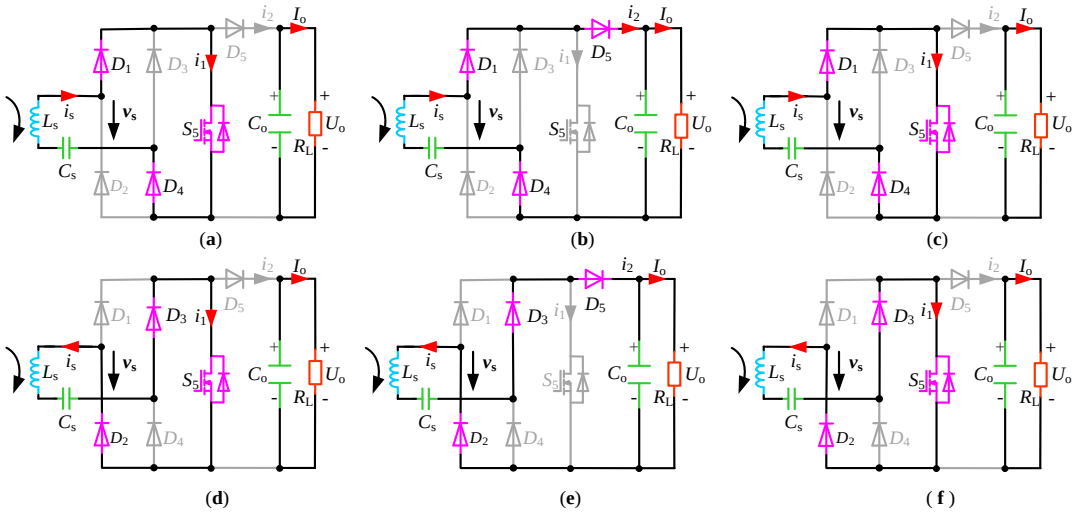

Figure 3. Operating modes of proposed receiver: (**a**) Mode 1; (**b**) Mode 2; (**c**) Mode 3; (**d**) Mode 4; (**e**) Mode 5; and (**f**) Mode 6.

2.2. Power Regulation

The CC and CV power transfer realizations are the basic requirements for battery charging systems. This section presents the theoretical analysis of secondary side control through proposed single-switch phase-controlled receiver.

The system operates at the resonant frequency, that is

$$\omega = \frac{1}{\sqrt{L_p C_p}} = \frac{1}{\sqrt{L_s C_s}} \tag{1}$$

R_p and R_s represent primary and secondary coil resistances, respectively. Then, the following equations are obtained according to Kirchhoff Voltage Law (KVL).

$$v_p = -j\omega M i_s + i_p R_p \tag{2}$$

$$j\omega M i_p = v_s + i_s R_s \tag{3}$$

According to Fourier series and fundamental harmonic analysis [23–25], the root-mean-square value of v_s (V_s) can be denoted as:

$$V_s = \frac{2\sqrt{2}}{\pi} U_o \sin\beta. \tag{4}$$

Without considering the switching losses, the input and output powers of the rectifier are equal.

$$V_s I_s \simeq U_o I_o \tag{5}$$

Then, I_o versus I_s is deduced.

$$I_o \simeq \frac{2\sqrt{2}\sin\beta}{\pi} I_s \tag{6}$$

According to Equation (2), i_s can be rewritten as

$$i_s = \frac{v_p - i_p R_p}{-j\omega M} \simeq \frac{v_p}{-j\omega M} \tag{7}$$

Thus, I_o and U_o can be approximately derived as Equations (8) and (9).

$$I_o \simeq \frac{2\sqrt{2}\sin\beta}{\pi\omega M} V_p \tag{8}$$

$$U_o \simeq \frac{2\sqrt{2}R_L \sin\beta}{\pi\omega M} V_p \tag{9}$$

A larger β means a larger I_o and U_o. Therefore, β can be utilized to achieve the CC and CV power transfer modes.

3. Implementation Methods

This section presents implementation techniques for realizing DPC and APC with the proposed receiver in WPT system.

3.1. Digital Phase Control

The schematic of the DPC system is shown in Figure 4, where two independent Digital Signal Processors (DSPs) are installed. Digital control is widely used for various applications due to its flexibility. Since the controller should be isolated from the main circuit for safety consideration, isolated driver circuits as well as isolated power supplies are installed on primary and secondary sides. Furthermore, isolated current and voltage sensors are required on the receiver side for output electrical information feedback. To avoid power oscillations, the synchronization of secondary receiver is of essential importance. In [24], secondary synchronization is realized by utilizing the resonant voltage across C_s. The synchronization circuit consists of a comparator and an isolator, as shown in Figure 4, where R_h and R_l are the divider resistances. The operating frequency of the receiver-side switches in the full active bridge is equal to the current frequency, whereas it is twice that frequency in the proposed receiver. Thus, the receiver is synchronized once every two periods.

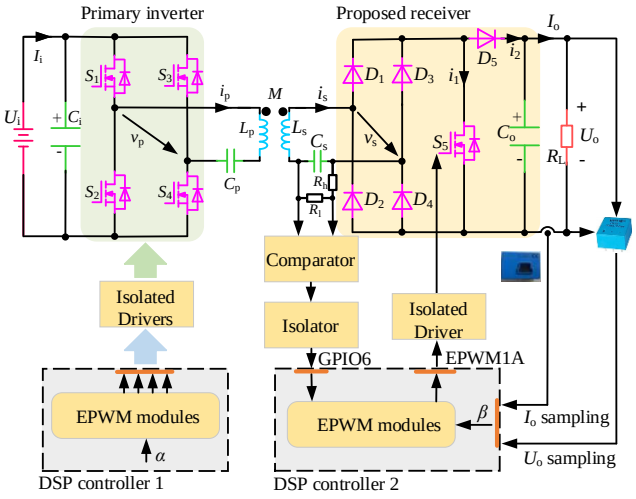

Figure 4. Schematic of DPC system.

Figure 5 shows the typical synchronization waveforms. The comparator turns the divided sinusoidal voltage into a square-wave synchronization signal. After passing a digital isolator, it is sent to the synchronization port of the DSP controller. TBPRD, CMPA, and CMPB are the time base period and comparing values of the reserved registers of the controller, respectively. The 0 and TBPRD shown in Figure 5 are the minimum and maximum values of the counter of the controller, i.e., CMPA and CMPB fall within the range of [0, TBPRD]. When the counter reaches CMPA, S_5 is turned off. When the counter reaches CMPB, S_5 is turned on. The relationships among TBPRD, CMPA, CMPB, and β are shown in Equations (10) and (11).

$$\text{CMPA} = \frac{180 - \beta}{180}\text{TBPRD} \tag{10}$$

$$\text{CMPB} = \frac{\beta}{180}\text{TBPRD} \tag{11}$$

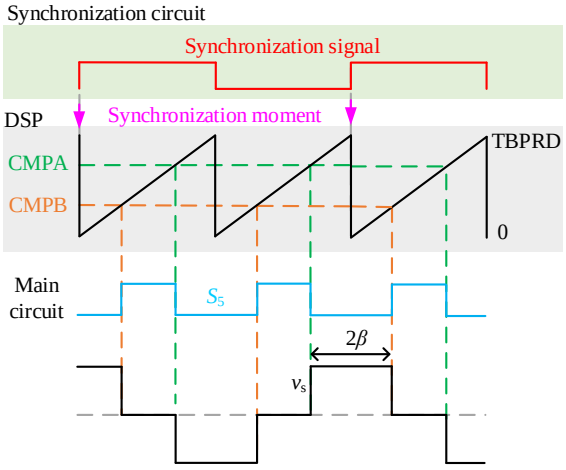

Figure 5. Typical synchronization waveforms.

TBPRD is determined by the inverter frequency, and the comparing values produce the desired β. Afterwards, the corresponding gate drive signal generates v_s in the main circuit.

As analyzed in Section 2, a larger β brings about larger I_o and U_o. Therefore, the output power regulation can be achieved by changing β. The algorithm flowchart of the CC and CV power transfer modes is shown in Figure 6, where I_o^* and U_o^* are the expected current and voltage values. Power transfer mode selection is determined by one bit, referred to as "Mode", which is defined in the controller. The designer can initialize the Mode by setting it at 1 or 0 in the software code. When the Mode is 1, the receiver operates at the CC power transfer mode, otherwise, it operates at the CV power transfer mode. I_o is sampled for the CC power transfer mode, and U_o for the CV power transfer mode. To obtain accurate sampling values, 20 samplings of I_o or U_o are averaged. β ranges from 0° to 90°. When I_o or U_o is smaller than the desired value, β is increased by 0.1°. Otherwise, β is decreased by 0.1°. This control algorithm is simple and effective. The primary controller is turned on and the primary active bridge inverts the high frequency voltage. The frequency locking signal is generated, whereas the receiver-side controllers remain on standby and the diode rectification is used by the receiver at first. When U_o reaches the threshold value, the controller is turned on.

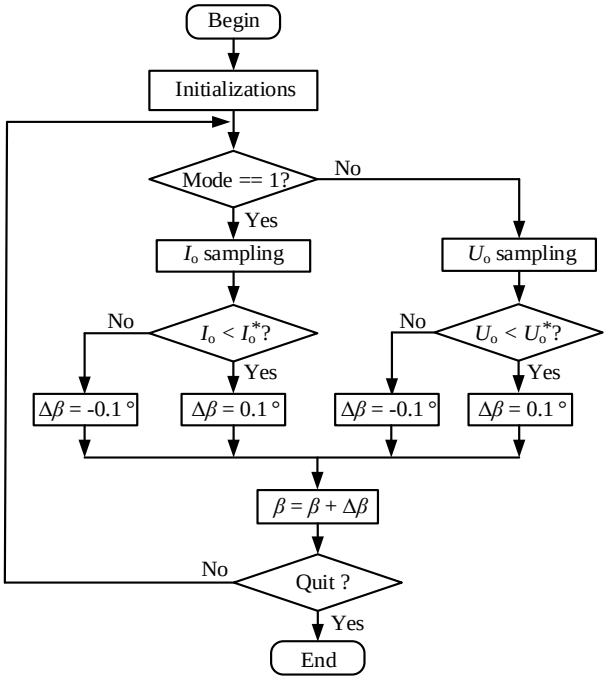

Figure 6. Algorithm flowchart of DPC receiver.

In full active bridge receivers, four gate drive signals should be controlled to generate v_s. However, β is determined by one signal in the proposed receiver, which makes the software code realization easier.

3.2. Analog Phase Control

The DPC method can achieve good control flexibility and performance. However, the receiver requires some auxiliary circuits. To further reduce the complexity and cost of the receiver, a novel APC method is presented as follows.

The schematic of the proposed APC system is shown in Figure 7. R_1 and R_2 are the divider resistances. R_3 and R_9 are the sampling resistances. The voltage across R_3 is fed back for the CC power transfer, and the divided voltage across R_2 for the CV power transfer. Since R_3 is small, and R_4 and R_5 are used to amplify the signal. In APC system, power transfer mode selection is realized by a 2:1 switch. R_1–R_5 should satisfy Equation (12).

$$I_o^* R_3 \frac{R_4 + R_5}{R_4} = U_o^* \frac{R_2}{R_1 + R_2} \tag{12}$$

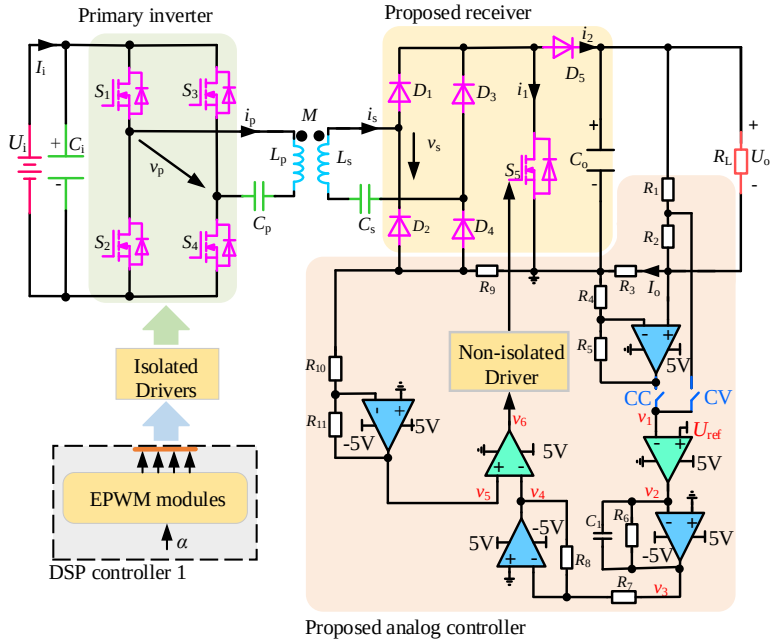

Figure 7. Schematic of APC system.

U_{ref} is a reference voltage. The relationships among U_o^*, I_o^*, and U_{ref} are given in Equations (13) and (14). Different output current and voltage can be achieved by setting U_{ref} and R_1–R_5.

$$I_o^* = \frac{U_{ref} R_4}{R_3 (R_4 + R_5)} \tag{13}$$

$$U_o^* = \frac{U_{ref} (R_1 + R_2)}{R_2} \tag{14}$$

R_6 and C_1 act as an integrator. Their values have a great influence on the dynamic and static performances of the system. To better demonstrate this characteristic, time constant τ is defined as Equation (15).

$$\tau = R_6 C_1 \tag{15}$$

A smaller τ brings about a faster dynamic response with a larger overshoot, whereas a larger τ corresponds to a better static performance with a slower dynamic response.

Figure 8 shows the typical waveforms of the APC receiver. When I_o (or U_o) is greater than I_o^* (or U_o^*), v_1 is greater than U_{ref}, and the comparator generates a zero v_2. Otherwise, a positive v_2 is produced. v_3 decreases for a positive v_2 and increases for a zero v_2. Since v_3 is negative, an inverting amplifier is used. The ratio of R_8 versus R_7 can regulate the response characteristic. i_s flows through R_9, and the voltage drop is amplified by R_{10} and R_{11}, which obtains a half-wave voltage v_5. Then, v_4 and v_5 are sent to a comparator, and they can produce the desired control signal. After passing the non-isolated driver circuit, the gate drive signal is fed to the switch. When S_5 is turned on, the receiver is short-circuited, which results in a zero v_s. When S_5 is turned off, v_s becomes U_o or $-U_o$. β is automatically regulated by the feedback signals.

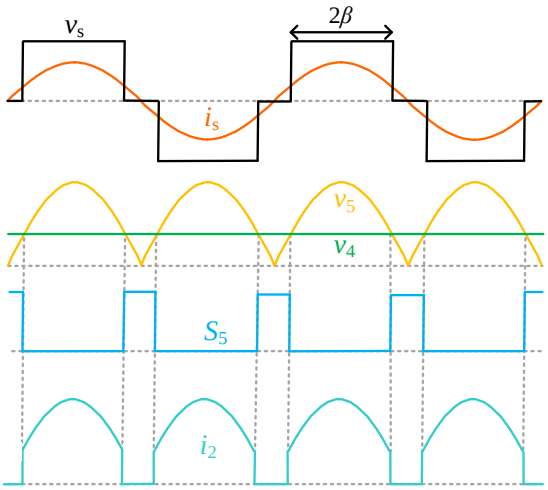

Figure 8. Typical waveforms of APC receiver. i_s, secondary resonant current (orange line); v_s, secondary resonant voltage (black line); v_4, feedback signal (green line); v_5, half-wave signal (yellow line); S_5, gate drive signal (blue line); i_2, current flowing through D_5 (light green line).

The CC and CV power transfer modes can be achieved through the proposed analog controller. Meanwhile, the receiver does not require synchronization techniques and additional programming. Thus, the proposed APC method significantly reduces the difficulty in implementation, the cost, volume, and weight of the receiver.

4. Simulation and Experiment

Results are obtained from simulation studies in PLECS and hardware prototype experiments. Both results are presented and compared to validate the feasibility of the proposed topology and control methods. The main parameters of the WPT system are listed in Table 1. L_p and L_s are 150 µH and 200 µH with a coil distance of 10 cm. The primary and secondary coils are compensated by 23 nF and 17 nF resonant capacitors, respectively. The inverting frequency of the transmitter is 85 kHz. The diodes are MUR3020PT, with a low forward voltage drop of 1 V. SiC MOSFETs are SCT3030KL. Heat sinks are installed on each diode and MOSFET.

Table 1. Main parameters of WPT system.

Symbol	Quantity	Value
L_p	coil inductance of transmitter	150 µH
L_s	coil inductance of receiver	200 µH
C_p	primary compensation capacitance	23 nF
C_s	secondary compensation capacitance	17 nF
f	inverting frequency	85 kHz

4.1. Digital Phase Control

The prototype photograph of the DPC system is shown in Figure 9. Two TMS320F28335 chips are used as the primary and secondary controllers. The transmitter inverts the DC voltage into high frequency resonant voltage v_p. Then, v_s is induced by the magnetic field generated by i_p. Afterwards, secondary resonant current i_s is rectified into DC current I_o by the proposed receiver. Finally, the power is consumed by Chroma programmable AC-DC electronic load model 63803. Current and voltage sensors are installed to sample the feedback signals for power regulation. ACPL-W346 chips are used as the isolated drivers which are supplied by isolated DC-DC converter G1212S-2W.

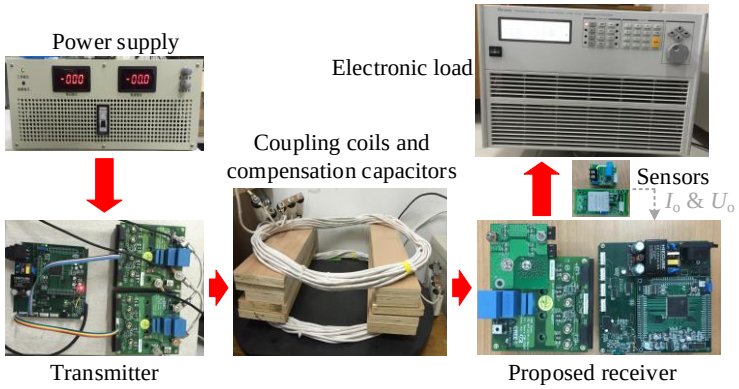

Figure 9. Prototype photograph of DPC system.

Figure 10 shows the typical waveforms of the DPC receiver. To ensure that the signal fed to the comparator stays within a proper range, the values of the divider resistances should be configured with the power level. In this paper, the high-side resistance R_h is 2 MΩ and the low-side resistance R_l is 10 kΩ. The voltage across C_p generates the synchronization signal, and it is fed to GPIO6 of the controller. v_s and i_s are controlled to be in phase. The desired output voltage or current is realized by regulating β.

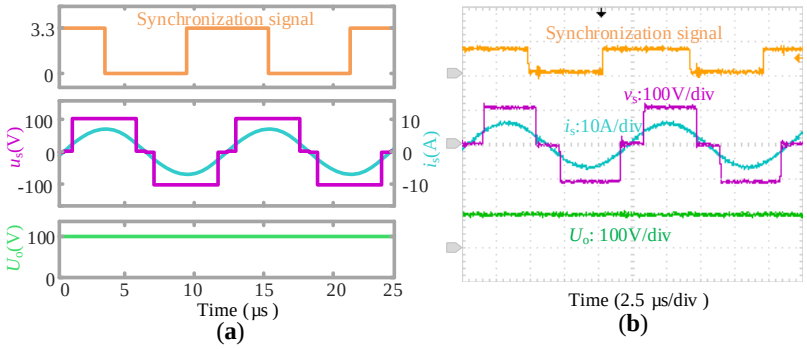

Figure 10. Typical waveforms of DPC receiver: (**a**) simulated; and (**b**) experimental. Synchronization signal (yellow lines); i_s, secondary resonant current (blue lines); v_s, secondary resonant voltage (purple lines); U_o, output voltage (green lines).

Figure 11a,b shows the simulated and experimental CC power transfer results by DPC. The reference current is set at 2 A, and R_L changes from 25 Ω to 50 Ω. When R_L is 25 Ω, the simulated and experimental values of β are 27.8° and 27.4°, respectively. The simulated and experimental output currents are 2.00 A and 1.96 A, which correspond to 83.3% and 80.8% DC-to-DC efficiencies, respectively. When R_L is 50 Ω, the simulated and experimental values of β are 28.6° and 27.5°, respectively. The simulated and experimental output currents are 1.99 A and 1.97 A, with DC-to-DC efficiencies of 90.0% and 86.2%, respectively. I_o keeps unchanged against load variations.

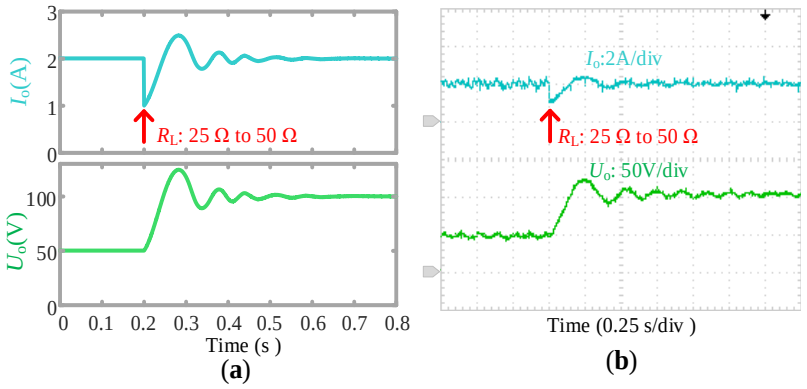

Figure 11. Simulated and experimental CC power transfer results of DPC system: (**a**) simulated; and (**b**) experimental. I_o, output current (blue lines); U_o, output voltage (green lines).

Figure 12a,b shows the simulated and experimental CV power transfer results by DPC. The reference voltage is set at 100 V. When R_L is 25 Ω, the simulated and experimental values of β are 73.9° and 73.5°, which produce 100.0 V and 101.2 V output voltages, respectively. The simulated and experimental efficiencies are 93.1% and 91.4%, respectively. When R_L is 50 Ω, the simulated and experimental values of β become 27.7° and 28.1°, respectively. The corresponding output voltages are 99.5 V and 100.5 V, with DC-to-DC efficiencies of 90.0% and 85.8%, respectively. During load variations, U_o remains at the desired level by regulating β accordingly.

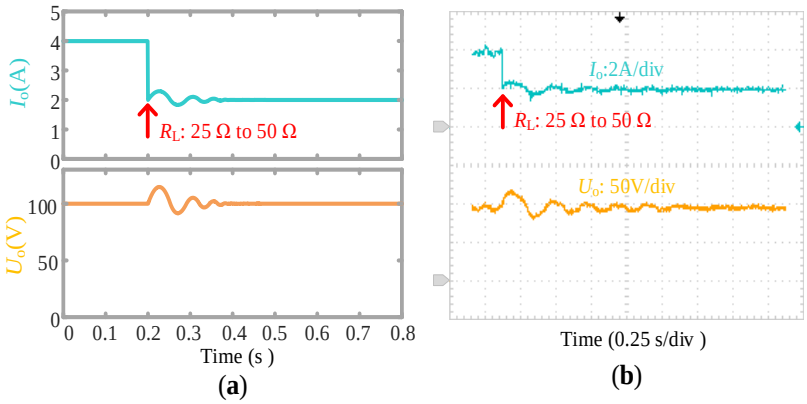

Figure 12. Simulated and experimental CV power transfer results of DPC system: (**a**) simulated; and (**b**) experimental. I_o, output current (blue lines); U_o, output voltage (yellow lines).

4.2. Analog Phase Control

A photograph of the APC receiver is shown in Figure 13. U_{ref} is set at 2.5 V. The divider resistances R_1 and R_2 are 91 kΩ and 2.2 kΩ, respectively. The sampling resistances R_3 and R_9 are 10 mΩ. R_4 and R_5 are 0.5 kΩ (1 kΩ//1 kΩ) and 62 kΩ, respectively. The ratios of R_7 versus R_8 and R_{11} versus R_{10} are 1 and 22, which ensures v_4 and v_5 falling within proper ranges. TLV3502 and THS4062 are used as the comparator and the operational amplifier, respectively. The configurations of the simulations are identical to the experimental prototype.

Figure 14 shows the logical waveforms of the APC receiver, including v_4, v_5, v_6, and v_s. Regulation circuits are installed on the main circuit. v_4 and v_5 are sent to TLV3502 which generates the control signal. When v_5 is smaller than v_4, v_6 becomes high level, and S_5 is turned on. Otherwise, v_6 becomes low level, and S_5 is turned off. Small oscillations appear in v_6, which should be interferences caused by the switching processes. When I_o or U_o is smaller than the expected value, v_4 decreases which brings about a larger β. Otherwise, v_4 increases, and a smaller β is produced.

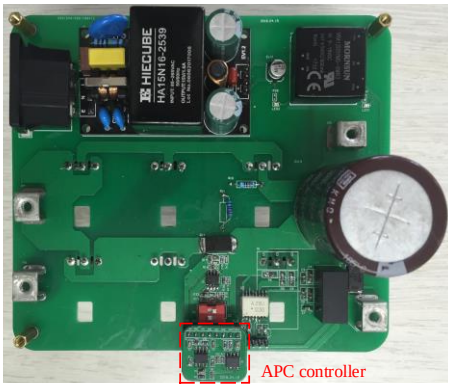

Figure 13. Photograph of APC receiver.

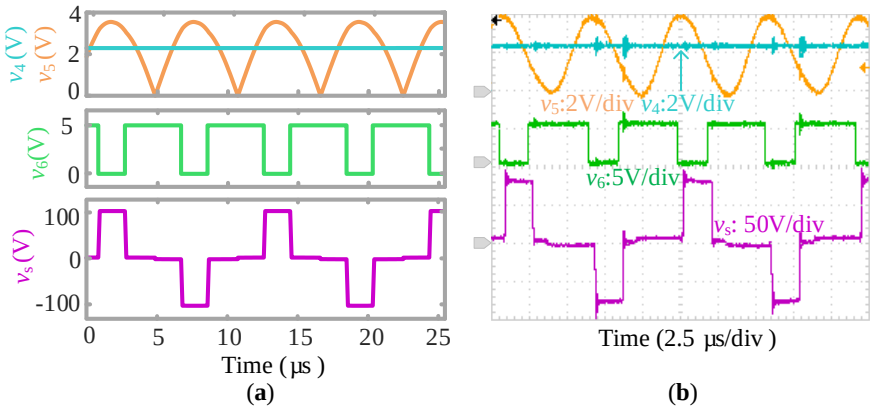

Figure 14. Logical waveforms of APC receiver: (**a**) simulated; and (**b**) experimental. v_4, feedback signal (blue lines); v_5, half-wave signal (yellow lines); v_6, control signal (green lines); v_s, secondary resonant voltage (purple lines).

Figure 15 shows the typical waveforms of the APC receiver. In simulations, v_s is in phase with i_s. However, in experiments, it takes some time for the signal to go through the operational amplifier, the comparator, the DSP, and the driver circuit. This time delay results in v_s lagging i_s by some degrees. High performance devices can reduce this time delay.

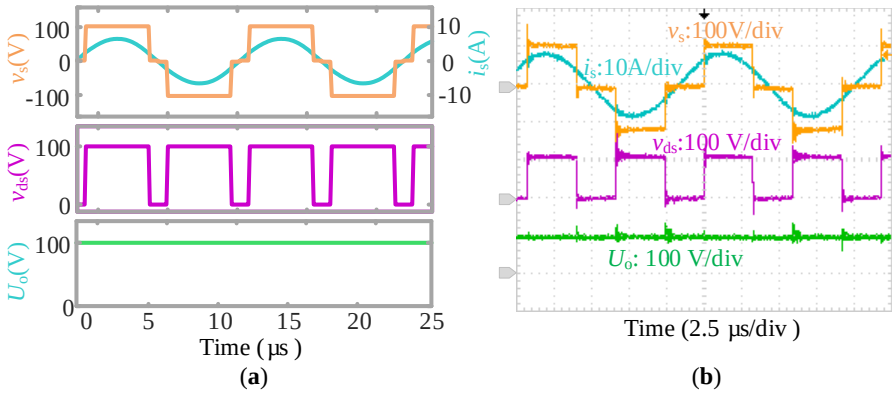

Figure 15. Typical waveforms of APC receiver: (**a**) simulated; and (**b**) experimental. I_s: secondary resonant current (blue lines); v_s, secondary resonant voltage (yellow lines); v_{ds}, voltage across S_5 (purple lines); U_o, output voltage (green lines).

Figure 16a,b shows the simulated and experimental results of the CC power transfer by APC. When R_L is 25 Ω, the simulated and experimental output currents are 1.99 A and 1.98 A, respectively.

The simulated and experimental DC-to-DC efficiencies are 82.5% and 78.2%. When R_L is 50 Ω, the simulated and experimental output currents are 1.99 A and 1.94 A, which correspond to 89.5% and 85.2% DC-to-DC efficiencies, respectively. In the CC mode, I_o maintains at the desired 2 A against load variations.

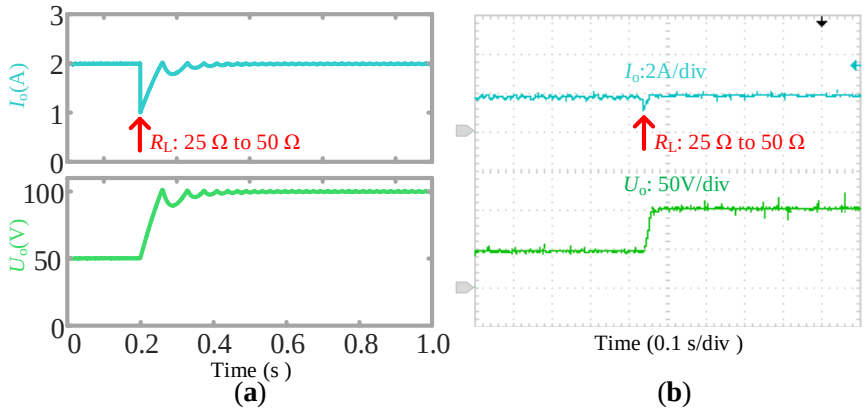

Figure 16. Simulated and experimental CC power transfer results of APC system: (**a**) simulated; and (**b**) experimental. I_o, output current (blue lines); U_o, output voltage (green lines).

Figure 17a,b shows the simulated and experimental results of the CV power transfer by APC. The reference voltage is set at 100 V. When R_L is 25 Ω, the simulated and experimental output voltages are 99.7 V and 103.7 V, whose DC-to-DC efficiencies are 92.2% and 88.9%, respectively. When R_L is 50 Ω, the simulated and experimental output voltages are 99.5 V and 104.6 V, respectively. The overall simulated and experimental efficiencies are 89.4% and 84.7%, respectively. In the CV mode, U_o remains unchanged against load variations.

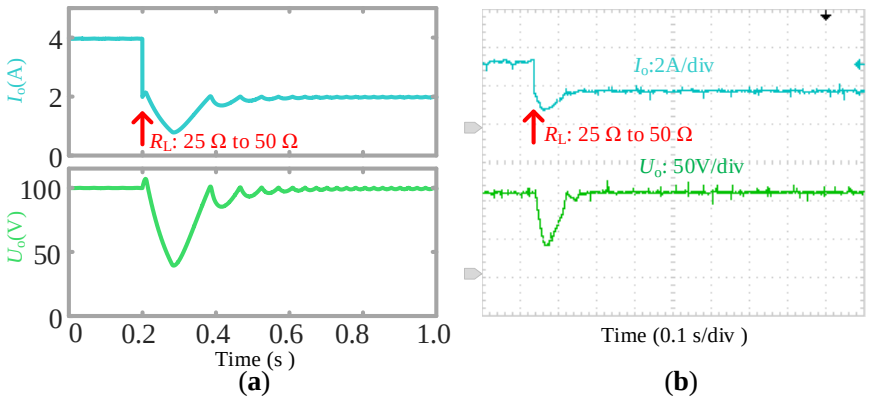

Figure 17. Simulated and experimental CV power transfer results of APC system: (**a**) simulated; and (**b**) experimental. I_o, output current (blue lines); U_o, output voltage (green lines).

Since simulations are closer to an ideal system than experiments, their efficiencies are higher than experimental ones. However, the dynamic and static performance are generally the same, which verifies the feasibility of the APC system.

4.3. Comparisons between Proposed Methods

Figure 18 shows the photograph of the two proposed controllers. The DPC controller is 9.0 cm × 9.0 cm × 2.7 cm, whereas the APC controller is only 2.4 cm × 2.0 cm × 0.3 cm. The analog controller is much smaller than the digital one. The volume, weight, and cost of the analog receiver can be significantly reduced.

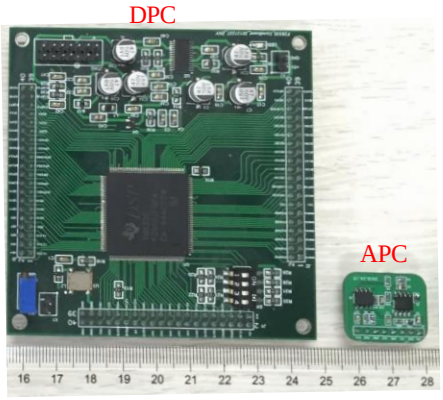

Figure 18. Photograph of two proposed controllers.

Although both the DPC and APC methods can realize the CC and CV power transfer modes, they differ in some aspects. Table 2 compares the differences of the two proposed methods. The DPC system is more complex: it requires a DSP controller, isolated power supplies and driver circuits, current and voltage sensors, and the synchronization circuit. However, the DPC system can eliminate the time delay caused by the regulation circuit and avoid additional power losses of the sampling and divider resistances in the APC receiver. The highest measured experimental efficiency of the APC system is 89.4%, whereas it is 91.4% in the DPC system. Thus, the DPC receiver contributes to a higher performance compared to the APC receiver. Furthermore, it is easier to change the received power through the software code as in the DPC system than changing the regulation resistances as in the APC system, i.e., the DPC system has a greater flexibility than the APC system. Conversely, the APC receiver is simpler since it does not require synchronization algorithms and dedicated programming. In addition, it needs fewer auxiliary devices, i.e., isolated power supplies and expensive sensors are not needed, as well as has a smaller printed circuit board layout. This makes the analog receiver lighter, more cost-effective, and compact.

Table 2. Comparisons between DPC and APC.

Methods	DPC	APC
Complexity	High	Low
Performance	Very High	Good
Flexibility	Very High	Good
Cost	High	Low
Weight	Heavy	Light
Volume	Large	Small

4.4. Comparisons among Different Topologies of WPT Receivers

Comparisons among different WPT receivers are presented in Table 3, and the advantages of the proposed topology and control methods are demonstrated below.

Table 3. Comparisons among different receivers for WPT systems.

Topologies	Capacitors	Inductors	Digital Controllers	Switches	Control Methods	Power Regulation Ability
DC-DC converters [3–8]	2	1	1	1	Duty ratio control	Full-controlled
Full bridge [12–25]	1	0	1	4	Phase control	Full-controlled
Semi-bridgeless [26,27]	1	0	1	2	Phase control	Full-controlled
Reported single-switch receivers [29–33]	1	0	1	1	Duty ratio control	Half-controlled
Proposed receiver	1	0	0 or 1	1	Phase control	Full-controlled

Compared to DC-DC converters used in the WPT systems, the proposed receiver advances in two aspects. Firstly, fewer capacitors and no inductors are required in the proposed receiver. It can reduce the volume and weight of the receiver. Secondly, AC-DC and DC-DC conversions are achieved simultaneously by the proposed receiver. Fewer cascaded circuits, therefore, bring about a higher overall efficiency.

Compared to full bridge and semi-bridgeless topologies, the proposed receiver advances in two aspects: Firstly, the proposed receiver is more cost-effective since the number of SiC MOSFETs and driver circuits used in the proposed receiver have been reduced by 75% as compared to full bridge topology, and 50% as compared to semi-bridgeless topology. In addition, a SiC diode, aiming to reduce high forward voltage, is not needed in the proposed receiver. Therefore, the cost reduction can be significant. Secondly, the proposed receiver has a higher reliability. Dead time is required to avoid short circuit in full bridge applications, whereas the proposed receiver gets rid of short circuit due to the reverse blocking of the diode.

Most reported single-switch receivers are half-controlled, which may fail to achieve the CC and CV power transfer modes. Furthermore, the receivers require a large capacitor to stabilize the output voltage due to the usage of duty ratio control. However, the proposed receiver is full-controlled and has a strong power regulation ability. Owing to the utilization of PC, a small filter capacitor is needed in the proposed receiver.

5. Conclusions

This paper presents a novel single-switch phase controlled active rectifier as receiver for WPT systems. Improved DPC and APC methods are proposed based on the receiver topology to achieve effective CC and CV power transfer modes. The proposed method prevents forward voltage losses in SiC switches and accidental shoot through states with improved switching patterns. The system is easy to implement, has a lower cost, smaller volume, lighter weight, and a higher reliability than conventional phase controlled receivers. Detailed analyses of the operating modes and implementation techniques are presented. Simulated and experimental results of a 400-W WPT system are included which show more than 91% overall efficiency and thereby demonstrate the feasibility of the proposed system.

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