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A New CUK-Based Z-Source Inverter

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Abstract: This paper proposes a new three-switch single-phase Z-source inverter (ZSI) based on a CUK converter, which is named a CUK-based ZSI. This topology has characteristics of buck-boost capability and dual grounding. In addition, the voltage gain of proposed inverter is higher than those of the single-phase quasi-Z-source and semi-Z-source inverters. Aside from that, a simple control method is presented to achieve the linear voltage gain. The operational principle of the proposed topology is described. Finally, a performance evaluation is carried out and the test results verify the effectiveness of the proposed solution.

Keywords: single-phase inverter; CUK converter; Z-source inverter

1. Introduction

In recent years, photovoltaic solar power has attracted more and more attention [1–5]. Because the output of the photovoltaic generation is DC, inverters are necessary for a photovoltaic generation system. However, the demerits of the conventional inverters are that their output AC voltage is lower than the input DC voltage. So, sometimes an additional DC-DC converter is needed before the inverter [6,7], which will increase the volume of the inverter and reduce the reliability of the system.

At the same time, the leakage current is an important problem for transformerless inverters [8]. So, in some types of inverters, a high-frequency transformer is used in a two- or multi-stage configuration. A transformer can provide galvanic isolation, but, at the same time, the inverters' efficiency is decreased because of additional losses caused by the transformer. Therefore, there is a trend toward developing transformerless inverters on purpose to reduce the cost and improve the system efficiency [9–13].

In order to solve the problem of conventional inverters, a lot of single-stage inverters with buck–boost capability were proposed in [14,15]. A new topology of the high-frequency alternating current (HFAC) inverter is presented in [16]. In [17], an AC-side voltage doubling converter is presented. Another interesting topology named UNI-AC (unified non-inverting and inverting AC–AC converter) is proposed in [18]. On the other hand, a Z-source inverter was first proposed in [19], which can achieve a boost function of input DC voltage by its X-shaped impedance network. More researchers have focused on the Z-source inverter because of its boost characteristic without an additional DC-DC converter.

As the Z-source inverter was proposed, different types of Z-source inverters were developed [20,21], and [22] illustrates a new semi quasi-Z-source inverter. Compared with the traditional single-phase ZSI, the topologies have features of lower cost and dual grounding, and they can achieve the same output performance as the traditional full bridge voltage source inverter (VSI). However, these topologies suffer from high voltage stress and need a nonlinear control method, which limits their applications. In order to solve these problems, new three-switch three-state single-phase Z-source inverters are created [23], which can be divided into two kinds of topologies. One is called boost-based ZSI, and the other is called buck-boost-based inverters. The topology named

boost-based ZSI is derived from combining boost converter and semi quasi Z-source inverter, and the topology named buck-boost-based ZSI is derived from combining buck-boost converter with semi quasi-Z-source inverter. Both topologies have the advantages of fewer switches, low voltage stress, and large power density compared to traditional single-phase ZSIs. Moreover, these topologies have simple linear control and the characteristic of dual grounding, which can be used for reducing leakage current. However, buck-boost-based type of TSTS-ZSIs cannot produce reactive power. As we know, Z-source inverters will have different characteristics based on different converters. The CUK converter has the advantages of the input supply current and the output load current both being continuous and the ripple being small, which is beneficial for filtering the input and output. Therefore, a new topology named CUK-based ZSI is presented. The following will present the analysis and performance evaluation.

2. Topologies Classification

2.1. CUK-Based ZSI

Figure 1 shows the proposed CUK-based ZSI. This topology is composed of a CUK converter and a semi Z-source inverter. In order to ensure that the boost function and the Z-source inversion work independently, only two switches can be turned on at the same time. Therefore, the gate signal in a switching period should be divided [23], and the control method is built in MATLAB as shown in Figure 2. In Figure 2, it is used to generate the gating signal, which ensures the proposed topology to achieve the sinusoidal voltage output, and the duty cycle of each switch is calculated by following equations.

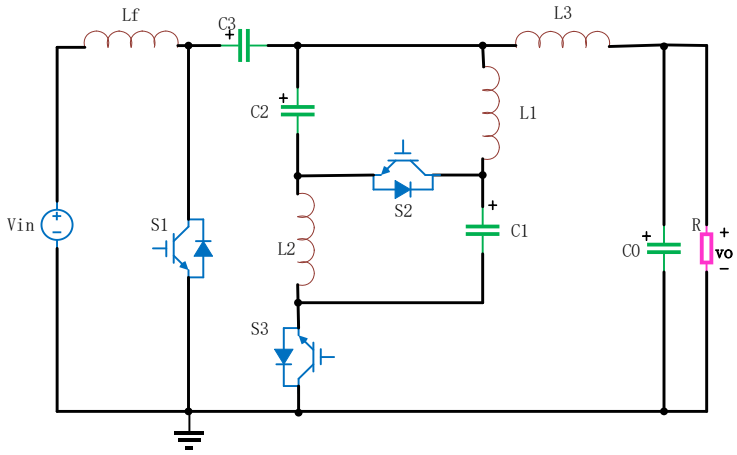


Figure 1. Proposed CUK-based ZSI.

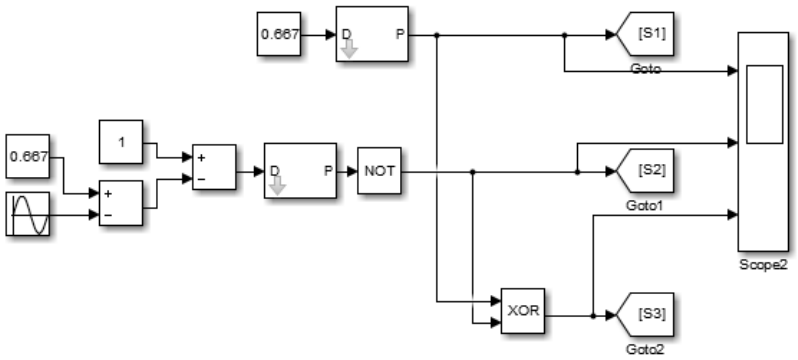


Figure 2. Drive signal built in MATLAB.

The output voltage of the CUK-based TSTS Z-source inverter is defined as follows:

$$v_o = V_o \sin \omega t = AV_{in} \sin \omega t \quad (1)$$

where V_{in} is the input voltage, A or the peak voltage gain is defined as $A = V_o/V_{in}$, and the maximum output voltage is V_o.

Boost part, to set D_1 (Duty cycle of S1) as a constant value and k is the maximum boost ratio is defined as follows [23]:

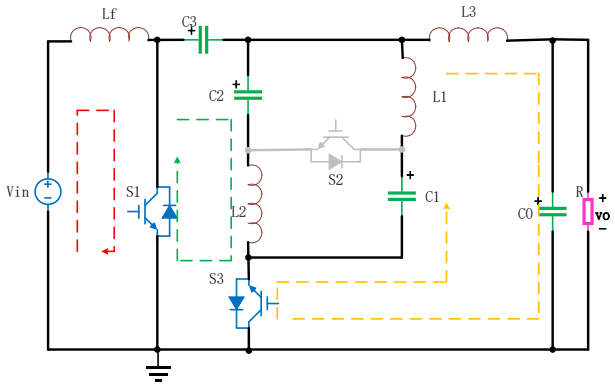
$$k = \frac{D_1}{1 - D_1} \Rightarrow D_1 = \frac{k}{1 + k} \quad (2)$$

In the inversion part, the sinusoidal output voltage v_o is generated by D_2 (duty cycle of S2) as a varied sinusoidal value. D_3 (duty cycle of S3) can be obtained from Figure 3. They are defined as follows [23]:

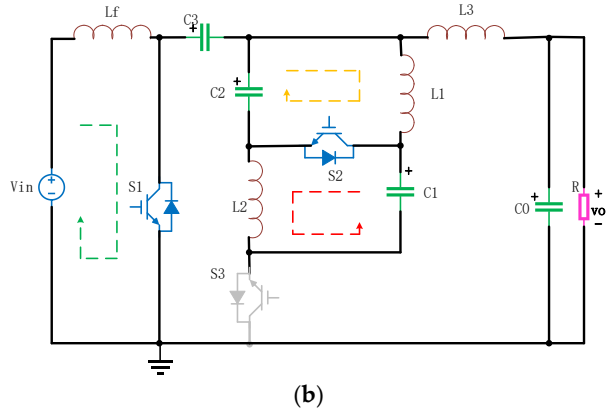
$$D_2 = \frac{k + 2}{2(k + 1)} - \frac{A}{2(k + 1)} \sin \omega t \quad (3)$$

$$D_3 = 2 - D_1 - D_2. \quad (4)$$

So, according to the above circuit and the switching period, the circuit in Figure 1 can be divided into three states in one switching period, whose equivalent circuits are shown in Figure 3a–c.

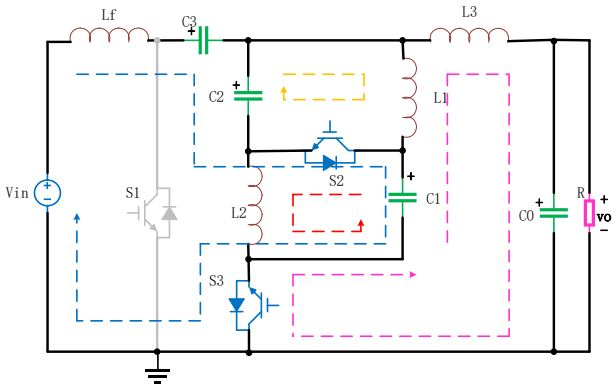


(**a**)



(**b**)

Figure 3. *Cont.*



(**c**)

Figure 3. Equivalent circuits of the CUK-based ZSI in Figure 3 in one switching period (**a**) S1 and S3 are ON, S2 is OFF; (**b**) S1and S2 are ON, S3 is OFF; (**c**) S2 and S3 are ON, S1 is OFF.

2.2. Mode Analysis of Proposed CUK-Based ZSI

Figure 3a–c show the operation modes of proposed CUK-based ZSI. The detailed operational principle is as follows:

- First mode: In this mode, switches S1 and S3 are turned on, whereas switch S2 is turned off, as depicted in Figure 3a. The inductor Lf is magnetized by input voltage V_{in}, and capacitors C1, C2 and C0 are charged; C3 is discharged. The equations of this mode can be expressed as:

$$\begin{cases} V_{C2} + V_{C3} = -V_{L2} \\ -V_{C0} + V_{C1} = V_{L1} + V_{L3} \\ V_{in} = V_{Lf} \end{cases} \tag{5}$$

$$\begin{cases} i_{C2} = i_{C3} = i_{L2} \\ i_{C1} = -i_{L1} = -i_{L3} \end{cases}, \tag{6}$$

  where V_{C0}, V_{C1}, V_{C2} and V_{C3} are the voltage of capacitors C0, C1, C2 and C3. V_{L1} and V_{L2} and V_{L3} are the voltage of inductors L1, L2 and L3, and V_{Lf} is the voltage of input inductor Lf. Similarly, i_{C1}, i_{C2} and i_{C3} are the current of capacitors C1, C2 and C3, and i_{L1}, i_{L2} and i_{L3} are the current of inductors L1, L2 and L3.
- Second mode: In this mode, switches S1 and S2 are turned on, whereas switch S3 is turned off, as depicted in Figure 3b. The inductor Lf is magnetized by input voltage V_{in}, and capacitors C1, C2 and C0 are discharged; C3 is charged. The equations of this mode can be expressed as:

$$\begin{cases} V_{C2} = V_{L1} \\ V_{C1} = V_{L2} \\ -V_{C3} - V_{C0} = V_{L3} \\ V_{in} = V_{Lf} \end{cases} \tag{7}$$

$$\begin{cases} i_{C3} = i_{L3} \\ i_{C2} = -i_{L1} \\ i_{C1} = -i_{L2} \end{cases}. \tag{8}$$

- Third mode: In this mode, switches S2 and S3 are turned on, whereas switch S1 is turned off, as depicted in Figure 3c. The capacitors C1, C2 and C0 are charged; C3 is discharged.

$$\begin{cases} V_{in} - (V_{C3} + V_{C2} + V_{C1}) = V_{Lf} \\ -V_{C2} = V_{L1} \\ -V_{C1} = V_{L2} \\ V_{C2} + V_{C1} - V_{C0} = V_{L3} \end{cases} \tag{9}$$

$$\begin{cases} i_{C1} = -i_{L1} = -i_{L3} = -i_{L2} \\ i_{C2} = -i_{L1} \\ i_{C3} = i_{Lf} \end{cases}, \tag{10}$$

where i_{Lf} is the current of inductor Lf.

2.3. Control of Proposed CUK-Based ZSI

The control block diagrams of the proposed inverters are shown in Figure 4a–c. According to Figure 4a, we input a constant value K, then compare with the carrier signal to produce the switch signal of S1, which is used to boost the voltage. According to Figure 4b, it is different from (a), because it inputs a sinusoidal value, and then, compared with a carrier signal, after reversing, the switch signal of S2 is obtained, which is used to generate output sinusoidal voltage. At the same time, the switch signal of S3 is decided by the switch signal of S1 and the switch signal of S2, and the switch signal of S1 and the switch signal of S2 pass through the XOR gate to get the switch signal of S3, as shown in Figure 4c, where the XOR gate is a digital logic gate that gives a true (1 or HIGH) output when the number of true inputs is odd.

XOR is a logic manipiulator.

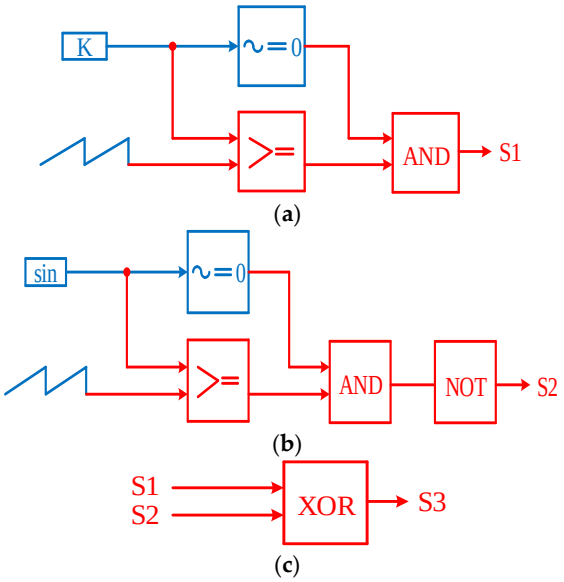


Figure 4. Control block diagram of the proposed inverter (**a**) the switch signal of S1; (**b**) the switch signal of S2; (**c**) the switch signal of S3.

3. Device Stress Calculation and Passive Component Design

3.1. Device Stress Calculation

Based on Figure 3 and Equations (5)–(10), the current of switches S1, S2 and S3 and the voltage of switches S1, S2 and S3 can be determined. Consequently, the following rate equations express the voltage and the current stresses of switches S1, S2 and S3.

$$V_{S\text{-}max} = (1 + k)V_{in} \tag{11}$$

$$I_{S\text{-}max} = (A + 1)I_o, \tag{12}$$

where I_o is the output current. $V_{S\text{-}max}$ and $I_{S\text{-}max}$ are the maximum voltage stresses and current stresses, respectively. The output current is considered to be a sinusoidal waveform. V_o is expressed in (1) and I_o similarly can be written as:

$$I_o = I_M \sin \omega t \tag{13}$$

where I_M denotes the output peak current.

3.2. Passive Component Design

Supposing that inductor L1 and inductor L2 are equal, and capacitor C1 and capacitor C2 are equal, according to the volt-second balance principle, it is easy to get the following equations:

$$\begin{cases} V_{C1} = V_{C2} = \frac{1-D_2}{D_2} V_{in} \\ V_{C3} = \frac{1}{1-D_1} V_{in} \end{cases} \tag{14}$$

$$\begin{cases} i_{L1} = i_{L2} = \frac{1-D_2}{D_2} I_o \\ i_{L3} = I_o \\ i_{Lf} = \frac{-D_1}{1-D_1} I_o \end{cases} \tag{15}$$

The inductor L and input inductor Lf, capacitors C and output capacitor can be calculated by the following equations. In order to calculate the current ripple of inductor Lf, the equation in the first mode is considered. Using this equation and knowing that $V_L = L(di_L/d_t)$, the current ripple of inductor Lf can be extracted as:

$$\Delta i_{L_f} = \frac{V_{in} D T_s}{Lf} \tag{16}$$

where Δi_{L_f} is the current ripple of inductor Lf and T_s denotes the switching period.

Therefore, the inductor Lf can be calculated by the following equation:

$$Lf = \frac{V_{in} D_1 T_s}{\Delta i_{Lf}}. \tag{17}$$

So, the current ripple of inductors L can be expressed by the same method, and the inductors L can be calculated by the following equations:

$$L1 = L2 = \frac{V_{in}(1 - D_2)T_s}{\Delta i_{L1}} \tag{18}$$

$$L3 = \frac{(V_{C0} V_{C3}) D_1 T_s}{\Delta i_{L3}} = \frac{V_{in} T_s}{\Delta i_{L3}}, \tag{19}$$

where Δi_{L1} and Δi_{L3} are the current ripple of inductor L1 and L3, respectively.

Similarly, by employing the equations in the first mode and knowing that $i_c = C(dV_c/d_t)$, the capacitors can be calculated by the following equations:

$$C1 = C2 = \frac{i_{L1} D_2 T_s}{\Delta V_{C2}} \tag{20}$$

$$C3 = \frac{i_{L3} D_1 T_s}{\Delta V_{C3}} \tag{21}$$

$$C0 = \frac{\Delta i_{L3} T_s}{2\Delta V_{C0}}, \tag{22}$$

where ΔV_{C0}, ΔV_{C2} and ΔV_{C3} are the voltage ripple of capacitors C0, C2 and C3, respectively.

4. Simulation and Comparison

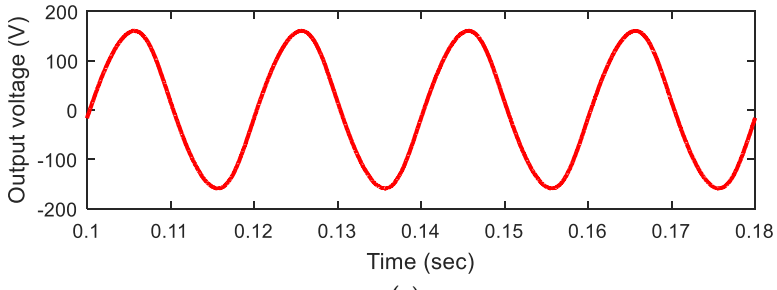
4.1. Simulation Conditions and Results

In order to test the performances of the proposed CUK-based ZSI, a series of simulations have been done in Matlab/Simulink®2015a. The simulation condition and parameters are shown in Table 1. The designs use an input voltage of 90 V for generating the output voltage at 110 V and 50 Hz. The switching frequency is considered to be 20 kHz. In the design procedure, the inductors are calculated using Equations (17)–(19) and supposing $\Delta i_L = 20\% I_L$ for all inductors. Similarly, the capacitors are designed according to Equations (20)–(22) with $\Delta V_C = 7\% V_C$, where ΔV_C are the voltage ripple of capacitors. What is more, IGBT is selected for each switch.

Table 1. Simulation parameters for current topology.

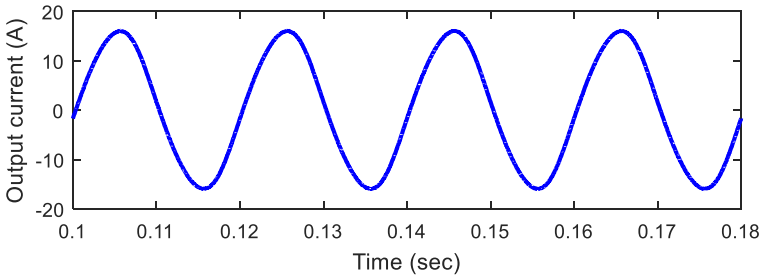
Parameters	Proposed Topologies
Input voltage, V_{in}	90 V
Output voltage (rms), V_o	110 V
Switching frequency, f_s	20 kHz
Output voltage gain, A	1.75
Maximum boost ratio, k	2
Inductance Lf	0.48 mH
Z-impedance inductance, L1 and L2	1 mH
Z-impedance capacitance, C1 and C2	46.3 μF
Capacitance C3	27.4 μF
Inductance L3	1.45 mH
Output capacitance, C0	10 μF

Using the parameters from Table 1, the simulations have been done. In order to test the reliability of the proposed topologies, simulations for proposed CUK-based ZSI are carried out. Firstly, the input voltage is set 90 V and load is 10 Ω. Figure 5a–c illustrate the load voltage, load voltage and FFT analysis, respectively. Figure 6a–c shows the voltage waveforms of the switches S1, S2 and S3. At the same time, the voltage waveform of the capacitors C1, C2, C3, and the output capacitor C0 are shown in Figure 7a–d. Lastly, the simulation of input voltage changes suddenly during the simulation is carried out, and the output results are shown in Figure 8a,b.



(**a**)

Figure 5. *Cont.*



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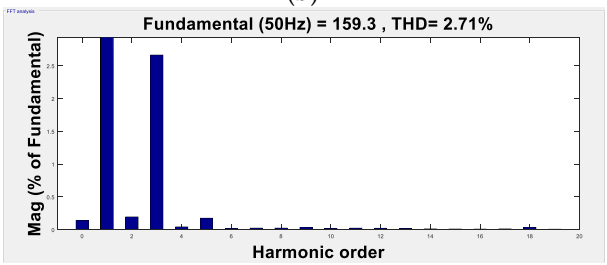
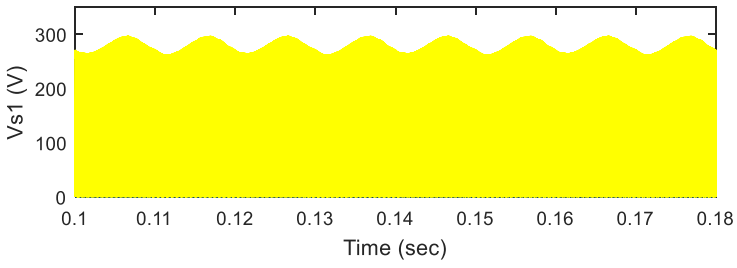


(**c**)

Figure 5. Input voltage at 90 V and load at 10 Ω for CUK-based ZSI (**a**) load voltage; (**b**) load current; (**c**) FFT analysis.



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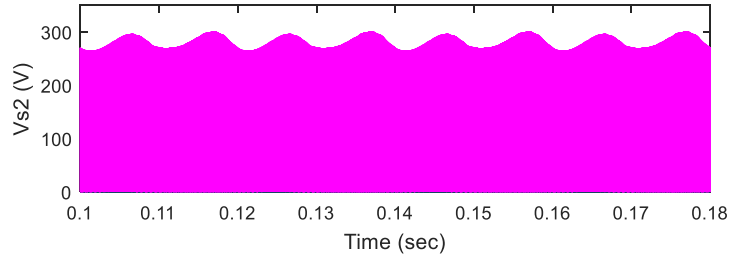

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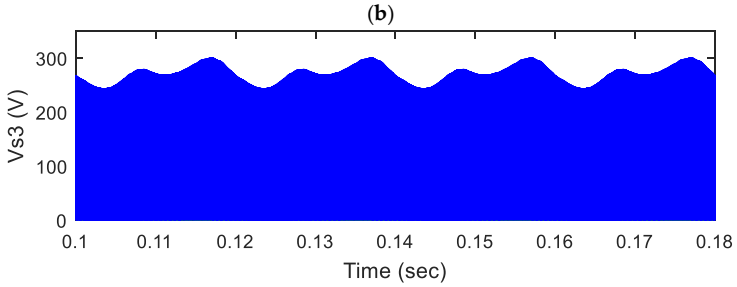


(**c**)

Figure 6. Input voltage at 90 V and load at 10 Ω for CUK-based ZSI. Voltage wave of (**a**) Switch S1; (**b**) Switch S2; (**c**) Switch S3.

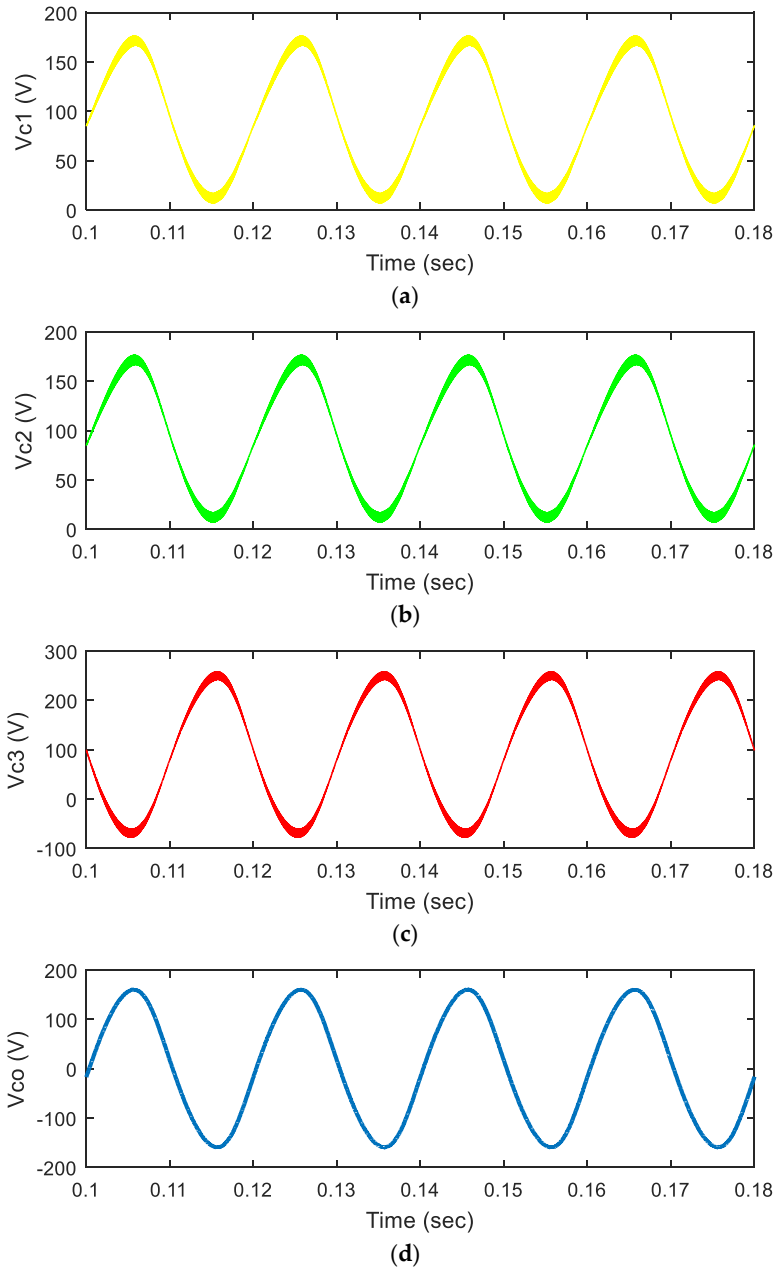


Figure 7. Input voltage at 90 V and load at 10 Ω for CUK-based ZSI. Voltage wave of (**a**) capacitor C1; (**b**) capacitor C2; (**c**) capacitor C3; (**d**) capacitor C0.

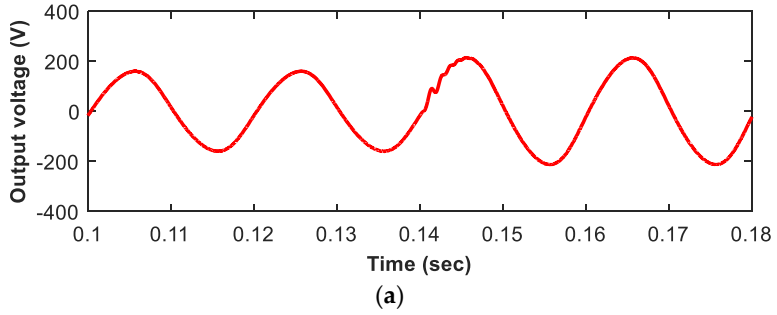
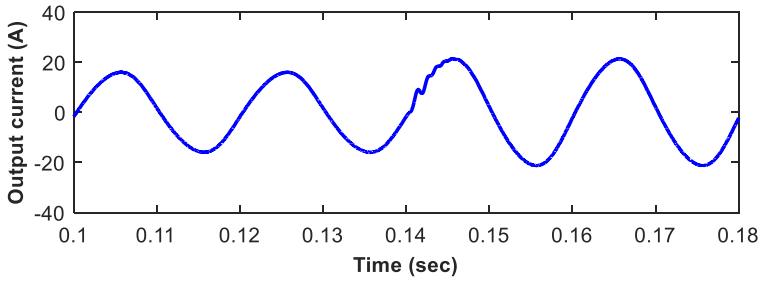


Figure 8. *Cont*.



(**b**)

Figure 8. Input voltage changes suddenly (from 90 V to 120 V) and load at 10 Ω for CUK-based ZSI. (**a**) Load voltage; (**b**) load current.

From the above simulation results, it can be observed when the input voltage is 90 V and load is 10 Ω, the output voltage and current satisfy the requirements, and the THD = 2.71%, which is well below 5%. On the other hand, the voltage stresses of switches are about 300 V. According to Figure 8, when the input voltage changes suddenly, although the waveform fluctuates in the course of the change, it tends to stabilize quickly. In summary, the proposed inverter can operate under different conditions with good performance.

4.2. Comparison

Table 2 shows the comparison among the proposed inverter and Semi-ZS-Based [24], Semi-ZSI [22], boost-based TSTS-ZSI [23] and buck-boost-based TSTS-ZSI [23]. These topologies are all based on Z-source inverters, and an extra boost stage is not needed anymore. On the other hand, they all have the characteristics of the common input and output terminals, which means these topologies can eliminate the leakage current for PV systems. Meanwhile, the voltage gain of the proposed topology is more than 1. The major feature compared with boost-based TSTS-ZSI and buck-boost-based TSTS-ZSI is that the proposed topology is based on a CUK converter. So it has the same advantages as a CUK converter.

Table 2. Comparative summary of the proposed inverter with other Z-source inverters.

Z-Source Inverter Topologies	Total no. Component			Complexness	Power Density	Cost	Voltage Gain	Switches' Voltage Stress	THD %
	S	L	C						
Semi-ZS-Based in [24]	2	3	3	simple	high	low	<1	/	/
Semi-ZSI in [22]	2	2	3	simple	high	low	<1	$(1+\frac{2}{A})V_o$	/
Boost-based TSTS-ZSI in [23]	3	3	3	simple	high	low	>1	$(1+\frac{2}{A})V_o$	2.82
Buck-boost-based TSTS-ZSI in [23]	3	3	4	simple	High	low	>1	$(1+\frac{1}{A})V_o$	3.15
Proposed	3	4	4	simple	High	low	>1	$(1+\frac{1}{A})V_o$	2.71

In Table 2, the THD is valid under the condition of input 90 V and full load. What is more, all of them have a simple topology; although the proposed inverter has one more inductor than buck-boost-based TSTS-ZSI, it still has good performance. So all of these inverters have high power density and low cost.

5. Experimental Verification

In order to further verify the effectiveness of the proposed inverter, the corresponding experiment is carried out. Input 90 V voltage and work under 30 Ω resistive load for the proposed inverter. According to Equations (11) and (12), the K40T1202 IGBT is used for each switch in the experiment.

Firstly, the proposed inverter is tested under 90V input voltage. Figure 9 shows the output voltage and current waveforms, which are in agreement with Figure 5. The voltage waveforms of S1, S2, and S3 are depicted in Figure 10a–c, which are in agreement with the simulation results in Figure 6. The capacitor voltages are shown in Figure 11a,b, and these waveforms match with Figure 7.

Another experiment is carried out when the load changes suddenly during the experiment. The output voltage and current are displayed in Figure 12.

It can be seen from Figure 12 that the proposed inverter still works well when the load changes suddenly. In conclusion, from the above experimental results, it can be observed that they are in good agreement with the theoretical analysis and the simulation results, which again confirms the effectiveness of the proposed inverter.

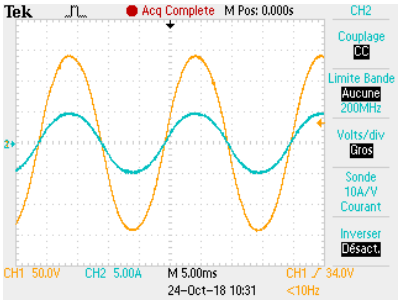


Figure 9. Input voltage at 90 V and load at 30 Ω. Experimental waveforms of v_o (CH1: Time (5 ms/div), v_o (50 V/div)) and I_o (CH2: Time (5 ms/div), I_o (5 A/div)).

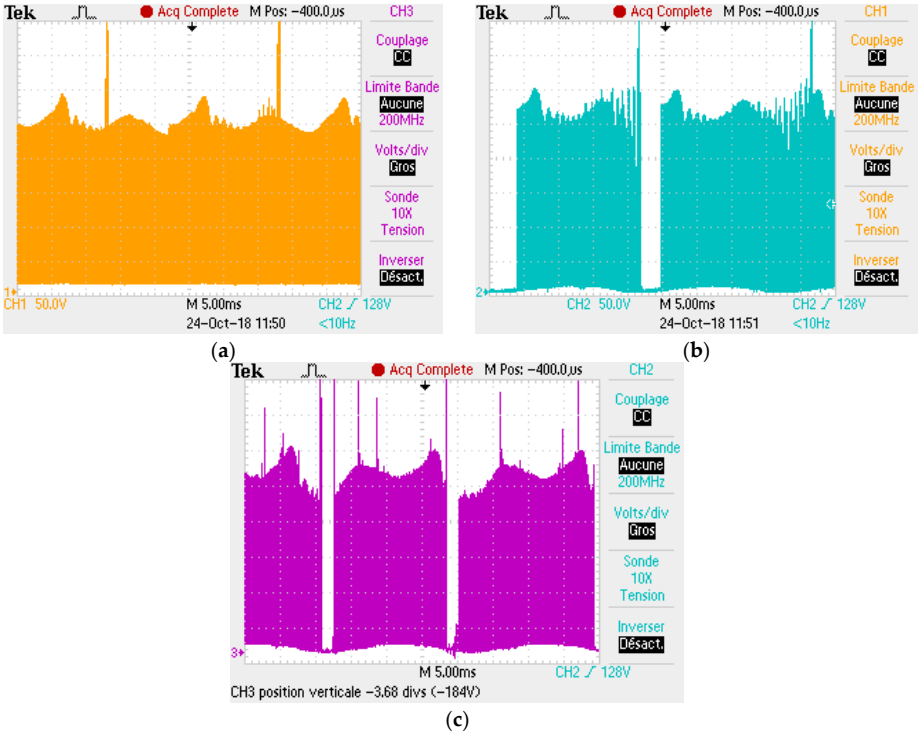
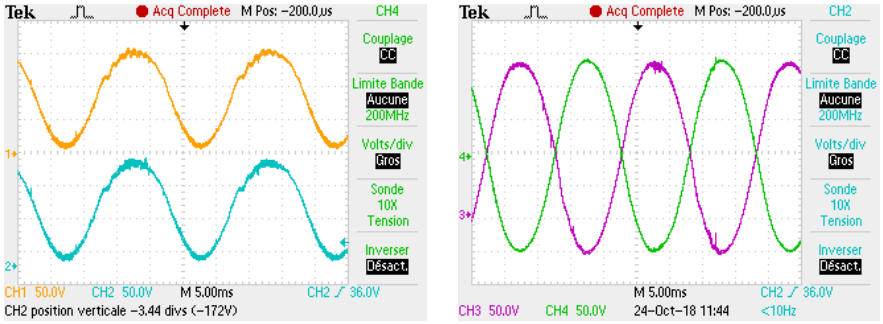


Figure 10. Input voltage at 90 V and load at 30 Ω. Experimental voltage waveforms of (**a**) switch S1; (**b**) switch S2; (**c**) switch S3 (Time (5 ms/div); V_S (50 V/div)).



(**a**) (**b**)

Figure 11. Input voltage at 90 V and load at 30 Ω. Experimental waveforms of (**a**) V_{c1} (CH1: Time (5 ms/div), V_{c1} (50 V/div)) and V_{c2} (CH2: Time (5 ms/div), V_{c2} (50 V/div)); (**b**) V_{c3} (CH3: Time (5 ms/div), V_{c3} (50 V/div)) and V_{c0} (CH4: Time (5 ms/div), V_{c0} (50 V/div)).

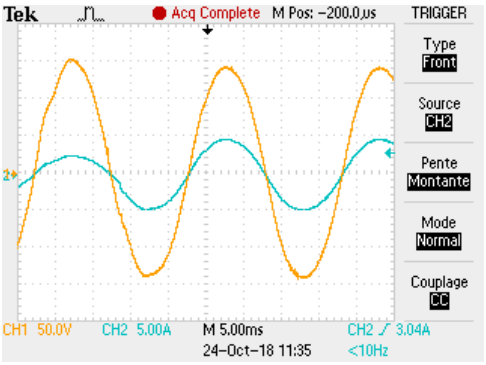


Figure 12. Input voltage at 90 V and load changes suddenly (from 60 Ω to 30 Ω). Experimental waveforms of v_o (CH1: Time (5 ms/div), v_o (50 V/div)) and I_o (CH2: Time (5 ms/div), I_o (5 A/div)).

6. Conclusions

The main contribution of this paper is to present a new ZSI topology, named CUK-based ZSI. Compared with traditional ZSI, this topology has fewer switches but can achieve high voltage gain. Moreover, this topology has the feature of a common input-output terminal, which is helpful for reducing leakage current. According to the concrete results from simulations and experiments, the proposed inverter works well. Figures 5 and 9 indicate that the proposed topology has a high voltage gain and a low THD, which is beneficial for many applications such as PV systems. However, the proposed inverter topology also has some drawbacks. Because the proposed topology has more inductors and capacitors than conventional single-phase Z-source inverters, there will be more system losses. Future research should focus on using the coupled-inductor technique and SiC devices to optimize the power density.

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Abbreviations

The following abbreviations are used in this manuscript:

Acronims	
ZSI	Z-source inverter
VSI	Voltage source inverter
TSTS	Three-switch three-state
FFT	Fast Fourier transform
THD	Total harmonic distortion
Nomenclature	
A	Peak voltage gain
k	Maximum boost radio
D_1, D_2, D_3	Duty cycle functions
ω	Output voltage angular frequency
S1, S2, S3	Semiconductor switches
V_{in}	DC input voltage
V_{Li}	Voltage of inductors
V_{Ci}	Voltage of capacitors
V_{si}	Voltage of switches
i_{Li}	Current of inductors
i_{Ci}	Current of capacitors
I_o	Output peak current
Δi_{Li}	Current ripple of inductors
ΔV_{Ci}	Voltage ripple of capacitors
T_s	Switching period
f_s	Switching frequency

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