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AlGaN/GaN MIS-HEMT with PECVD SiN_x, SiON, SiO_2 as Gate Dielectric and Passivation Layer

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Abstract: Three different insulator layers SiN_x, SiON, and SiO_2 were used as a gate dielectric and passivation layer in AlGaN/GaN metal–insulator–semiconductor high-electron-mobility transistors (MIS-HEMT). The SiN_x, SiON, and SiO_2 were deposited by a plasma-enhanced chemical vapor deposition (PECVD) system. Great differences in the gate leakage current, breakdown voltage, interface traps, and current collapse were observed. The SiON MIS-HEMT exhibited the highest breakdown voltage and I_{on}/I_{off} ratio. The SiN_x MIS-HEMT performed well in current collapse but exhibited the highest gate leakage current density. The SiO_2 MIS-HEMT possessed the lowest gate leakage current density but suffered from the early breakdown of the metal–insulator–semiconductor (MIS) diode. As for interface traps, the SiN_x MIS-HEMT has the largest shallow trap density and the lowest deep trap density. The SiO_2 MIS-HEMT has the largest deep trap density. The factors causing current collapse were confirmed by Photoluminescence (PL) spectra. Based on the direct current (DC) characteristics, SiN_x and SiON both have advantages and disadvantages.

Keywords: gallium nitride; MISHEMT; dielectric layer; interface traps; current collapse; PECVD

1. Introduction

In the past decades, the wide bandgap semiconductor material, gallium nitride (GaN), attracted great attention due to its wide bandgap, high breakdown electric field, and excellent thermal properties [1]. Gate leakage current and current collapse are the main issues that limit the performance of AlGaN/GaN high-electron-mobility transistors (HEMTs). To overcome these problems, different dielectric materials have been proposed for the fabrication of metal-insulator-semiconductor (MIS) HEMTs, such as SiO_2 [2–6], SiN_x [7–11], SiONe [12–14], ZrO_2 [15], Al_2O_3 [16–18], and HfO_2 [19], etc. Each material has advantages and disadvantages. Some groups studied stack dielectric layers like SiN_x/Al_2O_3 [20] and SiN_x/SiO_2 [21] to improve leakage current and stability. The Al_2O_3 and HfO_2 gate dielectric layer deposited by atomic layer deposition (ALD) has shown advantages in reducing gate leakage and eliminating current collapse [22,23]. However, Al_2O_3 and HfO_2 are not suitable as passivation layers due to the low deposition rate of ALD. The plasma-enhanced chemical vapor deposition (PECVD) is one of the key sectors in conventional GaN-based light emitting diode (LED) production lines and complementary metal–oxide–semiconductor (CMOS) production lines. Thus, lots of work has been done on PECVD-deposited silicon nitride, silicon oxide, and silicon oxynitride. Compared to SiN_x, SiO_2 has a larger conduction band offset with GaN, which is related to leakage current. However, SiN_x has a relatively higher dielectric constant (~7), which contributes to better

gate control of two dimensional electron gas (2DEG). As a trade-off, SiON can be modulated to retain some advantages from both SiN_x and SiO_2 and has been proved to be a good candidate for a gate dielectric [12]. Considering the passivation effect, these dielectric layers can reduce the surface states, modulate the strain, and improve the reliability [24–26]. Although some comparisons have been made on the above materials [13,27,28], some published data are often controversial and the overall result is still not sufficiently clear. This shows that many questions are still unanswered and a better understanding of the passivation effect on the device performance is required.

In this work, we have made comprehensive comparisons between MIS-HEMTs with PECVD-deposited SiN_x, SiON, and SiO_2 as a gate dielectric and passivation layer. The differences in direct current (DC) static characteristics and current collapse were investigated. The interface traps were studied by Capacitance versus Voltage (C-V) measurements and a pulse mode drain current versus gate-to-source voltage (Id-V_{gs}) test. The Photoluminescence (PL) spectra test was also applied to confirm the passivation effectiveness.

2. Materials and Methods

The AlGaN/GaN epilayer used in this work is grown on Si (111) substrate using metal–organic chemical vapor deposition (MOCVD). The epitaxial structure consists of a 3.5 μm GaN buffer layer, a 300 nm GaN channel layer, a 1 nm AlN interlayer, a 22 nm $Al_{0.23}Ga_{0.77}N$ barrier layer, and a 3 nm GaN cap layer. A 2DEG mobility of 1831 $cm^2/V{\cdot}s$ and a sheet carrier concentration of 8.3×10^{12} cm^{-2} are measured by Hall effect measurement.

The device fabrication of MIS-HEMT started with the cleaning of the epitaxial wafer with a standard solvent. Then, devices were isolated using BCl_3 and Cl_2 etching in an Inductively Coupled Plasma (ICP) system. Prior to the deposition of ohmic metal, surface treatment was performed by immersing in HCL for 60 s. The Ti/Al/Ni/Au metal stack was then deposited by E-beam evaporation. Rapid temperature annealing at 850 °C for 1 min in a N_2 environment was then performed to form ohmic contact. The contact resistance was 2.11 Ω·mm and the specific contact resistance was 1.75×10^{-4} Ω cm^2, as extracted by a circular transmission line model. After that, SiN_x, SiON, and SiO_2 dielectric layers with a thickness of 20 nm were deposited separately on the surfaces of different AlGaN/GaN samples using PECVD. Additionally, a Si dummy wafer and an AlGaN/GaN dummy wafer were loaded, together with the sample, in each deposition process. The dielectric/AlGaN/GaN samples were used for PL spectra measurement. The thickness and refractive index of deposited thin films were measured for the dummy wafer using an ellipsometer. The deposition properties of SiN_x, SiON, and SiO_2 are listed in Table 1.

Table 1. Deposition properties of SiN_x, SiON, and SiO_2.

Sample	Pressure (millitorr)	RF Power(W)	SiH_4 [1] (sccm[2])	N_2O (sccm)	NH_3 (sccm)	TEM (°C)	Refractive Index [3]
SiN_x	650	50	150	0	25	300	1.82
SiON	500	75	25	20	40	300	1.56
SiO_2	650	50	100	1000	0	300	1.46

[1] SiH_4 (5%)/N_2; [2] Standard Cubic Centimeter per Minute; [3] Refractive Index at the wavelength of 632.8 nm.

The dielectric layers above drain and source electrodes were then removed by ICP. Finally, all samples were carried out using the same gate contact process. A Ni/Au (50/150 nm) gate metal was deposited by E-Beam evaporation. All samples have the same epitaxial structure and fabrication process, except for the type of dielectric layers. The MIS-HEMTs with different dielectric layers are labeled as SiN_x MIS-HEMT, SiON MIS-HEMT, and SiO_2 MIS-HEMT, respectively. Figure 1 shows the schematic cross-sectional view of MIS-HEMT. The gate length L_G, gate width W_G, gate to drain distance L_{GD}, and gate to source distance L_{GS} are 3, 150, 20, and 10 μm, respectively.

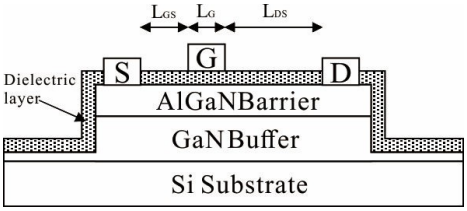

Figure 1. Metal–insulator–semiconductor high-electron-mobility transistors (MIS-HEMT) structure cross-section view.

3. Results and Discussion

Table 2 shows some selected properties of MIS-HEMTs. The typical DC output characteristics of SiN_x MIS-HEMT, SiON MIS-HEMT, and SiO_2 MIS-HEMT are shown in Figure 2a–c. The drain current densities at drain-to-source voltage Vds = 20 V and gate-to-source voltage V_{gs} = 8 V are 623 mA/mm, 590 mA/mm, and 620 mA/mm, respectively, for SiN_x MIS-HEMT, SiON MIS-HEMT, and SiO_2 MIS-HEMT. The specific on-resistance extracted at Vds = 3 V is 9.89 Ω·mm, 11.6 Ω·mm, and 11.4 Ω·mm, respectively. These output characteristics show that the SiN_x MIS-HEMT has the highest maximum drain current and lowest static on-resistance. Figure 2d shows the off-state breakdown characteristics measured at V_{gs} = −18 V. SiON MIS-HEMT exhibits a higher breakdown voltage compared with the other two samples. SiN_x performs slightly better in improving the saturated drain current of MIS-HEMT, and SiON can withstand a higher electric field strength.

Table 2. Selected properties of SiN_x, SiON, and SiO_2 MIS-HEMT.

Sample	I_{dmax} (mA/mm)	$g_m$max (mS/mm)	V_{th}	Gate Leakage [1] (mA/mm)	Off-State Breakdown Voltage (V)	%I [2]	Dynamic Ron/Static Ron [3]
SiN_x	623	62.7	−16.7	4.46 E-4	364	11.6%	1.18
SiON	590	55.3	−11.7	3.86 E-5	428	71.26%	5.64
SiO_2	620	81.3	−9.9	3.12 E-5	284	84.14%	24.5

[1] Gate leakage current density at two-terminal reverse voltage = −20 V; [2] Reduction of drain current and increase of Ron due to current collapse at off-state V_{gs} = −18 V, Vdstress = 50 V for 10 s; [3] Dynamic Ron at off-state Vds stress = 50 V and static Ron without stress.

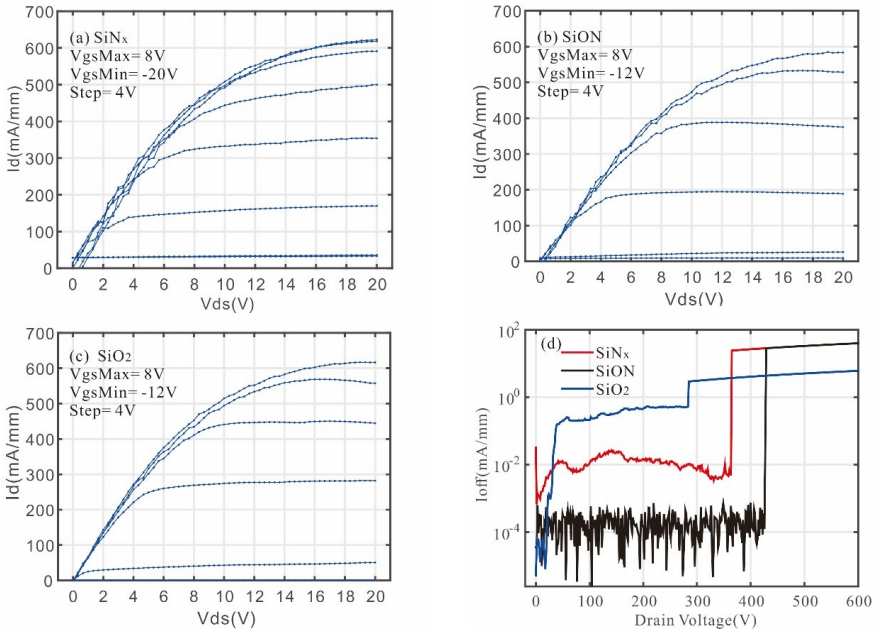

Figure 2. Output characteristic of (**a**) SiN_x MIS-HEMT, (**b**)SiON MIS-HEMT, and (**c**) SiO_2 MIS-HEMT. (**d**) off-state breakdown characteristic of the three samples, measured at V_{gs} = −18 V.

Figure 3d plots the gate-to-source two-terminal leakage current curve when V_{gs} changes from 5 to −40 V with drain electrode dangling. The gate-to-source leakage current (Igs) density of SiN_x MIS-HEMT is 4.46 × 10^{-4} mA/mm at V_{gs} = 20 V, which is 1 order larger than that of SiON or SiO_2 MIS-HEMT. This can be attributed to the lower conduction band offset of SiN_x from GaN [12]. As for SiO_2 MIS-HEMT, there is a rapid increase of leakage current when the gate voltage bias is lower than −35 V. This phenomenon means that the SiO_2 dielectric layers are more easily damaged than SiN_x and SiON.

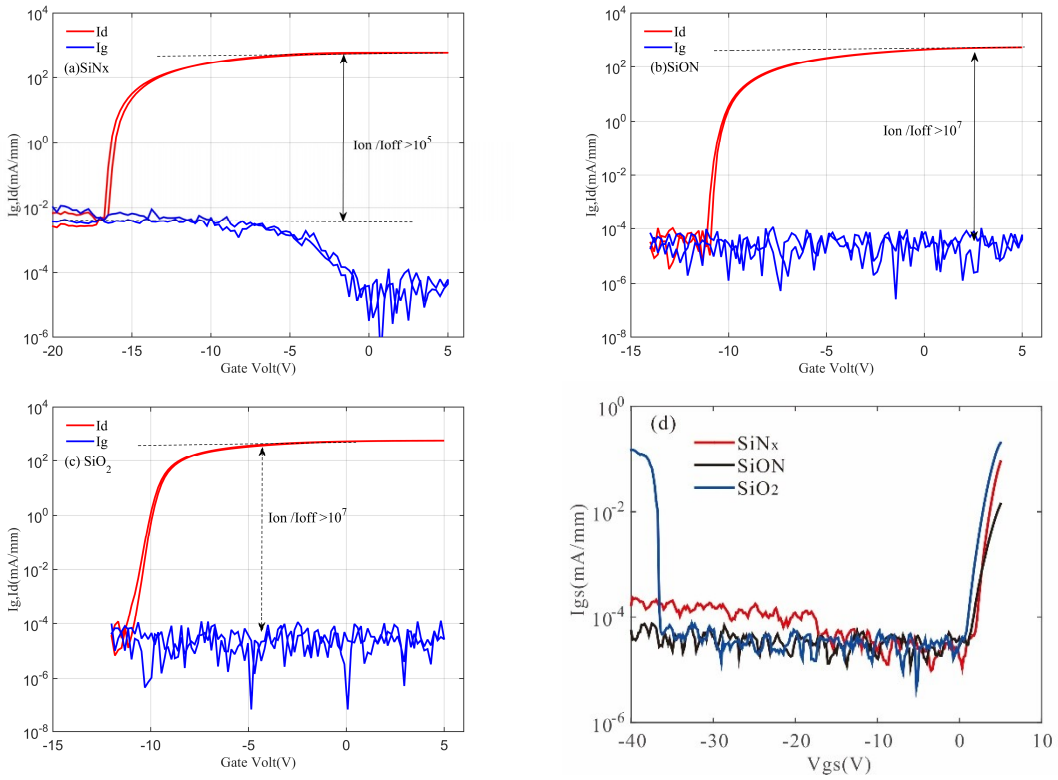

Figure 3. Transfer characteristic of (**a**) SiN_x MIS-HEMT, (**b**) SiON MIS-HEMT, and (**c**) SiO_2 MIS-HEMT, and (**d**) gate leakage current curve measured at two terminals for the three samples.

The transfer curves of the three samples are shown in Figure 3a–c. The drain voltage was fixed at 15 V, and the minimum gate voltage was −20 V, −14 V, and −12 V, respectively, for SiN_x MIS-HEMT, SiON MIS-HEMT, and SiO_2 MIS-HEMT. The drain current, Id, is almost equal to the gate current, Ig, in the off-state for all samples. This result reveals that the off-state drain leakage current is mainly from the gate electrode. As a result, the comparison of the off-state drain currents of these two samples agrees with the two-terminal gate leakage current. A high I_{on}/I_{off} ratio > 10^7 was observed on SiON MIS-HEMT and SiO_2 MIS-HEMT, which is two orders larger than SiN_x MIS-HEMT.

To investigate the interface condition of the three samples, a forward and backward C-V measurement with a frequency of 1 MHz was applied. As shown in Figure 4, each C-V curve has two rising slopes. The 1st slope represents the completed depletion of 2DEG and the 2nd slope indicates the electron transfer from AlGaN/GaN to dielectric/AlGaN interface [29,30]. A relatively low voltage corresponding to the 1st slope is observed in the SiN_x MIS structure. This may be attributed to the fixed charge in the dielectric/AlGaN interface. Some researches show that a large amount of fixed charges exist in the dielectric layer and dielectric/AlGaN interface [31–35], differing from interface traps analyzed in the work, these kinds of fixed charges are not modulated by the gate voltage and do not lead to voltage hysteresis. Therefore, they have a negligible effect on the CV hysteresis measurement. However, the positive fixed charge would cause a negative voltage shift of the flat band voltage (V_{FB}), and thus lead to a low threshold voltage, V_{th} [33]. More investigation concerning fixed

charges is needed in the future. In the CV curve, the backward hysteresis and threshold voltage shifts are always attributed to interface traps. The inset of Figure 4 shows that there is little voltage shift on the 2nd slope while obvious hysteresis occurred on the 1st slope of the SiON and SiO_2 MIS sample. This phenomenon occurs because larger number of deep traps with long emission time constants appear in the SiON and SiO_2 MIS structure. We also used dielectric capacitance in series with the barrier capacitance model to extract the Cox of the three samples [36]. The Cox is 297.86, 277.82, and 364.82 nF/cm^{-2} for SiN_x, SiON, and SiO_2 MIS-HEMT, respectively. C-V measurement provides a rough comparison of the three structures but its precision is limited by the sweeping rates. The pulse-mode Id-V_{gs} measurement was employed for a more accurate extraction of interface states.

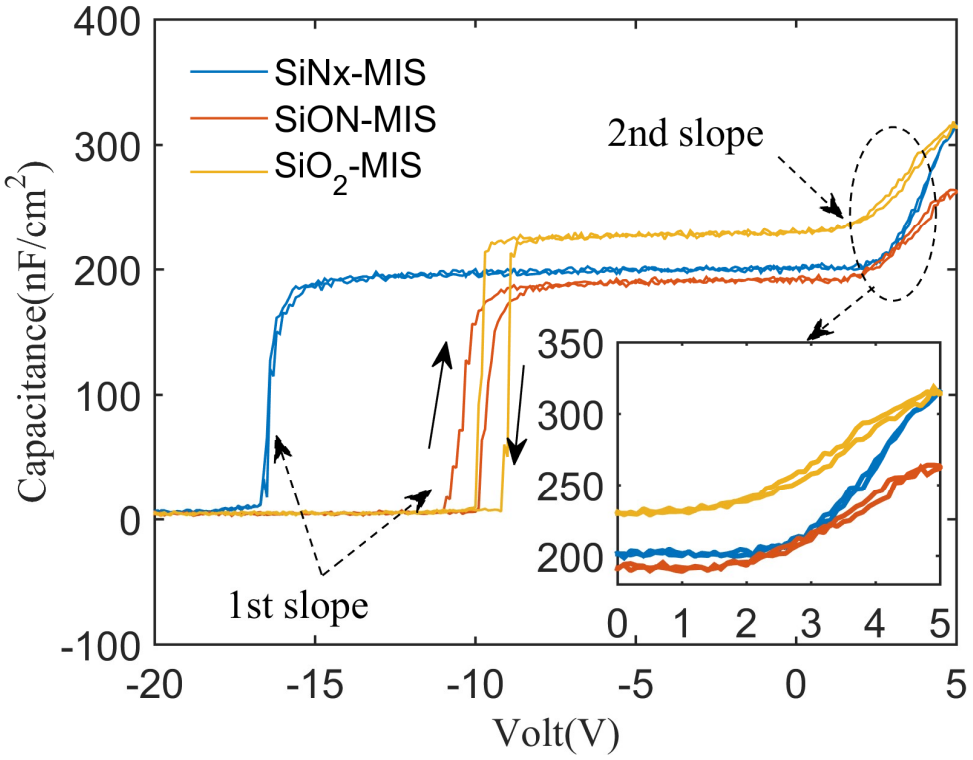

Figure 4. Forward and backward capacitance versus voltage (C-V) measurement with frequency of 1 MHz. Inset: magnified voltage range of 0~5 V.

In this work, the pulse period was fixed at 500 ms and the selected measured pulse widths were 100 µs, 1 ms, 10 ms, 100 ms, and 200 ms. Vds was kept at 1 V to reduce drain-to-gate field-assisted detrapping [29]. The inset of Figure 5b shows the forward sweep and backward sweep measurement conditions of V_{gs}. It is reported that the acceptor-like interface states were originally empty and would capture electrons during the forward sweep of V_{gs} with a low V_{gs} base [29]; therefore, the forward sweep curve was chosen to be the basic line. In the backward sweep of V_{gs}, interface traps with emission times longer than the measurement pulse width would remain occupied by electrons, which would lead to a positive shift of V_{th}. The detectable traps emission time τ is related to its energy using Shockley-Read-Hall statistics:

$$\tau = \frac{1}{v_{th}\sigma_n N_C}\exp\left(\frac{\Delta E}{kT}\right) \quad (1)$$

where v_{th}, σ_n, and N_C are the electron thermal velocity, electron capture cross-section, and electron concentration at the effective density of states in the conduction band in GaN. $\Delta E = E_C - E_T$ is the energy gap between the conduction band and interface trap. k is the Boltzman constant and T is the temperature.

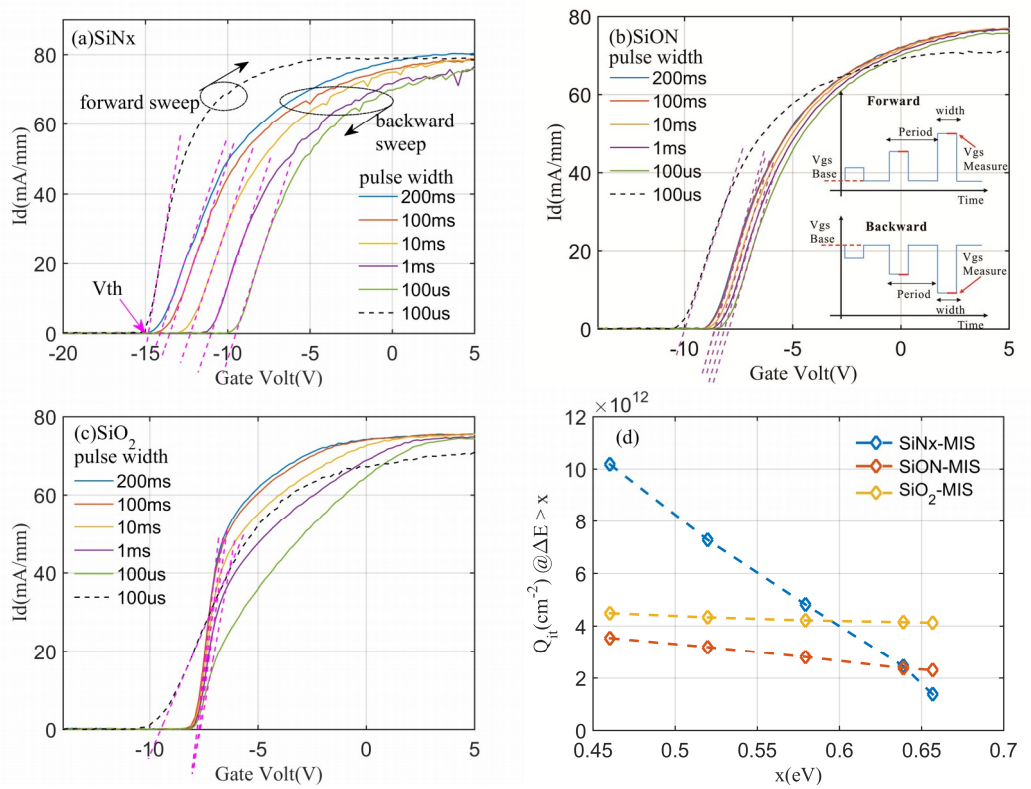

Figure 5. Pulse mode Id-V_{gs} curves with pulse width variations of 100 µs, 1 ms, 10 ms, 100 ms, and 200 ms. The pulse period is 500 ms. The Vds was kept at 1 VThe backward V_{gs} base is 5 V. (**a**) SiN_x MIS-HEMT with forward V_{gs} base of −20 V (**b**) SiON MIS-HEMT with forward V_{gs} base of −14 V. Inset: pulse V_{gs} condition with forward sweep and backward sweep (**c**) SiO_2 MIS-HEMT with forward V_{gs} base of −14 V (**d**) Interface trap charge density Q_{it} at ΔE > x(eV) of three samples.

For SiN_x MIS-HEMT, the forward V_{gs} base was −20 V. For SiON and SiO_2 MIS-HEMT, the forward V_{gs} base was −14 V. The backward V_{gs} base was 5 V for all three samples. As shown in Figure 5a–c, SiN_x MIS-HEMT shows a strong correlation between the measurement pulse width and the threshold voltage shift. SiO_2 MIS-HEMT shows little V_{th} change with different pulse widths. The corresponding interface-trapped charge density (Q_{it}) can be determined by:

$$Q_{it} = \frac{C_{ox} \cdot \Delta V_{th}}{q} \quad (2)$$

where C_{ox} values were extracted from C-V curves and the threshold voltage shift ΔV_{th} values were extracted from the results shown in Figure 5a–c.

Using Equations (1) and (2), Q_{it} with different ranges of ΔE were extracted and are shown in Figure 5d. At ΔE > 0.460 eV, the Q_{it} is 1.02×10^{13} cm^{-2}, 3.54×10^{12} cm^{-2}, and 4.49×10^{12} cm^{-2} for SiN_x, SiON, and SiO_2 MIS-HEMT, respectively. At ΔE > 0.657 eV, the Q_{it} turns out to be 1.38×10^{12} cm^{-2}, 2.31×10^{12} cm^{-2}, and 4.13×10^{12} cm^{-2}, respectively. SiN MIS-HEMT has the largest detected Q_{it} at ΔE > 0.460 eV. These kinds of interface traps have an emission time longer than 100 µs. In the backward sweep of V_{gs}, these traps would remain occupied by an electron, and lead to the largest V_{th} shift observed in SiN_x MIS-HEMT. In addition, the detectable Q_{it} density of the SiN_x sample includes a number of 8.81×10^{12} cm^{-2} located at 0.460 eV < ΔE < 0.657 eV. These kind of traps (acceptor like) are regarded as shallow traps with short emission times. As for the SiO_2 MIS-HEMT, the difference between Q_{it} at ΔE > 0.460 eV and Q_{it} at ΔE > 0.657 eV is small, which indicates that most of its interface traps are deep traps. In conclusion, SiN_x MIS-HEMT has the largest density of shallow interface traps and the lowest density of deep traps among the three samples. SiO_2 MIS-HEMT has the lowest density

of shallow traps and largest density of deep traps. The performance of SiON MIS-HEMT is between the SiN_x and SiO_2 sample. These results explain the difference in hysteresis in the 1st slope of the C-V curve. The larger deep trap densities of SiON and SiO_2 MIS-HEMT are responsible for the hysteresis in the 1st slope of the C-V curve. In addition, these calculated results show that shallow energy levels are more likely to be occupied by traps in the SiN_x/AlGaN interface than in the SiON/AlGaN interface and SiO_2/AlGaN interface. This offers chances for electron hopping, which could partially explain why SiN_x MIS-HEMT has the highest gate leakage current and the lowest I_{on}/I_{off} ratio among the three samples.

The Off-state Current collapse characteristic was measured by a slow switching test using an Agilent B1505A power device analyzer [37]. Various stress voltages from 5 V up to 50 V were applied on drain-to-source electrodes when V_{gs} was fixed at −18 V to ensure that the channel was pinched off. After the stress situation for 10 s, V_{gs} was changed to 0 V and the on-state Id-Vd curve was measured. In addition, the time interval was 10 ms between the two data points. This would lead to trap discharging and recover the current collapse to some extent. Therefore, the deep traps would be the major factor causing current collapse. Figure 6a–c shows that the degradation of the drain current was 11.6%, 71.26%, and 84.14%, respectively, for SiN_x MIS-HEMT, SiON MIS-HEMT, and SiO_2 MIS-HEMT. As Figure 6d shows, the dynamic Ron increases more quickly along with off-state drain bias stress (Vdstress) for SiO_2 MIS-HEMT. After 50 V Vdstress was applied to the devices, the ratio of dynamic Ron and static Ron turns out to be 1.18, 5.64, and 24.5, respectively, for SiN_x MIS-HEMT, SiON MIS-HEMT, and SiO_2 MIS-HEMT. Among these three samples, SiN_x MIS-HEMT shows better performance with regard to suppressing the current collapse than the other two samples. Though SiN_x MIS-HEMT has the largest detected interface trap density, most of them are relatively shallow traps located at 0.46 eV < ΔE < 0.657 eV. These kinds of shallow traps contribute less to current collapse. SiON and SiO_2 MIS-HEMT have higher trap density than SiN_x MIS-HEMT at ΔE > 0.657 eV. This leads to more serious current collapse observed in SiON and SiO_2 MIS-HEMT. The current collapse performance coincides with the extracted results of C-V and pulse Id-V_{gs} measurements for interface deep traps, which indicates that deep interface traps strongly influence the collapse characteristic.

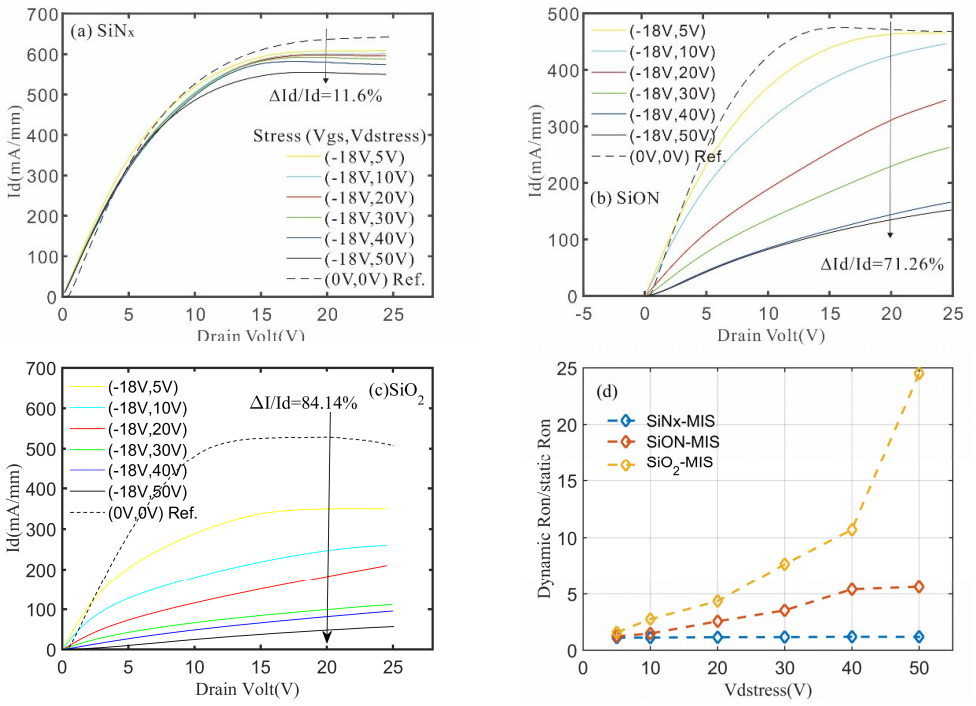

Figure 6. Id-Vds curves at V_{gs} = 0 V of (**a**) SiN_x MIS-HEMT (**b**) SiON MIS-HEMT (**c**) SiO_2 MIS-HEMT after off-state stress bias at V_{gs} = −18 V, Vds stress at 5, 10, 20, 30, 40, and 50 V for 10 s. (**d**) The ratio of dynamic Ron and static Ron versus different off-state Vds stress.

To further investigate the difference in characteristics of SiN_x, SiON and SiO_2 MIS-HEMT, room temperature photoluminescence (PL) spectra were recorded. As shown in the inset of Figure 7, the relative intensities of the yellow band (wavelength at approximately 560 nm) of the three dielectric/AlGaN/GaN samples are quite different. It has been reported that Si and O impurity, which would act as shallow donors, can effectively impact the yellow luminescence (YL) [38,39]. The largest YL intensity observed on SiO_2/AlGaN/GaN sample implies that it has a maximum number of Si and O shallow donors among the three samples. During the deposition of SiON and SiO_2, the reactive gas N_2O would cause uncontrollable oxidation of the AlGaN interface and therefore generate several kinds of surface states [40]. The SiN_x chemical deposition process involves NH_3 plasma treatment, which would be effective to suppress the N-vacancies-related surface defects at the AlGaN surface [41]. When the off-state stress is applied to the devices, the shallow donors, oxides, and defects mentioned above would capture electrons and cause the phenomenon of the virtual gate [42]. The formation of the virtual gate would increase the depletion region and thus cause the decrease of drain current. The above factors together lead to the different performance on current collapse of the three samples.

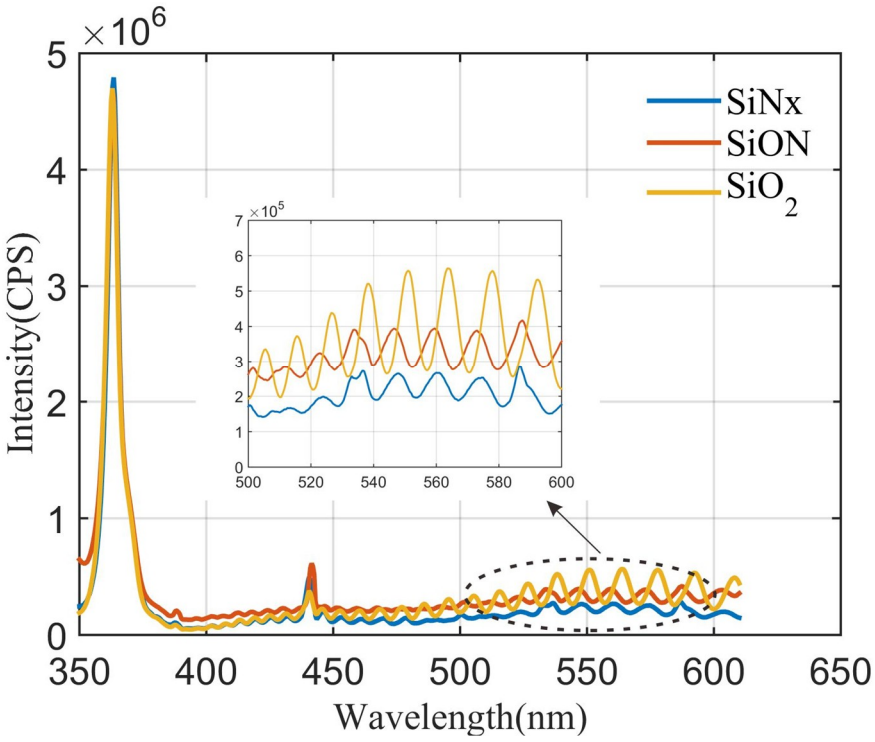

Figure 7. Photoluminescence (PL) spectra at room temperature of three samples.

4. Conclusions

In conclusion, we have fabricated AlGaN/GaN MIS-HEMTs with PECVD-deposited SiN_x, SiON, and SiO_2 as the gate dielectric and passivation layer. The DC static characteristics, interface traps, and current collapse of MIS-HEMTs with different dielectrics were comprehensively compared. The SiN_x sample performs well with regard to suppressing the current collapse but suffers from high leakage current and high shallow trap density. The SiON MIS-HEMT exhibits a low gate leakage current of 3.86×10^{-5} mA/mm and a high breakdown voltage of 428 V, which indicates it is a great candidate as a gate dielectric and passivation layer. However, its deposition parameters need to be further optimized in order to enhance the reliability and stability.

Author Contributions: Conceptualization, K.G. and D.C.; Formal analysis, K.G. and D.C.; Investigation, Q.Z.; Methodology, K.G. and Q.Z.; Supervision, H.W.; Writing original draft, K.G. and D.C.; D.C. designed the

experiment, prepared the samples and performed the measurements. K.G. contributed to the conception of the study and designed the experiment. Q.Z. contributed to the data analysis and wrote the manuscript. H.W. supervised the study and reviewed the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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