Evaluation of LDMOS Figure of Merit Using Device Simulation

Aiman Salih and Jiann-Shiun Yuan *

Department of Electrical and Computer Engineering, University of Central Florida, Orlando, FL 32816, USA; asalih1@knights.ucf.edu
* Correspondence: yuanj@mail.ucf.edu; Tel.: +1-407-8235719

Abstract: The benefit of the super-junction (SJ) technique at the low-voltage (30 V) range is investigated in this work. Optimizations such as adding a buffer layer to the device have been used, but simulation and theoretical evidences show that the benefits of the SJ technique are marginal for 30 V applications. The floating P structure proved to be a good replacement for SJ devices at the 30 V range due to a simpler fabrication process as well as performance gains achieved with optimization. Also, a new idea of combining the floating P layer with a shallow trench isolation layer is proposed and simulated using TCAD, yielding the figure of merit ($R_{DS(on)} \times Q_G$) of 5.93 mΩ-nC, which is a 39% improvement on the standard floating P device.

---

1. Introduction

Efficient power supplies with fast transient response and accurate voltage regulation for low-voltage applications are becoming more important in today's market. This can be mainly attributed to the fast growth and increase in demand for data-centers, as well as the massive increase in the amount of data being transmitted. It is estimated that the amount of annual global data-center traffic will increase from 4.7 zettabytes in 2015 to 15.3 zettabytes in 2020, where 1 ZB = 2^{40} gigabytes [1]. Also, the user base of consumer cloud storage is predicted to increase from 47 in 2015 to 59% in 2020 [1]. With the current system design of data-centers, there is a significant volume of these low-voltage power devices in use when it comes to voltage regulation [2]. As a result, it is critical to optimize the design of these power devices such that high efficiency and performance are achieved in data-center power regulators.

The laterally double-diffused metal oxide semiconductor (LDMOS) transistor offers higher levels of integration for integrated circuits (ICs) [3]. As a result, the LDMOS is viewed as a viable solution for advanced systems on a chip (SoC), which have power integrated within the solution combining both high speed digital logic CMOS and high power LDMOS devices onto the same silicon chip [4]. These SoCs are often found in Internet of Things (IoT) applications. LDMOS devices have also found a footing in advanced integrated power electronics modules and electric vehicles that are now rampant in the market.

The work presented gives a viable solution for improving upon the design of 30 V power devices. The super-junction (SJ) technique, which involves the use of consecutive N and P pillars in the device's drift region and is well established in the high voltage (600 V) range, is tested here for the low-voltage range. In [5] the authors attempt to integrate the SJ technique within their low-voltage device design, but from [6,7], and further investigation here, it can be seen that the SJ technique may not be preferred for low-voltage applications. An alternative approach to designing a 30 V power device is proposed by replacing the SJ pillars and the shallow trench isolation (STI) with a floating p-type layer in the drift region.

This paper contains five sections. Following the introduction, Section 2 discusses the low-voltage Super-Junction LDMOS that was investigated in this work. Section 3 covers all of the details for the floating P layer device and explains how it can be used to replace SJ devices at low-voltages (30 V range). Section 4 presents a new concept of combing both STI technology with a floating P layer to generate a device with a very low figure of merit (FOM) ($Q_G \times R_{DS(on)}$). Section 5 gives a summary.

2. Low-voltage SJ LDMOS Analysis

Figure 1 shows a conventional LDMOS used in our simulation, while the structure of the SJ LDMOS device is displayed in Figure 2. The SJ LDMOS in Figure 2 contains N and P SJ pillars. Shallow trench isolation (STI) is used in the drift region. This assists in absorbing the peak electric field that commonly occurs at the edge of the gate [8]. Both the conventional and SJ devices are simulated using two-dimensional (2D) and three-dimensional (3D) Sentaurus Device TCAD. For the conventional device, it was possible to simulate it in a 2D environment, while the SJ LDMOS is simulated in 3D. The SJ LDMOS is quite unique in that the SJ N and P pillars do not exist on the front facing 2D cross section, but the pillar array is placed within the width of the device, requiring a 3D simulation [9].
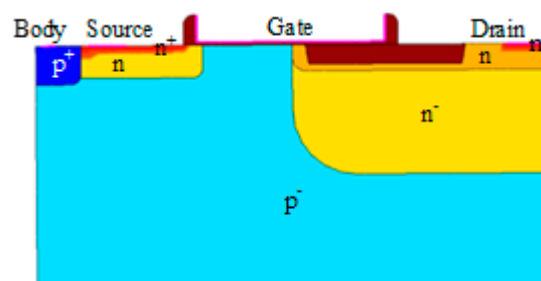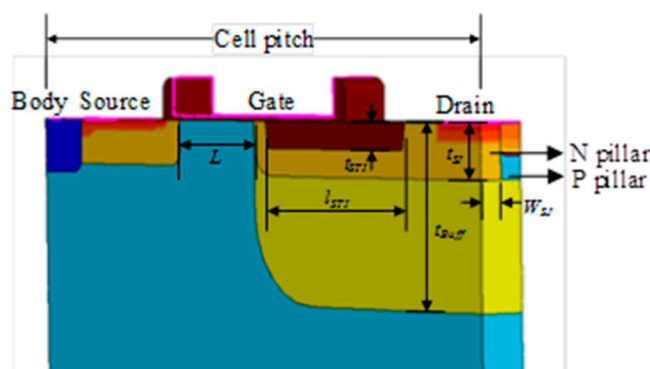

Figure 1. Conventional LDMOS device.

Figure 2. Super-junction LDMOS device.

Table 1 lists the super-junction LDMOS key device dimensions.

Table 1. Super-junction device dimensions.

Parameter	Size
cell pitch	8 μm
channel L	1.4 μm
t_{buff}	2 μm
t_{SJ}	0.6 μm
W_{SJ}	0.5 μm
l_{STI}	2.5 μm
t_{STI}	0.3 μm

The device simulation uses the following physics models: Old Slotboom model [10] for the effective intrinsic carrier density; while doping dependence [11], high field saturation [12], and Lombardi [13] models are used for the mobility dependence. Shockley Reed Hall [14], Auger [15], and Okuto avalanche models [16] for the recombination and breakdown current.

Figure 3 compares the on-state resistance ($R_{DS(on)}$) and gate charge (Q_G) between the conventional device and the SJ device. Both devices have a breakdown voltage of 30 V. The conventional device has a FOM of 123 mΩ-nC while the SJ device has a FOM of 51 mΩ-nC. Note that $R_{DS(on)}$ and Q_G are both normalized to an active area of 1 mm². $R_{DS(on)}$ was examined at the 1 A device operating point in the linear region. Q_G was extracted from the gate voltage (V_{GS}) versus Q_G plot in Sentaurus.
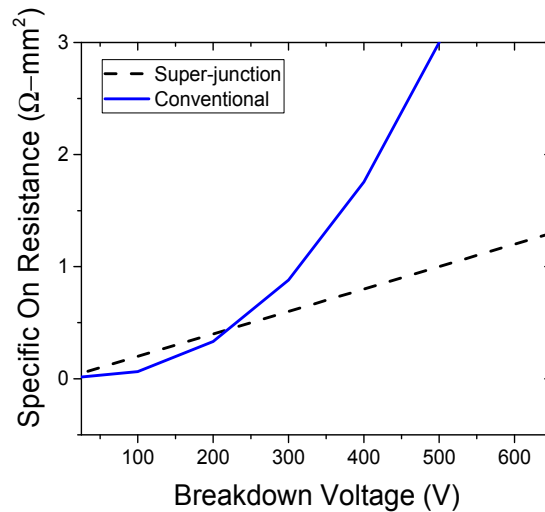

Figure 3. Simulated results of conventional and SJ devices' *BVDss* vs. Sp $R_{DS(on)}$.

From Table 2 we can see that at the same operating voltage of 30 V, the low-voltage SJ has a slight increase in $R_{DS(on)}$, but a lesser amount of charge is accumulated at the gate terminal. This leads the SJ device to have an overall improved FOM, lower than that of the conventional device. It is worth pointing out that lower Q_G leads to improved switching losses, while lower $R_{DS(on)}$ helps reduce conduction losses. Conduction losses are significant in switching power supplies at low frequency [17]. The conduction losses become an even more critical factor when looking at most modern soft switching topologies. Soft switching topologies significantly reduce the switching losses by switching at either zero current or zero voltage [18].

Table 2. Conventional versus SJ device for specific $R_{DS(on)}$ and Q_G.

	Conventional	SJ Device
$R_{DS(on)}$	87 mΩ-mm²	113 mΩ-mm²
Q_G	1.4 nC/mm²	0.45 nC/mm²

The lack of improvement in $R_{DS(on)}$ of the examined SJ LDMOS device reduces or negates the benefit of using SJ for the 30 V range. Equation (1) shows the on-state resistance as a function of breakdown voltage (*BVDss*) for both the conventional and SJ devices [6]:

$$R_{DS(on)} = \begin{cases} \dfrac{a \cdot \sqrt{B} \cdot BVDss^{\frac{5}{2}}}{\mu_n \cdot \varepsilon \cdot A} & \text{conventional} \\[2ex] \dfrac{a \cdot B^{\frac{1}{6}} \cdot BVDss^{\frac{7}{6}}}{q \cdot \mu_n \cdot N_D \cdot A} & \text{SJ device} \end{cases} \tag{1}$$

where *BVDss* is the breakdown voltage, *a* is a constant that discerns between low-voltage and high voltage devices (*a* = 6.21 for a 30 V conventional device & *a* = 1.87 for a 600 V conventional device, and *a* = 6.9 for a 30 V SJ device & *a* = 2.07 for a 600 V SJ device), *B* is the radiative recombination constant, μ_n is the electron mobility, ε is the silicon permittivity, N_D is the drift doping, and *A* is the active area.

Equation (1) is often used to derive the silicon limit line ($R_{DS(on)} \times$ active area). In capturing $R_{DS(on)}$ in Equation (1) as a function of *BVDss*, the analytical equation uses the constant *a*, whose value changes depending on the breakdown voltage of the device. This difference stems from the design of the device and the growth of drift region length as the device size gets larger for higher breakdown voltages. It is worth pointing out that the $R_{DS(on)}$ model presented in Equation (1) is based on a dominant drift resistance. As the size of the device and drift length decrease, the ratio over which the drift resistance contributes to the overall resistance also decreases. For example, for a 600 V device the drift resistance is 96.5% of the total resistance [6]. However, for a 30 V device, the drift resistance is only 29% of the overall on-state resistance. Figure 3 gives a plot of simulated results using Equation (1) comparing the *BVDss* versus $R_{DS(on)}$ trend for both the super-junction device and the conventional device. From Figure 3 it is evident that for devices with *BVDss* less than 200 V the conventional device achieves a lower $R_{DS(on)}$ than that of SJ, but this trend is reversed for devices with *BVDss* greater than 200 V. For this reason, and also from our obtained simulation results, it is evident that the use of SJ technique to design power devices is more suitable to design high voltage power devices [19] than low-voltage ones. The off-state breakdown voltage and on-resistance can be expressed by the analytical equations below:

$$BVDss = \sqrt{E_{crit}{}^2 - E_L{}^2} \cdot t_{SJ} \tag{2}$$

$$R_{DS(on)} \cdot A = \frac{t_{SJ} \cdot W_n}{\varepsilon \cdot \mu_n \cdot E_L} \tag{3}$$

where E_{crit} is the critical breakdown electric field for silicon, E_L = SJ pillars lateral electric field value, t_{SJ} is the SJ pillar depth, W_n is the SJ pillar width.

The SJ technique also comes with some process complexities. These arise from the meticulous need to accurately balance the implantation charge required to realize the N and P pillars in the fabrication process. Any implantation imbalance between the pillars leads to a significant reduction in the device's breakdown voltage [7]. Another issue stems from the scaling of these SJ pillars for low-voltage applications: Equations (2) and (3) list the *BVDss* and $R_{DS(on)}$ dependence on the depth and width of the SJ pillars [20]. Most modern SJ manufacturing, such as in [21], rely on ion implantation. However, the need to scale down the SJ pillars while at the same time still ensuring their optimal performance may make their fabrication process too challenging and costly, due to the ion scattering that becomes more problematic when features are small.

3. LDMOS with Floating P-Type Layer

The implementation of a floating p-type layer in place of the STI gate edge region is a technique that is examined for the LDMOS device; the method is also implemented in [22]. The technique was investigated for low-voltage devices to measure the possibility to outperform SJ in this voltage range. Figure 4 shows a cross section of the device considered. It can be seen from Figure 5 that the device has a simpler 2D cross section when compared to that of the SJ LDMOS. Its device dimensions are given in Table 3. The device cell pitch has also been modified and reduced from 8 μm to 3 μm. This achieves a higher cell density improving the on-state characteristics of the device. Table 2 lists some of the key device dimensions.
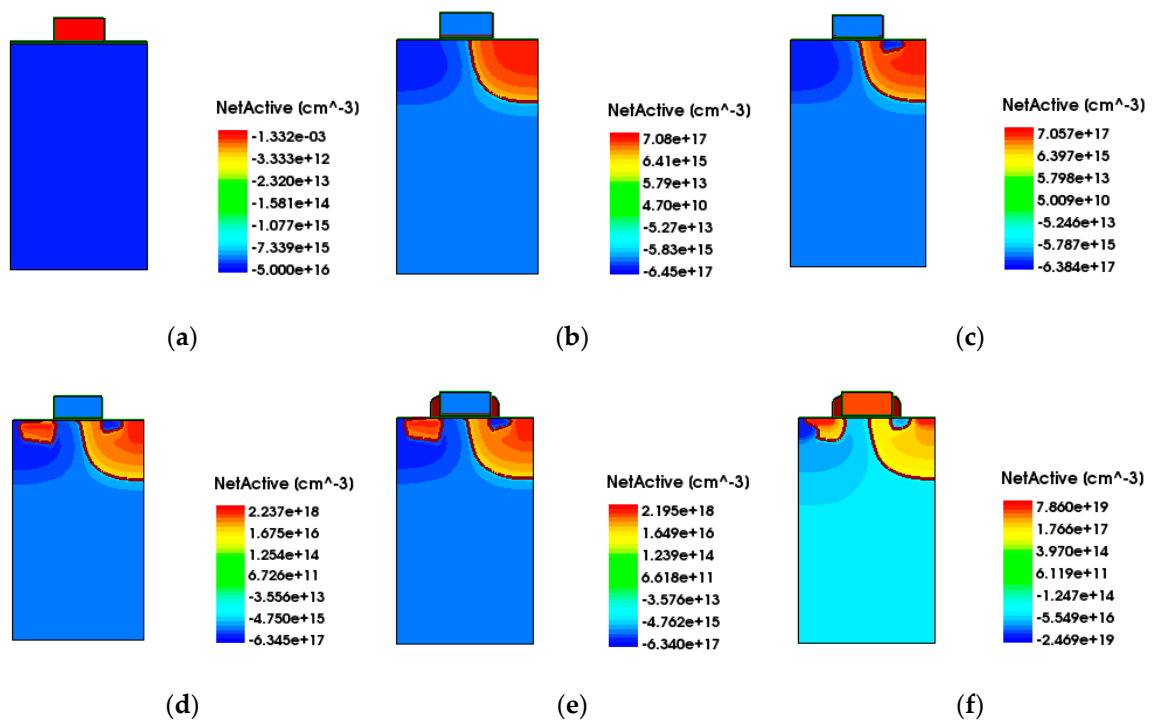
Figure 4. Floating P layer device process flow cross sections (**a**) gate poly & gate ox patterned on surface of wafer (**b**) N-well & P-well implanted (**c**) floating P layer deposited (**d**) source n-type layer deposited (**e**) oxide spacers formed (**f**) N$^+$ contacts and P$^+$ body contact formed.
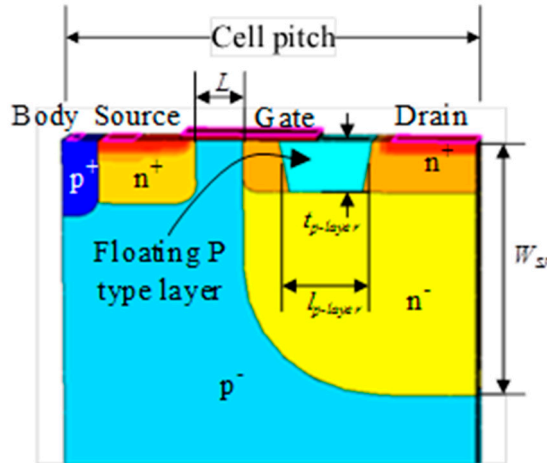
Figure 5. Floating P LDMOS device.

Table 3. LDMOS with floating p-type dimensions.

Parameter	Size
cell pitch	3 μm
channel L	0.34 μm
t_{buffer}	2 μm
$l_{p\text{-}layer}$	0.61 μm
$t_{p\text{-}layer}$	0.4 μm

A process simulation for the p-type layer device was developed. The process simulation sheds light on how the added device features can be incorporated with relative ease, especially when compared to the complex SJ process. Figure 4 shows cross sections of the device throughout the process.

The device is built on a <100> lattice p-type silicon wafer. The process is self-aligned to the gate: as such, the gate dielectric and the gate poly are initially deposited and patterned on the surface of the silicon wafer using the same mask. The P and N wells are then formed using the same mask with a combination of positive and negative photoresist, such that each dopant is deposited on either side of the gate. A dose of 3×10^{13} cm^{-2} with an energy of 150 keV is used for the N well, while a dose of 4×10^{13} cm^{-2} with an energy of 100 keV is used for the P well. The junction depth of the N well is around 1.35 μm, while the junction depth of the P well is around 1.40 μm.

For the floating p-type structure, implanting the dopants just under the edge of the gate on the drain side proved challenging, due to the fact that the process is self-aligned to the gate and the thickness of the polysilicon does not permit to implant the dopants directly. To solve this, an angled implant at varying energies was used to achieve the desired structure just under the gate edge. Four different doses of 3.5×10^{12} cm^2 were used to obtain the desired profile; the energies used are in the following order: 20, 40, 80, and 160 keV.

The process is completed by implanting the phosphorus dopants for the source; a dose of 4.5×10^{13} cm^2 is used with an energy of 70 keV. The dopants were activated using rapid thermal annealing (RTA) for 5 mins to stay within the thermal budget. Similarly the P$^+$ body dopants were introduced as well as the N$^+$ contact dopants, RTA is also used here to activate the dopants.

This floating P LDMOS process displays the feasibility and replicability of making the floating P device. The process advantage coupled with the performance improvement achieved with further optimization shows how the floating P layer device can outperform SJ devices at the 30 V application.

Table 4 gives a comparison of the $R_{DS(on)}$ and Q_G between the SJ device and the floating p-type layer device. Both devices have a breakdown voltage of 30 V. The FOM of both devices can be determined. The SJ device has a FOM of 51 mΩ-nC while the floating P layer device has a FOM of 9.75 mΩ-nC. Note that both $R_{DS(on)}$ and Q_G are both normalized to an active area of 1 mm^2. The performance enhancement seen in Table 4 stems from the cell pitch optimization that was given to the floating P device. This led for the device unit cell to occupy less area resulting in an improved normalized $R_{DS(on)}$ and Q_G values.

Table 4. SJ versus floating P device for specific $R_{DS(on)}$ and Q_G.

	SJ Device	**Floating P**
$R_{DS(on)}$	113 mΩ-mm^2	63 mΩ-mm^2
Q_G	0.45 nC/mm^2	0.16 nC/mm^2

4. LDMOS with STI Region Surrounded by P-Type Layer

It was observed that the peak electric field of the floating P LDMOS device occurred on the surface of the p-type layer as shown in Figure 6. It is known that the critical electric field of silicon is around 5×10^5 V/cm; the electric field on the surface exceeds that of the critical electric field as the device approaches breakdown and is the major source of impact ionization in the device. To counter the effects of the surface peak electric field, it was necessary to replace the material of the affected region with a material that has a higher critical electric field. Since the affected region is on the surface of the device, it is feasible with an SiO$_2$-filled trench realized at the same time and in the same way with the STI used in the fabrication process, as demonstrated in Figure 7.
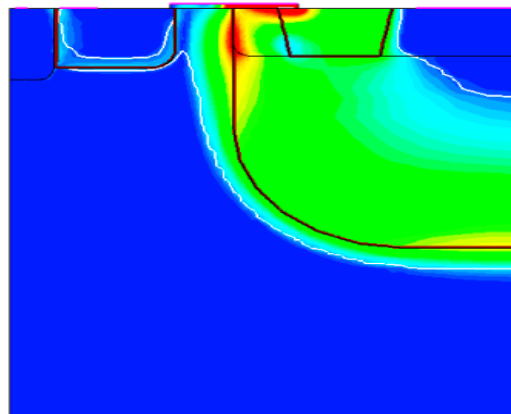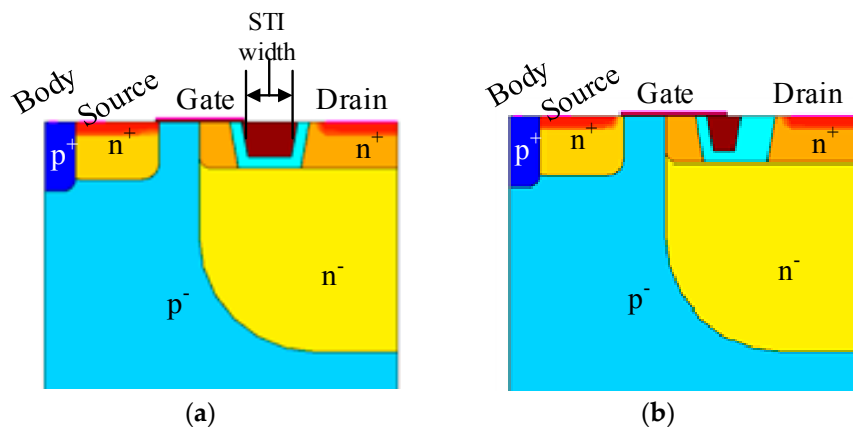
Figure 6. Floating P device electric field distribution.

(**a**)　　　　　　　　　　　　　　　　　　　　(**b**)

Figure 7. STI surrounded by floating P LDMOS (**a**) centered (**b**) staggered oxide.

Table 5 gives the performance of the LDMOS device when the STI surrounded floating P layer technique is applied. Both devices are designed with a breakdown voltage of 30 V. The simulation results show that the device with the floating P layer has a FOM of 9.75 mΩ-nC while the device with STI plus floating P layer has a FOM of 5.93 mΩ-nC. That is a 39% improvement in the FOM. From our understanding of the current state of art, the implementation of such floating P layer with a STI region is a new design that led towards the given low FOM value observed by device simulation.

Table 5. Floating P versus STI w/floating P device for specific $R_{DS(on)}$ and Q_G.

	Floating P	**STI + Floating P**
$R_{DS(on)}$	63 mΩ-mm^2	22.8 mΩ-mm^2
Q_G	0.16 nC/mm^2	0.26 nC/mm^2

From Table 5 one can notice that there is a slight increase in the gate charge of the STI plus floating P device which can be attributed to the wider surface area of the oxide in contact with silicon attracting a higher total number of charges. Despite this slight increase in Q_G, the on-state resistance was reduced by a significant amount. The increase in Q_G is due to the larger MOS capacitor plate area at the gate terminal caused by the addition of the STI region. The reduction in $R_{DS(on)}$ stems primarily from the decrease of the depth of the p-type layer, as some of it is occupied by STI, leading to a thinner space charge region to be formed in the in the N- buffer layer, which is in contact with the P layer. Since the buffer layer is lowly doped, any changes in the P layer dimensions would lead to sizable variation in

the depletion width. The smaller space charge region causes a reduction in the device sheet resistance which leads to the lower on-state resistance.

The performance of the device was optimized by adjusting the size and placement of the oxide STI region. Figure 8 plots the performance of the device when the STI is staggered by shifting it to the left. An STI width of around 0.25 μm was the optimal design point giving the desired 30 V breakdown and the $R_{DS(on)}$ value is equal to 22.8 mΩ-mm^2. Reducing the STI width from 0.25 μm to smaller values will increase the on-resistance and decrease the off-state breakdown voltage, as shown in Figure 8. For example, when the STI width is reduced from 0.25 μm to 0.125 μm, the $R_{DS(on)}$ increases from 23 to 23.3 mΩ-mm^2 and the breakdown voltage decreases from 30 to 29 V. On the other hand, when the STI width is increased from 0.25 μm to 0.375 μm, the $R_{DS(on)}$ decreases to 22.7 mΩ-mm^2 but the breakdown voltage decreases 29 V. Figure 9 plots the performance when the STI is centered with respect to the mid-point of the P type layer. In this case, the optimal width for the STI centered with respect to floating P type region is around 0.28 μm. Similarly, reducing the STI width from 0.28 μm to smaller values will increase the on-resistance and decrease the breakdown voltage (see Figure 9). When the STI width is decreased from 0.28 μm to 0.125 μm, the $R_{DS(on)}$ increases from 22.8 to 23.3 mΩ-mm^2 and the breakdown voltage drops to about 29 V. On the other hand, when the STI width is increased from 0.28 μm to 0.375 μm, the $R_{DS(on)}$ decreases to 22.5 mΩ-mm^2 but the breakdown voltage decreases 29 V as well.
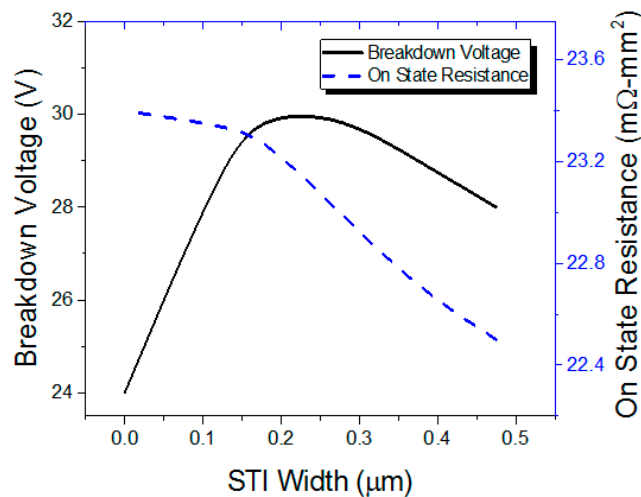

Figure 8. STI staggered with respect to floating P type region.
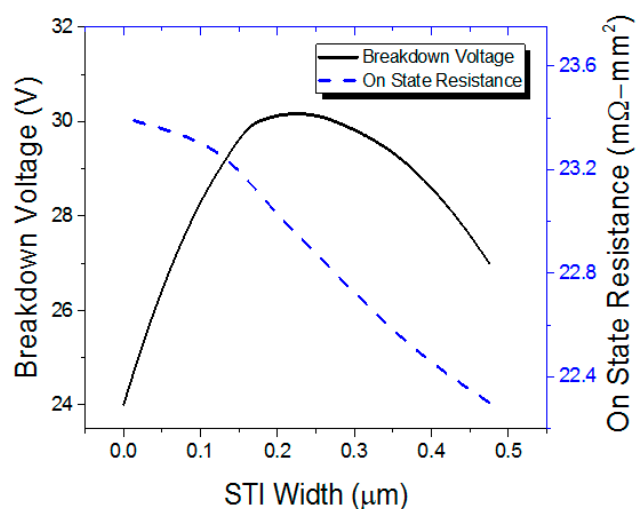

Figure 9. STI centered with respect to floating P type region.

From Figures 8 and 9 one can see that that the staggered STI achieves an overall better performance as far as the on-state resistance is concerned. Also, the staggered STI achieves a lower Q_G compared to the centered STI. This is due to the smaller surface area of the oxide under the gate field plate.

5. Conclusions

This work investigates the super-junction LDMOS figure of merit ($R_{DS(on)} \times Q_G$) for the 30 V application. The Sentaurus TCAD device simulation results indicate that the super-junction technique may not be suitable for low-voltage applications due to limited performance improvement in specific on-state resistance versus breakdown voltage. The process difficulties faced with creating long pillars for small feature sizes and charge balancing between the P and N pillars when the super-junction device is fabricated are added unfavorable factors for low-voltage super-junction device applications.

A replacement for the super-junction technique is suggested by removing the super-junction pillars and shallow trench isolation region and adding a floating p-type layer. This technique shows improvement in the device performance upon optimization. A process simulation for the device was developed; this process demonstrated the feasibility and replicability of using this technique in real application. Lastly a new technique of surrounding the shallow trench isolation region with a P type layer is introduced which to our understanding is a new design to achieve a low figure of merit. The figure of merit ($R_{DS(on)} \times Q_G$) improved, going from 9.75 mΩ-nC down to 5.93 mΩ-nC for the floating P device.

Author Contributions: Aiman Salih performed the device design and simulation as well as wrote the manuscript. Jiann-Shiun Yuan provided suggestion for simulation and revised the manuscript. Both of them proofread the final manuscript.

Conflicts of Interest: The authors declare no conflicts of interest.

References

1. Cisco. *Cisco Global Cloud index: Forecast and Methodology, 2015–2020*; Cisco Systems, Inc.: San Jose, CA, USA, 2016; Volume 26.
2. Yeaman, P. Datacenter Power Delivery Architectures: Efficiency and Annual Operating Cost. Available online: http://www.vicorpower.com/docuents/whitepaper/server_efficiency_vichip.pdf (accessed on 1 March 2017).
3. Mai, A.; Rucker, H.; Sorge, R.; Schmidt, D.; Wipf, C. Cost-effective integration of RF-LDMOS transistors in 0.13 μm CMOS technology. In Proceedings of the IEEE Typical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, San Diego, CA, USA, 19–21 January 2009; pp. 1–4.
4. Heyer, P. Meeting the Power Management Needs of Portable Products. Available online: http://www.eetimes.com/documents.asp?doc_id=1273021 (accessed on 28 March 2017).
5. Sabui, G.; Shen, Z. On the feasibility of further improving figure of merit (FOM) of low voltage power MOSFETs. In Proceedings of the IEEE International Symposium on Power Semiconductor Devices & ICs, Waikoloa, HI, USA, 15–19 June 2014; pp. 155–158.
6. Lutz, J.; Schlangenotto, H.; Scheuermann, U.; De Doncker, R. *Semiconductor Power Devices*; Sringer: Singapore, Singapore, 2011.
7. Wang, H.; Napoli, E.; Udrea, F. Breakdown voltage for superjunction power devices with charge imbalance: An analytical model valid for both punch through and non punch through devices. *IEEE Trans. Electron Devices* **2009**, *56*, 3175–3183. [CrossRef]
8. Hu, Y.; Booth, R.; White, M. An analytical model for the lateral channel electric field in LDD structures. *IEEE Trans. Electron Devices* **1990**, *37*, 2254–2264. [CrossRef]

9. Quddus, N.; Tu, Y.; Ishiguro, S. Drain voltage dependence of on resistance in 700 V super junction LDMOS transistor. In Proceedings of the IEEE International Symposium on Power Semiconductor Devices & ICs, Kitakyushu, Japan, 24–27 May 2004; pp. 201–204.

10. Slotboom, J.; de Graff, H. Measurement of bandgap narrowing in Si bipolar transistors. *Solid-State Electron.* **1976**, *19*, 857–862. [CrossRef]

11. Roulston, J.; Arora, N.; Chamberlain, S. Modeling and measurement of minority-carrier lifetime versus doping in diffused layers of n$^+$-p silicon diodes. *IEEE Trans. Electron Devices* **1982**, *29*, 281–291. [CrossRef]

12. Canali, C.; Majni, G.; Minder, R.; Ottaviani, G. Electron and hole drift velocity measurement in silicon and their empirical relaton to electric field and temperature. *IEEE Trans. Electron Devices* **1975**, *22*, 1045–1047. [CrossRef]

13. Lombardi, C.; Manzini, S.; Saporito, A.; Vanzi, M. A physically based mobility model for numerical simulation of nonplanar devices. *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.* **1988**, *7*, 1164–1171. [CrossRef]

14. Shockley, W.; Read, W. Statistics of the recombinations of holes and electrons. *Phys. Rev.* **1952**, *87*, 835. [CrossRef]

15. Herderson, I.; McGhee, J. A boundary determined Auger recombination model for semiconductor power diodes. *Math. Model.* **1987**, *8*, 279–282. [CrossRef]

16. Okuto, Y.; Crowell, C. Threshold energy effect on avalanche breakdown voltage in semiconductor junctions. *Solid-State Electron.* **1975**, *18*, 161–168. [CrossRef]

17. Lakkas, G. MOSFET power losses and how they affect power-supply efficiency. *Analog Appl. J.* **2016**, *Q1*, 22–26.

18. Hun, G.; Lee, C. An overview of soft-switching techniques for PWM converters. *Eur. Power Electron. Drives J.* **1993**, *3*, 39–50. [CrossRef]

19. Lorenz, L.; Deboy, G.; Knapp, A.; Marz, M. COOLMOS^{TM}-a new milestone in high voltage power MOS. In Proceedings of the IEEE International Symposium on Power Semiconductor Devices & ICs, Toronto, ON, Canada, 26–28 May 1999; pp. 3–10.

20. Saito, W. Comparison of theoretical limits between superjunction and field plate structures. In Proceedings of the IEEE International Symposium on Power Semiconductor Devices & ICs, Kanazawa, Japan, 26–30 May 2013; pp. 241–244.

21. Borany, J.; Friedrich, M.; Rub, M.; Deboy, G.; Butschke, J.; Letzkus, F. Application of ultra-high energy boron implantation for superjunction power (COOLMOS^{TM}) devices. *Nucl. Instrum. Methods Phys. Res. Sec. B* **2005**, *237*, 62–67. [CrossRef]

22. Sun, W.; Zhang, C.; Liu, S.; Su, W.; Zhang, A.; Wang, S.; Ma, S.; Huang, Y. Investigation on hot-carrier-induced degradation for the n-type lateral DMOS with floating p-top layer. In Proceedings of the IEEE International Symposium on Power Semiconductor Devices & ICs, Waikoloa, HI, USA, 15–19 June 2014; pp. 394–397.