electronics

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Prediction of the Nonlinearity by Segmentation and Matching Precision of a Hybrid R-I Digital-to-Analog Converter

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Received: 20 March 2018; Accepted: 1 June 2018; Published: 6 June 2018

Abstract: The data converters' nonlinearity, which is mainly caused by random mismatch, reflects the performance deviation between the actual realization and an ideal situation. The interpretation of the numerical relationship between the nonlinearity and matching precision for a hybrid digital-to-analog converter (DAC) consisting of a k-bit resistor-string and an m-bit current-steering array (R-I DAC) is a challenging task. In this article, we propose a method to predict the nonlinearity by the segmentation and matching-precision of an R-I DAC. First, we propose a mathematical model that focuses on the output and mismatches of an R-I DAC. The model shows that nonlinearity gets worse when the segmentation ratio (k/m) increases. Second, we derive theoretical expressions for the static nonlinearity and matching precision. It is shown that the resolution number of resistor (k) has more influence on nonlinearity than the resolution number of current steering (m). Designers can quickly determine the segmentation strategy and matching precision from the derived equations. Finally, we achieve a nonlinearity that is smaller than half the least significant bit (LSB) when the matching resolution in the bits of the resistors and current sources are $k + 4$ and $m + 2k + 2$, respectively. For the verification of the study proposed, three test groups of prototypes with different matching precisions are fabricated and measured. The measured static and dynamic performance of the designed DACs support our proposal expressions.

Keywords: digital-to-analog converter (DAC); static linearity; segmentation; matching resolution

1. Introduction

The data converters' nonlinearity, which is mainly caused by random mismatch, reflects the performance deviation between an actual realization and an ideal situation. The data converters' nonlinearity can be categorized into static nonlinearity and dynamic nonlinearity [1–3]. Static nonlinearity includes the differential nonlinearity (DNL) and integrated nonlinearity (INL). Dynamic nonlinearity mainly includes the spurious-free dynamic range (SFDR) and the effective number of bits (ENOB). The static nonlinearity is fundamental, and it sets an upper limit of the dynamic nonlinearity [2]. So, the static nonlinearity is addressed.

Static nonlinearity is mainly caused by mismatches that may be random, systematic, or a combination of both. While systematic mismatches can usually be compensated with layout skills and a choice of circuit architecture and calibration, the random mismatches due to the stochastic nature of physical geometry and doping cannot be avoided [4–6]. In such a case, random mismatches are the main cause of static nonlinearity. So, research on the mechanisms of random mismatches' effects on static nonlinearity has been a focus [4,6–12].

The static nonlinearity mechanism of traditional segmented cascade digital-to-analog converters (DACs) and two-step analog-to-digital converters (ADCs) have been fully understood [13]. A segmented DAC consists of several segments containing corresponding matching units. The static nonlinearity of a traditional segmented DAC is a *linear combination* of mismatches of different segments. Specifically, for traditional segmented cascade DACs consisting of two segmented parts, the part with the most significant bits (MSBs) mainly determines the accuracy of the overall converter, and the part with the least significant bits (LSBs) is required for the accuracy of the LSBs as a standalone converter [13]. For example, for an *n*-bit (*m*-bit MSBs and *k*-bit LSBs) traditional segment cascade DAC, the MSBs are required to have n-bit matching accuracy, while the LSBs are required to have *k*-bit matching accuracy.

A hybrid DAC consisting of a *k*-bit resistor string and an *m*-bit current-steering array (R-I DAC) was first proposed in the IEEE international system-on-chip conference (SOCC) 2015 [14]. The R-I DAC is a kind of segmented DAC, using a resistor string as the LSBs part for low-power consumption, and using a current-steering array as the MSBs part for high speed. So, it provides an alternative for medium-speed, low-power applications. Since it adopts an R-I hybrid segmented architecture, its voltage output is generated by multiplying the resistance with the current. The voltage-output linearity is ensured by the matching in resistor units, together with the matching in current source units. Since the output voltage is obtained by the multiplication of the resistance current, the output mismatch is generated by the mismatches of resistors and of current sources. The multiplication itself is a nonlinear operation that makes the accuracy analysis of R-I DAC more difficult than that of traditional segmented DACs. To get the insight of R-I accuracy, this article aims at analyzing the effect of the R-I DAC on the mismatch of the resistors and the current source.

As discussed before, the static nonlinearity of traditional segmented cascade DACs is a *linear combination* of mismatches of the different segments. In contrast, the static nonlinearity of the R-I DAC is a *nonlinear combination* of mismatches of the resistor-array segment and the current-array segment. As a result, the nonlinearity performance of the R-I DAC is worse than expected if the matching precision is designed with the conventional segment method [14]. As a practical example, although the accuracy is designed for 1-LSB DNL/INL based on a conventional segment design experience, the measured DNL/INL in Reference [14] is 6.38/7.55 LSB. To solve this problem of worse DNL/INL, this article explores the numerical relationship between nonlinearity and matching precision and segmentation for the R-I DAC, and gives equations to guide parameter design.

The major contributions of this article are summarized as follows. (1) We propose a mathematical model to describe the output of the R-I DAC with segmentation and matching precision. To visualize the nonlinearity mechanism of the R-I DAC, we present an algorithm for Monte Carlo simulation to illustrate the effect of segmentation and matching precision on nonlinearity, which shows that nonlinearity gets worse when the segmentation ratio (k/m) increases. (2) We mathematically derived the expressions of DNL/INL and matching precision. In addition, the mechanism of how the segmentation and matching precision affect dynamic performance is also explored. (3) With the derived equations, designers can quickly determine the segmentation strategy and matching precision. We achieve nonlinearity that is smaller than half the least significant bit (LSB) when the matching resolution in bits of resistors and current sources are $k + 4$ and $m + 2k + 2$, respectively. The proposed theory is verified with the measurement results of three test groups with different matching precisions.

The remainder of this paper is organized as follows. Section 2 introduces the architecture of the R-I DAC. Section 3 proposes a mathematical model of the output of the R-I DAC and discusses the variation regularity of the nonlinearity. Section 4 derives the mathematical expression of nonlinearity affected by segmentation and matching precision. Section 5 derives the mathematical expression of the matching precision of a given nonlinearity. Section 6 discusses the dynamic performance. Section 7 designs the prototypes and performs the measurements. Section 8 concludes our work.

2. The Architecture of the R-I Hybrid DAC

Resistor-string digital-to-analog converters (R-DACs) are mostly adopted in low-power, low-speed applications while current-steering DACs (I-DACs) are used in high-power, high-speed applications [2,5,15–18]. To make a trade-off between speed and power, a resistor-string and current-steering-array hybrid DAC (R-I DAC) was proposed [14].

The R-I DAC hybrid architecture is a form of segment technique. An n-bit R-I hybrid DAC is implemented using an m-bit current-steering sub-DAC (I-subDAC) as the most significant bits (MSBs), and a k-bit resistor-string sub-DAC (R-subDAC) as the least significant bits (LSBs). An output operational amplifier (OP) combines MSBs and LSBs. The OP is used in the summer amplifier, which is configured to generate the output voltage. The architecture of the $k + m$ bit resistor-string and current-steering-array hybrid DAC (R-I DAC) with the mismatches between the resistors and currents shown in Figure 1. The mismatch variation of each unit element of the R-subDAC and I-subDAC is modeled as normally distributed random variables, ΔR and ΔI respectively, with a relative variance δ^2 and ξ^2.

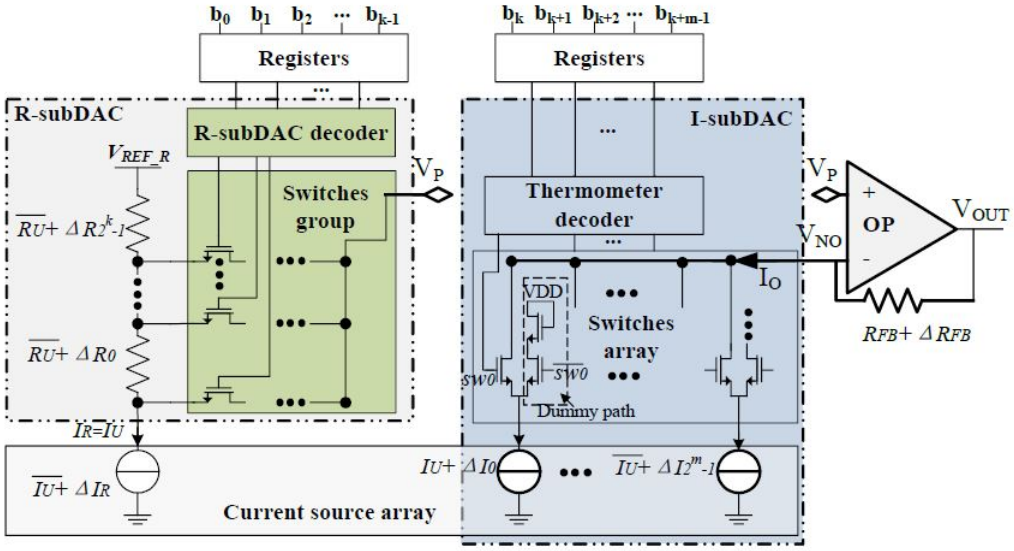


Figure 1. The $k + m$ bits resistor-string and current-steering-array hybrid DAC (R-I DAC) with the resistor's and current's mismatches.

The R-subDAC uses uniform resistors in the series to produce linear node voltages, where $V_{REF\text{-}R}$ is the reference voltage. The linear node voltages are connected to the output node V_P by the multiplexer. The multiplexer consists of the R-subDAC decoder and its switches group. There are three most common types of resistor string multiplexer architecture: two-dimensional address architecture, full decode architecture, and tree decode architecture [19]. They are different in decoder logic complexity, multiplexer resistance, and junction capacitances. The resolution number is a major consideration to select multiplexer schemes. The resolution number of R-subDAC in Reference [14] is six, and the two-dimensional address architecture is adopted. The R-subDAC resolution number of the prototypes in this article is four, and the tree decode architecture is adopted. The current I_R through the resistor string is provided by the matching current source array. The output node V_P of R-subDAC connects to the positive input of the output amplifier.

The I-subDAC adopts a glitchless scheme, which is the unary selection with a thermometer decoder [2]. Since the I-subDAC forms MSBs, which have greater weight than LSBs, the glitches generated by the MSBs affect the output more seriously. Since unary selection has less glitch distortion, as well as better DNL and INL than other architectures such as binary structure or segmentation [2], unary selection with a thermometer decoder is adopted. The unit of the current source array is

implemented by a sooch cascode current mirror to increase the equivalent resistance and reduce the overdrive voltage [2]. In the I-subDAC, dummy paths are used to keep the unity current generators in the saturation region. As a result, the output signal maintains a high response speed and low noise.

The output amplifier OP adopts a two-stage scheme: a folded cascode input stage and a class-AB output stage to achieve a large open-loop gain A_0 [13]. The larger open-loop gain A_0 is crucial for the precision of the R-I DAC output voltage. This is because the OP is used in a summer configuration, basing it on the feedback principle. Due to feedback theory, the actual output is $(V_P + I_O \times R_{FB}) \times A_0/(1 + A_0)$ [13]. So, the error between the actual and ideal output voltage V_{OUT} is $1/(1 + A_0) \times V_{OUT}$. The error voltage is required to be less than 1 LSB, so the A_0 is required to be greater than 2^n, that is, greater than 60.2 dB for a 10-bit DAC. The OP in this article achieves a gain of 83 dB, which is enough for a 13-bit resolution. For a 10-bit R-I DAC, the open-loop gain of the OP in this article is large enough. So, the remaining discussions ignore the error voltage and use the ideal expression for the output voltage.

Assuming the open-loop gain of OP is large enough, Equation (1) is the output expression of the $k + m$ bits R-I DAC, where I_U, I_R, R_{FB}, and R_U are the unity current of the current source array, the current through the resistor string, feedback resistance, and the unit resistance of the resistor string, respectively. They are designed as $I_U \cdot R_{FB} = 2^k \cdot I_R \cdot R_U$, $I_U = I_R$, $R_{FB} = 2^k \cdot R_U$, $n = m + k$. The b_x represents one bit of the digital input code, where a higher x indicates the more significant value of the bit.

$$V_{OUT} = I_U \cdot (2^{m-1}b_{k+m-1} + 2^{m-2}b_{k+m-2} + \ldots + 2b_{k+1} + b_k) \cdot R_{FB} + I_R \cdot R_U \cdot (2^{k-1}b_{k-1} + 2^{k-2}b_{k-2} + \ldots + 2b_1 + b_0) \quad (1)$$

A (6 + 6)-bit R-I DAC prototype was implemented in Reference [14]. To find the reasons for the worse DNL/INL than measured one in Reference [14], we started with numeric simulations for the nonlinearity of the R-I DAC. The following simulations and analysis contain some variables which are summarized in the appendix as variable notations.

3. Variation Regularity of the Nonlinearity Affected by Segmentation and Matching Precision of the R-I DAC

The R-I DAC consists of an R-subDAC and an I-subDAC. To connect them together, two pairs of matching elements are designed. One pair is I_U and I_R; and the other is R_{FB} and R_U, as shown in Figure 1. It is vital to find out the variation regularity of the nonlinearity affected by the segment ratio and matching precision of the R-I DAC.

The variation of each unit of the R-subDAC and I-subDAC are modeled as independent normal random variables, ΔR and ΔI, with a zero expected value and a relative variance δ^2 and ξ^2, respectively. The unit values I_U (R_U) are represented by the mismatch value ΔI_i (ΔR_i) and the expected value $\overline{I_U}$ ($\overline{R_U}$), as shown in Equation (2)

$$I_U = \overline{I_U} + \Delta I_i = \overline{I_U} \cdot (1 + \xi_i) \quad R_U = \overline{R_U} + \Delta R_i = \overline{R_U} \cdot (1 + \delta_i) \quad (2)$$

The controlling codes for the R-subDAC and I-subDAC are represented by BL and BH for a digital input with a decimal value of i, respectively, as shown in Equation (3). In Equation (3), B = floor(A) rounds the elements of A to the nearest integers that are less than or equal to A. M = mod (X, Y) returns the modulus after the division of X by Y.

$$\begin{aligned} BH_i &= 2^{m-1}b_{k+m-1} + 2^{m-2}b_{k+m-2} + \ldots + 2b_{k+1} + b_k = \text{floor}(\text{i}/2^k) \\ BL_i &= 2^{k-1}b_{k-1} + 2^{k-2}b_{k-2} + \ldots + 2b_1 + b_0 = \text{mod}(\text{i}, 2^k) \end{aligned} \quad (3)$$

By using Equations (2) and (3), Equation (1) can be re-written as Equation (4)

$$V_{OUT}(i) = \overline{I_U} \cdot \overline{R_U} \cdot (BH_i \cdot 2^k + BL_i) + \overline{I_U} \cdot \overline{R_U} \cdot (2^k \cdot \sum_{j=1}^{BH_i} \xi_j + BH_i \cdot \sum_{f=1}^{2^k} \delta_f + BL_i \cdot \xi_R + \sum_{j=1}^{BL_i} \delta_j + \xi_R \cdot \sum_{j=1}^{BL_i} \delta_j) \quad (4)$$

The physical implications of the mismatching components in Equation (4) are explained as follows. The ξ_j is a random relative mismatch of a current source unit in the current-steering array, so the component represents the accumulated nonlinearity in the I-subDAC. The δ_f is a random relative mismatch of a resistor unit in the feedback resistor, so the component represents the accumulated nonlinearity in the feedback resistor, which consists of 2^k R_U. The ξ_R is a random relative mismatch of the current source unit biasing the R-subDAC, so BL·ξ_R represents the variation of current that flows through the resistor string. The δ_j is a random relative mismatch of a resistor unit in the resistor divider, so the component represents the accumulated nonlinearity in the R-subDAC. With the expression of nonlinear output in Equation (4), the differential nonlinearity (DNL) and integrated nonlinearity (INL) can be expressed mathematically.

The DNL is the deviation of the difference between two adjacent analog output voltages from the ideal step size. INL describes the deviation between the actual output of DAC and an ideal one. The end-point fit line is used as the ideal one. The DNL and INL can be expressed as Equations (5) and (6), respectively [2]:

$$DNL(i) = \frac{(V_{OUT}(i) - V_{OUT}(i-1))}{\overline{I_U} \cdot \overline{R_U}} - 1 \tag{5}$$

$$INL(i) = \frac{V_{OUT}(i) - \frac{i}{2^{k+m}-1}(V_{OUT}(2^{k+m}-1) - V_{OUT}(0))}{\overline{I_U} \cdot \overline{R_U}} \tag{6}$$

To evaluate the quantity of DNL and INL caused by the mismatch, a Monte Carlo (MC) simulation is performed based on Equations (4)–(6). The algorithm for a MC simulation is described in Figure 2 and as follows. First, $(2^m - 1)$ and one normally distributed unit current source are generated for the current-steering array and the current unit biasing the resistor divider, respectively. The normally distributed unit resistors are generated for the resistor divider and the feedback resistor, respectively. Second, using Equations (4)–(6) with the normally distributed units, we calculate the DNL and INL. Third, the first and second steps are repeated 1000 times.

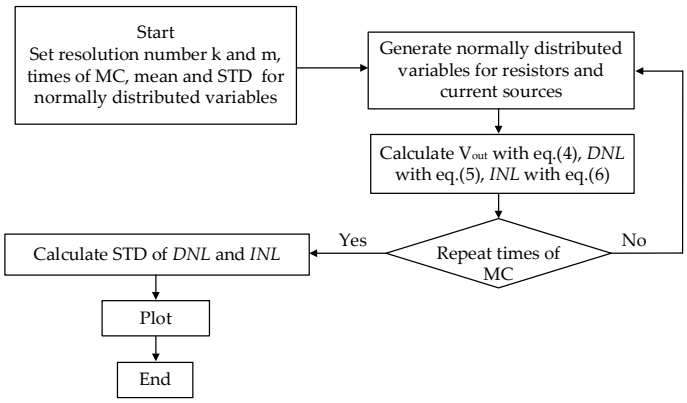


Figure 2. The algorithm of simulation.

Figure 3 shows the calculated standard deviation (STD) of the simulation results. To study the relationship between DNL/INL and the resolution number of k and m, in Figure 3a–c, we set the resistor units and current source units as normally distributed variables with an identical mean of 1 LSB and an identical STD, $\delta = \xi = 0.02$ LSBs. At the same time, Figure 3a–c explores four sets of different values of k and m, (a1) $k = 0$, $m = 10$, (a2) $k = 10$, $m = 0$, (b) $k = 4$, $m = 6$, and (c) $k = 8$, $m = 2$. The results of (a1) and (a2) are the same, so they are plotted in Figure 3a. To study the impact of differences in the mismatch between the two device types (current sources and resistors) on the DNL/INL, Figure 3d explores three sets of different values of δ and ξ when $k = 4$ and $m = 6$. Figure 3 shows four variation phenomena of nonlinearity when the segmentation ratio k/m or (δ, ξ) vary.

(1) For $k = 0$ or $m = 0$, as shown in Figure 3a, the maximum DNL and INL are the smallest compared with the other two sets of k and m. When k or m is zero, the DAC becomes a traditional R-DAC or I-DAC, not an R-I hybrid DAC, so the nonlinearity complies with the characteristic of the monotonic n-bit DAC, that is DNL = σ, INL = $0.5 \cdot \sqrt{2^n} \cdot \sigma$ [13].

(2) For nonzero k and m, as shown in Figure 3b,c, the maximum DNL happens at the transition when k bits of LSBs switch from 1 to 0 and add 1 to the MSBs, and happens $2^m - 1$ times. This phenomenon is caused by the segmented nature of the R-I DAC because the decoders for the R-subDAC and I-subDAC both adopt unary weighty control schemes.

(3) For nonzero k and m, as shown in Figure 3b,c, the maximum DNL and INL increase with the increase of the segmentation ratio k/m. The reason will be discussed in the following section.

(4) For (k, m) = (4, 6) and varying (δ, ξ), as shown in Figure 3d, the mismatch ξ in the current sources has more of an impact on the DNL/INL than the mismatch δ in the resisters. Specifically, the DNL/INL increases a little when (δ, ξ) varies from (0.02, 0.02) to (0.04, 0.02). The DNL/INL almost doubles when (δ, ξ) varies from (0.02, 0.02) to (0.02, 0.04). The reason will be discussed in the following section.

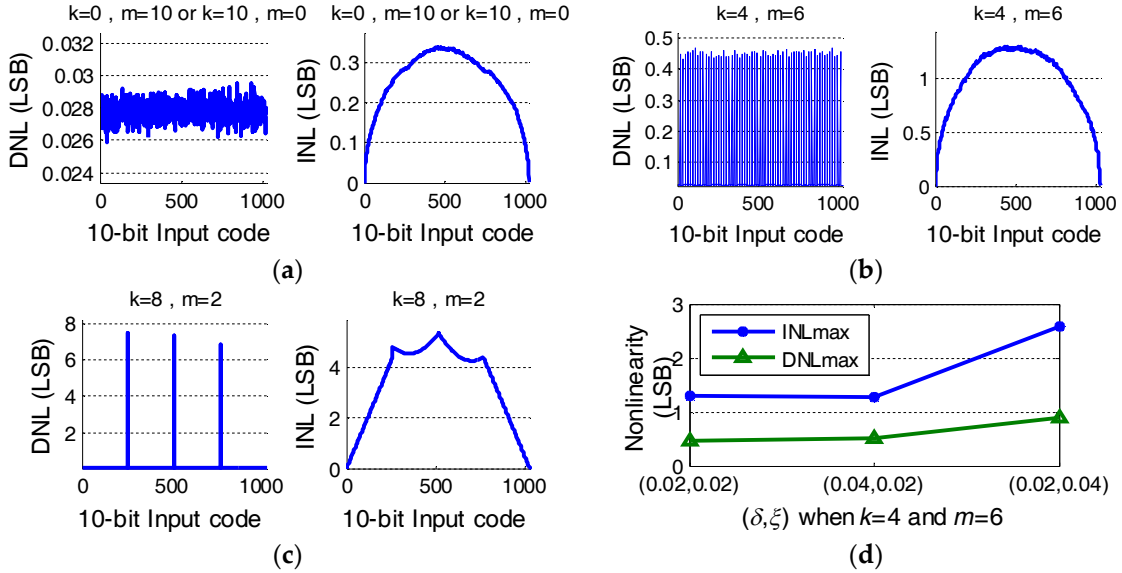


Figure 3. The standard deviation (STD) of differential nonlinearity (DNL) and integrated nonlinearity (INL) of 1000 Monte Carlo MATLAB simulations. (**a**–**c**) show the results when $\delta = \xi = 0.02$ and segmentation *(k/m)* varies: (**a**) $k = 0$, $m = 10$ or $k = 10$, $m = 0$, (**b**) $k = 4$, $m = 6$, (**c**) $k = 8$, $m = 2$. (**d**) is the maximum STD of DNL and INL when $k = 4$, $m = 6$, and (δ, ξ) varies.

4. Theoretical Expressions to Depict the Nonlinearity Affected by Segmentation and the Matching Precision of the R-I DAC

Section 3 studied the nonlinearity mechanism by numeric simulation. In this section, the nonlinearities—DNL/INL—are theoretically derived.

We obtain Equation (7) by neglecting the product of the small variables $\xi_R \cdot \sum_{j=1}^{BL} \delta_j$ in Equation (4)

$$V_{OUT}(i) \approx \overline{I_U} \cdot \overline{R_U} \left[i + (2^k \cdot \sum_{j=1}^{BH_i} \xi_j + BH_i \cdot \sum_{f=1}^{2^k} \delta_f + BL_i \cdot \xi_R + \sum_{j=1}^{BL_i} \delta_j) \right] \quad (7)$$

4.1. DNL Analysis

Combining Equations (5) and (7), we can obtain Equation (8). Due to the segmented nature of the R-I DAC, the worst-case DNL occurs at the transition when k bits of LSBs switch from 1 to 0 and add 1 to the MSBs; for example, changing 00 ... 00_11 ... 11 to 00 ... 01_00 ... 00. By simplifying Equation (8), we can obtain Equation (9):

$$DNL(i) = 2^k \cdot (\sum_{j=1}^{BH_i} \xi_j - \sum_{j=1}^{BH_{i-1}} \xi_j) + (BL_i - BL_{i-1}) \cdot \xi_R + (BH_i - BH_{i-1}) \cdot \sum_{f=1}^{2^k} \delta_f + (\sum_{j=1}^{BL_i} \delta_j - \sum_{j=1}^{BL_{i-1}} \delta_j) \quad (8)$$

$$DNL_{MAX}(i) = 2^k \cdot \xi_{BH_i} - (2^k - 1) \cdot \xi_R + \sum_{f=1}^{2^k} \delta_f - \sum_{j=1}^{2^k-1} \delta_j \quad (9)$$

The DNL analysis aims to find the expected maximum DNL. Based on the extreme value theory, for the samples that are independent and identically distributed random variables, the largest individual from the samples of size S increases with size S [20]. Since samples $X_1, X_2, \ldots, X_S$ are standard normal random variables, the expected value of maximum X_i (i from 1 to S, and $S = 2^m$) is shown as C in Figure 4. Figure 4 is the result of a simulation as follows. First, we set the value of m and generate the 2^m standard normal random samples. Second, we find their maximum and note it as X_i. Third, we repeat the previous two steps 10,000 times to get X_i (i from 1 to 10,000) for size 2^m. Finally, we calculate the mean of X_i (i from 1 to 10,000); then, we note this mean as the expected maximum individual value C for samples of size 2^m.

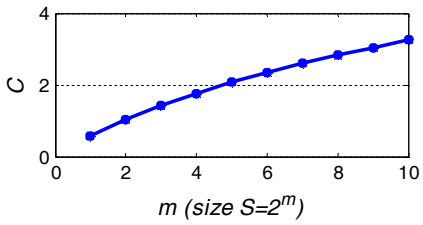


Figure 4. The expected value C of the maximum individual from samples of size $S = 2^m$, in which the samples are standard normal random variables.

Since there are 2^m samples of ξ_{BHi} in DNL_{MAX} for BH_i varying from 1 to 2^m, the expected maximum ξ_{BHi} increases with 2^m. So, the variance of ξ_{BHi} increases with m. Factor C describes the impact of m on the variance of the expected maximum value of ξ_{BHi} [18]. Factor C ranges from 1.02 to 3.25 when m varies from 2 to 10, and C = 2.3 for m = 6, as shown in Figure 4.

We get Equation (10) as the variance estimation of DNL in Equation (9):

$$\sigma^2_{DNL} = \sigma^2_{DNL1} + \sigma^2_{DNL2} = \left[2^{2k} \cdot C^2 \cdot \xi^2 + (2^k - 1)^2 \cdot \xi^2\right] + \left[2^k \cdot \delta^2 + (2^k - 1) \cdot \delta^2\right] \quad (10)$$

In Equation (10), the σ^2_{DNL1} is the variance estimation of DNL generated by the mismatches of the current units; the σ^2_{DNL2} is the variance of DNL generated by the mismatches of the resistor units. The variance of DNL in Equation (10) increasing with the k explains the third variation phenomenon of nonlinearity in Figure 3 by theory. The factor in σ^2_{DNL1} is greater than 2^k times the factor in σ^2_{DNL2}, which indicates that the mismatch in the current array has a much greater effect on DNL than that in the resistors.

4.2. INL Analysis

With the approximation $2^k - 1 \approx 2^k$, $2^m - 1 \approx 2^m$, $2^{m+k} - 1 \approx 2^{m+k}$, the *INL* can be expressed as Equation (11), where INL1, INL2, INL3, and INL4 are the nonlinearities generated by the mismatches

of the current-steering array, the feedback resistor, the resistor-divider biasing current, and the resistor-divider string, respectively.

$$\begin{aligned} &INL(i) = INL1 + INL2 + INL3 + INL4 \\ &= (2^k \cdot \sum_{j=1}^{BH_i} \xi_j - \tfrac{BH_i \cdot 2^k + BL_i}{2^m} \cdot \sum_{j=1}^{2^m} \xi_j) + (BH_i \cdot \sum_{f=1}^{2^k} \delta_f - \tfrac{BH_i \cdot 2^k + BL_i}{2^k} \cdot \sum_{f=1}^{2^k} \delta_f) \\ &+ (BL_i \cdot \xi_R - \tfrac{BH_i \cdot 2^k + BL_i}{2^m} \cdot \xi_R) + (\sum_{j=1}^{BL_i} \delta_j - \tfrac{BH_i \cdot 2^k + BL_i}{2^{k+m}} \cdot \sum_{j=1}^{2^k} \delta_j) \end{aligned} \tag{11}$$

Since the terms of INL are uncorrelated, the variance of INL is derived as Equation (12):

$$\begin{aligned} &\sigma^2{}_{INL} = \sigma^2{}_{INL1} + \sigma^2{}_{INL2} + \sigma^2{}_{INL3} + \sigma^2{}_{INL4} \\ &\begin{cases} \sigma^2{}_{INL1} = \xi^2 \cdot (2^{2k} \cdot BH_i - 2^{2k-m} \cdot {BH_i}^2 + 2^{-m} \cdot {BL_i}^2) \\ \sigma^2{}_{INL2} = \xi^2 \cdot ((1 - 2^{-m})^2 \cdot {BL_i}^2 + 2^{2k-2m} \cdot {BH_i}^2 + 2^{k+1-m} \cdot (2^{-m} - 1) \cdot BH_i \cdot BL_i) \\ \sigma^2{}_{INL3} = \delta^2 \cdot 2^{-k} \cdot {BL_i}^2 \\ \sigma^2{}_{INL4} = \delta^2 \cdot (BL_i + (2^{1-2m} - 2^{1-m}) \cdot BH_i \cdot BL_i + (2^{-(1-m)} - 1) \cdot 2^{1-m-k} \cdot {BL_i}^2 + 2^{k-2m} \cdot {BH_i}^2) \end{cases} \end{aligned} \tag{12}$$

It is too complicated to derive the mathematical expression of the maximum variance of the total INL. However, it can be upper bounded by taking the worst case of each component. The maximum variance of the total INL is less than or equal to the sum of the maximum variance of each INL components, as shown in Equations (12)–(14). The approximation is valid only when an input that almost causes the max of all of the INL components exists. The approximation error is less than 0.3 LSB when $k + m = 10$ and k is smaller than 8, as shown in Figure 4.

$$\sigma^2{}_{INL\_MAX} \leq \sigma^2{}_{INL\_MAX\_SUM} \tag{13}$$

$$\begin{aligned} &\sigma^2{}_{INL\_MAX\_SUM} = \sigma^2{}_{INL1\_MAX} + \sigma^2{}_{INL2\_MAX} + \sigma^2{}_{INL3\_MAX} + \sigma^2{}_{INL4\_MAX} \\ &\begin{cases} \sigma^2{}_{INL1\_MAX} \approx \xi^2 \cdot \left[2^{2k+m-2} + 2^{-m} \cdot (2^k - 1)^2\right] & \sigma^2{}_{INL2\_MAX} \approx \xi^2 \cdot \left[2^{k-m} \cdot (2^m - 1)\right]^2 \\ \sigma^2{}_{INL3\_MAX} = \delta^2 \cdot 2^{-k} \cdot (2^k - 1)^2 & \sigma^2{}_{INL4\_MAX} \approx \delta^2 \cdot 2^{k-2m} \cdot (2^m - 1)^2 \end{cases} \end{aligned} \tag{14}$$

where the maximum of each component in Equation (12) is derived as Equation (14).

Expressions (10) and (14) indicate that the nonlinearity roughly scales up by 2^{2k+m} of ξ^2 and 2^k of δ^2. To directly understand its quantity level, the coefficients of theoretical variance of the differential nonlinearity (DNL) and integrated nonlinearity (INL) are calculated by using Equations (10) and (14), respectively, as shown in Table 1. The coefficient of DNL and INL both reach 100,000 when k increases to 8. The factor of ξ^2 is approximately greater than 2^k times of the factor of δ^2. It indicates that the mismatch in the current array has a much greater effect on the nonlinearity than that in the resistors.

Table 1. The quantity comparison of theoretical variance of DNL and INL for different sets of k and m for a 10-bit R-I DAC.

Variance	k = 2, m = 8	k = 4, m = 6	k = 6, m = 4	k = 8, m = 2
$\sigma^2{}_{DNL}$	$139\xi^2 + 7\delta^2$	$1629\xi^2 + 31\delta^2$	$16735\xi^2 + 127\delta^2$	$134608\xi^2 + 511\delta^2$
$\sigma^2{}_{INL}$	$1040\xi^2 + 6.2\delta^2$	$4348\xi^2 + 30\delta^2$	$20232\xi^2 + 118\delta^2$	$118656\xi^2 + 398\delta^2$

To verify the accuracy of the theoretical deviation, a comparison between the nonlinearity from the numeric simulation and the theoretical prediction equation is made, as shown in Figure 5. The nonlinearity by numeric simulation is obtained from Figure 3. The maximum nonlinearity by theory is calculated by Equations (10) and (14) with ξ and δ both being 0.02 LSBs. In Figure 5, except the INL difference when k is 8 and m is 2, other differences between the simulation and theory are less than 0.5 LSBs. Since the nonlinearity increases as a k exponent of two, a k of less than 6 is recommended for the matching consideration.

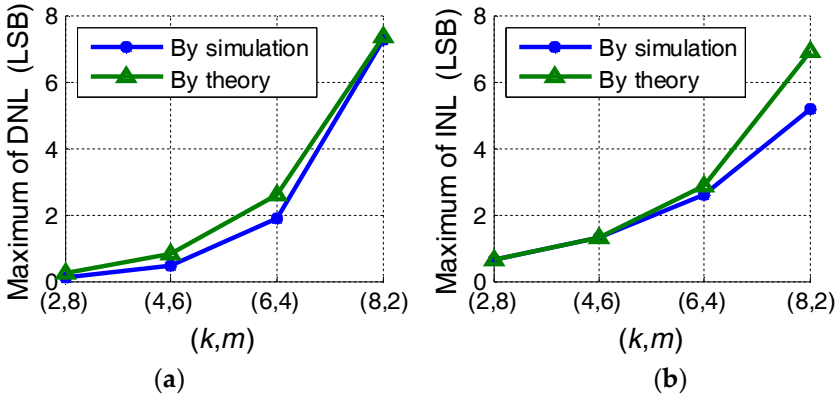


Figure 5. A comparison between the maximum nonlinearity from the numerical simulation and theoretical prediction equation. (**a**) DNL, (**b**) INL.

Previous analyses of DNL and INL gave the mathematical expressions to evaluate the nonlinearity with a specified matching resolution. The nonlinearity variance was approximately scaled up by 2^{2k+m} of ξ^2 and 2^k of δ^2. In the actual design, the mismatching resolution is usually calculated from a given DNL and INL. Section 5 derives the expressions of matching resolution with a given worst nonlinearity.

5. Determination of the Segmentation and Matching Precision of the R-I DAC

The goal of this section is to derive the matching resolution of each mismatched component with a given worst DNL and INL that is smaller than half an LSB. Assuming that each component contributes equally to the nonlinearity, that is:

$$\sigma^2{}_{DNL1} = \sigma^2{}_{DNL2} = \frac{(1/2)^2}{2} \tag{15}$$

$$\sigma^2{}_{INL1\_MAX} = \sigma^2{}_{INL2\_MAX} = \sigma^2{}_{INL3\_MAX} = \sigma^2{}_{INL4\_MAX} = \frac{(1/2)^2}{4} \tag{16}$$

By simplifying Equation (15), we can obtain Equation (17). Similarly, by simplifying Equation (16), we can obtain Equation (18):

$$\xi^2{}_{DNL} = \frac{1}{2^{2k+3} \cdot C^2 + 2^3 \cdot (2^k - 1)^2} \quad \delta^2{}_{DNL} = \frac{1}{2^{k+4} - 8} \tag{17}$$

$$\begin{array}{ll} \xi^2{}_{INL1} = \frac{1}{2^{2k+m+2} + 2^{2k-m+4} \cdot (1-2^{-k})^2} & \xi^2{}_{INL2} = \frac{1}{2^{2k+4} \cdot (1-2^{-m})^2} \\ \delta^2{}_{INL1} = \frac{1}{2^{k+4} \cdot (1-2^{-k})^2} & \delta^2{}_{INL2} = \frac{1}{2^{k+4} \cdot (1-2^{-m})^2} \end{array} \tag{18}$$

Combining Equations (17) and (18), the mismatching resolution can be expressed as Equations (19) and (20):

$$\xi^2 = \min(\xi^2{}_{DNL1}, \xi^2{}_{INL1}) = \frac{1}{2^{2k+m+2} + 2^{2k-m+4} \cdot (1-2^{-k})^2}, \text{for } (m \in [2,10], k \in [1,10]) \tag{19}$$

$$\begin{aligned} \delta^2 &= \min(\delta^2{}_{DNL1}, \delta^2{}_{INL1}, \delta^2{}_{INL2}) \\ &= \begin{cases} \frac{1}{2^{k+4}-8}, \text{for } (m \in [2, k+1], k \in [1,10]) \\ \frac{1}{2^{k+4} \cdot (1-2^{-m})^2}, \text{for } (m \in [k+2, 10], k \in [1,10]) \end{cases} \end{aligned} \tag{20}$$

The expressions of matching resolution are obtained by ignoring some insignificant factors, such as the product of small variables $\xi_R \cdot \sum_{j=1}^{BL} \delta_j$ in Equation (7). To verify its prediction accuracy of nonlinearity,

the Monte Carlo simulation is performed in a similar way to that in Figure 3. The simulations are carried out by MATLAB using the normal random distribution for the unit variation of I-subDAC and R-subDAC. The variation has zero mean and a relative variance of ξ^2 and δ^2, respectively, as defined by equations (19) and (20). By repeating the previous Monte Carlo simulation 100,000 times, we obtain the standard deviation (STD) of the DNL_max and INL for different combinations of k and m. All of the standard deviations are calculated after 100,000 Monte Carlo runs except $k = 8$ and $m = 8$, where the number of runs is 1000. The STD of nonlinearity varies between 0.18–0.42 LSB, as shown in Figure 6. For all of the combinations of k and m, the maximum of STD nonlinearity is smaller than 0.5 LSB. This conforms to our matching resolution analysis.

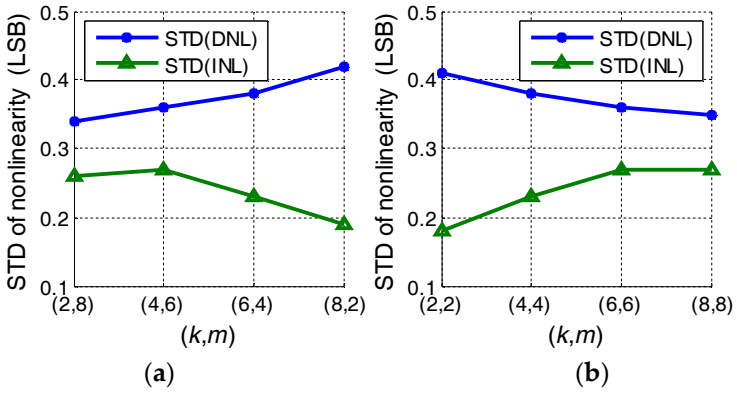


Figure 6. The predicted standard deviation (STD) of DNL and INL for different combinations of k and m for 100,000 Monte Carlo runs, using the matching resolution defined by Equations (19) and (20). (**a**) The ($k + m = 10$) bit resolution of the R-I DAC. (**b**) $k = m$ and K + M ranging from 4 to 16.

For the convenience of the description, the $n(\sigma^2)$ is defined as the matching resolution in bits, as a function of variance σ^2 of matching precision, $n(\sigma^2) = \log_2(1/\sigma^2)$. Using Equations (19) and (20), we can plot Figure 7.

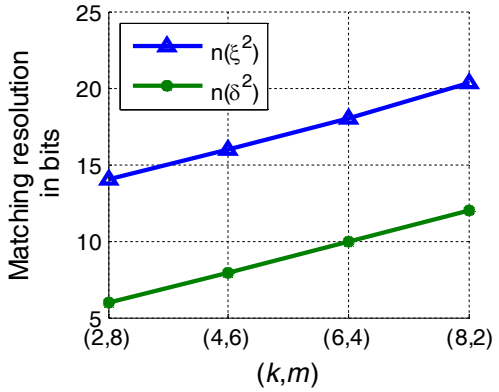


Figure 7. The matching resolution in bits for the different combinations of k and m for $n = k + m = 10$ by assuming that each component contributes equally to the nonlinearity.

When $k + m = 10$, we obtain $n(\xi^2) = 2k + m + 2 = n + k + 2$ and $n(\delta^2) = k + 4$ approximately from Equations (19) and (20) and Figure 7, by assuming an equal contribution of the resistor and current source mismatching to nonlinearity. The expressions provide a criterion to design the mismatching precision of the I-subDAC and R-subDAC. The k is very influential on the matching resolution in bits for the I-subDAC. Since $n(\xi^2)$ is proportional to $2k$, $n(\xi^2)$ increases greatly when k increases. To avoid too stringent matching requirements, it is recommended that k is less than 6.

6. Dynamic Performance Affected by the Segmentation and Matching Precision of R-I DAC

In previous sections, we discussed the relationship between the static nonlinearity DNL/INL and the segmentation, as well as the matching precision of the R-I DAC. The focus of this section is on how the segmentation and matching precision of the R-I DAC affects the dynamic nonlinearity.

One of the major factors in the dynamic performance is the static nonlinearities of DNL/INL. Besides the static nonlinearity, the other factors are glitches, timing mismatch errors, and some high-frequency parasitic parameters [21]. At a low frequency, the dynamic performance is mainly determined by the static nonlinearity, which does not scale with frequency. With the frequency increases, the glitches, timing mismatch errors, and some high-frequency parasitic parameters become more visible and dominant. So, the dynamic performance gets worse. Therefore, the static nonlinearity set an upper limit for the dynamic nonlinearity.

To evaluate the dynamic performance affected by segmentation and matching precision, a Monte Carlo simulation is performed in a similar way to that in Figure 3. Firstly, the matching accuracy of the resistor units and current-source units is set; then, the R-I DAC's output is calculated by Equation (4). This output is used to generate a sine-wave, and its spurious-free dynamic range (SFDR) and the effective number of bits (ENOB) are calculated. At last, the simulations are repeated 1000 times, and the SFDR and ENOB are plotted using a "boxplot" [22]. Boxplot: on each box, the central mark is the median, the edges of the box are the 25th and 75th percentiles, and the highest and lowest whiskers correspond to approximately $\pm 2.7\sigma$ and 99.3 coverage if the data are normally distributed. The results are shown in Figure 8.

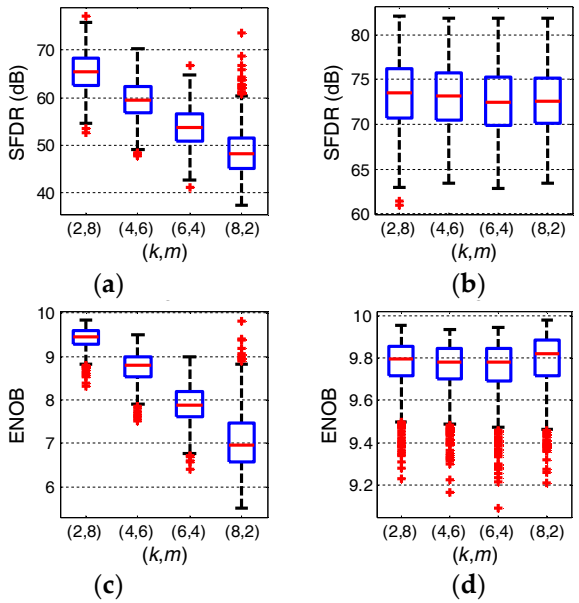


Figure 8. With the different matching accuracy among the resistor units and among the current-source units, the boxplot of spurious-free dynamic range (SFDR) (**a**,**b**) and the effective number of bits (ENOB) (**c**,**d**) of a 1000 Monte Carlo MATLAB simulations when k and m vary. In (**a**,**c**), $\delta = \xi = 0.02$. In (**b**,**d**), $\delta = \sqrt{2^{k+4}}$ and $\xi = \sqrt{2^{2k+m+2}}$, respectively.

In Figure 8a,c, the matching accuracy of the resistor units (δ) and current-source units (ξ) are set as constant values, both at 0.02. As a result, their SFDR and ENOB get worse, which is similar to the DNL/INL in Figure 3, when k increases and m decreases. In Figure 8a,c, the SFDR decreases from 65 dB to 48 dB, and the ENOB decreases from 9.5 bit to 7 bit, when k increases from 2 to 8 and m decreases from 8 to 2. The trend of the dynamic and static performance conform to the dynamic performance being limited by the static nonlinearity.

In contrast, SFDR and ENOB in Figure 8b,d remain constant, closing to the best theoretical achievable value with an increasing k and decreasing m. The SFDR is around 73 dB, and the ENOB is around 9.8 bits. The main reason is that in Figure 8b,d, the matching accuracy of resistor units and current-source units are set respectively as $\sqrt{2^{k+4}}$ and $\sqrt{2^{2k+m+2}}$. They are derived in Section 5, with a design goal of DNL/INL smaller than half an LSB. From Figure 8b,d, we can reach the conclusion that, with the proposed theoretical matching accuracy, the designed R-I DAC can not only achieve the static nonlinearity smaller than half an LSB, it can also assure the upper limit of the dynamic performance by being close to the best theoretically achievable value.

7. Implementation and Measurement for Verification

In the previous sections, simulations and theoretical derivation were used to analyze the nonlinearity affected by segmentation and mismatches. In this section, we discuss the design of the test chips using the proposed methodology.

Three test groups of prototypes of 10-bit (k = 4, m = 6) R-I DACs were implemented using the 180-nm standard complementary metal–oxide–semiconductor (CMOS) technology. These test chips groups only differed on the matching precision among the resistors and current sources in order to highlight the relationship between the matching precision and nonlinearity. Each test group had seven samples, and a total of 21 samples were under test.

To attenuate the gradient-mismatch effects on nonlinearity, the common centroid and Q random layout skills were used in the resistors matching and current-sources matching, respectively, as shown in Figure 9 [5,23]. Similar to Reference [5], Q is referred to as one unit in every quadrant (A/B/C/D in Figure 9b), which altogether composed one current source in the layout. For example, current source 1 implemented by A1, B1, C1, and D1 in parallel. DM is the dummy unit. RSi and RFi are the unary resistor of the resistor-string (R-subDAC) and feedback resistor (R_{FB}), respectively, where i is from 1 to 16. The "random" is not in the column or row sequence that was optimized to compensate for the quadratic-like residual errors.

In addition to the common-centroid layout, the sizing is another implementation consideration for matching precision [6,23]. Sizing the matching transistors (resistors) is a process of determining the value and the matching precision of the current (resistance). The value of the current (resistance) is a function of the width-to-length ratio (W/L), and the matching precision of the current (resistance) is a function of unary device size (W*L). So, the unary device shape, that is, the width and length, are determined by the value and the matching precision of the current (resistance). For resistors, the matching precision δ is provided by the proposed Equation (20), and the resistor size W*L is determined by the function W*L = a_{ref}/δ^2, where a_{ref} is the reference resistor area provided by the foundry document for a 1% target precision [14]. The resistor length-to-width ratio is L/W = R/R_S, where R is the designed resistance and R_S is the sheet resistance. For the current source transistor, the matching precision ξ is provided by the proposed Equation (19), and the transistor size W*L is determined by the function $W * L = [A_\beta^2 + \frac{4A_{VT}^2}{(V_{GS}-V_T)^2}]/2\xi^2$, where V_{GS} and V_T are the gate-source voltage and the threshold voltage of a metal-oxide-semiconductor (MOS) transistor, respectively, and the mismatch of the technology parameters ${A_{VT}}^2$ and ${A_\beta}^2$ are 22 mV^2 * μm^2 and 0.04%* μm^2 respectively, from the foundry document [6,14]. The transistor width to the length ratio is $\frac{W}{L} = \frac{2I}{\mu_n C_{ox}(V_{GS}-V_T)^2}$, where I and $\mu_n C_{ox}$ are the designed unary current and the I-V coefficient, respectively. The required resistor and transistor sizes of the R-I DAC are larger than that of the conventional segmented DAC architectures, because the requirement of the matching in the R-I DAC is more stringent.

DM	DM	DM	DM
DM	RF1B	RS1B	DM
DM	RF2B	RS2B	DM
DM	RF3B	RS3B	DM
DM	···	···	DM
DM	**RF*i*B**	RS*i*B	DM
DM	···	···	DM
DM	RF15B	RS15B	DM
DM	RF16B	RS16B	DM
DM	RS16A	RF16A	DM
DM	RS15A	RF15A	DM
DM	···	···	DM
DM	RS*i*A	**RF*i*A**	DM
DM	···	···	DM
DM	RS3A	RF3A	DM
DM	RS2A	RF2A	DM
DM	RS1A	RF1A	DM
DM	DM	DM	DM

(**a**)

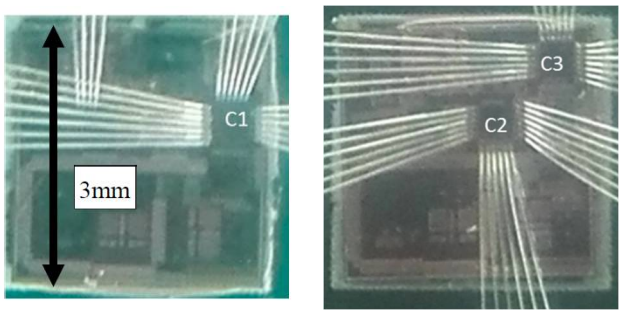
DM	DM	DM	DM	DM	DM	DM	DM	DM	DM	DM	DM	DM	DM	DM	DM	DM	DM	DM
DM	A55	A40	A23	A62	A38	A4	A56	A33	D33	D56	D4	D38	D62	D23	D40	D55	DM	
DM	A14	A12	A51	A8	A34	A46	A24	A64	D64	D24	D46	D34	D8	D51	D12	D14	DM	
DM	A37	A29	**A1**	A19	A31	A11	A21	A36	D36	D21	D11	D31	D19	**D1**	D29	D37	DM	
DM	A6	A18	A50	A16	A61	A5	A42	A26	D26	D42	D5	D61	D16	D50	D18	D6	DM	
DM	A32	A43	A10	A53	A41	A15	A63	A52	D52	D63	D15	D41	D53	D10	D43	D32	DM	
DM	A54	A22	A45	A3	A58	A47	A20	A9	D9	D20	D47	D58	D3	D45	D22	D54	DM	
DM	A27	A13	A48	A59	A7	A60	A44	A30	D30	D44	D60	D7	D59	D48	D13	D27	DM	
DM	A49	A35	A25	A39	A28	A17	A57	A2	D2	D57	D17	D28	D39	D25	D35	D49	DM	
DM	B49	B35	B25	B39	B28	B17	B57	B2	C2	C57	C17	C28	C39	C25	C35	C49	DM	
DM	B27	B13	B48	B59	B7	B60	B44	B30	C30	C44	C60	C7	C59	C48	C13	C27	DM	
DM	B54	B22	B45	B3	B58	B47	B20	B9	C9	C20	C47	C58	C3	C45	C22	C54	DM	
DM	B32	B43	B10	B53	B41	B15	B63	B52	C52	C63	C15	C41	C53	C10	C43	C32	DM	
DM	B6	B18	B50	B16	B61	B5	B42	B26	C26	C42	C5	C61	C16	C50	C18	C6	DM	
DM	B37	B29	**B1**	B19	B31	B11	B21	B36	C36	C21	C11	C31	C19	**C1**	C29	C37	DM	
DM	B14	B12	B51	B8	B34	B46	B24	B64	C64	C24	C46	C34	C8	C51	C12	C14	DM	
DM	B55	B40	B23	B62	B38	B4	B56	B33	C33	C56	C4	C38	C62	C23	C40	C55	DM	
DM	DM	DM	DM	DM	DM	DM	DM	DM	DM	DM	DM	DM	DM	DM	DM	DM	DM	DM

(**b**)

Figure 9. The common-centroid layout of (**a**) matching resistors, unary resistor RS*i* (RF*i*) implemented as two units in red—RS*i*A (RF*i*A), and RS*i*B (RF*i*B)—in series, where the background color of RS*i*A (RS*i*B) and RF*i*A (RF*i*B) are gray and yellow, respectively, and (**b**) matching the current sources, unary current sources implemented as four units (A, B, C, and D with background color of yellow, gray, orange and green, respectively) in parallel. For example, current source 1 consists of A1, B1, C1 and D1 in red. DM is the dummy unit.

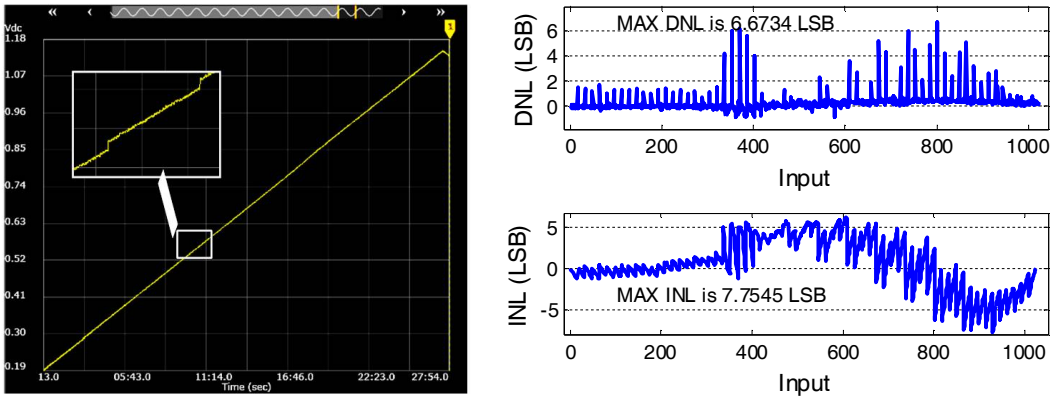
The resistors were implemented by the high-sheet-resistance poly resistor, which was 1000 ohm/square. The resistance of the unit resistor is R_U = 200 Ω. The matching precision due to the resistor size follows the guidelines of Reference [23]. The current source was implemented as a two-transistor cascode type. The matching precision due to the size of current source was determined with an INL yield model for the unary selection current-steering array [10,24]. The current of the unit current source was 5 μA. The overdrive voltage V_{GS}-V_T was set to 300 mV to compromise the current matching precision and transistor size [13–15]. The different matching precisions due to the size of the resistor (res-size) and the current source (cur-size) are listed in Table 2. The OP with an open-loop gain of 83 dB was adopted in our design. With such a large open-loop gain, the OP does not affect the precision and nonlinearity according to the analysis in Section 2. The test chips of group 1 and group 2 both used the large cur-size. Their measured nonlinearities are much better than the test group 3, in which a small cur-size was adopted. The chip bonding photos are shown in Figure 10.

To test the proposed R-I DAC, the input data sequence was generated by a field-programmable gate array (FPGA) [3,24]. The output voltage was measured by a $6\frac{1}{2}$-digit performance digital multimeter (DMM) Keysight-34461A. The output of test group 3, with an input of a full swing triangle wave, is shown in Figure 11. In Figure 11, the x-axis is time was proportional to the input, and the y-axis was the measured voltage. The magnified part shows the nonlinearity caused by the mismatching of the current-source transistors in test group 3.



(**a**) (**b**)

Figure 10. The chip-bonding photos of (**a**) test group 1; (**b**) test group 2; and test group 3.



(**a**) (**b**)

Figure 11. (**a**) The measured output of test group 3 with an input of a full swing triangle wave. (**b**) The static nonlinearity DNL/INL of the measured output versus the digital input, a result of Figure 11a.

The output voltage noise spectra density is measured by a spectrum analyzer (Rohde&Schwarz-FSV7), as shown in Figure 12 [25].

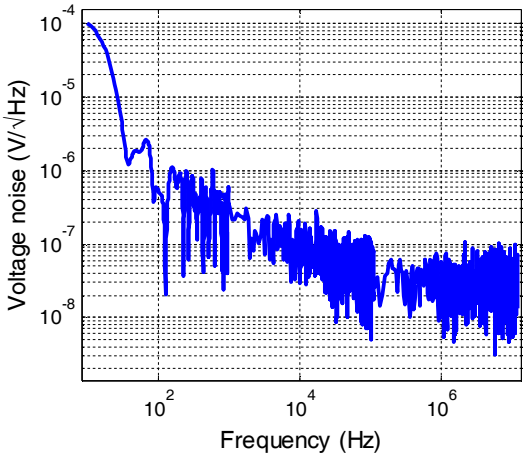


Figure 12. Output voltage noise spectra density measured results.

Table 2. The different sizes of resistors and current-source results in different measured nonlinearities.

Test Chip Group	Size of Matching (Multiplier × W × L, the Unit is μm × μm)	Designed Precision (Absolute Voltage, Relative Precision Variance)	Measured Precision (Absolute Voltage, Relative Precision Variance)	Measured Nonlinearity (DNL and INL in LSB, Relative Precision)
Test group 1 (large res-size, large cur-size)	Resistor size (2 × 2 × 29.78) Current-source transistor size (4 × 4.42 × 50)	62.5 μV, $1/2^{8}$ 28 μV, $1/2^{15.1}$	200 μV, $1/2^{6.3}$ 200 μV, $1/2^{12.3}$	1.5 and 2.3, $1/2^{9.4}$ and $1/2^{8.8}$
Test group 2 (small res-size, large cur-size)	Resistor size (2 × 0.8 × 11.605) Current-source transistor size (4 × 4.42 × 50)	250 μV, $1/2^{6}$ 28 μV, $1/2^{15.1}$	540 μV, $1/2^{4.9}$ 200 μV, $1/2^{12.3}$	1.7 and 1.7, $1/2^{9.2}$ and $1/2^{9.2}$
Test group 3 (large res-size, small cur-size)	Resistor size (2 × 2 × 29.78) Current-source transistor size (4 × 0.375 × 4.245)	62.5 μV, $1/2^{8}$ 16 mV, $1/2^{6}$	200 μV, $1/2^{6.3}$ 9 mV, $1/2^{6.8}$	6.7 and 7.7, $1/2^{7.2}$ and $1/2^{7.0}$

The DMM measurement precision is 3 μV with a 1.2-V input range. The measured low-frequency peak-to-peak noise voltage is 200 μV. This measurement of the noise floor determines the minimum measured absolute voltage, which limits the measured precision in Table 2. Since the measurement precision is 200 μV, it cannot measure the voltage below 200 μV. Therefore, for the actual measured voltage possibly less than 200 μV, we use 200 μV (worst-case value) to represent the measured value, which causes some error, but is acceptable for estimation.

Using the measured relative precision variances in Table 2 and Equations (10) and (14), we can calculate the STD of nonlinearity. The calculated nonlinearity and the measured nonlinearity are plotted, as shown in Figure 13. The measured standard deviation of nonlinearity is less than two times that of the theoretical one, as shown in Figure 13. Since the nonlinearity is modeled as a normal probability distribution, the probability of one sample being less than two times the standard deviation is 95% [26]. Therefore, the difference between the measured results and the theoretical one falls within 95% of the normal distribution curve. In other words, our measured results match the theoretical ones in the statistical sense [26].

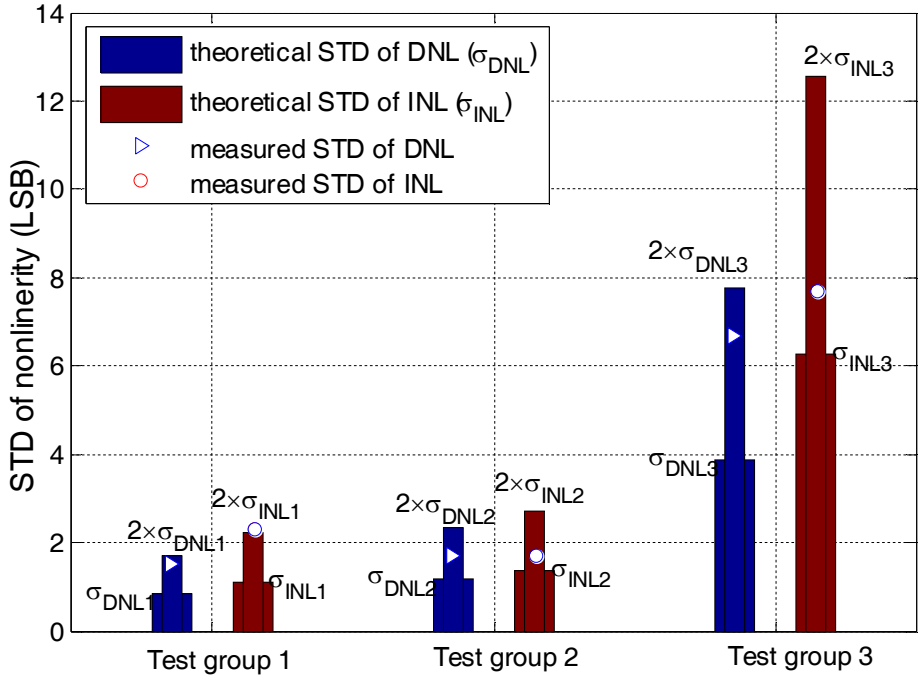


Figure 13. The comparison between the theoretical calculated nonlinearity and the measured nonlinearity. The theoretical calculation of nonlinearity is computed using the measured relative precision variances in Table 2 and Equations (10) and (14).

There is a discrepancy between the proposed theoretical STD of DNL/INL and the measured DNL/INL. The calculated STD of DNL/INL should be worse than the measured DNL/INL because, for test group 1 in Table 2, the measured precision of the resistors and current source are both worse than designed. However, the calculated STD of DNL/INL is better than the measured DNL/INL although their differences are insignificant, shown in Figure 13. The first reason is that if the matching resolution in bits $n(\xi^2)$ and $n(\delta^2)$ are large enough, the variations of $n(\xi^2)$ and $n(\delta^2)$ have little impact on the DNL/INL. For example, when $n(\delta^2)$ is 6.3 and $n(\xi^2)$ varies from 12 to 14 and to 16, the DNL/INL varies from 0.89/1.2 to 0.70/0.80 and to 0.64/0.66. Therefore, the calculated STD of DNL/INL is not much worse. The second reason is that the measured DNL/INL is subject to the interference of the test environment, such as the power supply ripple and drifts of the reference voltage or current, especially when 1 LSB voltage is as small as 1 mV. So, the measured DNL/INL is slightly worse than expected. Therefore, the discrepancy is reasonable.

The measured dynamic performances are shown in Figure 14. The Rohde and Schwarz-FSV7 signal and spectrum analyzer measures the spectrum of the DAC output. The peak-to-peak voltage of the DAC sine-wave output is 1 V under a 1.35-V supply voltage. To avoid an overload effect on the spectrum analyzer, the DAC output is connected with the input of a spectrum analyzer through a series 4.7 kΩ resistor. Figure 14 is measured at a medium clock frequency and with a small input tone to stress the effect of segmentation and matching precision on the nonlinearity. Since the R-I DAC is designed for low-power applications, a low-power output operational amplifier (OP) is adopted, which limits the R-I DAC dynamic performance at high frequency. If the high-frequency and large input tones are used in the measurement, the poor high-frequency dynamic performance of the output OP overrides the effect of segmentation and matching precision on the nonlinearity. Therefore, the performance is measured at a medium clock frequency and with a small input tone to stress the focus of this article. Figure 14a shows the spectrum of the test group 1 with an input of a 40.88-kHz sine-wave at a clock frequency of 3.125 MHz. Figure 14b shows the dynamic performance, including the spurious-free dynamic range (SFDR), the total harmonic distortion (THD), the signal-to-noise ratio (SNR), and the effective number of bits (ENOB), of test groups 1–3. The SFDR of test groups 1–3 are around 65 dB, and the THD is around 60 dB. The differences of SFDR among test groups 1–3 are not obvious. The prime reason is the dynamic limitation of the low-power output of OP, which sets an upper limit of SFDR. Even though there is a limitation in OP, the THD of test group 3 is 2 dB less than that of test group 1, following the trend predicted in Section 6. The SNR and ENOB in Figure 14 decrease more obviously when the mismatch increases, as shown in Figure 13. The ENOB of test group 1 is 8.5 bits, which is 1.3 bits less than the one theoretically predicted by Figure 8d. It is reasonable because as a general rule, there is a 1-bit degradation in the measurement compared with the theoretical one [27].

In addition to nonlinearity, the sizing and power constraints also impact the choice of segmentation. When k increases and m decreases by 1 bit, the total resistor size quadruples, because both the resistor amount and the unary resistor size doubles. Meanwhile, the total size of the matching current source array stays the same, because the current source amount halves and the unary current source transistor size doubles. As a result, the total size of the R-I DAC increases dramatically if k is large. In addition, the large size increases the parasitics and degrades the speed. So, the sizing constraint limits the choice of a large k. In contrast, the power of the I-subDAC halves when k increases and m decreases by 1 bit, but the power reduction of the I-subDAC becomes unnecessary if the I-subDAC consumes a minority of the total power. The I-subDAC consumes less than a third of the total power in the implemented 10-bit (k = 4, m = 6) prototypes. So, further increasing k makes little contribution to the power reduction. In conclusion, the choice of segmentation should be compromised among the matching precision (for nonlinearity), total size, speed, and power, and a large k is not recommended.

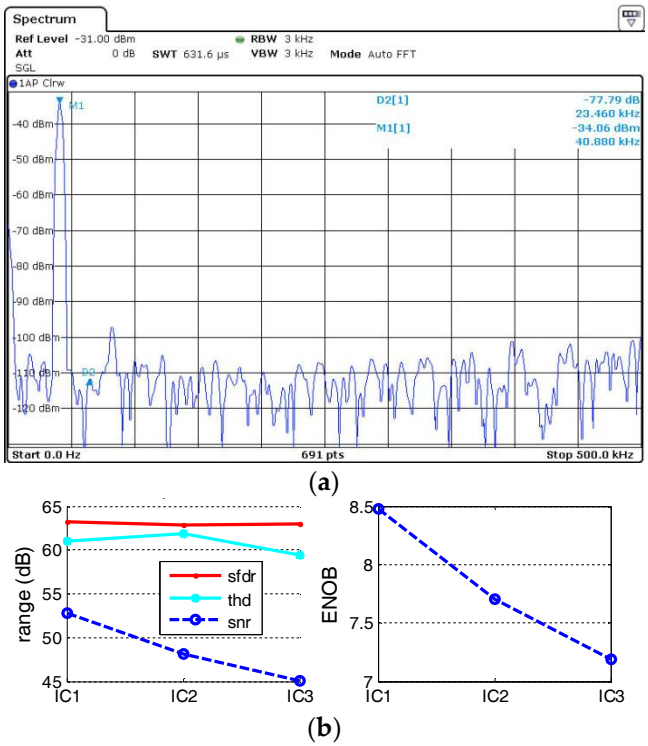


Figure 14. (**a**) The measured spectrum of test group 1, with an input of a 40.88 kHz sine-wave at a clock frequency of 3.125 MHz. (**b**) The measured dynamic performance including spurious-free dynamic range (SFDR), the total harmonic distortion (THD), the signal-to-noise ratio (SNR), and the effective number of bits (ENOB) of test groups 1–3 under the identical test environment, as in Figure 11a.

Setting the values of the unary current and the unary resistor should compromise between the matching precision, size, and power. Lowering the unary current reduces the total power, but may result in a poor match, because the value and the matching precision together determine the unary device shape, that is, the width and length. The shape should follow the reliability guide of the layout to achieve the designed matching precision. In addition, there is a relationship between the current and resistor, as higher currents require lower resistors for the same output voltage. Therefore, after the matching precision specification is determined, the values of the unary current and the unary resistor should be simultaneously designed under the guidance of device sizing method and the layout reliability.

To verify the proposed methodology, three test groups differing on the matching precision among the resistors and current sources have been fabricated and tested. The measured results (Table 2 and Figure 13) are compared with the theoretical results for static nonlinearity (Equations (10) and (14)) and matching precision (Equations (19) and (20)). The verification supports the proposed prediction of nonlinearity by segmentation and matching precision. First, the resolution number of resistor (k) has more influence on the nonlinearity than the resolution number of current steering (m). Second, the nonlinearity gets worse when the segmentation ratio (k/m) increases. Finally, setting the matching resolution in bits of the resistors and current sources as $k + 4$ and $m + 2k + 2$, respectively, will obtain a DNL/INL that is smaller than half the LSBs.

8. Conclusions

Since the output of the R-I DAC is generated by the multiplication of the resistance and the current, the total mismatch gets amplified in a nonlinear way, which makes the accuracy analysis of the R-I DAC not as easy as that of conventional DACs. So, this article is motivated to interpret the numerical relationship between the nonlinearity and matching precision for the R-I DAC. In this

article, we proposed a mathematical model that focused on the output and mismatches of the R-I DAC. To visualize the nonlinearity mechanism of the R-I DAC, we presented a simulation algorithm and illustrated the variation regularity of the nonlinearity. The regularity showed that the nonlinearity gets worse when the segmentation ratio (k/m) increases, and that the resolution number of resistor (k) has more influence on nonlinearity than the resolution number of current steering (m). In addition, we derived the theoretical expressions for static nonlinearity and matching precision. The numerical simulation and theoretical derivation concluded that the nonlinearity variance is proportional to the sum of $2^k\delta^2$ and $2^{n+k}\xi^2$. For a 10-bit R-I DAC, it is recommended that k is less than 6 to avoid matching requirements that are too stringent. When nonlinearity is required to be smaller than half an LSB, the matching resolution in bits of resistors and current sources are $k + 4$ and $m + 2k + 2$, respectively. The proposed theory is supported by the measured results of static and dynamic performance.

Author Contributions: Q.H. and F.Y. contributed to the main idea of this article; Q.H. performed the simulations, theoretical deviations, experiments and data analysis; Q.H. wrote the paper. F.Y. provided the funding, supervised the research, and revised the paper.

Acknowledgments: This work was supported in part by National key R&D plan (Grant number 2016YFC0105002 and 61674162), Shenzhen Key Lab for RF Integrated Circuits, Shenzhen Shared Technology Service Center for Internet of Things, Guangdong government funds (Grant numbers 2013S046 and 2015B010104005), Shenzhen government funds (Grant numbers JCYJ20160331192843950), and Shenzhen Peacock Plan.

Conflicts of Interest: The authors declare no conflict of interest.

Appendix A Variable Notations

Symbol	Definition
k	A k-bit resistor-string sub-DAC as LSBs
m	An m-bit current-steering sub-DAC as MSBs
n	An n-bit R-I hybrid DAC, $n = k + m$
I_U, and I_R	The unity current of the current source array, and the current through resistor-string, they are design to match, $I_U = I_R$.
R_{FB}, and R_U	Feedback resistance, and the unit resistance of resistor string, they are design to match, $R_{FB} = 2^k \cdot R_U$.
ΔI_i (ΔR_i), $\overline{I_U}$ ($\overline{R_U}$)	A random absolute mismatch value ΔI_i (ΔR_i) $\overline{I_U} = I_U - \Delta I_i$ ($\overline{R_U} = R_U - \Delta R_i$) Expected value
σ, ξ (δ)	The σ defines a general relative mismatch. The $\xi(\delta)$ is a specific random relative mismatch $\xi_i = \frac{\Delta I_i}{I_U}$ ($\delta_i = \frac{\Delta R_i}{R_U}$)
i	A digital input for R-I DAC with a decimal value
BL_i and BH_i	The digital input codes for R-sub DAC and I-sub DAC, respectively$BH_i = \text{floor}(\text{i}/2^k)$, $BL_i = \text{mod}(\text{i}, 2^k)B = \text{floor}(A)$ rounds the elements of A to the nearest integers less than or equal to A. $M = \text{mod}(X, Y)$ returns the modulus after division of X by Y.
b_x	The b_x represents one bit of the digital input code, where a bigger x indicates the more significant value of the bit.
$n(\sigma^2)$	The matching precision in bits, as a function of variance σ^2 of matching precision, $n(\sigma^2) = \log_2(1/\sigma^2)$.

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