Design, Simulation and Hardware Implementation of Shunt Hybrid Compensator Using Synchronous Rotating Reference Frame (SRRF)-Based Control Technique

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Abstract: This paper deals with the design, simulation, and implementation of shunt hybrid compensator to maintain the power quality in three-phase distribution networks feeding different types balanced and unbalanced nonlinear loads. The configuration of the compensator consists of a selective harmonic elimination passive filter, a series-connected conventional six-pulse IGBT inverter, acting as the active filter terminated with a DC link capacitor. The theory and modelling of the compensator based on current harmonic components at the load end and their decomposition in *d-q* axis frame of reference are utilized in the reference current generation algorithm. Accordingly, the source current waveform is made to follow the reference current waveform using a high-frequency, carrier-based controller. Further, this inner current control loop is supported by a slower outer voltage control loop for sustaining desirable DC link voltage. Performance of the compensator is evaluated through MATLAB simulation covering different types of loads and reduction of harmonic currents and THD at the supply side along with excellent regulation of DC link voltage are confirmed. The performance of a hybrid compensator designed and fabricated using the above principles is evaluated and corroborated with the simulation results.

Keywords: harmonics; hybrid power filter; active power filter; power quality; total harmonic distortion

1. Introduction

One major area of research that has gained attention in recent times is maintaining power quality of distribution systems. The power quality issues arise due to the widespread usage of processed power in industrial applications and commercial/domestic applications [1–3]. For example, variable speed drives are implemented through power modulators which consist of high-power controlled/uncontrolled rectifiers feeding variable voltage and variable frequency multiphase inverters. Similarly, commercial power consumption is characterised by appliances like computers, photocopiers, and fax machines, along with fluorescent and CFL lamps. All the above represent nonlinear loads, resulting in lower supply-side power factor and waveform distortion, indicated by harmonic components in voltage and current. The adverse effect of harmonics includes heating and extra losses, saturation and malfunctioning of distribution transformers, interference with communication signals, damages to consumer utilities, and in extreme cases, the failure of supply-side equipment [4].

The initial steps towards mitigation of the above problems were focused on the low power factor at the supply side only, whereby a passive power filter (PPF) connected in shunt compensates for the lagging reactive current, which was extended with selective harmonic elimination. The disadvantage of this approach is insensitivity with load current changes and fluctuations in supply-side voltage.

The filter performance also depends on the load power factor, which may be variable. For example, in [5], the load is a motor that can work at different conditions. As a means of overcoming these problems, various active compensator topologies comprising of series and shunt elements have been proposed which have gained wide acceptance. However, some of the disadvantages, like high initial and operating cost due to the use of high-rating semiconductors and also the need for maintaining a high DC link voltage, have limited the application of pure shunt active power filter in medium- and high-power installations [6,7]. As a result, the stage was set for development of shunt hybrid power filters (HPFs), which represent a judicious combination of both passive and active power filters (APFs). The various hybrid compensator configurations are: (i) series active power filter and shunt passive power filter, (ii) shunt active power filter and shunt passive power filter and (iii) a series combination of passive power filter and active power compensator connected in shunt with the system. The series element in configuration (i) has to be rated for maximum load current and is not flexible for many applications. The configuration (ii) with two independent compensators in parallel requires both blocks to be rated at the supply voltage leading to high DC link capacitor voltage rating [8–10].

In comparison, the third topology where the passive power filter elements appear in series with the standard active power filter circuitry poses important advantages in terms of reflecting nearly zero impedance of the passive power filter for load current harmonics and at the same time high impedance for system side voltage harmonics. Further, it leads to absorbing the fundamental voltage component across the passive power filter, thereby reducing the voltage rating of the DC link capacitor to only the harmonic components which are to be suppressed. Accordingly, the rating and cost of the capacitor and the power semiconductor switches in the compensator are considerably reduced [8]. Further, this topology is effective in preventing system resonance, reducing switching noise and avoidance of any circulating current in the compensator.

The control requirements for all configurations involving active power filter boil down to the generation of reference current waveform, switching and triggering timings for semiconductor switches to match the source current and also for maintaining the desired voltage across the DC link capacitor. Accordingly, a variety of control schemes supported by related algorithms have been reported in the literature [11–20]. Time domain methods provide fast response, compared with frequency domain methods. Accordingly, many authors have proposed control techniques such as instantaneous reactive power theory, synchronous rotating reference frame (SRRF) theory, sliding mode controller, neural network techniques and feedforward control to improve the performance of both active as well as hybrid filters.

In this paper, the third topology has been utilised, where the passive power filter is designed with the aim of 5th and 7th selective harmonic elimination along with an active power compensator connected in series. The active component of the compensator is modelled in the stationary abc frame of mains and further transformed to the rotating dq frame to avoid time dependence of parameters to reduce the control complexity. A control technique using PI controller, based on decoupled currents, is used to inject currents from the compensator to ensure tracking of the reference waveform [13,14,21]. An independent outer control loop using another PI controller regulates the DC link voltage for sustained operation of the compensator. The parallel combination of 5th and 7th tuned passive harmonic filters connected in series with active filter configuration, the fundamental voltage of the system mainly drops on the PPF capacitor, not in the APF. Hence, the APF DC link voltage has been reduced with an objective of APF voltage rating reduction. The passive filter parameters present in this topology not only function as harmonic filter but also act as a filter for the switching ripples present in the system. Finally, the entire power and control circuits are fabricated, where the FPGA development kit SPARTAN-6 has been employed as the controller. Further, the performance improvement of the supply system along with the fabricated compensator has been evaluated by carrying out by a series of experiments on a prototype system and the results are presented covering different loading conditions.

2. System Configuration of Hybrid Compensator

The system shown in Figure 1 consists of a standard three-phase 400 V, 50 Hz mains connected to a pair of three-phase uncontrolled bridge rectifiers feeding individual R-L, R-C loads, which introduce harmonic currents in the supply system due to the nonlinearity. The shunt compensator contains 5th and 7th tuned passive filters, which are in parallel and the combination is connected in series with low voltage rated active power filter. The parallel connected passive filters having selective harmonic elimination are meant for effective reactive power compensation. This system eliminates the inherent disadvantages of both active and passive filters. The hybrid compensator is operated such that the distortion currents generated due to nonlinear loads are confined within the PPF and do not flow in the AC supply mains. The fundamental voltage drop across passive power filter components permits shunt APF to operate at low DC link voltage. The three-phase source voltage, the voltage at the point of common coupling, load and compensator currents are denoted as V_{abc}, V_{s123}, i_{L123} and i_{c123}, respectively, and shown individually in Figure 1.
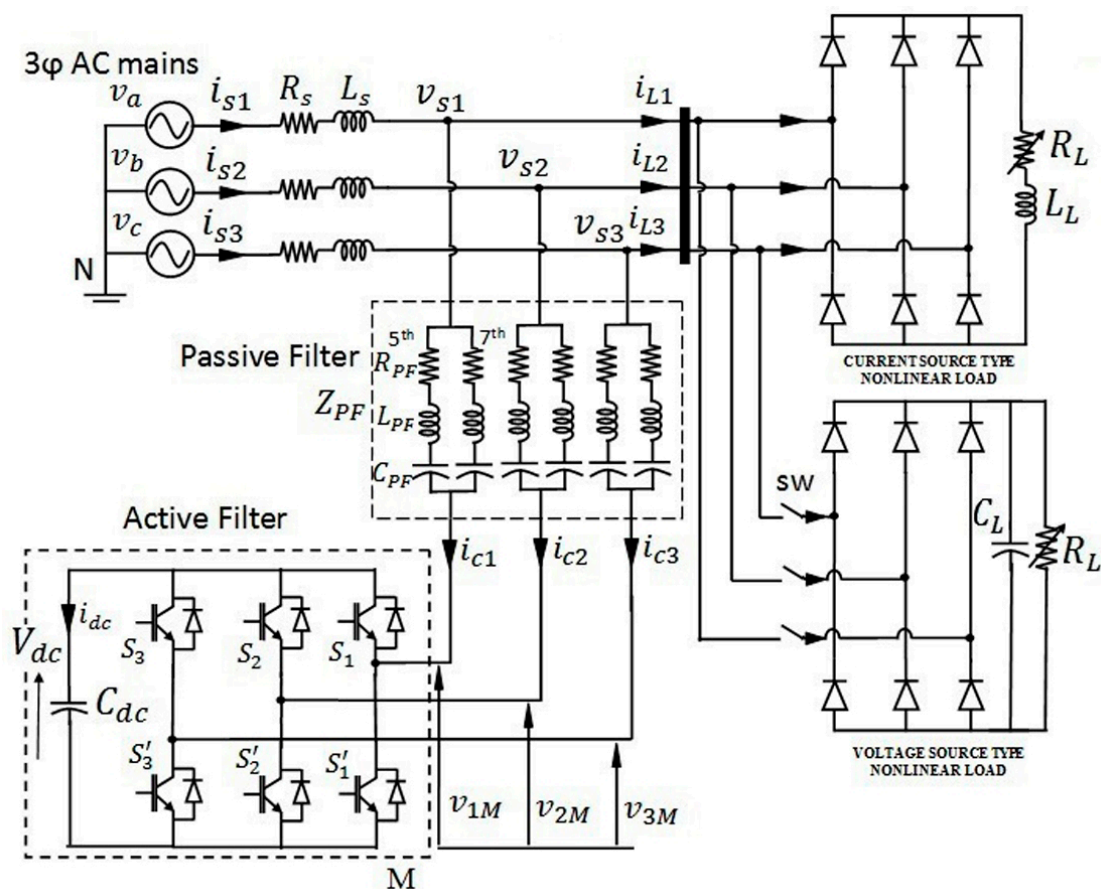

Figure 1. Configuration of the shunt hybrid compensator.

2.1. Modelling of Shunt Hybrid Power Compensator

By applying Kirchhoff's laws in Figure 1, the following equations in differential form in stationary three-phase reference frame are obtained, where the R_{PFe}, L_{PFeq} and C_{PFeq} are equivalent parameter values of the 5th and 7th selective harmonic filters.

$$v_{sk} = L_{PFeq}\frac{di_{ck}}{dt} + R_{PFeq}i_{ck} + (1/C_{PFeq})\int i_{ck}dt + v_{kM} + v_{MN} \tag{1}$$

where k = 1, 2, 3 represent the three phases.

Differentiation of Equation (1) to eliminate the integral term yields

$$\frac{dv_{sk}}{dt} = L_{PFeq} \frac{d^2 i_{ck}}{dt^2} + R_{PFeq} \frac{di_{ck}}{dt} + \frac{1}{C_{PFeq}} i_{ck} + \frac{dv_{kM}}{dt} + \frac{dv_{MN}}{dt} \tag{2}$$

Assuming balanced three-phase supply voltage yields

$$v_{s1} + v_{s2} + v_{s3} = 0$$

Summing the three equations included in (1) for $k = 1, 2, 3$ and assuming nonexistence of the zero-sequence current into three-wire system [16] results in

$$v_{MN} = -\frac{1}{3} \sum_{k=1}^{3} v_{kM} \tag{3}$$

The switching function C_k [12] of the kth leg of the inverter is the state of the power semiconductor devices S_k and S'_k and is defined as

$$C_k = \begin{cases} 1, & if \ S_k \ is \ On \ and \ S'_k \ is \ Off \\ 0, & if \ S_k \ is \ Off \ and \ S'_k \ is \ On \end{cases} \tag{4}$$

Thus, with $v_{kM} = C_k V_{dc}$ and differentiation of the same, this leads to

$$\frac{dv_{kM}}{dt} = C_k \frac{dV_{dc}}{dt} \tag{5}$$

By differentiating Equation (3), we get

$$\frac{dv_{MN}}{dt} = -\frac{1}{3} \sum_{k=1}^{3} \frac{d}{dt} (C_k V_{dc}) \tag{6}$$

Substitution of Equations (5) and (6) into (2) and rearranging the same yields

$$\frac{d^2 i_{ck}}{dt^2} = -\frac{R_{PFeq}}{L_{PFeq}} \frac{di_{ck}}{dt} - \frac{1}{C_{PFeq} L_{PFeq}} i_{ck} - \frac{1}{L_{PFeq}} \left(C_k - \frac{1}{3} \sum_{m=1}^{3} C_m \right) \frac{dV_{dc}}{dt} + \frac{1}{L_{PFeq}} \frac{dv_{sk}}{dt} \tag{7}$$

defining the switching state function as $q_{nk} = \left(C_k - \frac{1}{3} \sum_{m=1}^{3} C_m \right)_n$, where, $n = 0$ or 1.

In other words, the vector q_n epends on the parameters C_1, C_2, C_3 through a matrix transformation given below, indicating the interaction among the three phases [15].

$$\begin{bmatrix} q_{n1} \\ q_{n2} \\ q_{n3} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} C_1 \\ C_2 \\ C_3 \end{bmatrix} \tag{8}$$

$$\frac{d^2 i_{ck}}{dt^2} = -\frac{R_{PFeq}}{L_{PFeq}} \frac{di_{ck}}{dt} - \frac{1}{C_{PFeq} L_{PFeq}} i_{ck} - \frac{1}{L_{PFeq}} q_{nk} \frac{dV_{dc}}{dt} + \frac{1}{L_{PFeq}} \frac{dv_{sk}}{dt} \tag{9}$$

The capacitor current $i_{dc} = i_{c1} + i_{c2} + i_{c3}$ and is related to V_{dc} by

$$\frac{dV_{dc}}{dt} = \frac{1}{C_{dc}} i_{dc} \tag{10}$$

Expressing the DClink capacitor current i_{dc} in terms of the switching and compensator currents, the following equation is obtained

$$\frac{dV_{dc}}{dt} = \frac{1}{C_{dc}} \sum_{k=1}^{3} q_{nk} i_{ck} = \frac{1}{C_{dc}} [q_{n123}]^T [i_{c123}] \tag{11}$$

In the nonexistence of zero-sequence currents, the variables i_{c3} and q_{n3} can be eliminated by the substitution of $i_{c3} = -(i_{c1} + i_{c2})$ and $q_{n3} = -(q_{n1} + q_{n2})$ so that Equation (11) for the modelling of the capacitor is modified as follows.

$$\frac{dV_{dc}}{dt} = \frac{1}{C_{dc}} [2q_{n1} + q_{n2}] i_{c1} + \frac{1}{C_{dc}} [q_{n1} + 2q_{n2}] i_{c2} \tag{12}$$

The complete model of the shunt hybrid power compensator in *abc* reference frame is indicated by Equations (9) and (12).

2.2. Equations in dq Frame

The model given by Equations (9) and (12) is transformed into synchronous orthogonal frame using the transformation matrix [13]

$$T_{dq}^{123} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta - \frac{4\pi}{3}\right) \\ -\sin\theta & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta - \frac{4\pi}{3}\right) \end{bmatrix} \tag{13}$$

where $\theta = \omega t$ and ω represents the mains frequency.

Since T_{dq}^{123} is orthogonal, $\left(T_{dq}^{123}\right)^{-1} = \left(T_{dq}^{123}\right)^T$ and Equation (12) can be written as

$$\frac{dV_{dc}}{dt} = \frac{1}{C_{dc}} \left(T_{dq}^{123} [q_{ndq}]\right)^T \left(T_{dq}^{123} [i_{dq}]\right) = \frac{1}{C_{dc}} [q_{ndq}] [i_{dq}] \tag{14}$$

On the other hand, Equation (9) can be written as

$$\frac{d^2}{dt^2} [i_{c12}] = -\frac{R_{PFeq}}{L_{PFeq}} \frac{d}{dt} [i_{c12}] - \frac{1}{C_{PFeq} L_{PFeq}} [i_{c12}] - \frac{1}{L_{PFeq}} [q_{n12}] \frac{dV_{dc}}{dt} + \frac{1}{L_{PFeq}} \frac{d}{dt} [v_{s12}] \tag{15}$$

The three-phase current with the absence of zero-sequence components can be converted into *d-q* frame using reduced transformation matrix. Applying the transformations in Equation (15), the complete *d-q* frame dynamic model of the system is obtained as follows;

$$L_{PFeq} \frac{d^2 i_d}{dt^2} = -R_{PFeq} \frac{di_d}{dt} + 2\omega L_{PFeq} \frac{di_q}{dt} - \left(-\omega^2 L_{PFeq} + \frac{1}{C_{PFeq}}\right) i_d + \omega R_{PFeq} i_q - q_{nd} \frac{dV_{dc}}{dt} + \frac{dv_d}{dt} - \omega v_q \tag{16}$$

$$L_{PFeq} \frac{d^2 i_q}{dt^2} = -R_{PFeq} \frac{di_q}{dt} - 2\omega L_{PFeq} \frac{di_d}{dt} - \left(-\omega^2 L_{PFeq} + \frac{1}{C_{PFeq}}\right) i_q - \omega R_{PFeq} i_d - q_{nq} \frac{dV_{dc}}{dt} + \frac{dv_q}{dt} + \omega v_d \tag{17}$$

$$C_{dc} \frac{dV_{dc}}{dt} = q_{nd} i_d + q_{nq} i_q \tag{18}$$

The role of i_d in Equation (16) is interpreted as the component for meeting the switching losses in the compensator, whereas the component i_q is utilised to supply reactive power and maintain the DClink voltage across the capacitor for sustaining the compensator action.

It is specifically noted that this set of Equations (16)–(18) contain nonlinear terms involving the control variables q_{nd} and q_{nq}. Accordingly, the implementation of this control strategy is termed as nonlinear control technique by many authors in the literature [12,15,16].

2.3. Control of Harmonic Currents

Based on the load and compensator models presented in Section 2.2, the control problem is formulated with the objective of minimizing supply-side current harmonics and improving the power factor. Also, for maintaining the performance during load fluctuations, it is necessary to maintain a desired DC link capacitor voltage. The control law is derived using the following approach.

Rewriting Equations (16) and (17) in a more convenient form, we get

$$
\begin{aligned}
L_{PFeq}\frac{d^2 i_d}{dt^2} + R_{PFeq}\ \frac{di_d}{dt} + \left(-\omega^2 L_{PFeq} + \frac{1}{C_{PFeq}}\right) i_d \\
= 2\omega L_{PFeq}\frac{di_q}{dt} + \omega R_{PFeq}i_q - q_{nd}\frac{dV_{dc}}{dt} + \frac{dv_d}{dt} - \omega v_q
\end{aligned}
\tag{19}
$$

$$
\begin{aligned}
L_{PFeq}\frac{d^2 i_q}{dt^2} + R_{PFeq}\ \frac{di_q}{dt} + \left(-\omega^2 L_{PFeq} + \frac{1}{C_{PFeq}}\right) i_q \\
= -2\omega L_{PFeq}\frac{di_q}{dt} - \omega R_{PFeq}i_d - q_{nq}\frac{dV_{dc}}{dt} + \frac{dv_q}{dt} + \omega v_d
\end{aligned}
\tag{20}
$$

The control variables u_d and u_q are defined as

$$
u_d = 2\omega L_{PFeq}\frac{di_q}{dt} + \omega R_{PFeq}i_q - q_{nd}\frac{dV_{dc}}{dt} + \frac{dv_d}{dt} - \omega v_q
\tag{21}
$$

$$
u_q = -2\omega L_{PFeq}\frac{di_d}{dt} - \omega R_{PFeq}i_d - q_{nq}\frac{dV_{dc}}{dt} + \frac{dV_q}{dt} + \omega v_d
\tag{22}
$$

Using the idea of decoupling the current harmonic components for the purpose of tracking the reference current, the error signals $\bar{i}_d = i_d^* - i_d$ and $\bar{i}_q = i_q^* - i_q$ are generated and processed through a pair of PI controllers [12,14] to obtain u_d and u_q signals which are given below.

i_d^* and i_q^* are the reference currents deduced from the load current, i_d and i_q are the actual compensator currents. Load current in d-q coordinate is processed using a pair of fourth-order Butterworth low-pass filters with cut-off frequency set at 60 Hz to extract the harmonic current references alone.

$$
u_d = K_P \bar{i}_d + K_I \int \bar{i}_d dt
$$

$$
u_q = K_P \bar{i}_q + K_I \int \bar{i}_q dt
$$

From Equations (19) and (20), we obtain the transfer function as follows

$$
\frac{I_d(s)}{U_d(s)} = \frac{I_q(s)}{U_q(s)} = \frac{1}{L_{PFeq}\left(s^2 + \frac{R_{PFeq}}{L_{PFeq}}s + \frac{1}{C_{PFeq}L_{PFeq}} - \omega^2\right)}
\tag{23}
$$

The current control of the closed-loop system is shown in Figure 2 and represents the signal flow of the variables $i_q(s)$; the other component $i_d(s)$ is obtained concurrently in a similar manner. The transfer function of the full closed-loop control module is derived as

$$
\frac{I_q(s)}{I_q^*(s)} = \frac{K_P}{L_{PFeq}}\left[\frac{s + \frac{K_I}{K_P}}{s^3 + \frac{R_{PFeq}}{L_{PFeq}}s^2 + \left(\frac{1}{C_{PFeq}L_{PFeq}} - \omega^2 + \frac{K_P}{L_{PFeq}}\right)s + \frac{K_I}{L_{PFeq}}}\right]
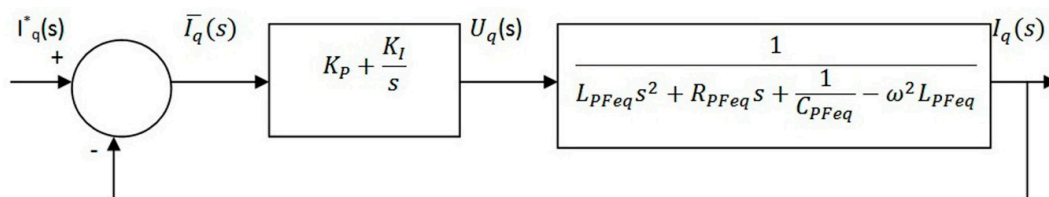\tag{24}
$$

Figure 2. Structure of current control loop for i_q and i_d.

From Equations (21) and (22), the control variables of the proposed system are defined by the following equations.

$$q_{nd} = \frac{2\omega L_{PFeq}\frac{di_q}{dt} + \omega R_{PFeq}i_q + \frac{dV_d}{dt} - \omega v_q - u_d}{\frac{dV_{dc}}{dt}} \tag{25}$$

$$q_{nq} = \frac{-2\omega L_{PFeq}\frac{di_d}{dt} + \omega R_{PFeq}i_d + \frac{dV_q}{dt} - \omega v_d - u_q}{\frac{dV_{dc}}{dt}} \tag{26}$$

The above equations represent both the decoupled linear compensation part and cancellation of nonlinearity.

2.4. DC Link Voltage Control

The capacitor in the APF does not need any external DC source but gets charged through the rectifier action of the built-in reverse diodes across the six Insulated-gate bipolar transistors (IGBTs). The power loss in the capacitor and switching losses in the inverter have to be met by the active component id of the compensator current from the mains, while the component i_q supplies the reactive power stored in the capacitor. The power losses in this circuit can reduce the DC link capacitor voltage, thereby weakening the function of the active filter. Hence, it is necessary to maintain the voltage across the DC link capacitor at a designed reference value by an additional voltage regulator, which modifies the PWM signals appropriately. This regulator is implemented by using a PI controller [12], which processes the error between the reference voltage V_{dc}^* and the actual capacitor voltage V_{dc}. The parameters of the PI regulator are chosen in such a way that the DC voltage is maintained around its desired value. The design values for the PI controller parameters have been obtained following the approach suggested by Salem Rahmani et al. [13,14]. The overall transfer function of this controller is incorporated as a subsystem in the simulation schematic.

The control scheme of the proposed hybrid power compensator is shown in Figure 3, where the various signals such as V_{dc}, V_{dc}^*, i_d, i_q, i_d^* and i_q^* are processed using Equations (21) to (26) to obtain the gate trigger signals.
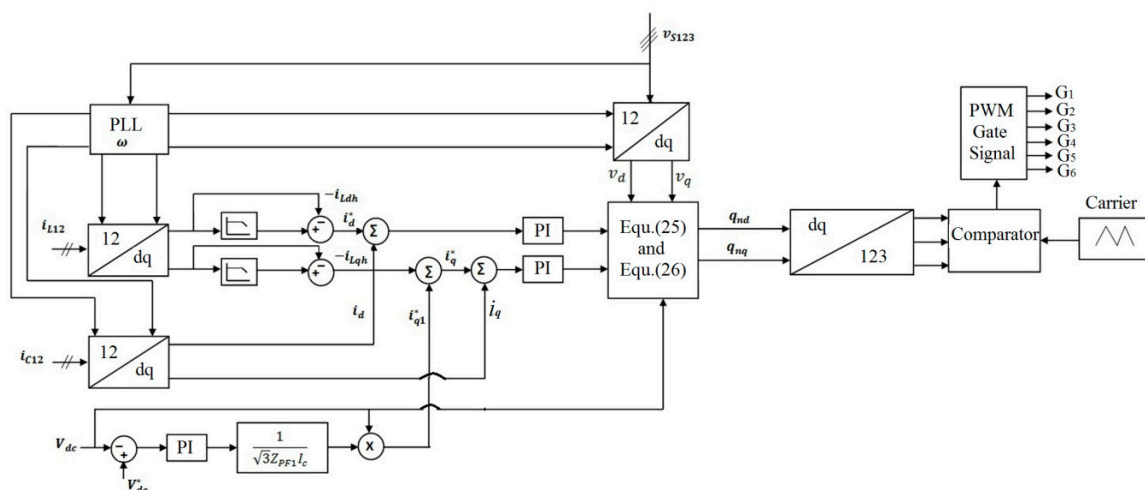

Figure 3. Control structure of the shunt hybrid compensator.

2.5. Simulink Model of the Shunt Hybrid Power Compensator

The Simulink schematic of the power distribution system along with the proposed shunt hybrid power compensator, which translates the entire system equations presented in Section 2 into functional blocks in the Simulink model, has been developed using MATLAB software. The nonlinear load has been modelled using a three-phase full bridge diode rectifier feeding RL and RC loads separately as

subsystems and connected to the three phase mains. At the source side, a resistor–inductor combination is used to represent the line impedance of each phase before PCC. The unbalance case in the nonlinear load has been formed by connecting a single-phase diode rectifier feeding RL load between phase1 and ground. The synchronization of the subsystem with main supply frequency is accomplished by using a three-phase discrete PLL block [22–25]. The PLL block detects the supply frequency; the detected supply frequency is used to synchronize the compensator *d-q* axis current and the distorted load *d-q* axis current to extract harmonic component needs to be compensated. During load disturbance and supply voltage distortions, the variation in the supply frequency is detected by the PLL block and synchronizes the subsystems accordingly.

The hybrid filter consists of a parallel connection of selective 5th and 7th harmonic elimination passive filters as depicted in Figure 1 along with APF. The entire system simulation is carried out in a discrete mode, variable step size with ode45 (Dormand–Prince) solver.

3. Simulation Results

To evaluate the performance of the shunt HPF controlled by the proposed control algorithm, a Simulink-based schematic was created so as to operate from a 400 V, 50 Hz supply. The load consists of a set of balanced and unbalanced nonlinear loads, which are selectively connected for successive simulation runs. In this work, the performances of the compensator corresponding to the following loads are analysed: (i) three-phase rectifier feeding RL load, (ii) three-phase rectifier feeding RC load, (iii) dynamic load variation and (iv) unbalanced load. Table 1 indicates the specification of the system parameters used in the simulation.

Table 1. Parameters of the system.

Phase Voltage and Frequency	Vsrms = 230 V and fs = 50 Hz
Impedance of the line	Rs = 0.1 Ω, Ls = 4 mH
Nonlinear load of current source type	RL = 50 Ω, LL = 10 mH
Nonlinear load of voltage source type	RL = 32 Ω, CL = 1000 μF
5th tuned PPF parameters	R = 0.1 Ω, L = 10 mH, C = 40 μF
7th tuned PPF parameters	R = 0.1 Ω, L = 7 mH, C = 30 μF
DClink voltage and capacitance	V_{dc} = 25 V, C_{dc} = 6600 μF
Parameters of the outer loop PI controller	k1 = 0.22 and k2 = 15.85
Inner loop PI controller parameters	K_P = 0.6 and K_I = 1.2

3.1. Performance of Shunt HPF to the Nonlinear Load of Current Source Type

The three-phase mains supply a diode bridge rectifier, whose output is wired to a balanced R-L load, which imposes a typical nonlinearity, resulting in harmonic currents at the supply end. The proposed hybrid shunt compensator is wired at PCC as shown in Figure 1. The results are shown in Figure 4a–e covering the waveforms of the supply voltage, currents of the load, source current after compensation, currents of the compensator and DC link voltage, respectively. The waveform depicts that the supply current waveform is almost sinusoidal after compensation and the DC link capacitor voltage is maintained constant. Figure 5 depicts the simulation results covering the harmonic spectrum of the supply current before and after compensation. The results indicate that the THD of the supply current is reduced from 25.74% without compensator to 4.68% with compensator. It is seen that the proposed control strategy with shunt HPF can mitigate the current harmonics present in the supply system within the limit specified by IEEE 519-1992 standards.
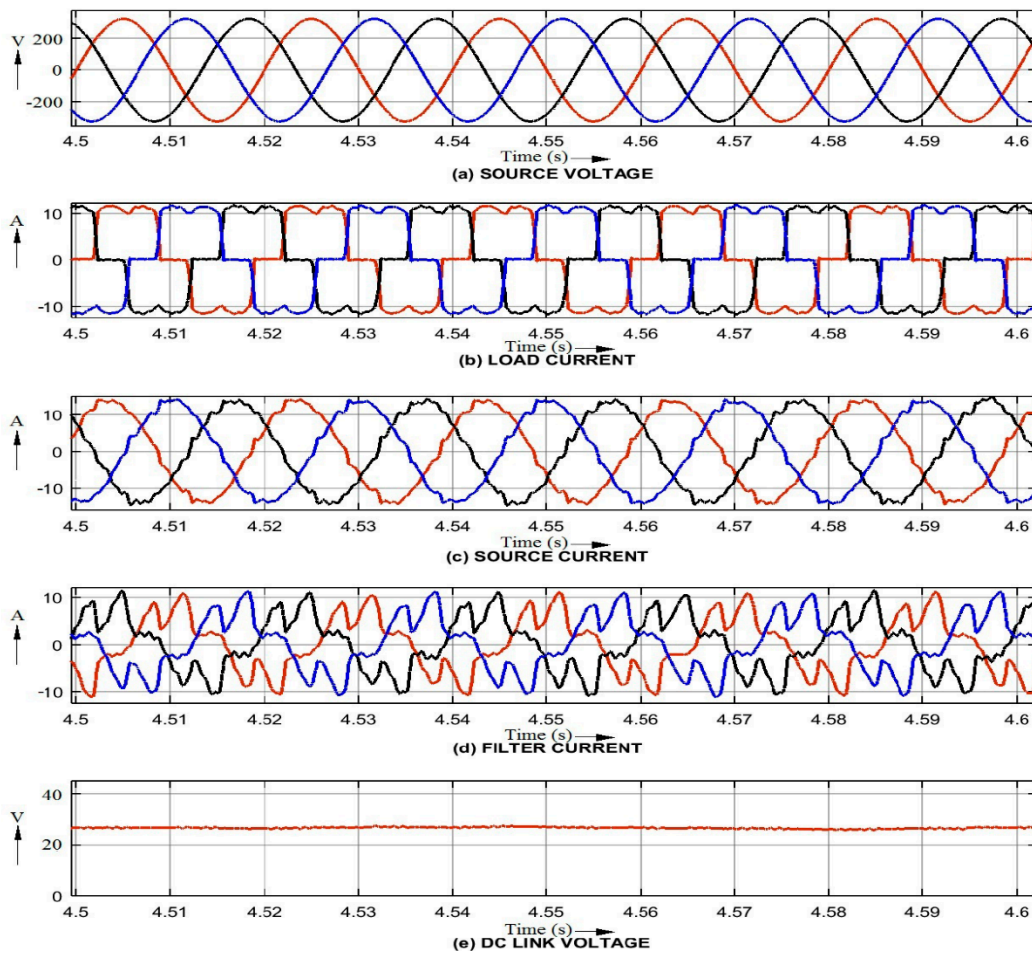
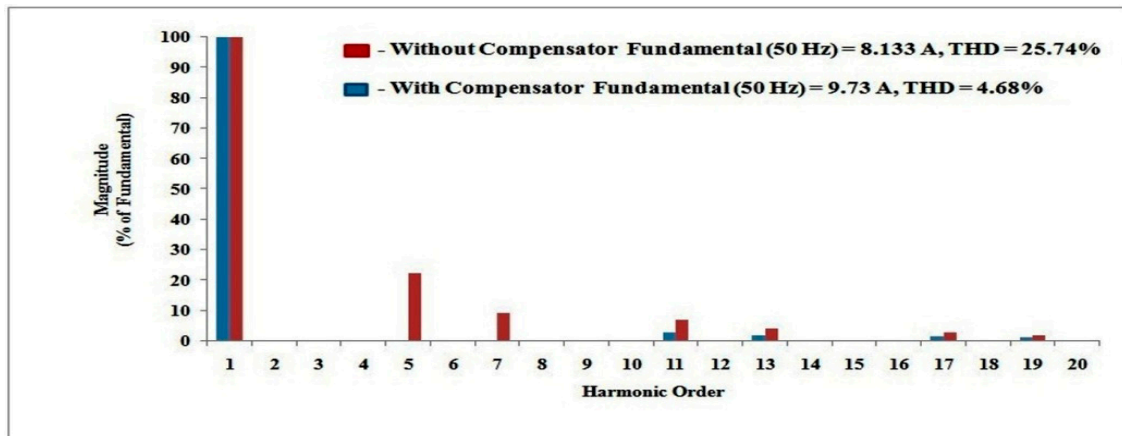**Figure 4.** Performance of the compensator to the nonlinear load of current source type.

Figure 5. FFT analysis of the supply current with and without compensator.

3.2. Varying Three-Phase Rectifier-Fed RL Load

Since the load in a distribution system can vary concerning time, it is essential to verify the suitability of the designed filter under varying load conditions. The simulation results for sudden change of load current from 9.74 A (rms) to 17.17 A at $t = 4$ s and restoration of the same to the previous value at $t = 4.1$ s are presented in Figure 6a–e covering source voltage, load current, source current, compensator current and DC link voltage waveforms, respectively. The THD of the supply current before step change in the load current has been improved from 25.74% without compensator to 4.55%

with compensator. Similarly, after a step change in the load current, the supply current THD has been reduced from 23.06% to 4.14% with compensator. In both the cases, the compensator is capable of maintaining the THD of the source-side current within the limit specified by the IEEE 519-1992 standards. It is observed from Figure 6e,c that the compensator is able to maintain the DC link voltage as constant and supply current waveforms to be sinusoidal.
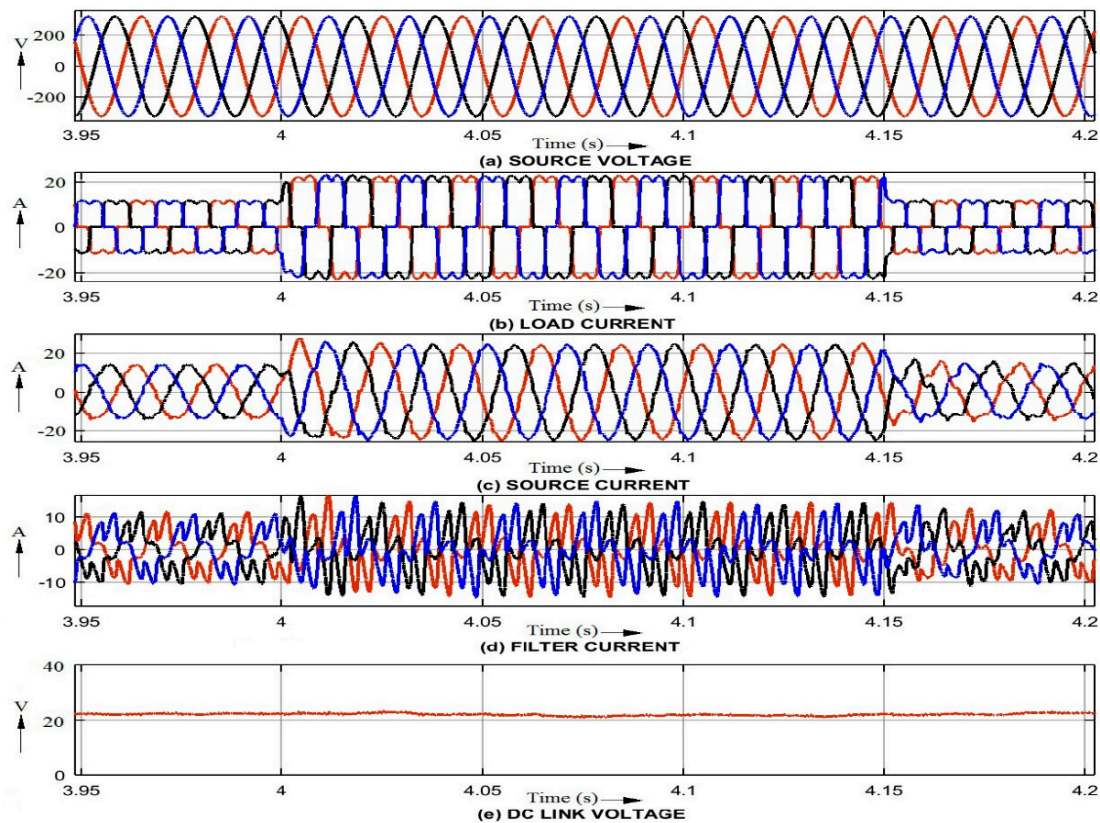
Figure 6. Response of the compensator to sudden change of load current.

3.3. Three-Phase Rectifier-Fed RC Load

The load in the simulation schematic is replaced by an R-C circuit with parameter values as shown in Table 1 and the simulation is executed to obtain the performance of the compensator. Figure 7a–e shows the source voltage, load current, supply current after compensation, compensator current and DC link voltage waveforms, respectively. It is observed from the figures that the DC link voltage of the compensator is maintained constant during compensation, and the supply current variation approaches a sinusoidal waveform. Figure 8 shows the harmonic spectrum of line currents from mains before and after compensation. It shows that the THD of the source current is reduced considerably from 27.49% to 4.08%. The system is highly nonlinear and subjected to disturbances due to loading. Hence, in practice, the DC link voltage varies slightly due to ripples and disturbances inherent in the operation of the compensator.
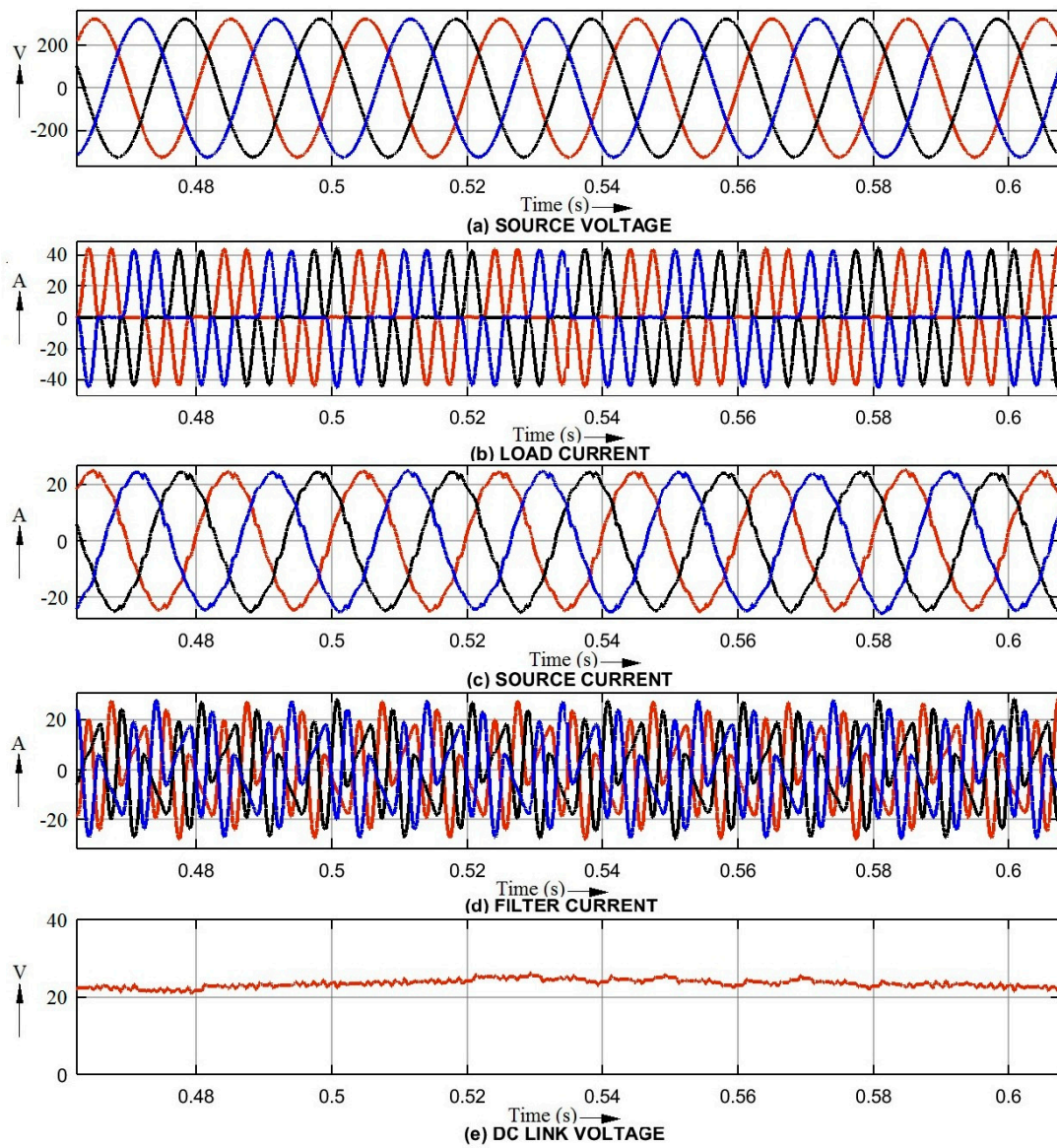
Figure 7. Performance of compensator for voltage source type nonlinear load.
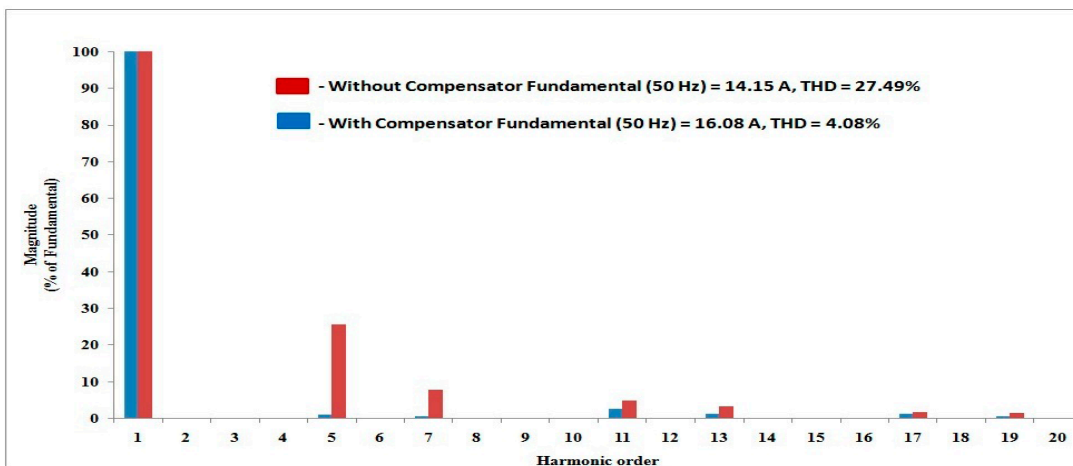

Figure 8. Harmonic spectrum of supply current before and after compensation.

### 3.4. Varying Three-Phase Rectifier-Fed RC Load

By introducing a 100% step increase followed by a similar decrease in the load current of the R-C circuit, the ability of the hybrid compensator to mitigate the harmonic current under varying load conditions is examined in the simulation setup. The results of this simulation, where the load current changes from 16.05 A (rms) to 30.32 A at $t = 2$ s and restoration of the same to 16.05 A are shown in Figure 9a–e. These depict the supply voltage, load current, supply current after compensation, compensator current and the DC link voltage, respectively. The obtained results indicate that the desirable features in the performance of the hybrid filter are maintained even after the step changes in the load within a very short time. The THD of the source current has been reduced from 27.49% without compensator to 3.46% with compensator before the step change is made in the load current. Similarly, the THD has been reduced from 20.91% to 4.77% after the step change. It is seen that the compensator operation reduces the harmonic content within a THD of 5%, in addition to maintaining a steady DC link voltage.
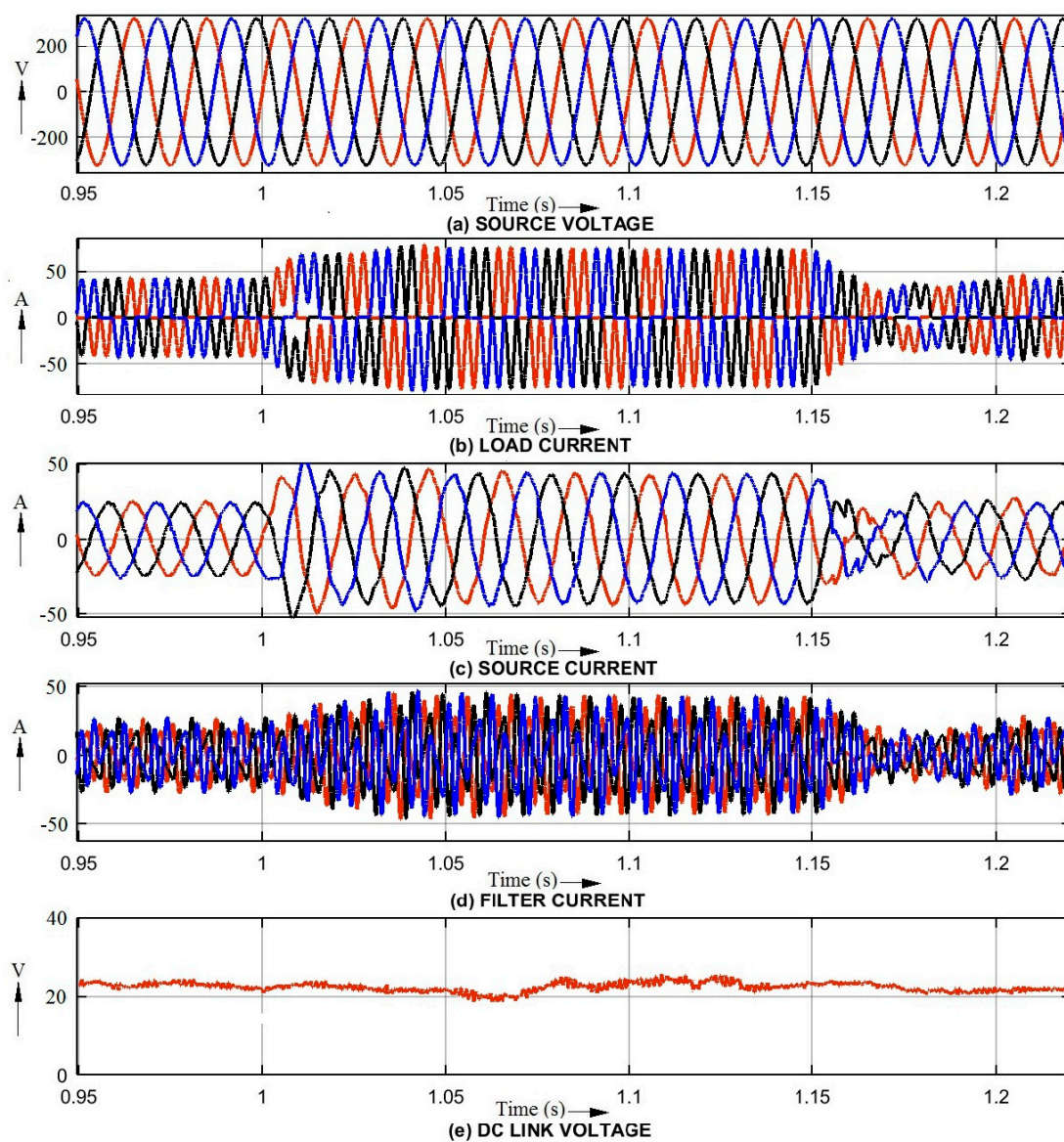
Figure 9. Performance of the compensator for variation in three-phase rectifier-fed RC load.

3.5. Unbalanced Loading Condition

To study the performance of a shunt hybrid power compensator employing synchronous rotating reference-based nonlinear control method, an unbalance in load is created by connecting a single-phase rectifier feeding R-L load across the phase 'a' and phase 'b' of the supply system. The compensation performance at steady state of the proposed compensator, such as the supply voltage, load current, supply current, compensator current and DC link voltage waveforms, is depicted in Figure 10a–e. The THD of supply phase 'a' current is reduced from 9.46% to 2.54% after compensation. Similarly, supply phase 'b' current has been reduced from 7.04% to 1.91%, while phase 'c' current has been reduced from 25.47% to 5.37%.
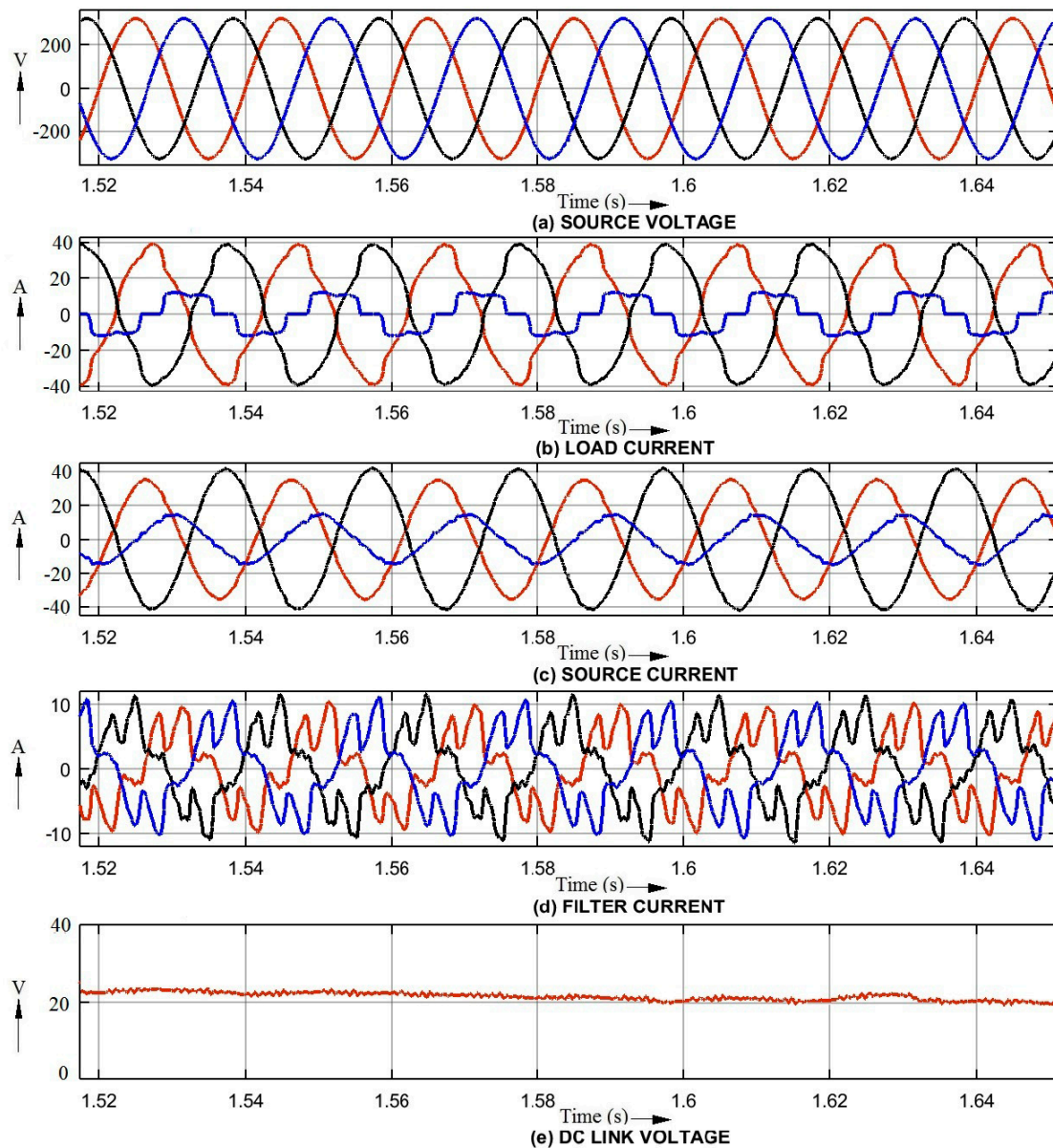
Figure 10. Performance of the compensator to the unbalanced nonlinear load.

It is seen from the obtained results that the proposed control method with shunt hybrid compensator effectively compensates the harmonic distortion present in the supply current under unbalanced loading conditions.

Since the load in a distribution system can vary with respect to time, it is essential to verify the suitability of the designed filter under varying load conditions. During dynamic variations in the load

current and unbalance, as shown in Figures 6, 9 and 10, the compensator is able to maintain constant DC link voltage as well as reduce the amount of harmonics present in the system.

4. Hardware Fabrication

A prototype of the distribution system along with the passive and active parts of the hybrid compensator has been fabricated and experimental work on the same was carried out. Figure 11 shows the overall setup of the experimental work. The active filter part of the prototype has been developed using intelligent power module PEC16DSMO1. The IPM consists of a three-phase six-pulse inverter with six IGBT semiconductor power switches and is controlled in real time based on the software control program from the SPARTAN-6 FPGA development board. These IGBT switches are capable of operating at high frequencies of the carrier waveform up to 20 kHz.
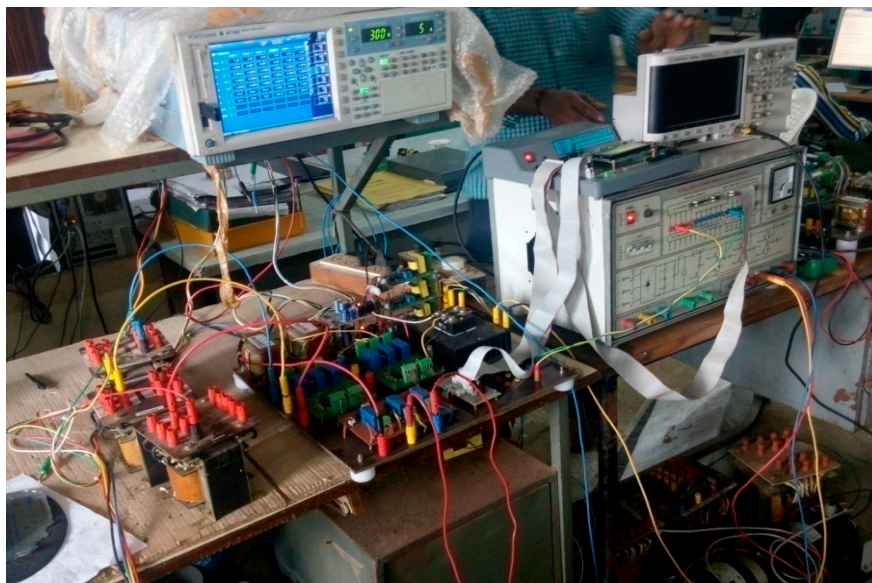

Figure 11. Experimental setup.

4.1. Hardware Resultsand Discussion

A series of experiments involving different types of loads and their dynamic variations have been conducted, and the performance of the compensator has been evaluated. A six-channel YOKOGAWA Power Quality Analyser has been used to capture the signals such as supply voltage, source current, load current, compensator current and DC link voltage. The hardware system parameters are shown in Table 2

Table 2. Experimental circuit parameters.

Active Power Filter	Intelligent Power Module (IPM) PEC16DSMO1 with 6 IGBT Switches
IGBT rating	25 A, 1200 V
Switching frequency of APF switches	2 kHz
Current sensors	LTS 25-NP
Voltage sensors	LV 25-P
Filter inductors	7 mH and 10 mH
Filter capacitors	30 μF and 40 μF
DC link capacitor	6400 μF

4.1.1. Performance of the Compensator for Current Source Type Nonlinear Load

Figure 12 shows the experimental response of the compensator for the current source type nonlinear load. The compensation performance of the hybrid filter has been verified by turn on the compensator at the point 'S' as shown in Figure 12. It is seen from the figure that the source current becomes sinusoidal after the operation of compensator at point 'S'. The harmonic spectrum of the source current without and with compensator is shown in Figure 13a,b and it is observed that the THD of the source current has been reduced from 26.225% to 2.212%.
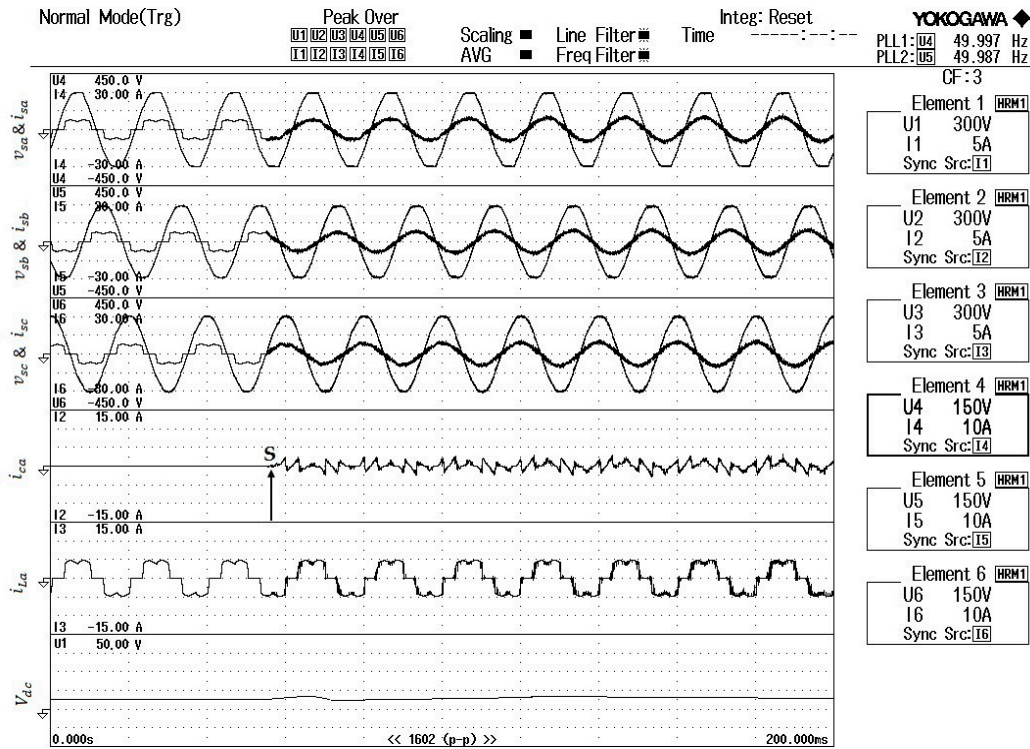

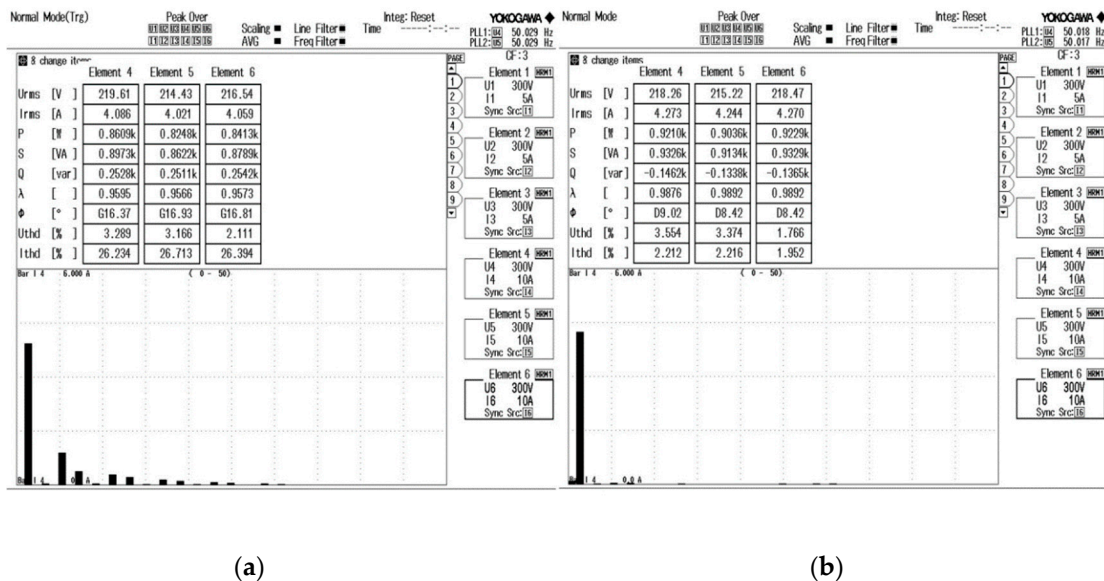**Figure 12.** Hardware response of the compensator for current source type load.

(**a**)   (**b**)

Figure 13. FFT spectrum of source current (**a**) before compensation and (**b**) after compensation.

4.1.2. Performance of the Compensator for Varying Current Source Type Nonlinear Load

The performance of the hybrid compensator has been verified experimentally by creating a step change in the load current at 'A' as shown in Figure 14. It is observed that the source current in all the three phases are sinusoidal and the compensator is able compensate the harmonic distortion even after a step change in the load current. The THD of the source current after compensation has been observed as 3.26%, which is less than 5% as specified by IEEE 519-1992 standards.
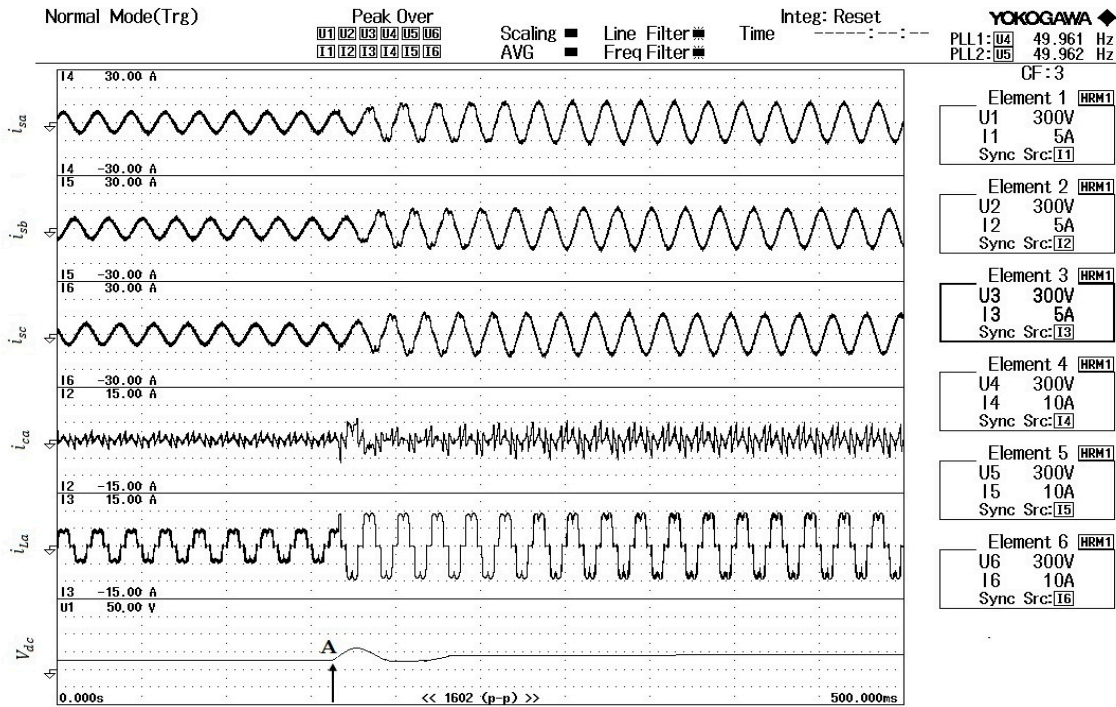

Figure 14. Performance of the compensator for time-varying current source type nonlinear load.

4.1.3. Performance of the Compensator for Voltage Source Type Nonlinear Load

The performance of the compensator for voltage source type nonlinear load has been experimentally verified by connecting the nonlinear load in the three-phase supply system. Figure 15 shows the three-phase source currents of all phases individually, compensator current of one phase, load current of one phase and DC link voltage, respectively. It is seen that the supply current after compensation is sinusoidal without distortion and the DC link voltage of the compensator is also maintained constant.

The FFT spectrum of the source current before and after compensation is shown in Figure 16a,b, respectively. It is observed from the FFT spectrum that the supply current harmonics have been reduced from 67.795% without compensator to 4.136% with compensator. It has been confirmed from the above results that the designed control strategy with proposed shunt hybrid power compensator is able to effectively compensate both the types of nonlinear load distortions present in the supply current. It is observed that the experimental work results are closely matching with simulation work results in all cases and the obtained performance waveforms are also matching with each other.
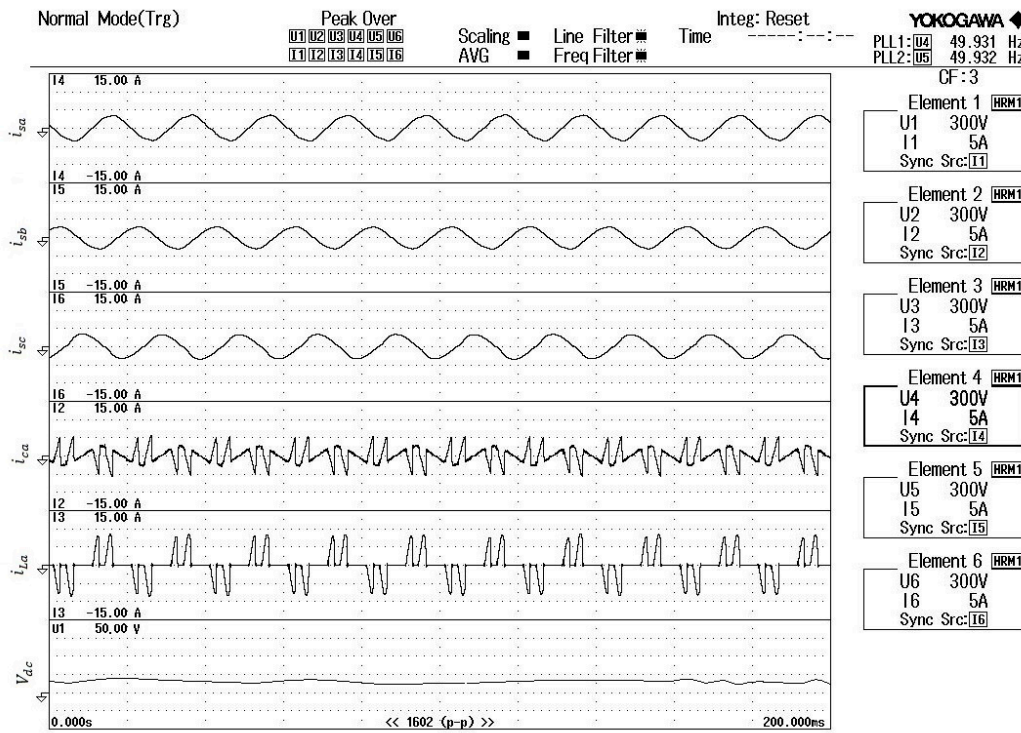
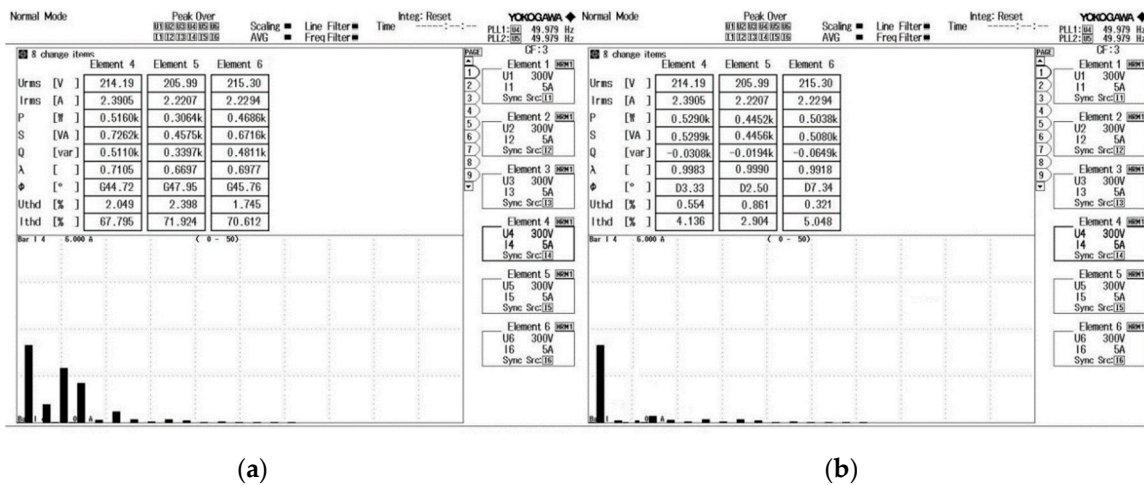**Figure 15.** Performance of the compensator for voltage source type nonlinear load.

(**a**)   (**b**)

Figure 16. FFT Spectrum of source current (**a**) before compensation and (**b**) after compensation.

4.1.4. Performance Comparison and Discussion

Performance of the proposed hybrid filter with the adopted control strategy has been compared with some other control methods proposed in the literature. Table 3 shows the comparison of various control techniques proposed in the literature for harmonic reduction. It is clearly understood from Table 3 that the synchronous rotating reference theory based nonlinear control with the adopted hybrid filter topology proposed in this work gives better THD in the source current during supply feeds of different types of nonlinear loads. Most of the techniques proposed in the literature cover only current source type nonlinear load. In this work, different types of nonlinear loads and various loading conditio..ns are considered during simulation and experimental work. The experimental work has been carried out for low current rating nonlinear loads compared to the simulation work. Hence, it has been observed that the experimental THD values are better than the simulation results.

Furthermore, the hardware setup has been developed for low rating loads only due to the cost. The results of simulation indicate effectiveness of the compensator topology and versatility of the control scheme for meeting the requirements of a set of nonlinear loads indicated above. In addition, the *kVA* ratings of the designed active filter for both types of load are only a small percentage of the respective load ratings, which is a major advantage of this scheme. Although the overall performance of the hybrid compensator has been highly satisfactory, while covering alternate cases of load, their fluctuations and unbalance, it appears that the PI controller-based algorithm shows a minor deficiency, when the passive filter parameter values undergo even minor changes. This can be traced to the presence of fixed values of the PI controller gain and time constant parameters. A possible and feasible solution to this issue of filter parameter variations is to adaptively adjust the PI parameters' value. Although a three-phase distribution system for power quality enhancement has been considered in this paper, it is limited to a three-wire system only with isolated neutral. Hence, issues arising out of zero-sequence currents due to load unbalance have not been considered. This research work can be extended for a three-phase, four-wire system. Further, incorporation of controllers utilizing various other soft computing techniques like neural, fuzzy-neural and genetic algorithms can be carried out as further work.

Table 3. Comparison of the performance of various control techniques.

Control Methods	SRF Theory-Based Nonlinear Control for SHAPF [13]	p-q Theory-Based Control for SHAPF [26]	SRF Theory-Based Control for SHAPF [27]	Parallel Connected SHAPF [28]
THD% Three-phase rectifier-fed RL load	4.6	4.32	-	4.3
THD% Three-phase rectifier-fed RC load	4.08	4.15	-	-
Unbalanced load % THD	2.29 to 4.80	-	1.18 to 2	4.5 to 4.7
DC link voltage	25 V APF rating is less	50 V APF rating is moderate	220 V APF rating is more	26 V APF rating is less

5. Conclusions

A three-phase hybrid compensator scheme discussed in this paper is configured with 5th and 7th selective harmonic elimination passive filter in series with an active filter in the form of an IGBT-based PWM inverter, triggered using a control algorithm, based on a synchronously rotating reference frame (SRRF) in the *d-q* axis. The overall objective is to improve the steady state power factor and to ensure dynamic harmonic compensation at the supply side of three-phase mains. Accordingly, the entire system is simulated using Simulink and the results are presented, covering a set of nonlinear loads. The simulation results indicate the effectiveness of the compensator topology and versatility of the control scheme for meeting the requirements of a set of nonlinear loads. It is seen that significant reduction of source current THD is obtained within limits specified by IEEE 519-1992 standard along with excellent regulation of the DC link voltage.

A series of experiments were carried out using the above prototype along with alternate nonlinear loads and the overall performance of the hybrid filter was recorded using six channels DSO. The THD values as measured by the DSO over a series of experiments were found to be closely matching with corresponding THD values obtained during simulation for all loading conditions. It is further verified that the experimental results compared favourably with the simulation waveforms, thereby validating the simulation model. The experimental results confirm the effectiveness of the SRRF-based control strategy for the hybrid compensator scheme to achieve source side current harmonics reduction and power factor improvement to near unity.

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