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Maximal Q Factor for an On-Chip, Fuse-Based Trimmable Capacitor

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Abstract: This paper presents a circuit for realising a fuse-programmable capacitor on-chip. The trimming mechanism is implemented using integrated circuit fuses which can be blown in order to lower the resulting equivalent capacitance. However, for integrated circuits, the non-zero fuse resistance for active fuses and finite fuse resistance for blown fuses limit the Q factor of the resulting capacitor. In this work, we present a method on how to arrange the fuses in order to achieve maximal worst-case Q factor for the given circuit topology given the process parameters and requirements on capacitance. We also analyse and discuss the accuracy and limitations of the topology with regard to fuse resistance and parasitic elements such as bond pads.

Keywords: fuse; resonant circuit; trimmable capacitor; single-chip

1. Introduction

The goal to design resonant circuits for single-chip RF systems has created the need for trimmable [1] IC capacitors. Applications for such circuits exist in the field of wireless transfer of power directly to a single-chip system, where the RF inductor is integrated on the die. Examples of applications include implantable chips in humans for biomedical purposes [2,3], and sensors for condition monitoring of power semiconductors, where a wireless power supply and communication interface provides galvanic isolation from the high-voltage power semiconductors [4,5].

For both examples, the on-chip coils would be optimised based on the properties of the surrounding materials: tissue data [6] in the case for biomedical implants, and power semiconductor module geometry data [5] in the case for sensors for condition monitoring. In these types of application, a capacitor can be used to form a resonant circuit with the receiver on-chip coil, which boosts the voltage induced in the coil. However, for resonant circuits in single-chip systems such as described above, the obtained resonant frequency may deviate from the desired one because of large tolerances in the IC manufacturing process. Obtaining a specific frequency can be important for RF applications for which the frequency must lie within a frequency band which allows sufficient energy to be radiated, for example an ISM band [7]. Tunability is also important for applications where many devices must be powered by the same transmitter and thus operate at the same frequency. One way to adjust the resonant frequency is to trim the value of the capacitor in an LC circuit.

As an alternative to relatively costly laser-trimmed [8] IC capacitors, in this paper we discuss how to optimise fuse-based binary-weighted trimmable capacitors in order to maximise their Q factors which in turn will maximise the Q factors for any resonant circuits built from such capacitors. One such circuit could be an LC circuit consisting of an RF receiver coil and a resonant trimmable capacitor used for frequency tuning. The main issue we address is the effect of non-zero and finite resistance for active and blown IC fuses, respectively.

Although the theory presented in this work is valid not only for fuses, but also for semiconductor switches such as MOSFETs, this paper addresses only fuses. This decision is motivated by the fact that for applications which require a wireless power supply, no power source is available to bias a semiconductor into a desired switching state. Furthermore, even if semiconductors were to be used, such as in [9], effects from e.g., parasitic capacitance and temperature-dependent leakage current would still have to be taken into account.

Furthermore, because fuses are one-time programmable, if possible, we recommend using capacitive structures which have good temperature and bias stability such as MIM capacitors [10], which also exhibit high Q factors. In contrast, using MOSFET capacitors would introduce a strong dependence on bias for the resulting capacitance [11]. Furthermore, if no power source is available for bias, the MOSFETs would be biased in the region where the capacitance varies the most and the variation in capacitance with voltage would be extremely strong [11], defeating the purpose of trimming.

For biomedical implants, a concern could be that the impedance of an implanted coil would be sensitive to the electromagnetic properties of the surrounding tissue which are only known approximately and may change over time, which in turn would result in a change in resonant frequency. However, the encapsulation of the IC chip can be made comparable in size to the coil diameter, for example a $2 \times 2\,\mathrm{mm}^2$ chip with a 1 mm encapsulation. In such a case, the electromagnetic fields generated by the on-chip coil will extend mainly into the encapsulation material (whose electromagnetic properties are known to a high accuracy and do not change) and not into the surrounding tissue. Thus the resonance frequency can be trimmed before implantation and will not change over time.

The paper is organised as follows. In Section 2, we introduce the circuit and discuss how to optimise it for maximum Q factor and in Section 3 we discuss the accuracy of the optimised circuit. In Section 4, we present an example relating the theory to an application and discuss the results. The conclusion is presented in Section 5.

2. Trimmable Capacitor Bank

Consider the trimmable capacitor bank shown in Figure 1. The circuit comprises one base capacitor, C, in parallel with m binary-weighed trim capacitors, $C_0, C_1, ..., C_{m-1}$, distributed as $C_n = C_x/2^n$. The trim capacitors can be deactivated by blowing their corresponding fuse in $\{F_0, F_1, ..., F_{m-1}\}$. The equivalent capacitance, C_{eq}, seen between nodes a and b can be written as

$$C_{\mathrm{eq}} = C + \sum_{n=0}^{m-1} F_n \frac{C_x}{2^n}, \tag{1}$$

where F_n is 0 if fuse n is blown and 1 if it is active. From Equation (1), it can be seen that by letting F_n represent bit n of an m-bit binary number, C_{eq} can be controlled from C to $C + \Delta C$ with the resolution of the smallest trim capacitance, $C_{\mathrm{res}} = C_{m-1} = C_x/2^{m-1}$. Because ΔC is the sum of all the trim capacitances, it can be written as

$$\Delta C = \sum_{n=0}^{m-1} \frac{C_x}{2^n}. \tag{2}$$

By solving Equation (2) for C_x, we arrive at the following expression:

$$C_x = \frac{\Delta C}{2(1 - 1/2^m)}. \tag{3}$$

Thus, from the base capacitance, C, and trim capacitance, ΔC, needed for the application, values can be selected for all the capacitors in the circuit of Figure 1.

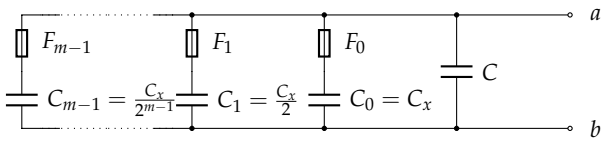


Figure 1. Fuse-based trimmable capacitor.

2.1. Finite/Non-Zero Fuse Resistance

For ICs, both the fuse on-resistance, $R_{\mathrm{f,\,on}}$, and off-resistance, $R_{\mathrm{f,\,off}}$ can be significant. In many process technologies, a unit fuse is available with a fixed on- and off-resistance and for the examples in this work, values of $R_{\mathrm{f,\,on}} = 25\,\Omega$ and $R_{\mathrm{f,\,off}} = 80\,\mathrm{k}\Omega$, relevant to a 180 nm process, are assumed. It is however possible to realise arbitrary on- and off-resistances, $r_{\mathrm{f,\,on}}$ and $r_{\mathrm{f,\,off}}$ by connecting a number of fuses in series and/or parallel and then either blowing all or none of the fuses in a branch. Because $R_{\mathrm{f,\,on}}$ and $R_{\mathrm{f,\,off}}$ are constant, the on-resistance of the resulting network will always be linearly related to its off-resistance by a factor,

$$k_{\mathrm{f}} = \frac{R_{\mathrm{f,\,on}}}{R_{\mathrm{f,\,off}}} = \frac{r_{\mathrm{f,\,on}}}{r_{\mathrm{f,\,off}}}. \tag{4}$$

The question thus arises on how to select $r_{\mathrm{f,\,on}}$ (or, equivalently $r_{\mathrm{f,\,off}}$) in order to maximise the Q factor for the resulting capacitor for the worst-case configuration of active/blown fuses. It should be noted that both $R_{\mathrm{f,\,on}}$ and $R_{\mathrm{f,\,off}}$ is highly process dependent, which may make fuse trimming less attractive in some processes than others, particularly those in which k_{f} is small, which will be demonstrated later in this section.

2.2. Q Factor Optimisation for a Single Branch

Consider starting with the base capacitance, C, and adding a single fuse-controlled branch to that circuit. The resulting Q factor, $Q_{\mathrm{eq}}(a_{\mathrm{f}})$, for arbitrarily selected component values are plotted in Figure 2 as a function of the fuse scaling factor, a_{f}, with the fuse resistance, R_{f}, attaining values for both active and blown fuses. Here a_{f} is the factor by which a fuse is scaled by a series and/or parallel connection that gives a scaled fuse resistance $r_{\mathrm{f}} = a_{\mathrm{f}} R_{\mathrm{f}}$, and also $r_{\mathrm{f,\,on}} = a_{\mathrm{f}} R_{\mathrm{f,\,on}}$ and $r_{\mathrm{f,\,off}} = a_{\mathrm{f}} R_{\mathrm{off}}$. In order to maximise the resulting worst-case Q factor, we want to find the value of a_{f} for which the worst-case $Q_{\mathrm{eq}}(a_{\mathrm{f}})$ for both cases of R_{f} is as large as possible. That is, we want to maximise the function

$$f(a_{\mathrm{f}}) = \min\left(Q_{\mathrm{eq}}(a_{\mathrm{f}})\Big|_{R_{\mathrm{f}}=R_{\mathrm{f,\,on}}}, Q_{\mathrm{eq}}(a_{\mathrm{f}})\Big|_{R_{\mathrm{f}}=R_{\mathrm{f,\,off}}} \right). \tag{5}$$

From the figure, it can be seen that the maximum Q_{eq} is obtained either for very small values for a_{f} or for very large values for a_{f}. In fact, Q_{eq} tends towards infinity for such values. The reason for this is that, for very small a_{f}, the fuse behaves as a short circuit for both its active and blown state and thus does not contribute significantly to the total equivalent resistance of the circuit. The contrary is true for very large a_{f}, where the fuse behaves as an open circuit for both cases and thus the branch does not contribute significantly to the equivalent impedance. Thus, if we choose such extreme values for a_{f}, the resulting equivalent capacitance can no longer be controlled by the fuse. Therefore, we must choose a value for a_{f} in a region where the fuse behaves as a short circuit for active fuses (to the left of the minimum $Q_{\mathrm{eq}}(a_{\mathrm{f}})$ of the blue solid line), and as an open circuit for blown fuses (to the right of the minimum $Q_{\mathrm{eq}}(a_{\mathrm{f}})$ for the red dashed line). It can be seen from Figure 2 that a local maximum for $f(a_{\mathrm{f}})$ within this region occurs at the intersection point of the of the curves representing the Q factor for $R_{\mathrm{f}} = R_{\mathrm{f,\,on}}$ and $R_{\mathrm{f}} = R_{\mathrm{f,\,off}}$, respectively.

Note that this point represents the fuse resistances for which the Q factor has degraded equally for the active and blown states of the fuse. Deviating from this point increases the Q factor for one of these states, but decreases it for the other. The intersection point thus represents the highest possible worst-case Q factor for the equivalent capacitor. It should also be noted that Figure 2 assumes infinite

Q factors for all involved capacitors. If IC capacitors can be manufactured with a Q factor of Q_{cap}, for extreme values for a_{f}, Q_{eq} would approach Q_{cap} asymptotically instead of tending towards infinity. In fact, this behaviour is shown in a lighter shade in the figure. The simplification is made because it is reasonable to assume that the series resistance contributed to one of the capacitors by a scaled fuse will be much larger than the ESR of the capacitor itself. Thus, for non-extreme values for a_{f}, which are the values we are interested in, Q_{cap} will be much larger than Q_{eq}.

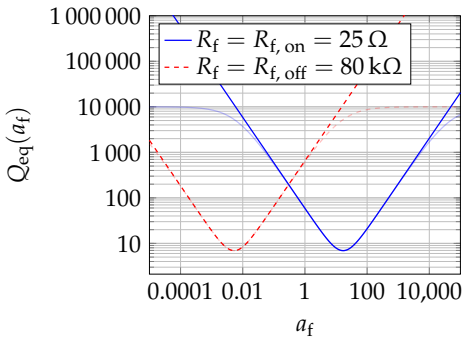


Figure 2. Q factor, $Q_{\text{eq}}(a_{\text{f}})$, for a 3 pF capacitor in parallel with a series combination of a fuse and a 1 pF capacitor, plotted as a function of fuse scaling factor, a_{f}. $Q_{\text{eq}}(a_{\text{f}})$ is plotted for both active and blown fuses corresponding to different fuse resistances. Plots for manufactured capacitors with both infinte Q factors and Q factors of 10 000 are shown, with the latter case in a lighter shade.

In the pursuit to find an expression for the intersection point of Figure 2, consider the equivalent impedance, Z_{eq}, resulting from the parallel connection of two impedances, $Z_1 = R_1 + \text{j}X_1$ and $Z_2 = R_2 + \text{j}X_2$. Here, symbols R and X denote the resistance and reactance, respectively, of the impedance Z with corresponding index. It can be shown that Z_{eq} is given by

$$Z_{\text{eq}} = Z_1 || Z_2 = \frac{Z_1 Z_2}{Z_1 + Z_2} = \frac{X_1\left(R_2^2 + X_2^2\right) + X_2\left(R_1^2 + X_1^2\right) + \text{j}\left[R_1\left(R_2^2 + X_2^2\right) + R_2\left(R_1^2 + X_1^2\right)\right]}{(R_1 + R_2)^2 + (X_1 + X_2)^2}. \quad (6)$$

Regarding the resulting impedance as a capacitor with a series resistance, the resulting Q factor is given by

$$Q_{\text{eq}} = -\frac{\Im\left\{Z_{\text{eq}}\right\}}{\Re\left\{Z_{\text{eq}}\right\}} = -\frac{R_1\left(R_2^2 + X_2^2\right) + R_2\left(R_1^2 + X_1^2\right)}{X_1\left(R_2^2 + X_2^2\right) + X_2\left(R_1^2 + X_1^2\right)}. \quad (7)$$

To find the intersection point of Figure 2 in terms of the scaled fuse resistance, $r_{\text{f, on}} = a_{\text{f}} R_{\text{f, on}}$, we set

$$Q_{\text{eq}}(a_{\text{f}})\Big|_{R_1 = r_{\text{f, on}}} = Q_{\text{eq}}(a_{\text{f}})\Big|_{R_1 = k_{\text{f}} r_{\text{f, on}}}, \quad (8)$$

where k_{f} is given by Equation (4) and a_{f} is the scaling factor which can be obtained by a series and/or parallel connection of fuses. Substituting Equation (7) into Equation (8) yields

$$-\frac{r_{\text{f, on}}\left(R_2^2 + X_2^2\right) + R_2\left(r_{\text{f, on}}^2 + X_1^2\right)}{X_1\left(R_2^2 + X_2^2\right) + X_2\left(r_{\text{f, on}}^2 + X_1^2\right)} = -\frac{k_{\text{f}} r_{\text{f, on}}\left(R_2^2 + X_2^2\right) + R_2\left(k_{\text{f}}^2 r_{\text{f, on}}^2 + X_1^2\right)}{X_1\left(R_2^2 + X_2^2\right) + X_2\left(k_{\text{f}}^2 r_{\text{f, on}}^2 + X_1^2\right)}. \quad (9)$$

Solving Equation (9) for $r_{\text{f, on}}$ yields

$$r_{\text{f, on}} = R_2 \frac{1}{2k_{\text{f}}} \frac{X_1}{X_2} \pm \sqrt{\left(R_2 \frac{1}{2k_{\text{f}}} \frac{X_1}{X_2}\right)^2 + \frac{1}{k_{\text{f}}}\left(R_2^2 \frac{X_1}{X_2} + X_1 X_2 + X_1^2\right)}. \quad (10)$$

Relating this expression to Figure 1, we substitute $X_1 = -1/(\omega C_n)$, $X_2 = -1/(\omega C)$ and $R_2 = R$, where C_n is the added capacitance in the branch currently being added, C is the base capacitance

including all thus far added branches, R is the resistance in series with C resulting from all fuse resistances from all thus far added branches and ω is the angular frequency under which the circuit is intended to operate. Thus, $r_{\mathrm{f,\,on}}$ as a function of branch number, n, can be written as

$$r_{\mathrm{f,\,on}}(n) = R\frac{1}{2k_\mathrm{f}}\frac{C}{C_n} \pm \sqrt{\left(R\frac{1}{2k_\mathrm{f}}\frac{C}{C_n}\right)^2 + \frac{1}{k_\mathrm{f}}\left(R^2\frac{C}{C_n} + \frac{1}{\omega^2 C C_n} + \frac{1}{\omega^2 C_n^2}\right)}. \tag{11}$$

Let Q represent the Q factor given by the series combination of C and R. Then, $Q = 1/\omega CR$. Substituting this expression into Equation (11) yields

$$r_{\mathrm{f,\,on}}(n) = R\frac{1}{2k_\mathrm{f}Q\omega C_n} \pm \sqrt{\left(\frac{1}{2k_\mathrm{f}Q\omega C_n}\right)^2 + \frac{1}{k_\mathrm{f}\omega C_n}\left[R\left(Q + \frac{1}{Q}\right) + \frac{1}{\omega C_n}\right]}. \tag{12}$$

For practical component values, the inequalities $Q \gg 1/Q$ and

$$2k_\mathrm{f}Q^2 \gg \frac{1}{R(Q + 1/Q)\omega C_n + 1} \tag{13}$$

hold and because $r_{\mathrm{f,\,on}} > 0$, Equation (12) reduces to

$$r_{\mathrm{f,\,on}}(n) \approx \sqrt{\frac{1}{k_\mathrm{f}\omega C_n}\left(RQ + \frac{1}{\omega C_n}\right)} = \sqrt{\frac{1}{k_\mathrm{f}\omega C_n}\left(\frac{1}{\omega C} + \frac{1}{\omega C_n}\right)}. \tag{14}$$

Thus we have arrived at an expression for how to select the scaled fuse resistance, $r_{\mathrm{f,\,on}}(n)$, when adding one fuse-controlled branch to the base capacitance.

2.3. Q Factor Optimisation for Multiple Branches

In order to find $r_{\mathrm{f,\,on}}(n)$ for the fuses in each branch, one possible solution is to use Equation (14) recursively for all the branches. However, there is a challenge associated with this approach. Consider adding the first branch to the base capacitance. In this case, it is obvious which value to use for C. However, for the next branch, C might take on two different values depending on whether the fuse will be active or blown in the first branch, so we would also need to consider the case for when C is substituted for $C + \Delta C$. When adding the third branch, there will be four possible values for C. In fact, the number of values would double for each new branch added.

Because of this complexity, we do not pursue this approach further. Instead, we use Equation (14) to obtain an expression for the Q factor, Q_n, of the branch being added when its fuse is active:

$$Q_n = \frac{1/\omega C_n}{r_{\mathrm{f,\,on}}(n)} = \sqrt{\frac{k_\mathrm{f}}{1 + \frac{C_n}{C}}}. \tag{15}$$

If only one branch would be added, we could use Equation (15) to know which Q factor it should have in its active state, which would in turn yield a value for $r_{\mathrm{f,\,on}}(n)$. However, as explained above, we don't know which value to use for C in the coming branches because the fuse configuration is unknown. Thus, it appears that we can only use Equation (15) to find $r_{\mathrm{f,\,on}}(n)$ for one of the branches.

However, consider the case when all branches have the same Q factor with all fuses active. We denote this Q factor Q_on. The equivalent Q factor does not change if multiple branches with identical Q factor are connected in parallel. Therefore, for a certain fuse configuration, we would have one equivalent Q factor, Q_on, for all active branches and one equivalent Q factor, Q_off, for all blown branches. Because the Q factor is inversely proportional to the branch resistance, $Q_\mathrm{on} = k_\mathrm{f}Q_\mathrm{off}$. If we attempt to increase Q_on by increasing the Q factor for a single branch, the Q factor for that branch in its blown state will also increase. While this would result in an increased Q_eq for when this branch is

active, it would decrease it for when it is blown. Refer to Figure 2 and note that at the intersection point, an increased Q_{on} would mean a decreased a_{f} and thus a decreased scaled fuse resistance, $r_{\text{f, on}}(n)$. Following the blue solid line from the intersection point for decreasing a_{f} yields a higher Q_{eq}. However, for Q_{off}, following the red dashed line for decreasing a_{f} yields a lower Q_{eq}.

Similarly, we could try to increase the worst-case Q_{eq} by increasing Q_{off}. However, this would also increase it for Q_{on} and, by the same reasoning as before, would result in a lower worst-case Q_{eq}. Attempting to change the fuse resistance for multiple branches simultaneously will also not improve the worst-case Q_{eq} because for the worst-case, the fuse state resulting in the lowest Q_{eq} will be in use for each branch. Thus, we conclude that Q_{eq} will be maximised when all branches have the same Q factor. This Q factor can be found by considering the equivalent circuit for all branches with the fuses in their active state and then using Equation (15) and substituting C_n for the equivalent parallel resistance for the branches, ΔC, to find the Q factor for a branch, $Q_{\text{branch}} = Q_n$, for all n:

$$Q_{\text{branch}} = \sqrt{\frac{k_{\text{f}}}{1 + \frac{\Delta C}{C}}}. \tag{16}$$

Equations (15) and (16) can then be used to find $r_{\text{f, on}}(n)$ as

$$r_{\text{f, on}}(n) = \frac{1}{Q_{\text{branch}}} \frac{1}{\omega C_n} = \frac{1}{Q_{\text{branch}}} \frac{2^n}{\omega C_x}. \tag{17}$$

This is an expression for the scaled fuse resistance, $r_{\text{f, on}}(n)$, for each branch, which yields the maximal worst-case equivalent Q factor, Q_{eq}. Here, $C_n = C_x/2^n$ was used in order to obtain an expression for $r_{\text{f, on}}(n)$ as a function of C_x. It should be noted that if the exact value for $r_{\text{f, on}}(n)$ required by Equation (17) cannot be obtained because a prohibitively large number of fuses would be required, an error will be introduced in Q_{branch}. Because the Q factor of a capacitor is given by its reactance divided by its resistance (that is, in the case for Q_{branch}, divided by $r_{\text{f, on}}(n)$), the relative error in the worst-case Q_{branch} will be no greater than the relative worst-case error in $r_{\text{f, on}}(n)$, or equivalently, no greater than the relative error in the fuse scaling factor, a_{f}, in the fuse with the largest relative scaling mismatch.

To obtain an expression for the resulting worst-case equivalent Q factor when a fuse-controlled branch is connected in parallel with the base capacitance, C, we use Equation (7) and substitute

$$R_1 = r_{\text{f, on, eq}} = \frac{1}{Q_{\text{branch}}} \frac{1}{\omega \Delta C}, \tag{18}$$

$$R_2 = 0, \tag{19}$$

$$X_1 = \frac{1}{\omega \Delta C}, \tag{20}$$

$$X_2 = \frac{1}{\omega C}, \tag{21}$$

where $r_{\text{f, on, eq}}$ is the scaled fuse on-resistance obtained for a branch with ΔC as series capacitance. The resulting expression is given by

$$Q_{\text{eq}} = Q_{\text{branch}} \left(1 + \frac{C}{\Delta C}\right) + \frac{1}{Q_{\text{branch}}} \frac{C}{\Delta C}. \tag{22}$$

Inserting Equation (16) into Equation (22) and making the assumption that $Q_{\text{branch}} \gg 1$ yields

$$Q_{\text{eq}} \approx \left(1 + \frac{C}{\Delta C}\right) \sqrt{\frac{k_{\text{f}}}{1 + \frac{\Delta C}{C}}} = \sqrt{k_{\text{f}} \frac{(1 + C/\Delta C)^2}{1 + \Delta C/C}}. \tag{23}$$

From Equation (23) it can be seen that increasing the ratio of base capacitance to trim capacitance, $C/\Delta C$, increases Q_{eq}. This is intuitive because that increases the ratio of capacitance contributed by capacitors with no series resistance to capacitance contributed by capacitors with series resistance. It can also be seen that a higher ratio, k_{f}, between off and on resistance for the fuses used will increase Q_{eq}, which is also intutive because higher quality fuses should yield better Q factors.

It is interesting to note that highest possible worst-case Q factor, Q_{eq}, depends only on the ratio between desired base and trim capacitance as well as on the ratio of resistance between blown and active fuses for the process technology and is thus frequency-independent.

3. Capacitance Accuracy

Because C_{eq} is the result of connecting a capacitor with no series resistance in parallel to a number of capacitors with series resistance, the resulting capacitance value will not be exactly equal to the target capacitance. Another contribution to the mismatch in capacitance comes from parasitic elements such as bond pads used to program (blow) the fuses. In this section, we quantify these mismatches.

3.1. Effects of Fuse Resistance

Consider adding a single branch to the base capacitance, C. If the fuse for that branch is active, the contributed capacitance will be slightly lower than the actual value of the capacitor in that branch, C_n, because of the series resistance of the branch. On the other hand, if the fuse for that branch is blown, the intent is that no capacitance should be contributed, but because of the finite fuse resistance, indeed some capacitance will be contributed. Thus, we see that active branches contribute too little capacitance, whereas blown branches contribute too much capacitance. The magnitude of the mismatch of target capacitance to actual capacitance will thus be largest either for all fuses active or for all fuses blown.

For the case for all fuses active, the equivalent impedance, Z_{eq}, can be found from Equation (6). Since we are only interested in the difference in *capacitance*, we are only interested in the reactive part of Z_{eq}. Using the substitutions in Equations (18)–(21), it can be shown that the reactive part of Z_{eq} is given by

$$\hat{X}_{\text{eq}} = -\frac{\left(1+\frac{1}{Q_{\text{branch}}^2}\right)\frac{1}{\omega\Delta C}+\frac{1}{\omega C}}{\left(1+\frac{1}{Q_{\text{branch}}^2}\right)\frac{C}{\Delta C}+\frac{\Delta C}{C}+2}. \tag{24}$$

The maximum difference between the target capacitance, $(C+\Delta C)$, and the capacitance contributed by $\hat{X}_{\text{eq}}$ is given by

$$\hat{C}_{\text{error}} = (C+\Delta C) - \left(-\frac{1}{\omega \hat{X}_{\text{eq}}}\right). \tag{25}$$

Substituting Equation (24) into Equation (25) yields, after some algebra,

$$\hat{C}_{\text{error}} = \frac{1}{Q_{\text{branch}}^2+1}\frac{\left(1+\frac{1}{Q_{\text{branch}}^2}\right)C\cdot\Delta C}{\left(1+\frac{1}{Q_{\text{branch}}^2}\right)C+\Delta C}, \tag{26}$$

which for $Q_{\text{branch}}^2 \gg 1$ reduces to

$$\hat{C}_{\text{error}} \approx \frac{1}{Q_{\text{branch}}^2}\frac{C\cdot\Delta C}{C+\Delta C}. \tag{27}$$

Thus, we have arrived at an expression for the maximum error in capacitance, $\hat{C}_{\text{error}}$, for all fuses active. It is interesting to note that Equation (27) can be interpreted as follows: The maximum error in

capacitance equals the equivalent capacitance of two series-connected capacitors of capacitance C and ΔC, respectively, scaled by the factor $1/Q_{\text{branch}}^2$.

An expression for for the equivalent reactance for the case for all fuses blown, here denoted $\check{X}_{\text{eq}}$, can be obtained from Equation (6) using the substitutions in Equations (19)–(21), and substituting

$$R_1 = k_{\text{f}} r_{\text{f, on, eq}} = \frac{k_{\text{f}}}{Q_{\text{branch}}} \frac{1}{\omega \Delta C}. \tag{28}$$

Utilising Equation (16) and solving for k_{f}, $\check{X}_{\text{eq}}$ is given as

$$\check{X}_{\text{eq}} = -\frac{\left[1 + Q_{\text{branch}}^2 \left(1 + \frac{\Delta C}{C}\right)\right] \frac{1}{\omega \Delta C} + \frac{1}{\omega C}}{\left[1 + Q_{\text{branch}}^2 \left(1 + \frac{\Delta C}{C}\right)\right] \frac{C}{\Delta C} + \frac{\Delta C}{C} + 2}. \tag{29}$$

The maximum difference between the target capacitance, C, and the capacitance contributed by $\check{X}_{\text{eq}}$ is given by

$$\check{C}_{\text{error}} = C - \left(-\frac{1}{\omega \check{X}_{\text{eq}}}\right). \tag{30}$$

It can be shown that substituting Equation (29) into Equation (30) yields

$$\check{C}_{\text{error}} = -\frac{1}{Q_{\text{branch}}^2 + 1} \frac{\left(1 + \frac{1}{Q_{\text{branch}}^2}\right) C \cdot \Delta C}{\left(1 + \frac{1}{Q_{\text{branch}}^2}\right) C + \Delta C}, \tag{31}$$

which is exactly equal in magnitude to $\hat{C}_{\text{error}}$ in Equation (26), but with opposite sign; $\check{C}_{\text{error}} = -\hat{C}_{\text{error}}$. The error in capacitance for any fuse configuration, C_{error}, will thus lie within the interval

$$-\hat{C}_{\text{error}} \leq C_{\text{error}} \leq \hat{C}_{\text{error}}. \tag{32}$$

In assessing the accuracy we have neglected the effects of capacitance variations with respect to process, voltage and temperature. As stated in the introduction, we recommend using MIM capacitors to realise the trim capacitor presented in this work because of their temperature and voltage stability [10]. However, the capacitors will still be subject some variation, especially as a result of variations in the manufacturing process. Because fuses are one-time programmable, they can not be used to compensate for variations in temperature or voltage which change over time, but they can be used to compensate for process variation. As an example, consider the application of an LC resonator discussed in the introduction. If the low-frequency inductance and the untrimmed resonant frequency are measured, the base capacitance, C, can be estimated from the resonance equation:

$$f_0 = \frac{1}{2\pi\sqrt{LC}}, \tag{33}$$

where f_0 is the resonant frequency and L is the inductance of the resonator. When C is known, Equation (33) can be used again to calculate the value needed for the trim capacitance, ΔC, in order to realise the desired value for f_0. If care is taken when designing the chip layout, the variations between C and ΔC can be matched to a high degree of accuracy and thus by estimating C, an estimation for ΔC can also be obtained.

However, if the on-chip inductance can not be measured with sufficient accuracy or if the parasitic capacitance of the inductive element is significant, a two-step (or multi-step) procedure could be performed in order to estimate values for the reactive elements. One measurement of f_0 could be taken before fuse-programming and a second one after blowing the most significant fuse, F_0.

Then, a least-squares approximation could be performed in order to obtain estimations of the sought values. However, for this case, because F_0 is used for parameter estimations instead of for trimming, the Q factor of the resulting capacitor would decrease compared to a single-step estimation procedure.

3.2. Parasitic Bond Pad Capacitance

To program (blow) a fuse, a large current is required. The current can be supplied through probe needles touching bond-pads on both sides of a fuse during factory testing. However, because bond-pads typically present a parasitic capacitance to ground on the order of hundreds of femtofarads, they can be an obstacle for the accuracy of the trimmable capacitor. This effect becomes significant when the bond pad capacitance becomes comparable to the smallest capacitor in the circuit, $C_{m-1} = C_x/2^{m-1}$. Note also that if a fuse consists of multiple fuses in series, an additional bond pad will be required for each series connection in order to be able to blow every fuse.

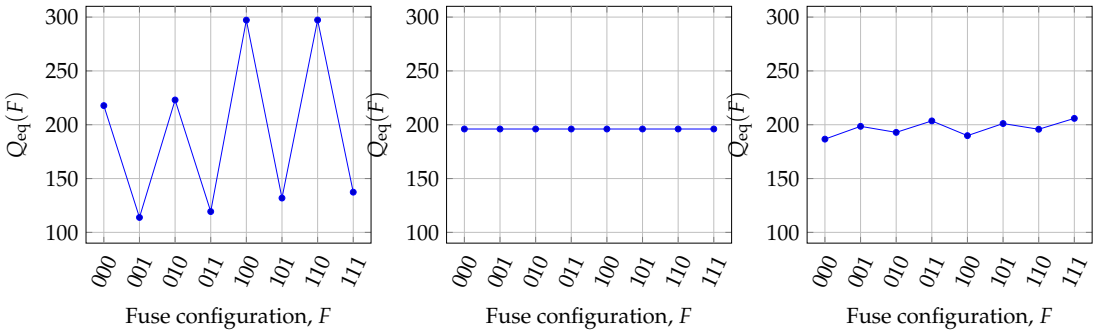
If a higher resolution is required than what a bond pad-based system can provide, probe pads could be used instead. Probe pads can typically be made small enough to present a parasitic capacitance to ground of the order of only a few femtofarads.

Another possibility is to let the programming of fuses be controlled by transistors. However, the ratio of capacitance to current-driving capability of transistors as well as the current required to blow a fuse is very dependent on process technology, and thus we do not attempt to assess the viability of this idea further in this work.

4. Discussion and Examples

In this section we discuss the performance of the circuit of this work by relating it to an example application.

Consider an application where we need a base capacitance, C, of 3 pF and a trim capacitance, ΔC, of 1 pF with a 3-bit resolution and at an operating frequency of 433 MHz. We thus use the circuit in Figure 1 and choose $C_x = 571$ fF according to Equation (3). The resolution is thus $C_{\text{res}} = C_2 = C_x/2^2 = 143$ fF. The question arises on how to select the scaled fuse resistance for the different fuses, $r_{\text{f, on}}(n)$. Consider first the naive design in which all fuses have the same resistance and consist only of a single fuse whose resistance is $R_{\text{f, on}} = 25\,\Omega$ while active and $R_{\text{f, off}} = 80\,\text{k}\Omega$ while blown. Figure 3a shows the resulting equivalent Q factor, $Q_{\text{eq}}(F)$, as a function of fuse configuration, F. Here, F is represented by a 3-bit binary number where 1 signifies an active fuse and 0 signifies that a fuse is blown. While the best-case Q factor is high at $Q_{\text{eq}}(110) = 297$, the worst-case Q factor is much lower at $Q_{\text{eq}}(001) = 114$.



(**a**) Naive design (**b**) Ideal design (**c**) Practical design

Figure 3. Equivalent Q factor, $Q_{\text{eq}}(F)$, of a trimmable capacitor of $C = 3$ pF and $\Delta C = 1$ pF, operating at 433 MHz as a function of the configuration of 3 fuses, represented by a binary number, F, where the nth bit represents fuse n, F_n. $F_n = 1$ signifies an active fuse, while $F_n = 0$ signifies that fuse n is blown. Plots are shown for three designs: (**a**) The naive design, where all fuses have the same resistance, R_{f}; (**b**) The ideal design, where all fuses have been scaled to their optimal resistance $r_{\text{f}} = a_{\text{f}} R_{\text{f}}$; and (**c**) The practical design, where all the fuses consist of series/parallel combinations of one or two fuses of resistance R_{f} in order to approximate $r_{\text{f, on}}$.

A more balanced equivalent Q factor can be achieved if Equations (16) and (17) are used to obtain an expression for the scaled fuse resistance, $r_{\mathrm{f,\,on}}(n)$. Using these equations, we get

$$r_{\mathrm{f}}(0) = 13.13\,\Omega, \tag{34}$$
$$r_{\mathrm{f}}(1) = 26.26\,\Omega, \tag{35}$$
$$r_{\mathrm{f}}(2) = 52.52\,\Omega. \tag{36}$$

Figure 3b shows the resulting Q factor, $Q_{\mathrm{eq}}(F)$, as a function of F. It can be seen from the figure that the Q factor is constant independent of fuse configuration and that the worst-case Q factor has been increased to $Q_{\mathrm{eq}}(F) = 196$, a 72 % increase compared to the naive design. Note that, as expected, this value for Q_{eq} coincides with the value at the intersection point of Figure 2.

The improvement results from the fact that we have identified that some configurations yield a much higher Q factor than others and made appropriate adjustments. By sacrificing the Q factor of the good configurations we have increased it for the worse ones resulting in a better Q factor for the worst case. The variation of the Q factor from 114 to 297 has been reduced to no variation at all.

Because of the potential high fuse count, it may be impractical to realise the values for $r_{\mathrm{f,\,on}}(n)$ in Equations (34)–(36) to a high degree of accuracy with a series/parallel combination of a single fuse resistance, $R_{\mathrm{f,\,on}}$. However, the following combinations yield values that are within 6 % of the desired ones using only one or two fuses for each branch:

$$r_{\mathrm{f,\,on}}(0) = (25\,\Omega)||(25\,\Omega) = 12.5\,\Omega, \tag{37}$$
$$r_{\mathrm{f,\,on}}(1) = 25\,\Omega, \tag{38}$$
$$r_{\mathrm{f,\,on}}(2) = 25\,\Omega + 25\,\Omega = 50\,\Omega. \tag{39}$$

Figure 3c shows the resulting equivalent Q factor, $Q_{\mathrm{eq}}(F)$. The worst-case value has now decreased to $Q_{\mathrm{eq}}(000) = 187$, a 5 % decrease compared to the ideal design. A result of this deviation from the ideal is that the Q factor is once again not completely constant.

The number of bond pads required to be able to blow all fuses amounts to 6 because there are a total of 5 fuses in the circuit and one additional bond pad for the current return path is required. Standard-size bond pads for a 180 nm process present a capacitance to ground around of 140 fF per pad. The total amount of capacitance from bond pads would thus be much larger than $C_{\mathrm{res}} = 143$ fF and we would need to consider a different approach. Scaling down the pad area to 10×10 µm^2, probe pads with a capacitance of approximately 3.5 fF per pad can be manufactured. Using such pads to program the fuses results in a total parasitic capacitance contribution from pads of maximum 21 fF, which is about a factor of 7 smaller than the resolution, C_{res}. The variation in capacitance due to the non-ideal Q factors of the trim branches amounts to 344 aF, close to the ideal case of 312 aF, calculated from Equation (26), which is far below the intended resolution.

In the previous example, the worst-case Q factor for the naive design is smaller than that for the practical design, however, not by a huge factor. This is because the process parameters, $R_{\mathrm{f,\,on}}$ and $R_{\mathrm{f,\,off}}$, the desired base and trim capacitances, C and ΔC, number of bits, m, as well as the operating frequency happen to be of values which are beneficial for high Q factors. Consider what would happen if both specified capacitances, C and ΔC, are decreased by a factor of 10. Equations (16) and (17) show that significantly larger values would be needed for the scaled fuse resistance, $r_{\mathrm{f,\,on}}(n)$. Figure 4 shows the equivalent Q factor, $Q_{\mathrm{eq}}(F)$, as a function of fuse configuration, F, for $C = 300$ fF and $\Delta C = 100$ fF. Interestingly, identical graphs would be produced if either the operating frequency or $R_{\mathrm{f,\,on}}$ and $R_{\mathrm{f,\,off}}$ were decreased by a factor of 10 instead of C and ΔC. From the figure, it can be seen that the fuse configuration $F = 111$ achieves a much more favourable Q factor than the other configurations, with $Q_{\mathrm{eq}}(111) = 1370$. The worst-case Q factor is significantly lower at $Q_{\mathrm{eq}}(000) = 22.9$. Relating to Figure 2, the reason for this behaviour is that the fuse scaling factor, a_{f}, for each fuse is not high enough and the operating point ends up to the left of the intersection point yielding very high Q factors

for active fuses, but very low ones for blown fuses. Coming back to Figure 4, we see that only the case for all fuses active yields a high Q factor. By scaling the fuses appropriately and because the maximum worst-case Q factor is frequency-independent and constant for constant $k_f = R_{f,\,off}/R_{f,\,on}$ and $\Delta C/C$, we can again achieve the Q factors of Figure 3b with a worst-case (and best-case) Q factor of $Q_{eq}(F) = 196$.

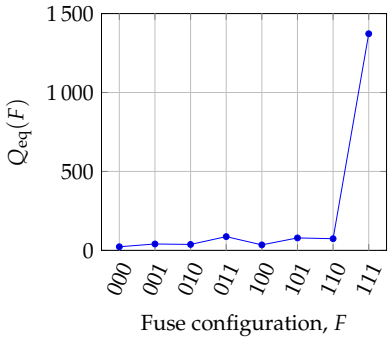


Figure 4. Equivalent Q factor, $Q_{eq}(F)$, of a trimmable capacitor as a function of the configuration of 3 fuses with the same resistance, R_f. All parameters are the same as in Figure 3a, except the specified capacitances, C and ΔC, have both been decreased by a factor of 10.

To illustrate what could happen if care is not taken to ensure a sufficiently high Q factor, consider what would happen if a state-of-the art coil was to be used with the capacitor from the last example to form an LC resonator. Q factors of on-chip coils of 11.05 [2] and 10.5 [3] operating at hundreds of MHz have been demonstrated. Connecting one such coil to a capacitor with a worst-case Q factor of 22.9, as in the example, the worst-case Q factor of the resulting LC circuit would be reduced by over 30 % compared to the original Q factor of the coil. However, if the method described in this work was to be used, the coils could be connected to a capacitor with a worst-case Q factor of 187 as in Figure 3c, reducing the worst-case Q factor of the resulting LC circuit by less than 6 %.

Another challenge arises when we attempt to implement a practical circuit approximating the ideal design for this case of smaller capacitances. For instance, the highest resistance we would need to realise is $R_2 = 525\,\text{k}\Omega$ for which 21 fuses would be needed. Such a circuit would require around 40 bond or probe pads which would present a relatively large parasitic pad capacitance, 140 fF in the worst case, to the trim capacitor, limiting the resolution. Since the desired resolution is even less than that at 100 fF, the circuit designers should consider accepting a lower resolution, reducing the number of bits and/or reducing the base capacitance, C.

The requirement of high numbers of series fuses arises when the largest scaled fuse resistance, $r_{f,\,on}(m-1)$, becomes much larger than $R_{f,\,on}$. Equations (16) and (17) show that this occurs when

$$\frac{2^{m-1}}{\omega C_x}\sqrt{\frac{1+\frac{\Delta C}{C}}{k_f}} \gg R_{f,\,on}. \tag{40}$$

Thus, for higher frequencies, larger specified capacitances, larger fuse resistances or a fewer number of bits than for the previous example, a high number of series fuses would not be an issue. In this case, most fuses will be required in parallel instead, to achieve sufficiently low values for $r_{f,\,on}(n)$.

5. Conclusions

In this paper, we present a circuit implementing a fuse-based IC trimmable capacitor. A theory is presented on how to choose fuse resistances in order to achieve the highest possible worst-case Q factor for the capacitor. One advantage of a fused-based approach is that it is cheaper than the

alternative method of laser trimming. The theory presented in this work is novel in that, to the authors' knowledge, high-Q, fuse-based trimmable IC capacitors have not previously been published.

We show that proper selection of fuse resistances not only maximises the worst-case Q factor, but also makes it constant and independent of fuse configuration. This makes it possible to build applications such as on-chip tunable LC resonant circuits with a predictable Q factor that is independent of tuned frequency without resorting to laser trimming.

Furthermore the accuracy of the capacitance is discussed and it is concluded that capacitance from bond pads may be a limiting factor. This limitation can to some extent be overcome by the use of smaller, low capacitance probe pads.

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