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A 2.5-GHz 1-V High Efficiency CMOS Power Amplifier IC with a Dual-Switching Transistor and Third Harmonic Tuning Technique

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Abstract: This paper presents a 2.5-GHz low-voltage, high-efficiency CMOS power amplifier (PA) IC in 0.18-μm CMOS technology. The combination of a dual-switching transistor (DST) and a third harmonic tuning technique is proposed. The DST effectively improves the gain at the saturation power region when the additional gain extension of the secondary switching transistor compensates for the gain compression of the primary one. To achieve high-efficiency performance, the third harmonic tuning circuit is connected in parallel to the output load. Therefore, the flattened drain current and voltage waveforms are generated, which in turn reduce the overlapping and the dc power consumption significantly. In addition, a 0.5-V back-gate voltage is applied to the primary switching transistor to realize the low-voltage operation. At 1 V of supply voltage, the proposed PA has achieved a power added efficiency (PAE) of 34.5% and a saturated output power of 10.1 dBm.

Keywords: dual-switching transistor; third harmonic tuning; low voltage; high efficiency; CMOS power amplifier IC

1. Introduction

For modern communication systems, such as short-range wireless applications, a high-efficiency power amplifier plays an important role in maintaining the battery life. To increase the efficiency, switching-mode amplifiers, such as class-E and class-F, are widely used [1–4]. By minimizing the overlap between the drain current and voltage waveforms, the dc power dissipation of the amplifiers can be diminished. The output power of switching-mode amplifiers is also comparable to current-mode ones for the same device peak voltage and current [5].

Unfortunately, efficiency and supply voltage represent a trade-off in switching-mode power amplifiers (PAs). Several techniques have been proposed for improving efficiency at low supply voltages [6–11]. The fully integrated PAs with a power combiner, such as multiple LC baluns [6], a transformer [7], and a distributed active transformer [8,9], were proposed to boost the power added efficiency (PAE) at low supply voltages. PAE is the ratio of the produced signal power (the difference between the output and input power) and the dc power consumption. However, large combiners lead to high insertion losses and enlarge the chip size. Another approach to increase the efficiency of a low supply voltage PA is an injection-locking technique [10,11]. Although this technique provides high gain and high efficiency, the circuit is complicated.

The harmonic manipulation techniques, such as class-J [12] and a tuned amplifier [13–15], are also attractive to improve efficiency. However, class-J employs only second harmonic tuning at the output port, while the tuned amplifier in [15] utilizes second and third harmonic tuning at the input and

output ports. Both of the techniques increase the fundamental output power with high efficiency. The amplifier using a second harmonic short in [16] has a higher output power capability of 6.6% than the conventional class-E amplifier. However, the peak drain voltage increases significantly.

In this work, a high-efficiency CMOS PA IC operating at a low supply voltage is proposed using 0.18-μm CMOS technology. To boost the PAE, a dual-switching transistor (DST) was adopted in combination with a third harmonic tuning technique [17]. The class-E PA topology was employed as a basic structure, and 0.5-V positive, back-gate voltage was injected for low-voltage operation. A detailed theoretical and circuit analysis was performed, and the optimum circuit parameters were derived.

This paper is organized as follows. In Section 2, the circuit analysis of the proposed configuration is described, and the optimum circuit parameters are derived. Section 3 shows the simulation results of the proposed PA. Section 4 discusses the measurement results and compares them with recently reported PAs. Our conclusions are presented in Section 5.

2. Circuit Analysis

2.1. Dual-Switching Transistor (DST)

Figure 1a,b show the operation principle and the input/output characteristics of the DST structure, respectively. The structure consists of two switching transistors: (1) the primary switching transistor M_1 biased at class-AB and (2) the secondary switching transistor M_2 biased at class-B, which are connected in parallel. Only single input and output matching circuits were employed, thus providing less complexity for the single chip implementation. To realize the class-AB operation of M_1, the positive back-gate voltage V_{bg} was injected. Hence, the threshold voltage decreased so that the overdrive voltage of M_1 would be sufficient for the class-AB operation.

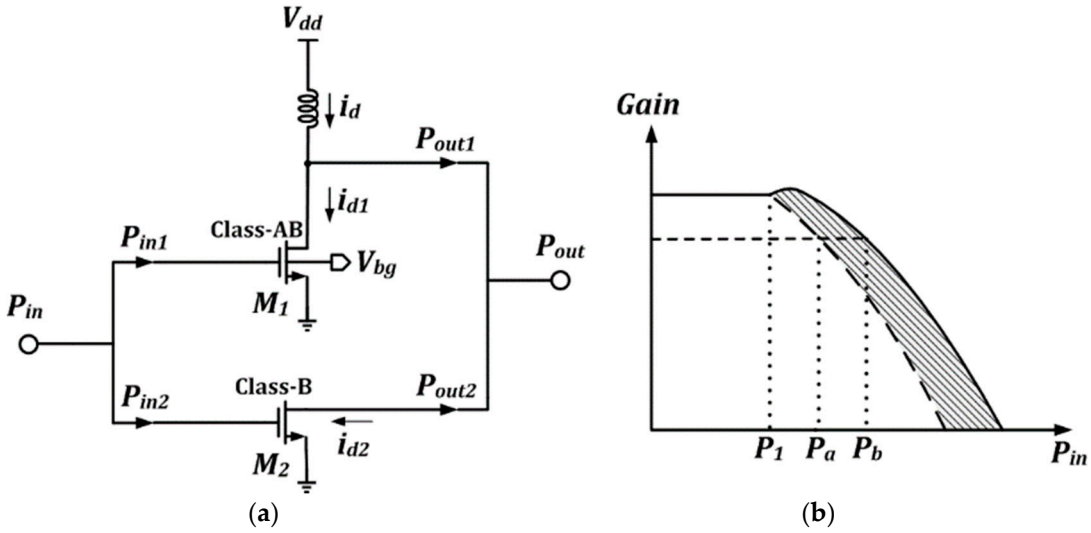

Figure 1. (**a**) Operation principle and (**b**) Input/output characteristics of the dual-switching transistor (DST).

At small input power ($P_{in} < P_1$), the total output power is mainly contributed by M_1 ($P_{out} = P_{out1}$), because M_1 is in active operation. In this condition, the total dissipation power P_{DC} of the amplifier is equal to $V_{dd}I_{d1}$.

At large input power ($P_{in} > P_1$), both of the switching transistors are active. M_1 operates near the saturation power level and corresponds to its output power ($P_{out1} = P_{sat1}$), while M_2 delivers the output power of P_{out2}. Therefore, the total output power of the amplifier P_{out} is the sum of the two transistors ($P_{sat1} + P_{out2}$). To maximize the PAE, the size of M_2 is set to be sufficiently smaller than M_1, hence the $i_{d2} << i_{d1}$ and P_{DC} is expected to be slightly higher than $V_{dd}I_{d1}$. The overlapping between the drain voltage and current waveforms of the DST should be minimized by adjusting the conduction

angle of M_2. Consequently, the PAE at the saturation power level is approximately represented as follows:

$$PAE = \frac{(P_{sat1} + P_{out2}) - P_{in}}{V_{dd} I_{d1}} * 100\%. \quad (1)$$

In addition, the additional gain expansion generated at the saturation power level by the DST (shaded area in Figure 1b) improves the linearity of the amplifier, $P_b > P_a$, where P_b is the input P1dB of the proposed amplifier and P_a is the input P1dB of the conventional class-AB amplifier.

2.2. Third Harmonic Tuning Technique

The third harmonic tuning technique shapes the voltage and current waveforms of the switching transistor at the drain node to minimize the dc power dissipation [18]. The technique is realized by connecting a series C_3–L_3 resonated at $3f_o$ to the output node of the conventional class-E amplifier, as shown in Figure 2. Due to the resonator C_3–L_3, under specified conditions, the third harmonic component of the drain voltage and current waveforms can be controlled.

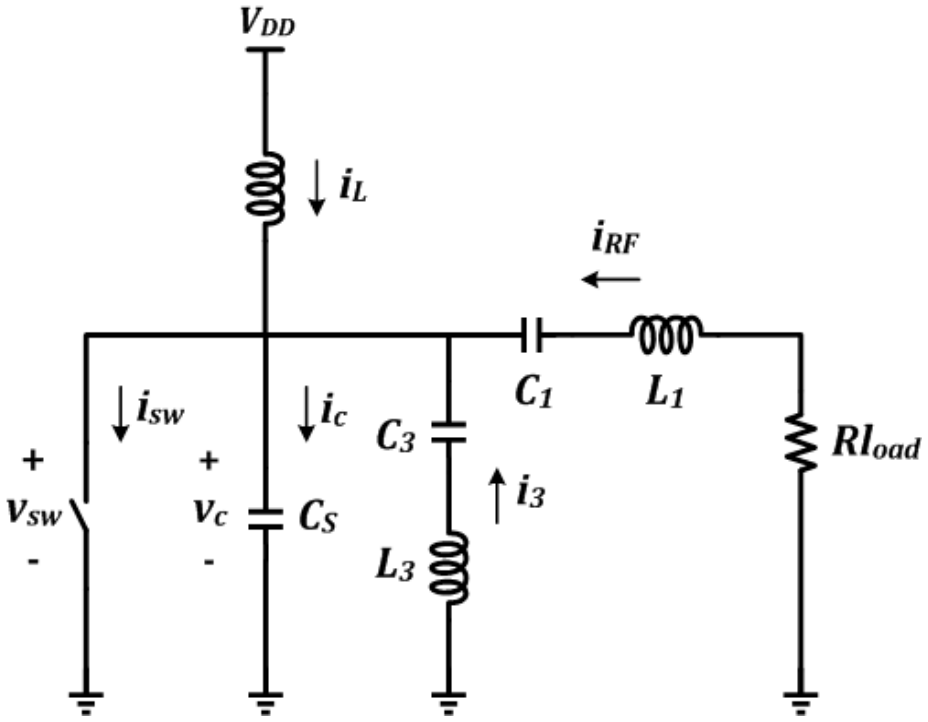

Figure 2. Basic configuration of the third harmonic tuning circuit.

Based on a zero-voltage switching (ZVS) condition, a series of mathematical analyses was conducted to describe the operation principle of the amplifier with the third harmonic tuning circuit. The following assumptions were considered: (1) the transistor is an ideal switch, and (2) all passive elements are lossless and linear. For the operation, the transistor was driven at frequency *fo* and at 50% of the duty cycle (on at $0 \leq \omega t < \pi$ and off at $\pi \leq \omega t < 2\pi$).

The loaded Q-factor of C_1–L_1 and C_3–L_3 were assumed to be infinite. The fundamental output current I_{RF} and the third harmonic current I_3 are represented as follows:

$$i_{RF}(\omega t) = I_{RF} \sin(\omega t + \theta). \quad (2)$$

$$i_3(\omega t) = I_3 \sin(3\omega t). \quad (3)$$

2.2.1. On-State Condition, $0 \leq \omega t < \pi$

When the switch is turned on, the current flowing to the capacitor i_c is equal to 0. Therefore, the capacitor voltage v_c is equal to 0. At this interval, the current that flows to the switch i_{sw} is given by

$$i_{SW}(\omega t) = I_L + I_{RF}\sin(\omega t + \theta) + I_3\sin(3\omega t) \tag{4}$$

where I_L and θ denote the dc current and the initial phase angle, respectively.

Due to the characteristics of the shunt capacitor C_s, the initial current of i_{sw} during the on/off transition is zero. Hence, the following is true:

$$\frac{I_L}{I_{RF}} = -\sin\theta. \tag{5}$$

2.2.2. Off-State Condition, $\pi \leq \omega t < 2\pi$

When the switch is turned off, i_{sw} is equal to 0. Therefore, i_c can be defined as follows,

$$i_C(\omega t) = I_L + I_{RF}\sin(\omega t + \theta) + I_3\sin(3\omega t) \tag{6}$$

generating the voltage across the capacitor v_c as,

$$\begin{aligned} v_c(\omega t) &= \tfrac{1}{\omega C_s}\int_{\pi}^{\omega t} I_C(\omega t)d\omega t \\ &= \tfrac{1}{\omega C_s}\left\{ \begin{array}{c} I_L(\omega t - \pi) - \frac{1}{3}I_3(\cos 3\omega t + 1) \\ -I_R[\cos(\theta + \omega t) + \cos\theta] \end{array} \right\}. \end{aligned} \tag{7}$$

To solve the above equations, it is assumed that the real part of the third harmonic output impedance Z_3 is equal to zero. The Fourier series analyses for $v_c(\omega t)$ and $i_o(\omega t)$ are derived to obtain the third harmonic component. Note that $i_o(\omega t)$ is the sum of $i_{RF}(\omega t)$ and $i_3(\omega t)$, i.e.,

$$i_o(\omega t) = I_{RF}\sin(\omega t + \theta) + I_3\sin(3\omega t). \tag{8}$$

The third harmonic coefficient of v_c is given by

$$V_{c,3} = \frac{1}{2\pi}\int_{\pi}^{\omega t} v_c(\omega t)e^{-j3\omega t}d\omega t. \tag{9}$$

The third harmonic coefficient of i_o is expressed as

$$I_{o,3} = \frac{1}{2\pi}\int_{\pi}^{\omega t} i_o(\omega t)e^{-j3\omega t}d\omega t. \tag{10}$$

Substituting Equations (7)–(10), Z_3 can be obtained as

$$\begin{aligned} Z_3 &= \frac{V_{c,3}}{I_{o,3}} \\ &= \frac{j(-4jI_L + 3\pi jI_3 + I_L 3\pi - 2I_3 - 6I_{RF}\cos\theta)}{9I_3\pi\omega C} \end{aligned} \tag{11}$$

Setting the real part of Z_3 to zero and substituting Equation (5) for Equation (11) yields the following:

$$\frac{I_L}{I_3} = \frac{2}{3\pi + 6\cot\theta}. \tag{12}$$

The initial phase angle (θ) can be obtained by deriving the third harmonic coefficient of i_{sw}, as follows:

$$\begin{aligned} I_{sw,3} &= \frac{1}{2\pi}\int_0^{2\pi} i_{sw}(\omega t)e^{-j3\omega t}d\omega t \\ &= -j\left(\frac{I_L}{3\pi}+\frac{I_3}{4}\right) \end{aligned} \tag{13}$$

At the initial condition i_{sw} (0) = 0, we have the following:

$$\frac{I_3}{I_L} = \frac{4}{3\pi}. \tag{14}$$

Substituting Equation (12) with Equation (14) generates the initial phase angle θ of -35°. Thus, the ratio I_L/I_{RF} of 0.57 and I_L/I_3 of 2.34 are obtained.

Considering that 100% efficiency is realized when the total output power is equal to the dc power consumption, the following is true:

$$\begin{aligned} P_{DC} &= P_{out} \\ I_L V_{DD} &= \tfrac{1}{2} {I_{RF}}^2 R_{load} \end{aligned} \tag{15}$$

where V_{DD} can be defined by applying the Fourier series expansion to Equation (7), i.e.,

$$\begin{aligned} V_{DD} &= \frac{1}{2\pi}\int_0^{2\pi} v_{sw}(\omega t)d\omega t \\ &= -\frac{1}{\omega C_s}\left(\frac{I_3}{3}+I_{RF}\cos\theta\right) \end{aligned} \tag{16}$$

To realize a good switching condition, the optimum shunt capacitor C_s can be determined by substituting Equation (16) with Equation (15):

$$C_s = \frac{\pi \sin^2\theta}{\omega R_{load}}. \tag{17}$$

In the circuit implementation, C_s is set as the total external capacitance and output capacitance of the switching transistor.

2.2.3. Switching Waveforms

The normalized switching waveforms of drain current $i_{sw}(\omega t)$ for $0 \leq \omega t < \pi$ and drain voltage $v_c(\omega t)$ for $\pi \leq \omega t < 2\pi$ are given by using Equations (4), (7), and (16) and the ratio of I_L/I_{RF} and I_L/I_3 as follows:

$$\frac{i_{sw}(\omega t)}{I_L} = 1 - \sin\omega t\cot\theta - \cos\omega t + \frac{4}{3\pi}\sin 3\omega t \tag{18}$$

$$\frac{v_c(\omega t)}{V_{DD}} = \frac{(\pi-\omega t)+\frac{4}{9\pi}(\cos 3\omega t+1)-\cot\theta(\cos\omega t+1)+\sin\omega t}{\frac{4}{9\pi}-\cot\theta}. \tag{19}$$

Figure 3 illustrates the normalized drain voltage (dotted line) and current waveforms (solid line) during a time period T. Because the transistor is turned on at $0 \leq T < T/2$, there is no voltage across the switch and the current flowing to the switch consists of dc, fundamental, and the third harmonic components. Because the transistor is turned off at $T/2 \leq T < T$, all the currents flow to the shunt capacitor C_s. As shown in Figure 3, the third harmonic tuning technique flattens the waveforms and reduces the overlapping. Therefore, it is expected to achieve low dc power dissipation and high PAE. Because the technique only controls a single harmonic component at the output node, it offers a more suitable structure for single chip PA solutions than class F or class F^{-1}.

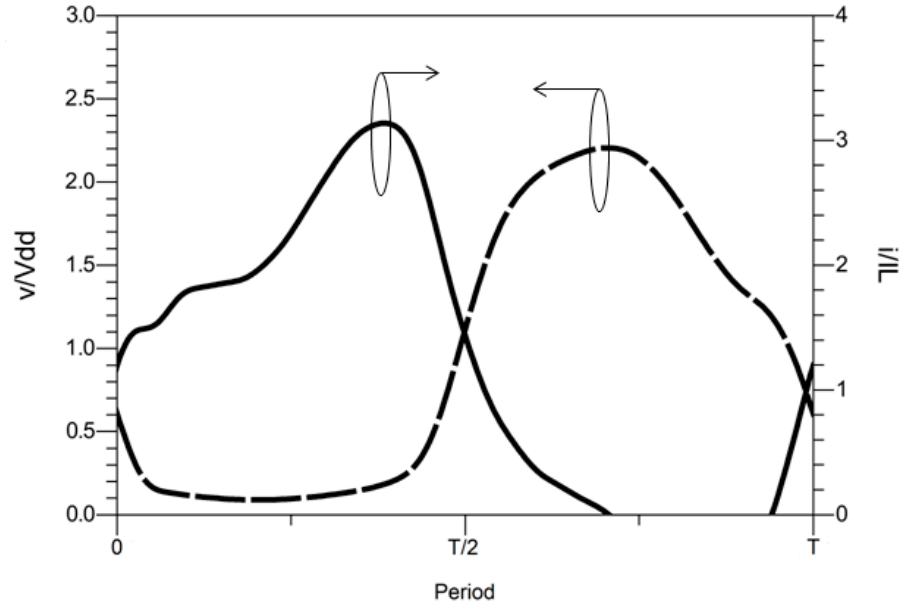

Figure 3. Simulated normalized switching waveforms.

Compared with the conventional class-E PA [19] and the second harmonic tuning PA [16], the PA with third harmonic tuning technique has a lower peak voltage waveform. The voltage stress of the switching transistor is reduced, and it is expected to get higher output power capability. For the CMOS process, the output power capability P_c calculates the maximum achievable output power for a given voltage stress V_{peak} and rms drain current I_{rms} and is expressed as follows:

$$P_C = \frac{P_{out}}{V_{peak} I_{rms}}. \tag{20}$$

The resonator C_3–L_3 induces a parasitic capacitance at the fundamental frequency and reduces the impedance at the output port. As a result, the loaded Q-factor of C_1–L_1, which is resonated at f_o, is decreased. The third harmonic resonator is designed by choosing an inductor with a high Q-factor at $3f_o$ as L_3. To compromise with the overall chip area and insertion loss, the layout dimension of the inductor is optimized. Then, the series capacitance C_3 is defined by the equation $C_3 = 1/9(\pi f_o)^2 L_3$. The parasitic capacitance of the resonator should be minimized to maintain the optimum shunt capacitance C_s of the amplifier. Consequently, by selecting the Q-factor of 10, the third harmonic resonator is optimized to L_3 = 2.5 nH and C_3 =180 fF.

2.3. Back-Gate Bias Technique

The back-gate bias technique is a method to modify the threshold voltage level and the on-resistance (R_{on}) of the MOSFET by connecting the body terminal to the positive or negative voltage. In this paper, a positive back-gate voltage was applied at the body of M_1 so that the threshold voltage and the R_{on} decreased. The technique led to the p-well of the body and n+ of the source being connected in a forward bias condition. Therefore, the positive back-gate bias voltage selection is very important to minimize an excessive dc leakage current from the body to the source [20]. A solid back-gate body potential should have an ideal connection to the ground, hence a large by-pass capacitance is placed between the body and the ground. Figure 4 shows the comparison between the positive back-gate voltage versus the threshold voltage at 0.5-V bias voltage.

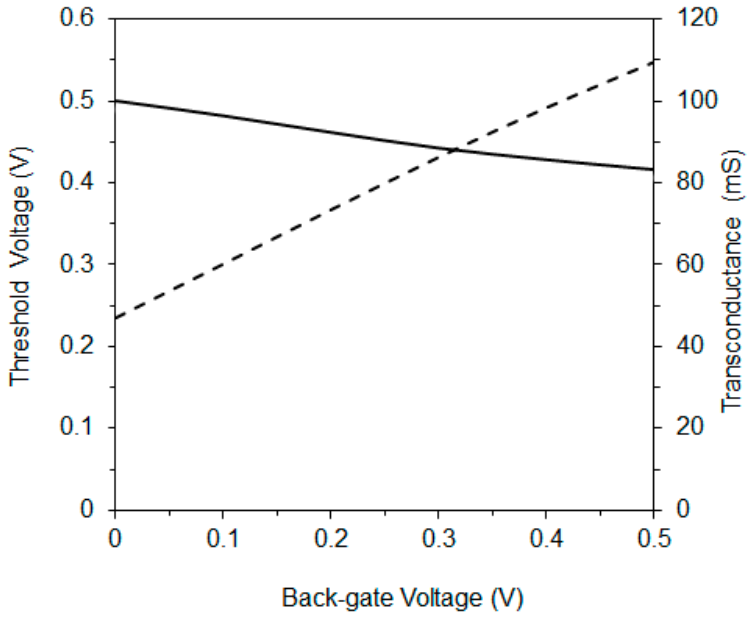

Figure 4. Simulated threshold voltage and transconductance versus back-gate voltage variations of the M_1 at 0.5-V bias voltage.

2.4. Circuit Configuration of the Proposed PA

Figure 5a shows the circuit schematic of the proposed CMOS PA IC. To achieve high PAE at a low supply voltage, a combination of the DST and the third harmonic tuning circuit (C_3–L_3) is proposed. The supply voltage V_{dd} of 1 V was applied with the bias voltage V_{bias} of 0.5 V. In addition, a 0.5-V positive body bias was injected into the body terminal (B) of M_1 by the external biasing terminal (V_{bg}) to decrease the threshold voltage level of 75 mV, which was optimum for the class-AB operation when there was no input power. In addition, the body of M_2 was connected to the ground for the class-B operation. The RC feedback network was employed to modify the input and the output resistance for the impedance matching requirement, as well as to increase the stability of the device; hence, the PA was always unconditionally stable.

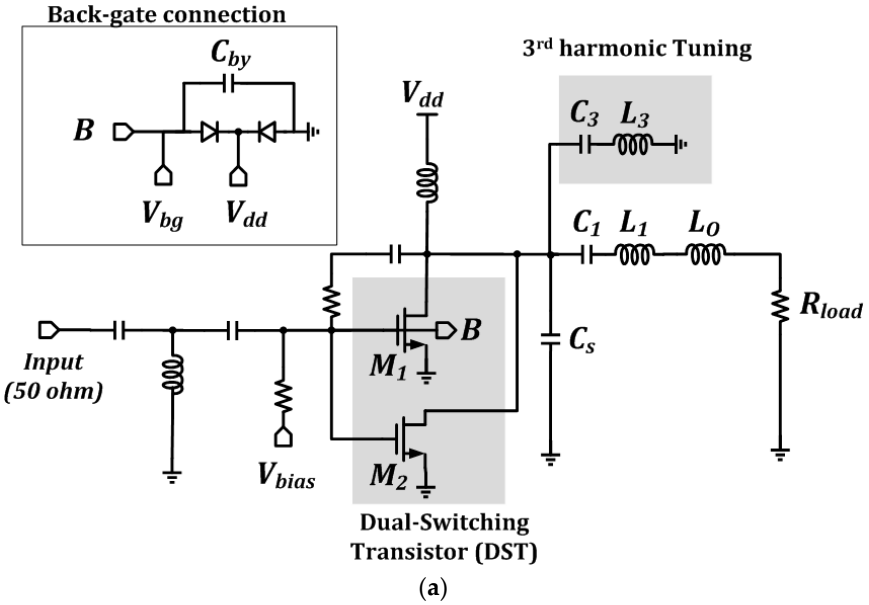

Figure 5. *Cont.*

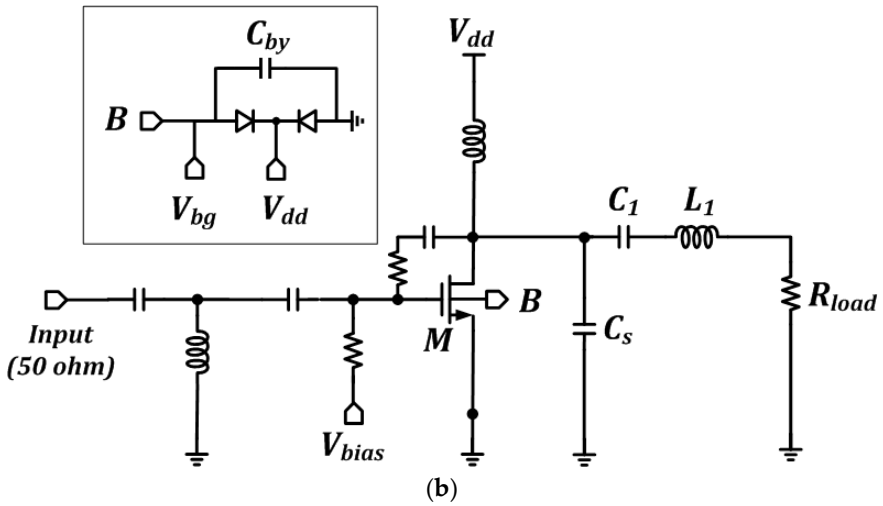

Figure 5. Circuit schematics of (**a**) the proposed power amplifier (PA) IC, and (**b**) the conventional class-E PA IC.

To minimize the drain loss, a large transistor size was selected. The large size, however, decreased the gain and increased the input power. In this work, the optimized total gate width of 464-μm with a gate length of 0.18-μm was utilized to obtain the power gain higher than 10 dB at 2.5-GHz. Because a large transistor size leads to high output capacitance, the shunt capacitor C_S was selected by considering the total output capacitance of the DST. Furthermore, the small inductor L_O was inserted at the output for impedance matching.

To verify the effectiveness of the proposed configuration, a 2.5-GHz conventional class-E PA was designed as illustrated in Figure 5b. The size of the switching transistor M was set equal to the total size of the switching transistors in the proposed PA. The 0.5-V back-gate voltage V_{bg} was injected, and the switching transistor was biased at class-AB with 1-V supply voltage

3. Simulation Results

The prototype of the proposed circuits was designed and fabricated using six metal layer (1P6M) 0.18-μm CMOS technology by TSMC. This CMOS process offered two ultra-thick top metal layers, 4-μm or 2-μm thick, for inductor implementation. High-density MIM capacitors of 1fF/μm^2 and 2fF/μm^2 were also provided. For noise isolation from the P-substrate, deep n-wells were available.

The small-signal and large-signal responses of the proposed PA IC were simulated on a wafer using ADS 2011 by Keysight [21] and Virtuoso ADE IC 6.1.5 by Cadence [22]. Input and output matching circuits were simulated and optimized using Momentum EM simulation in ADS 2011, while layout and verification were performed by Virtuoso ADE IC 6.1.5, respectively.

Figure 6 illustrates the small-signal input–output response of the proposed PA IC. The S_{11} and the S_{22} are −13.9 dB and −12.5 dB at 2.5 GHz, respectively. The maximum S_{21} is 11.2 dB with a 3-dB bandwidth from 1.65 GHz to 3.8 GHz.

Because the third harmonic tuning technique was very effective to decrease the dc power consumption, it is expected that the proposed CMOS PA has high efficiency. Figure 7 shows the simulated dc drain current of the proposed PA IC (solid line) and the conventional PA IC (dotted line) versus the input power. The proposed CMOS PA exhibited a lower dc current than the conventional one under small-signal conditions.

Figure 8 shows the simulated input–output response of the proposed and conventional class-E PAs with sweeping the input power. It confirmed that the proposed PA IC achieves better gain linearity with better PAE than the conventional class-E PA IC. At an input power of lower than -10 dBm, M_2 was turned off and the input signal was mainly amplified by M_1. When the input power increased, the output power of M_2 became higher to compensate for the gain compression of M_1, achieving a

higher linear performance. From the simulation, it was shown that the proposed PA had a power gain of 11.5 dB, an output P1dB of 8.1 dBm, and a peak PAE of 38.5%.

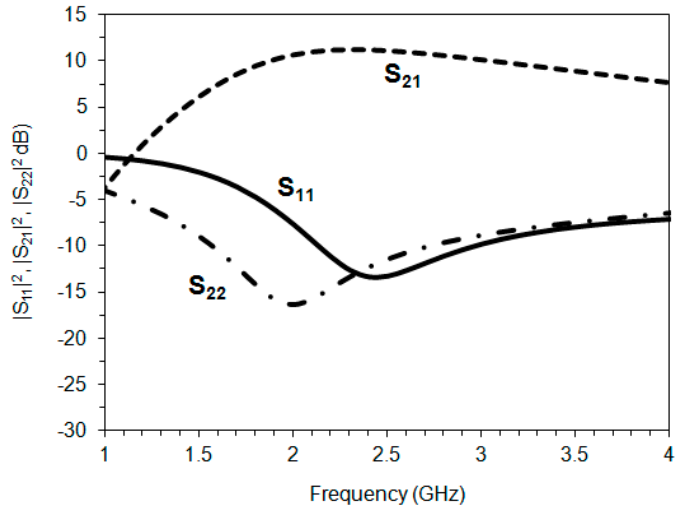

Figure 6. Simulation results of S_{11}, S_{21}, and S_{22} of the proposed PA IC.

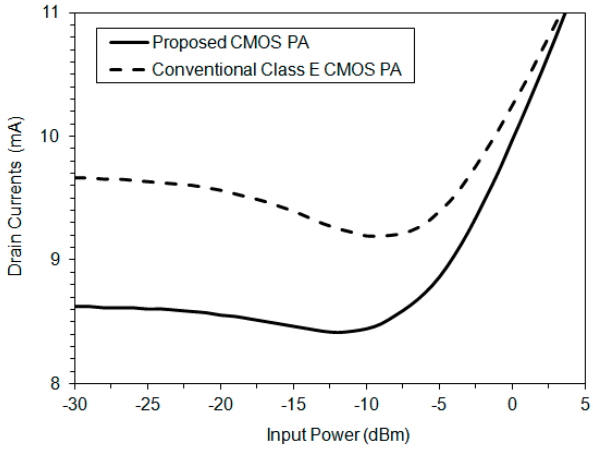

Figure 7. Simulation results of the drain currents versus the input power of the proposed PA IC (solid line) and the conventional PA IC (dotted line).

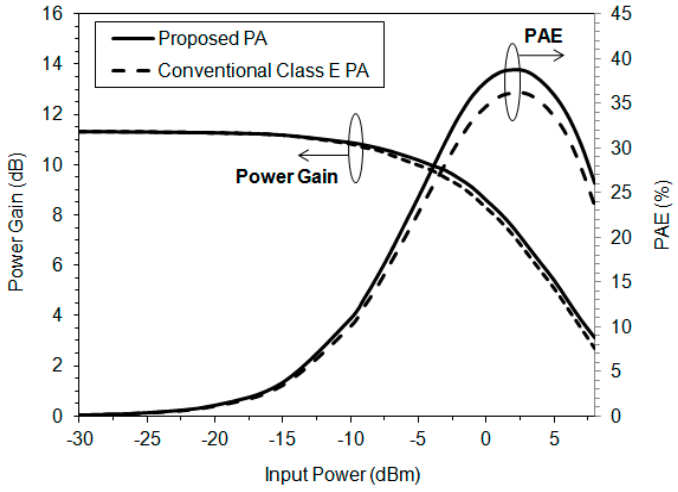

Figure 8. Simulated input–output response of the proposed PA (solid line) and the conventional class-E PA (dotted line) PA.

4. Measurement Results

The chip photograph of the proposed PA IC is depicted in Figure 9. The proposed PA was designed in 0.18-µm CMOS technology and measured on a wafer. The chip size is 0.9-mm by 1.1-mm. Figure 10 shows the measurement setup and probing situation of the proposed CMOS PA IC. The chip was probed using Summit 11201B Cascade Microtech with a single-ended GSG probe at the input and output RF signals. The RF input was generated using an Agilent E8267D vector signal generator, while the dc source was provided by using Yokogawa GS200.

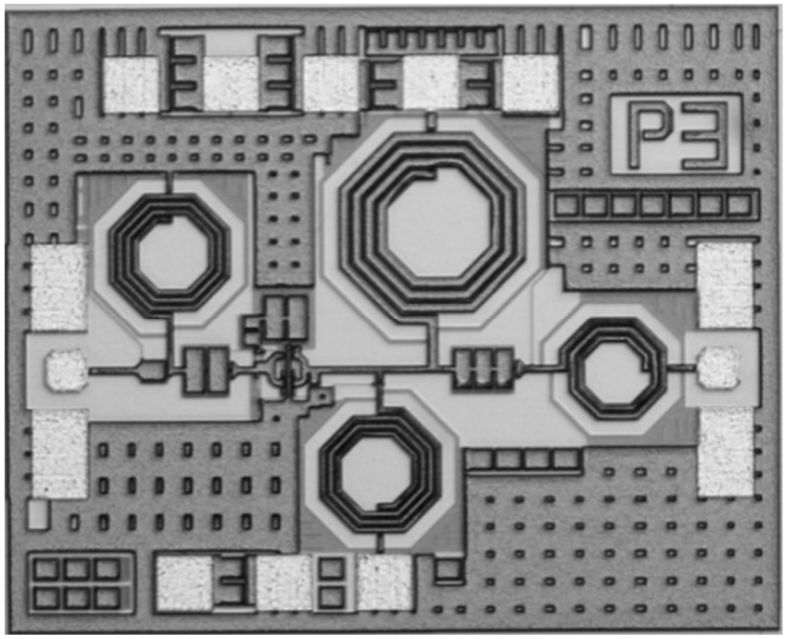

Figure 9. Photograph of the chip of the proposed circuits.

(**a**) (**b**)

Figure 10. (**a**) Measurement setup; and (**b**) probing situation of the proposed CMOS PA IC.

In the measurement process, 5 chips were measured for whole data variations, i.e., dc, small-signal, and large-signal performances. The average of the standard deviation of the I_{DS} measurement was 0.03 mA, and the averages of the standard deviations of S_{11}, S_{21}, and S_{22} were 0.05 dB, 0.06 dB, and 0.1 dB, respectively. To demonstrate the uniformity performance of the PA chips, the I_{DS} characteristics of chip 00 and chip 20 over the supply voltage (V_{dd}), bias voltage (V_{bias}), and back-gate voltage (V_{bg}) variations are illustrated in Figure 11.

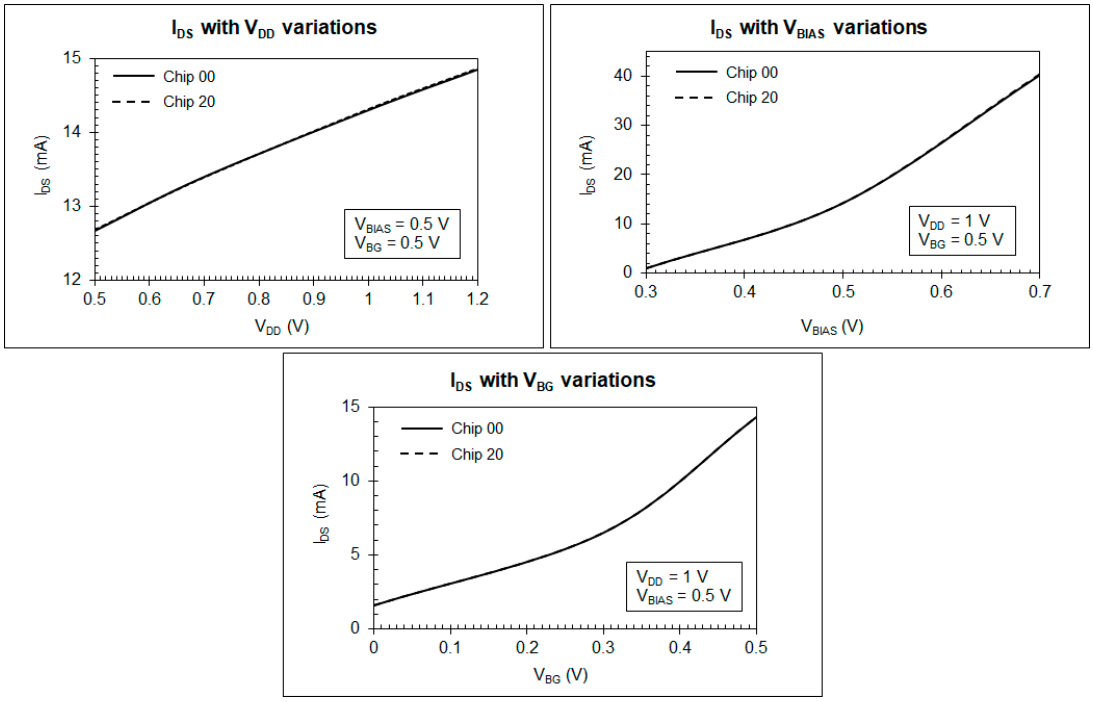

Figure 11. The uniformity dc performance measurement results of the proposed CMOS PA IC.

In order to demonstrate the small-signal performance based on S-parameters, the output RF was measured using the Agilent E8361A vector network analyzer. Figure 12 illustrates the comparison between the measured small-signal S-parameters (solid line) and the simulated small-signal S-parameters (dashed line) of the proposed circuits at 1 V of supply voltage. The quiescent current was 14.31 mA at 0.5 V of gate bias voltage. As expected, the measured S_{11} and S_{22} at 2.5 GHz were lower than -10 dB. The maximum small signal gain was 11.0 dB at 2.5 GHz with a 3-dB bandwidth from 1.7 GHz to 4.1 GHz. Figure 12 shows that measurement results agree well with the simulation results.

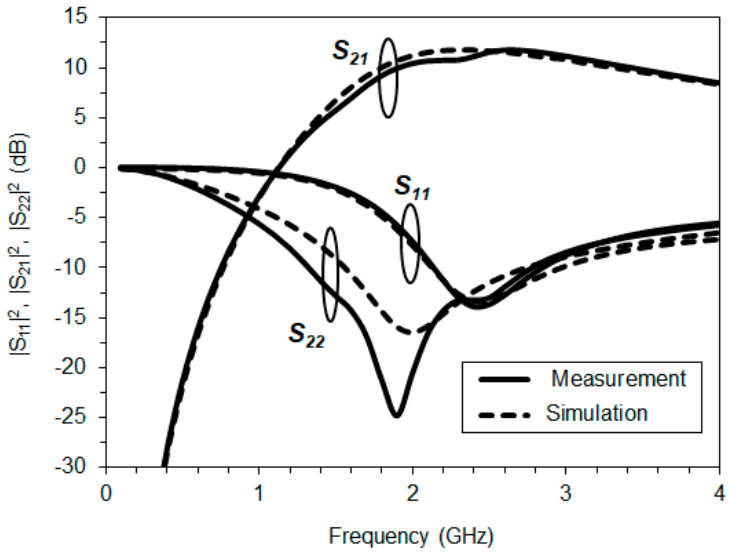

Figure 12. The measurement results (solid line) versus the simulation results (dashed line) of S_{11}, S_{21}, and S_{22} of the proposed PA IC at 1 V of supply voltage.

The measurement results of the power gain and the output power of the proposed CMOS PA IC are shown in Figure 13. To measure the output power, an Agilent E4448A spectrum analyzer

was utilized. At a supply voltage of 1 V, the proposed PA achieved a saturated output power of 10.1 dBm and an output P1dB of 8.0 dBm. Figure 14 illustrates the measurement results of the PAE of the proposed PA (solid line) and the conventional class-E PA (dotted line) at 1 V of supply voltage. The proposed PA achieved a higher PAE than the conventional PA, with a peak PAE of 34.5%.

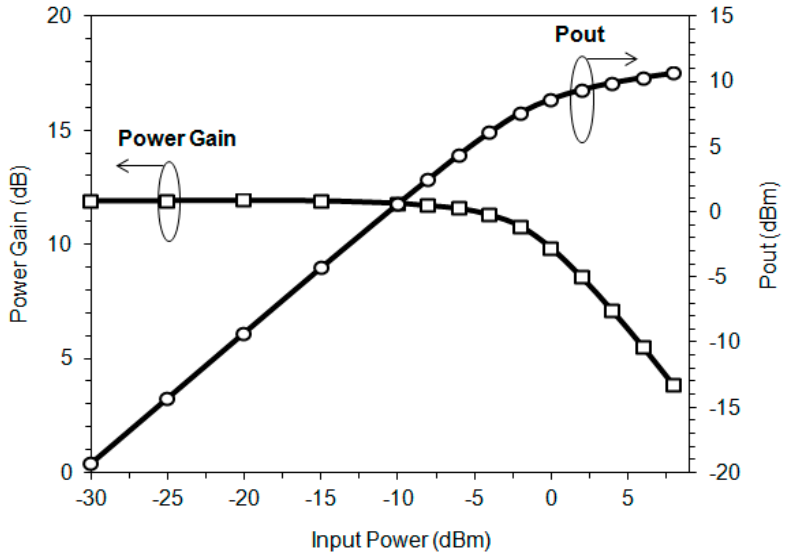

Figure 13. Measurement results of the power gain and pout of the proposed PA IC versus the input power.

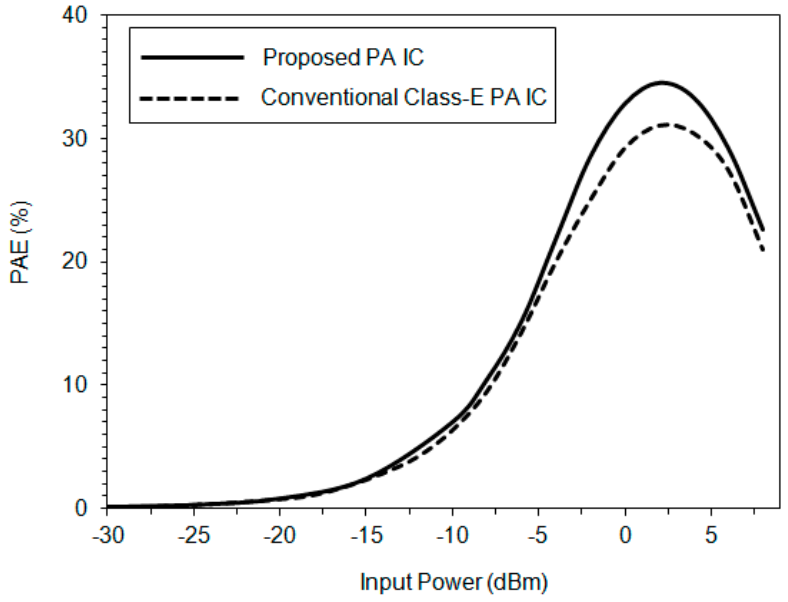

Figure 14. PAE of the proposed PA (solid line) and the conventional class-E PA (dotted line) versus the input power at a supply voltage of 1 V.

Figure 15 shows the measurement results of the output power and the P1dB of the proposed PA (solid line) and the conventional class-E PA (dotted line) versus the supply voltage variations from 0.5 V to 1.2 V. The proposed PA achieved larger saturated output power and P1dB than did the conventional PA. The dependency of the efficiency performances (drain efficiency (DE) and PAE) on the supply voltage is illustrated in Figure 16. The proposed PA achieved higher efficiency than the conventional PA at low-voltage operation. Because the load line was adjusted to obtain high efficiency at a supply voltage of 1 V, the efficiency at 1.2 V was slightly lower than that at 1 V.

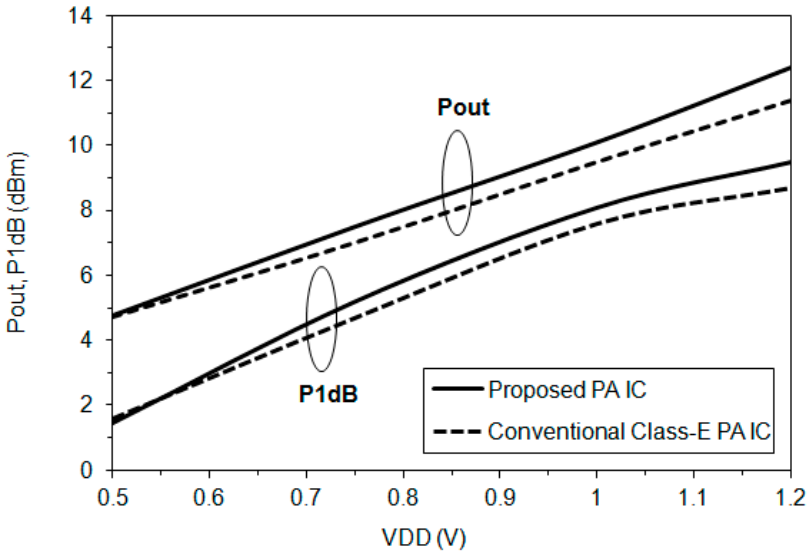

Figure 15. The pout and P1dB of the proposed PA (solid line) and the conventional class-E PA (dotted line) versus supply the voltage variations.

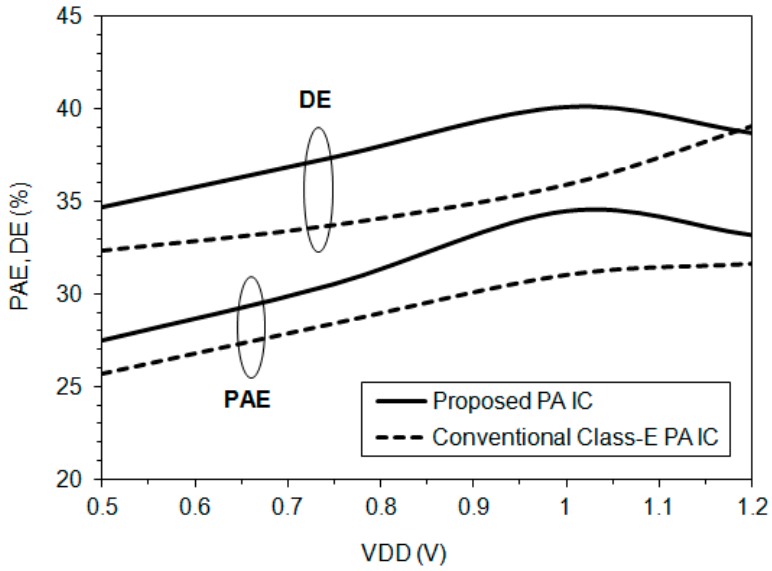

Figure 16. The drain efficiency (DE) and PAE of the proposed PA (solid line) and the conventional class-E PA (dotted line) versus the supply voltage.

Table 1 shows the performance of the proposed PA IC with several published works of low-voltage operation PAs. The proposed PA IC has achieved excellent PAE with sufficient output power at low-voltage operation compared with the previously published works.

Table 1. Summary of the proposed PA IC with several published works.

Reference	Technology	Frequency	Supply Voltage	PAE	Pout	Chip Size
[11]	0.18 µm	2.4 GHz	1.5 V	36%	7.6 dBm	0.6 mm^2
[23]	90 nm	2.4 GHz	1.2 V	32%	1.2 dBm	N/A
[24]	0.18 µm	2.4 GHz	1.8 V	21%	6.4 dBm	1.8 mm^2
[25]	90 nm	2.4 GHz	1.2 V	30%	9 dBm	1 mm^2
[26]	0.13 µm	1.9 GHz	1.2 V	26%	4.1 dBm	N/A
This work	**180 nm**	**2.5 GHz**	**1.0 V**	**34.5%**	**10.1 dBm**	**0.99 mm^2**

5. Conclusions

A 2.5-GHz fully integrated CMOS PA IC has been designed and fully evaluated in 0.18-µm CMOS technology for low-voltage operation. As the input power increased, the proposed dual-switching transistor (DST) effectively improved the gain linearity with high efficiency. In addition, the third harmonic termination technique compressed the voltage waveform and modified the current waveform to realize low dc power dissipation.

At 1 V of supply voltage, the proposed CMOS PA IC exhibited a power gain of 11.0 dB, an output P1dB of 8.0 dBm, and a peak PAE of 34.5%. The measured P1dB and PAE of the proposed PA were higher than those of recently reported works. Therefore, the proposed PA IC is applicable for low-voltage operation.

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