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Partial Isolation Type Saddle-FinFET(Pi-FinFET) for Sub-30 nm DRAM Cell Transistors

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Abstract: In this paper, we proposed a novel saddle type FinFET (S-FinFET) to effectively solve problems occurring under the capacitor node of a dynamic random-access memory (DRAM) cell and showed how its structure was superior to conventional S-FinFETs in terms of short channel effect (SCE), subthreshold slope (SS), and gate-induced drain leakage (GIDL). The proposed FinFET exhibited four times lower I_{off} than modified S-FinFET, called RFinFET, with more improved drain-induced barrier lowering (DIBL) characteristics, while minimizing I_{on} reduction compared to RFinFET. Our results also confirmed that the proposed device showed improved drain-induced barrier lowering (DIBL) and I_{off} characteristics as gate channel length decreased.

Keywords: gate-induced drain leakage (GIDL); drain-induced barrier lowering (DIBL); recessed channel array transistor (RCAT); on-current (I_{on}); off-current (I_{off}); subthreshold slope (SS); threshold voltage (V_{TH}); saddle FinFET (S-FinFET); potential drop width (PDW); shallow trench isolation (STI); source/drain (S/D)

1. Introduction

With decreasing dynamic random-access memory (DRAM) cell size, a recessed channel array transistor (RCAT) has been proposed to overcome the short channel effect (SCE) of conventional MOSFETs with planar channels. Although the recessed channel of RCAT has improved short channel effect (SCE), RCAT suffers from low driving current and V_{TH} sensitivity due to the shape of the bottom corner of the recessed channel [1]. To solve these problems, a saddle FinFET (S-FinFET) has been proposed with a tri-gate that wraps both the recessed channel surface and the side surface [2–4]. S-FinFET not only exhibits excellent short channel effect characteristics, but also maintains excellent subthreshold swing (SS), high I_{on}, and nearly constant V_{TH}. However, S-FinFET has higher gate-induced drain leakage (GIDL) than RCAT because the overlap region between the gate and drain regions is wider in S-FinFET. Although modified S-FinFET, called RFinFET, has emerged to reduce leakage by GIDL, RFinFET still needs to operate in sub-30 nm cell size [5,6]. Minimizing I_{off} in DRAM applications is a critical issue to achieving long refresh time. If this problem is not addressed, conventional S-FinFETs, including S-FinFET and RFinFET, will experience significant drawbacks in the application of DRAM technology. Therefore, a new device structure with an improved I_{off} is required. In this paper, we proposed a new device with a partial isolation region under the storage node of conventional S-FinFET. This structure can be fabricated by using an isotropic dry etching

technique for the buried insulator under the cell transistor [7,8]. We analyzed electrical characteristics of this proposed device and compared them with those of conventional S-FinFETs of the same size. We also showed the optimized parameters of the buried insulator using a three-dimensional (3D) device simulator in sub-30 nm cell size [9]. The device described in this paper has reliable source/drain (S/D) doping concentration with a Gaussian profile. The simulator is well tuned to predict DRAM cell transistor leakage distribution [10,11].

2. Device Structure

The partial isolation type S-FinFET (Pi-FinFET) is a structure with a buried insulator at a certain depth from the storage node of a conventional S-FinFET. Figure 1a shows a 3D schematic of a Pi-FinFET. Silicon film thickness, buried insulator thickness, and L_{in}, as shown in Figure 1a,b, are defined as the distance from the contact surface of the storage node to the buried insulator, the thickness of the buried insulator in the direction perpendicular to the channel, and the distance from the side gate oxide to the buried insulator, respectively. L_g, L_{side}, L_{ov_xj}, and L_{ov_side} represent gate channel length, the length of the side-gate in the direction parallel to the channel, the overlapped length of the side-gate and S/D doping region shown in Figure 1a, and the side-channel width shown in Figure 1c, respectively. When L_{side} and L_{ov_xj} are increased, the width of the overlap region of the gate and the S/D region will also increase. The n^+ poly gate with a gate work function of 4.2 eV was applied. L_g, L_{side}, L_{ov_side} and the recessed depth are 30 nm, 42 nm, 10 nm, and 100 nm, respectively. RFinFET is the modified S-FinFET with a structure in which the overlap region between the side-gate and the S/D region is removed [5]. Therefore, the Pi-FinFETs proposed in this paper can be divided into Pi-SFinFET and Pi-RFinFET depending on the presence or absence of the overlap region between the side-gate and the S/D region. Namely, in this paper, the L_{ov_xj} of Pi-RFinFET is 0 nm and that of Pi-SFinFET is 70 nm.
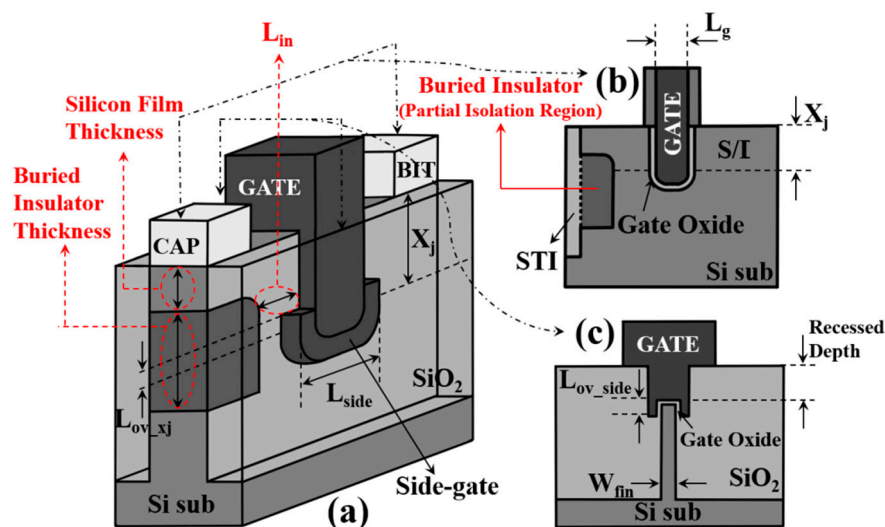

Figure 1. (**a**) 3D schematic view of Pi-FinFET; (**b**) Cross-sectional view across the gate; (**c**) Cross-sectional view of the thin body. The gate wraps three surfaces of the recessed channel, similar to a FinFET. The buried insulator material is used with SiO_2 below the storage node. The buried insulator is penetrated from the shallow trench isolation (STI) region. The X_j of the source/drain (S/D) is located 112 nm from the top surface of the S/D region with a Gaussian profile. The peak concentration of the S/D Gaussian doping profile is 1.5×10^{20} cm^{-3}, and the uniform body doping concentration is 5×10^{17} cm^{-3}.

3. Results and Discussion

Log and linear I_D-V_{GS} curves shown in Figure 2 are the result of comparing conventional S-FinFETs and RCAT with the Pi-FinFETs proposed in this paper. Silicon film thickness, buried insulator thickness, and L_{in} of Pi-FinFET was set at 20 nm, 100 nm, and 20 nm, respectively. As shown in Figure 2, the four

saddle type FinFETs have significantly higher I_{on} than RCAT. Moreover, the dotted red ellipse in Figure 2 show that Pi-SFinFET has about three times smaller I_{off} than S-FinFET, while Pi-RFinFET has about four times smaller I_{off} than RFinFET at V_{GS} of -0.5 V. To understand physical characteristics of I_{off} reduction for Pi-FinFET, device simulations have been performed using the TCAD tool [9,10]. The 3-D simulator is well tuned to predict the leakage current such as GIDL by applying the Hurkx band-to-band tunneling model.
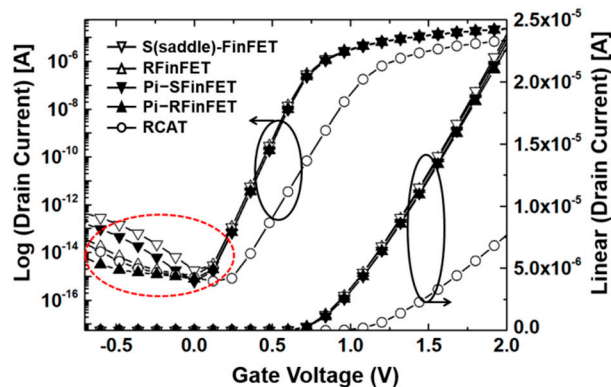
Figure 2. I_{DS}-V_{GS} characteristic for S-FinFET, RFinFET, Pi-FinFETs, and RCAT at V_{DS} = 1.5 V. $I_{off(S\text{-}FinFET)} = 1.62 \times 10^{-13}$ A, $I_{off(RFinFET)} = 7.80 \times 10^{-15}$ A, $I_{off.Pi\text{-}SFinFET} = 5.19 \times 10^{-14}$ A, $I_{off.RFinFET} = 1.92 \times 10^{-15}$ A at V_{GS} of -0.5 V.

Figure 3 shows the simulated potential contour near the drain region of conventional S-FinFET and Pi-FinFET at V_{DS} of 1.5 V and V_{GS} of -0.5 V. We defined the gap of equipotential lines as the potential drop width (PDW). In particular, dotted arrows in Figure 3a,b indicate PDW from 1.8 V to -0.4 V. As shown in Figure 3a, the conventional S-FinFET has intensive and narrow PDW from 1.8 V to -0.4 V near the drain/body (D/B) junction. On the other hand, PDW is mostly limited by the buried insulator of Pi-FinFET, as shown in Figure 3b. Namely, the rather constant electric field in the buried insulator of Pi-FinFET induces a wider PDW near the drain region [12]. The dotted red ellipse in Figure 3b shows that the PDW is wider in the silicon layer compared to the conventional S-FinFET. In other words, Pi-FinFET can reduce the electric field affecting GIDL in the silicon layer between the gate and drain regions. Moreover, the penetration of the electric field from the drain to the source affecting drain-induced barrier lowering (DIBL) is minimized in Pi-FinFET.

Figure 4a shows that I_{off} and I_{on} decrease as L_{in} decreases when L_g is 30 nm. If the ratio of L_{in} to L_g is as small as 50% or less, the lateral PDW of the silicon layer induced by the buried insulator will become narrow. This is because the deep penetration of the buried insulator limits the lateral PDW in the narrow silicon layer between the gate and drain regions. As a result, it induces abnormal I_{off} increase and I_{on} decrease, as shown in Figure 4a. Therefore, in order to maintain a relatively high I_{on} while maintaining a low I_{off}, it is desirable to define the ratio of L_{in} to L_g to 50 to 83.3%, respectively. As shown in Figure 4a, I_{off} is minimized when the ratio of L_{in} to L_g is 66.7%. As shown in Figure 4b, DIBL and SS characteristics are consistently improved because of wider PDW when L_{in} is decreased. Figure 5 shows I_{off} and DIBL characteristics according to L_g at V_{DS} of 1.5 V and V_{GS} of -0.5 V. L_{in} values in Figure 5 were set to maintain 60% of L_g. Pi-FinFETs consistently exhibited improved I_{off} and DIBL characteristics compared to conventional S-FinFETs regardless of L_g. Especially, Pi-FinFETs exhibited improved DIBL characteristics with opposite tendency compared to conventional S-FinFETs as L_g decreases, as shown in Figure 5b.
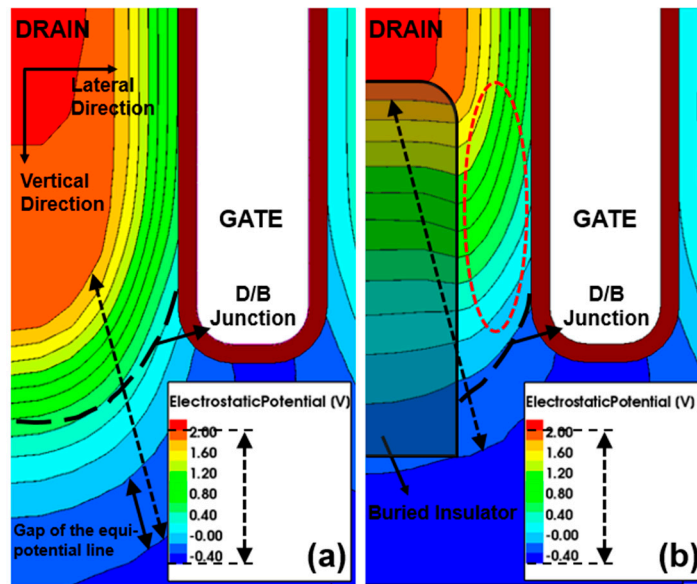
Figure 3. Potential contour indicating equipotential line distribution near the drain region at V_{DS} = 1.5 V, V_{GS} = −0.5 V. (**a**) Conventional S-FinFET, (**b**) Pi-FinFET. Dotted arrows indicate potential drop width (PDW) from 1.8 V to −0.4 V, while dotted red ellipse shows wider PDW compared to conventional S-FinFET.
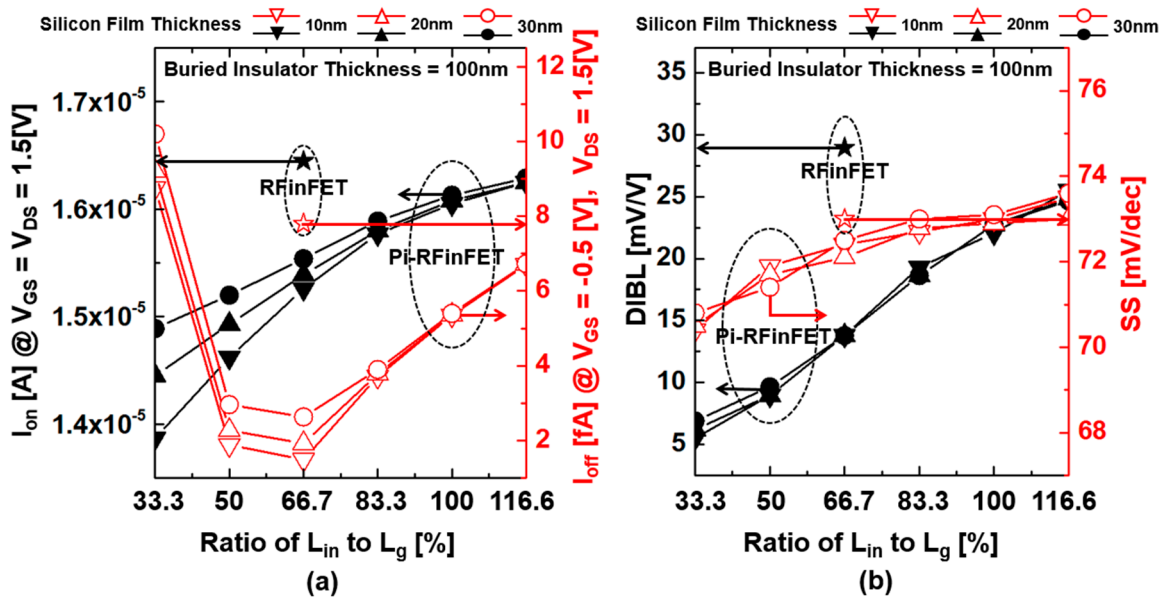

Figure 4. (**a**) I_{on}, I_{off} and (**b**) drain-induced barrier lowering (DIBL), subthreshold slope (SS) characteristics of Pi-RFinFET and Pi-FinFET according to the ratio of L_{in} to L_g when L_g is 30 nm.
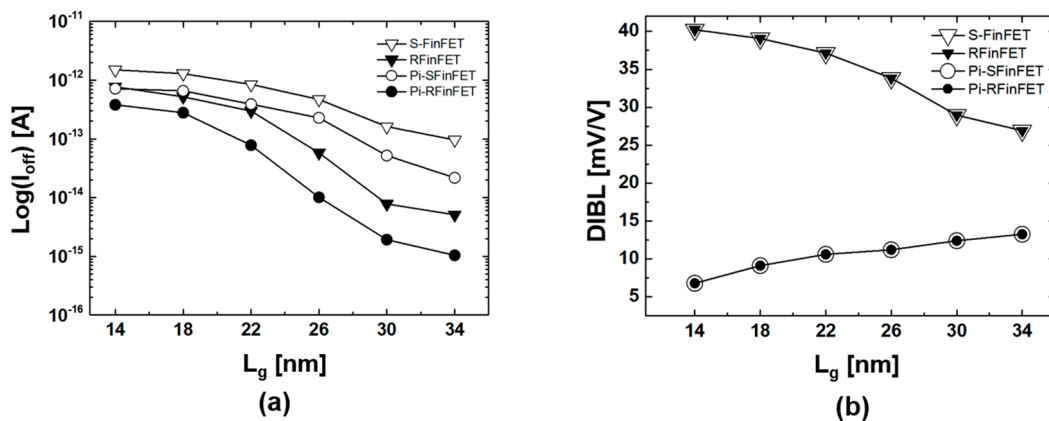
Figure 5. (**a**) I_{off} ($V_{GS} = -0.5$ V, $V_{DS} = 1.5$ V) and (**b**) DIBL ($V_{DS.low} = 0.05$ V, $V_{DS.high} = 1.5$ V) dependence on L_g of conventional S-FinFETs and Pi-FinFETs.

Figure 6 also shows the DIBL and $g_{m.max}$ characteristics of Pi-FinFETs and S-FinFETs according to the recessed depth. As shown in Figure 6, as the recessed depth decreases, DIBL characteristics of S-FinFETs increases sharply, whereas the DIBL of Pi-FinFETs is relatively constant because the PDW of Pi-FinFETs is wider. As the recessed depth decreases, the $g_{m.max}$, which represents the on-current characteristic, is improved. In other words, Pi-FinFETs have found that the recessed depth can be set more flexibly than conventional S-FinFETs.
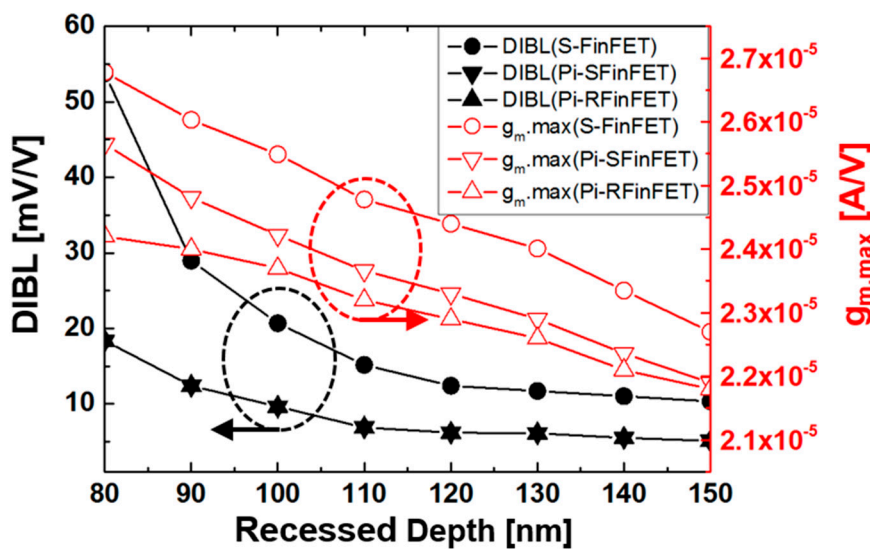

Figure 6. DIBL ($V_{DS.low} = 0.05$ V, $V_{DS.high} = 1.5$ V) and $g_{m.max}$ characteristics of Pi-FinFETs and S-FinFET according to the recessed depth when L_g is 30 nm.

4. Conclusions

We proposed a new device with a partial isolation region under the storage node of conventional saddle-FinFETs. This device can be classified as either Pi-SFinFET or Pi-RFinFET depending on the overlap area of the side gate and the S/D region. The proposed device not only maintains high DIBL characteristics regardless of the gate channel length, but also reduces the I_{off} by up to four times compared to the conventional saddle-FinFETs. It also minimizes I_{on} reductions. From the study, we concluded that Pi-FinFET is a promising candidate for sub 30 nm DRAM technology.

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