electronics

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A 6-Bit Ku Band Digital Step Attenuator with Low Phase Variation in 0.13-µm SiGe BiCMOS

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Received: 19 September 2019; Accepted: 9 October 2019; Published: 11 October 2019

Abstract: A 6-bit Ku band digital step attenuator with low phase variation is presented in this paper. The attenuator is designed with 0.13-µm SiGe BiCMOS process technology using triple well isolation N-Metal-Oxide-Semiconductor (TWNMOS) and through-silicon-via (TSV). TWNMOS is mainly used to improve the performance of switches and reduce the insertion loss (IL). TSV is utilized to provide approximately ideal global current ground plane with low impedance for the attenuator. In addition, substrate floating technique and new capacitance compensation technique are adopted in the attenuator to improve the linearity and decrease the phase variation. The measured results show that the attenuator IL is 6.99–9.33 dB; the maximum relative attenuation is 31.87–30.31 dB with 0.5-dB step (64 states), the root mean square (RMS) for the amplitude error is 0.58–0.36 dB and the phase error RMS is 2.06–3.46° in the 12–17 GHz frequency range. The total chip area is 1×0.9 mm^2.

Keywords: digital step attenuator; low phase variation; triple well isolation NMOS; wideband; CMOS integrated circuits

1. Introduction

The attenuator is one of the key components of modern communications. It is widely used in the transmitter/receiver (T/R) module of phased array radar system [1,2], and its main function is to achieve amplitude control. Compared with the X-type attenuator [3] and variable gain amplifier (VGA) [4,5], the passive digital step attenuator has the advantages of low power consumption, high linearity, wide frequency band and low temperature drift. Therefore, the design of attenuator with high resolution, large attenuation, low IL and low phase variation has great value, and very broad application prospects.

A variety of passive attenuator circuits have been designed in [6–24]. There are three most-used topologies in the passive attenuators: Switched path attenuators [6–9], distributed attenuators [10,11] and switched T/Pi attenuators [12–24]. Switched path attenuators topology use single-pole-double-throw (SPDT) switches to control the signal between reference thru line path and the resistive attenuation network path. This topology exhibits low phase variation, but has high insertion loss and large chip area, so it is not suitable for multi-bit CMOS digital step attenuator. Transistors as varistors and the half/quarter-wavelength of the transmission lines (TLs) together constitute the distributed attenuators topology. Due to the relative attenuation signal paths across the transmission lines have no series switches, this topology has the advantage of low IL. Meanwhile, the use of the TLs greatly increases the chip area. Switched T/Pi attenuators topology is composed by the resistor attenuation network and series shunt single-pole-single-throw (SPST) switches. Its chip area is very compact and suitable for multi-bit integration.

In order to meet the design requirements of phased array system for attenuators with high resolution, large attenuation, low IL and low phase change, this paper proposed a 6-bit CMOS digital step attenuator using switched T/Pi topology. The switches are designed and optimized by TWNMOS and through-silicon-via (TSV), in order to improve the performance and reduce the IL of the switches. Moreover, the attenuator adopted substrate floating and new capacitance compensation technology, which improved linearity and reduced the phase variation.

2. Proposed Circuit Design and Analysis

The switch is one of the key building blocks in the digital step attenuator [25,26]. In this paper, the triple well isolation NMOS is adopted in the switch shown in Figure 1a. Figure 1b,c illustrate the simplified equivalent circuits for on-state and off-state of the switch. As shown in Figure 1, the on-resistance R_{ch} and parasitic resistance at source and drain terminals of NMOS switch will contribute to the insertion loss in the signal path. The parasitic capacitors C_{GS}, C_{GD}, C_{SB} and C_{DB} will contribute to the off-capacitance C_{off} of NMOS switch and act as a leak path from input to output at the off-state. A large resistor R_G (10 kΩ) is used to prevent the RF signal from leaking through the bias line. Body floating technique is used to improve power handling of the switch by reducing the signal loss through source/drain-to-body junctions. To implement this technique, a large resistor R_B (10 kΩ) is added to the body terminal of the switch to enhance the linearity and insertion loss performance. Meanwhile, TSV is utilized to provide approximately ideal global current ground plane with low impedance for the attenuator.

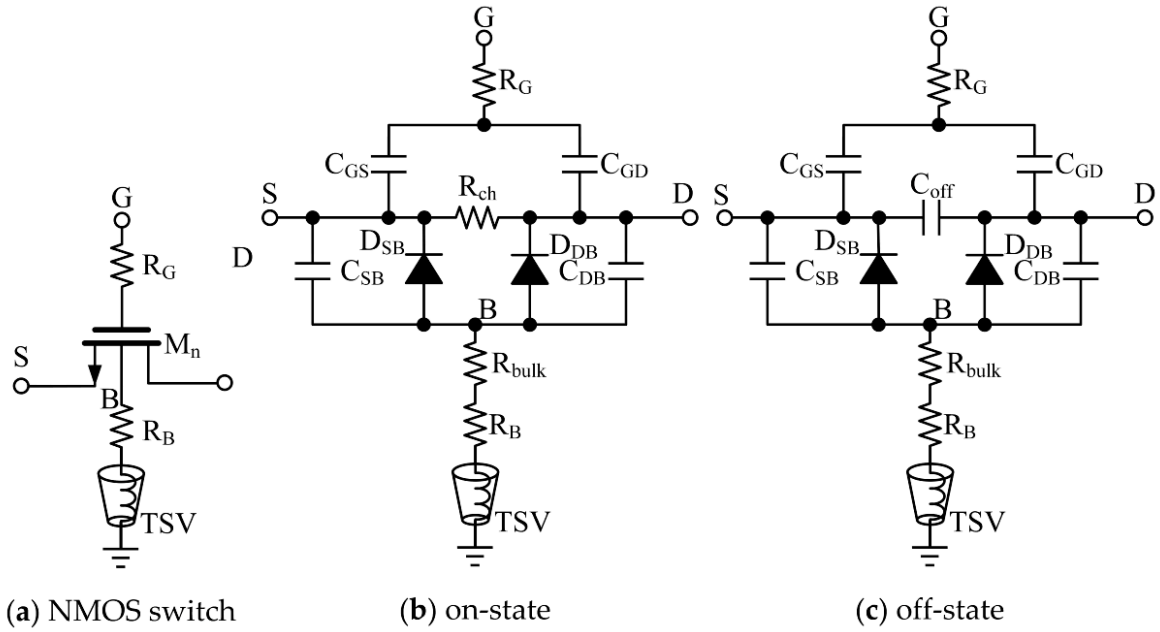


Figure 1. (**a**) The NMOS switch in the proposed attenuator; (**b**) The on-state simplified equivalent circuits of the switch; (**c**) The off-state simplified equivalent circuits of the switch.

Inductive and capacitive correction structure digital step attenuator is adopted in [18] to achieve low phase variations. Although the inductance correction structure can achieve low IL, it occupies a large chip area. Capacitance correction structure has the advantages of lower phase variation and better agreement with simulation results in the broadband frequency range, but it has larger IL than inductance correction structure. In order to solve the contradiction between large IL and low phase variation of capacitance correction structure, especially large attenuation units, such as 8 dB and 16 dB attenuation cells. A new capacitance compensation technique is proposed in this paper. The topology of the proposed capacitance compensation correction network attenuation cell circuits in the digital step attenuator is shown in Figure 2.

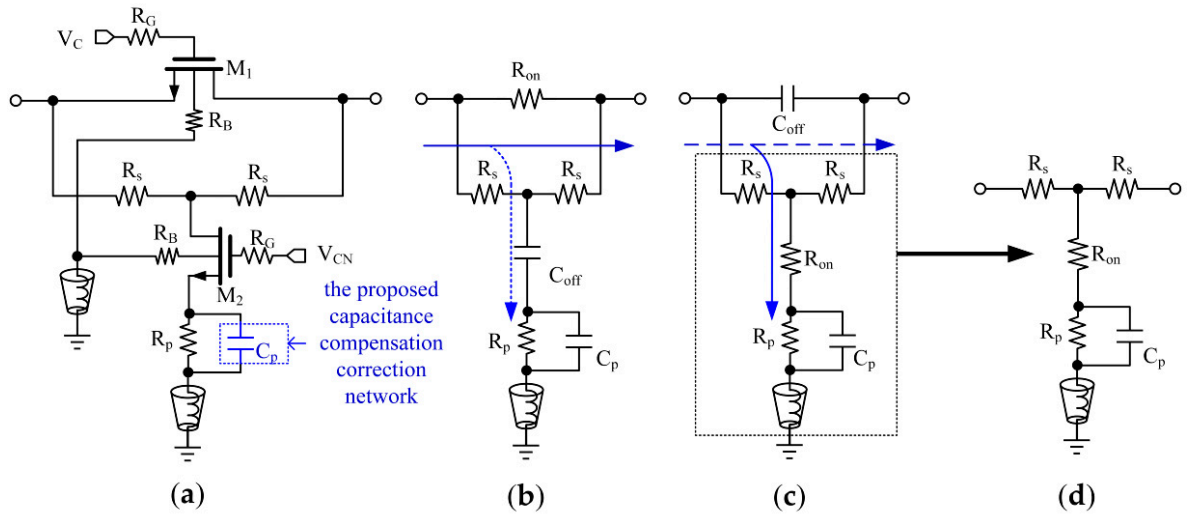


Figure 2. (**a**) The proposed T-type attenuator topology with capacitance compensation correction network; (**b**) The reference state equivalent circuit; (**c**) The attenuation state equivalent circuit; (**d**) The equivalent circuit of the capacitance compensation correction network at the attenuation state.

In the proposed circuit structure, a parallel capacitor C_P is added to the shunt branch of the traditional T-type attenuator in Figure 2a. R_{on} is the on-resistance, and C_{off} is the off-capacitance of the transistor. When the switch M_1 is on, and M_2 is off, the attenuator works in the reference state. The signal passes through the series path, as shown in Figure 2b. When the switch M_1 is off, and M_2 is on, it works in the attenuation state. The signal flows from the shunt attenuation branch to the ground, as shown in Figure 2c. Parallel capacitor C_P is introduced as a phase correction device in the attenuation branch. Therefore, the correction network will affect the performance of the attenuation state. In order to facilitate the theoretical analysis, the TSV and body series parasitic inductance are neglected. The simplified equivalent circuit of the phase correction branch is as shown in Figure 2d, and the transmission phase of the network can be derived from the transmission (ABCD) matrix of the attenuation state; the equation of transmission phase θ can be deduced as follows (see Appendix A for detailed derivation):

$$\theta = \tan^{-1} \frac{-C_p R_p^2 (Z_0 + R_s)}{(R_p + R_{on})(2R_p + 2R_{on} + Z_0 + R_s)/\omega + 2R_p^4 C_p^2 \omega + R_p^2 C_p (Z_0 + R_s)}, \quad (1)$$

where ω is the operating angular frequency. Z_0 is the characteristic impedance. For simplicity, all parameters in the equation are treated as the constant except the operating angular frequency ω.

The theoretical mathematical analysis image of function θ can be drawn using MATLAB in Figure 3a. The slope of θ changes from negative to positive value at the broadband angular frequency range. When the slope is zero, there exists a critical frequency f ($f = \omega/2\pi$), which can be used to correct the transmission phase error.

Figure 3b shows the practical simulation results in 0.13 µm SiGe BiCMOS process of the transmission phase of the phase correction branch in Figure 2d. The transmission phase varies with parallel C_p value (swept from 60 fF to 180 fF) at the broadband frequency range. Figure 3a,b possess a similar variation tendency, which verifies the theoretical analysis results in Equation (1).

Figure 4a shows the proposed T-type attenuator topology transmission phases of reference and attenuation states are simulated with various parallel capacitor C_p value. The phases of attenuation states have the same variation trend as those of the phase correction branch in Figure 3b.

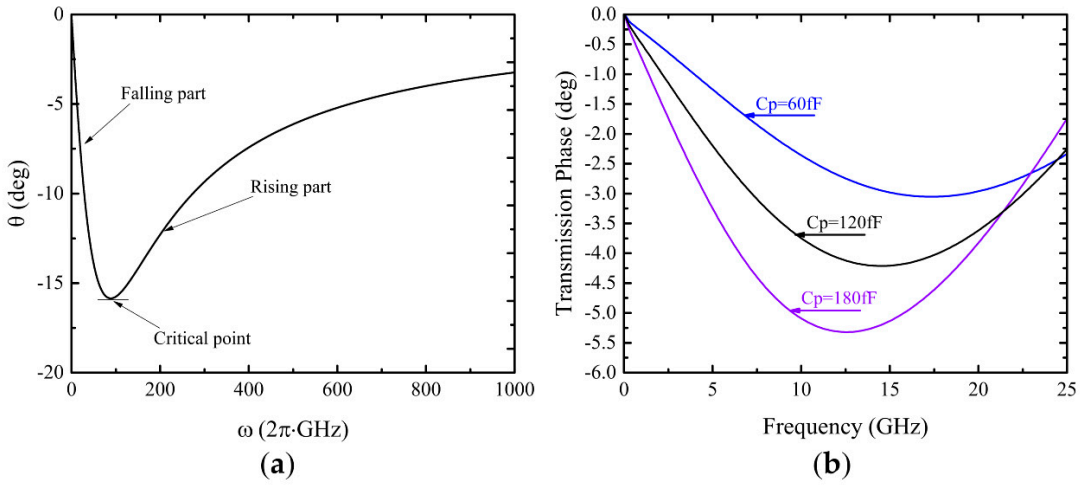


Figure 3. (**a**) The theoretical mathematical analysis image of Equation (1); (**b**) The practical simulation results of the transmission phase of the phase correction branch in 0.13 μm SiGe BiCMOS.

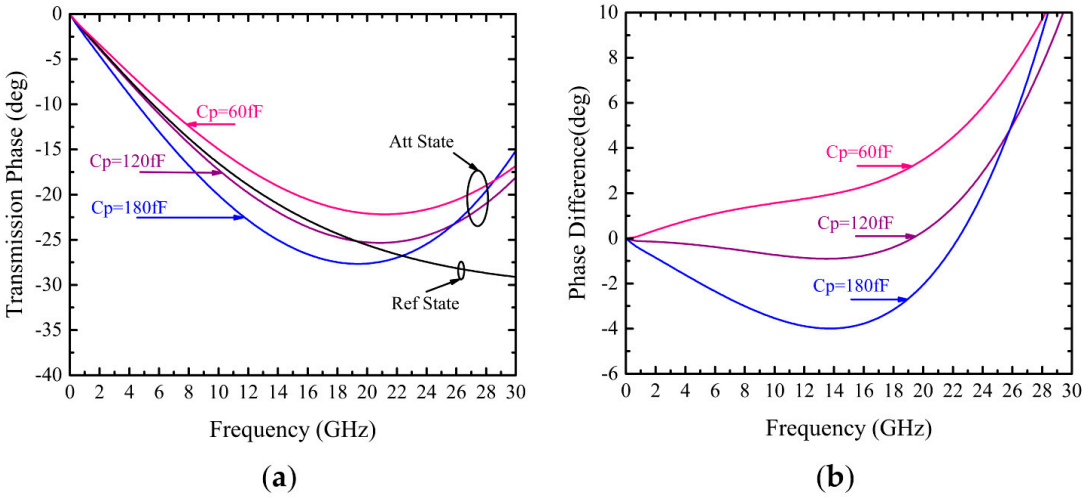


Figure 4. (**a**) The simulated transmission phase results of the proposed T-type attenuator topology of reference and attenuation states with various C_p value; (**b**) the phase difference of reference and attenuation states with various C_p value.

It is obvious that the capacitance variation influences the attenuation state significantly, whereas, it has less effect on the reference state. By adjusting the capacitance C_p value, we can control the transmission phase of reference and attenuation states to intersect at different frequencies to produce zero phase difference. The low phase difference in a specific frequency band can be achieved by choosing the appropriate capacitance C_p value, as shown in Figure 4b.

Figure 5a shows the simulation attenuation results with traditional T-type and proposed C_p T-type topology in 4 dB attenuation cell. The simulation phase difference results with traditional T-type and proposed C_p T-type topology in 4 dB attenuation cell is illustrated in Figure 5b. With C_p compensation circuit structure, Flatness of the phase difference is better in a wide bandwidth range.

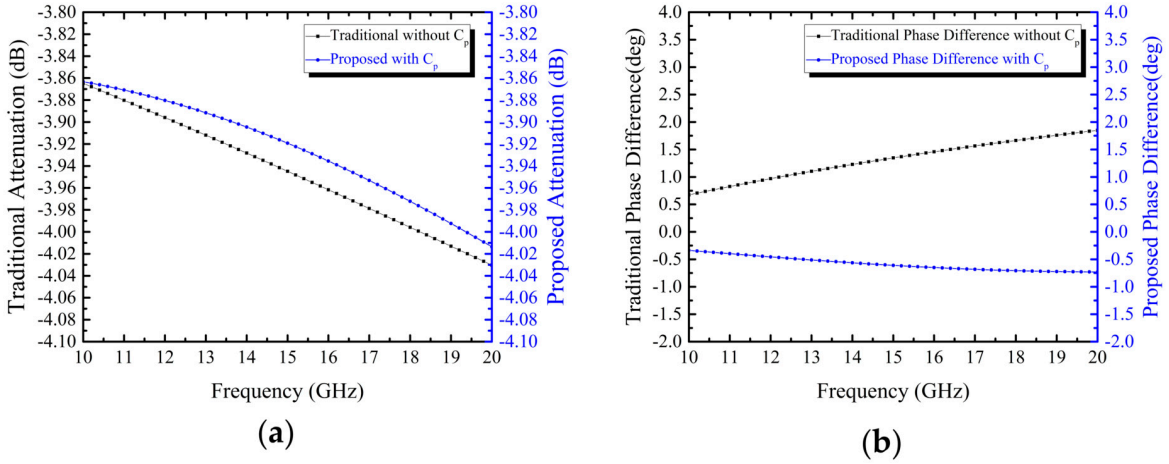


Figure 5. (**a**) The simulation attenuation results with traditional T-type and proposed C_p T-type topology in 4 dB attenuation cell; (**b**) the simulation phase difference results with traditional T-type and proposed C_p T-type topology in 4 dB attenuation cell.

Meanwhile, in order to study the influence of TSV on phase difference, parasitic parameters of TSV with different sizes can be obtained by the electromagnetic field (EM) simulation. Table 1 shows parasitic inductance and resistance of TSV with different sizes.

Table 1. Parasitic inductance and resistance of TSV with different sizes.

Number of Row Vias.	Number of Column Vias	Parasitic Inductance (pH)	Parasitic Resistance (mΩ)
1	3	33	37
2	2	28	26
1	7	23	17
1	12	17	9
2	7	15	10
2	5	11	5
2	12	8	5
2	22	6	3

TSV is utilized to provide approximately ideal global current ground plane with low impedance for the attenuator. Take the proposed C_p T-type topology in 4 dB attenuation cell as an example, the TSV connected to the switch body terminal mainly provides on-chip grounding of the substrate, and its effect on the phase variation of the attenuator can be neglected. The TSV connected to capacitance compensation correction branch of the attenuation cell also provides on-chip grounding. The parallel capacitor C_p grounding terminal of the capacitance compensation correction branch in attenuation cell is not ideal, which results in an additional phase variation of the attenuator circuit. Although the effect of TSV on attenuator performance is small, it cannot be ignored. The simulation phase difference results with TSV size variation in proposed C_p T-type topology in 4 dB attenuation cell is illustrated in Figure 6. In microwave and millimeter wave bands, TSV will inevitably introduce parasitic inductance and resistance. The parasitic parameters are related to their size (i.e., the number of rows and columns vias). The larger the size, the smaller the parasitic inductance and resistance, but the bigger size will occupy a large area of the layout, so a compromise should be considered. After careful consideration, the TSV size of 2×5 was selected in this design.

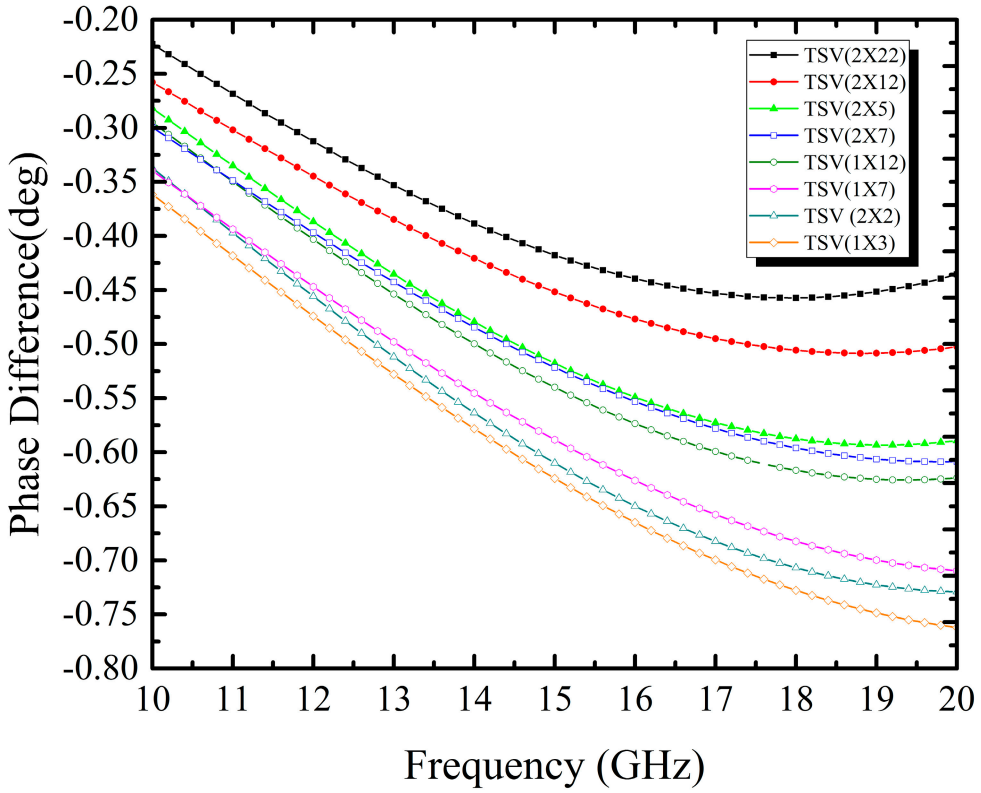


Figure 6. The simulation phase difference results with TSV size variation in proposed C_p T-type topology in 4 dB attenuation cell.

The proposed capacitance compensation correction network and switch are also applicable to the Pi and bridge-T type attenuation cells. They have the same operation principle to realize low phase difference as the proposed T-type attenuator topology.

Traditional capacitance C_c and C_p compensation correction networks are widely used in the digital control step attenuator circuit [18,20,21], but there are large insertion losses, especially in large 8 and 16 dB attenuation units. In order to solve this problem, a parallel capacitor C_p is added to the attenuation shunt branch in 8 and 16 dB attenuation cells. Take 16 dB attenuation unit as an example: Figure 7a shows the simulation IL results with traditional C_c and proposed $C_c + C_p$ compensation in 16 dB attenuation cell. The IL decreases obviously with the increase of frequency in the proposed $C_c + C_p$ compensation structure. The simulated attenuation, phase difference results with traditional C_c and proposed $C_c + C_p$ compensation in 16 dB attenuation cell is illustrated in Figure 7b. With $C_c + C_p$ compensation circuit structure, the attenuation and phase difference change more smoothly in a wide frequency band.

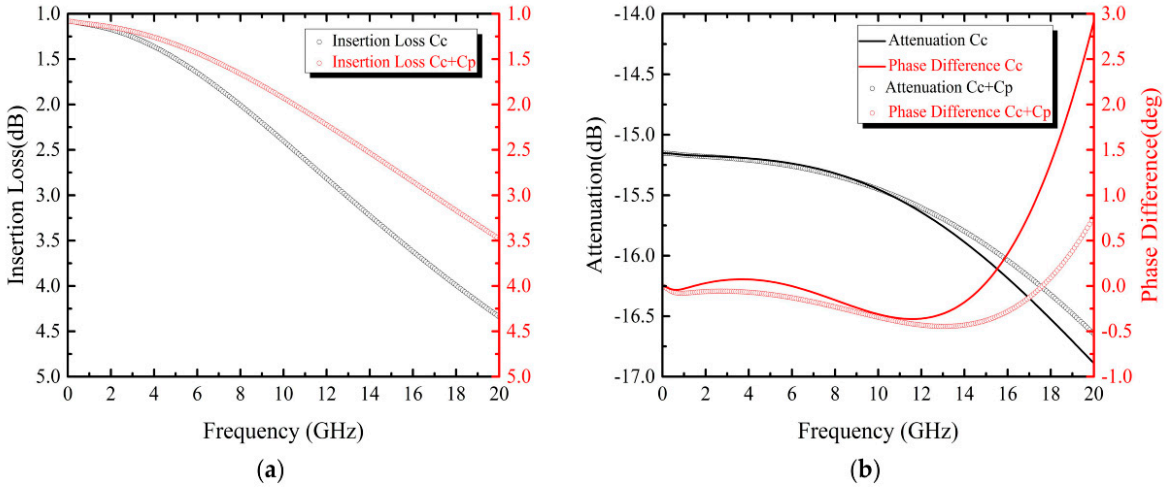
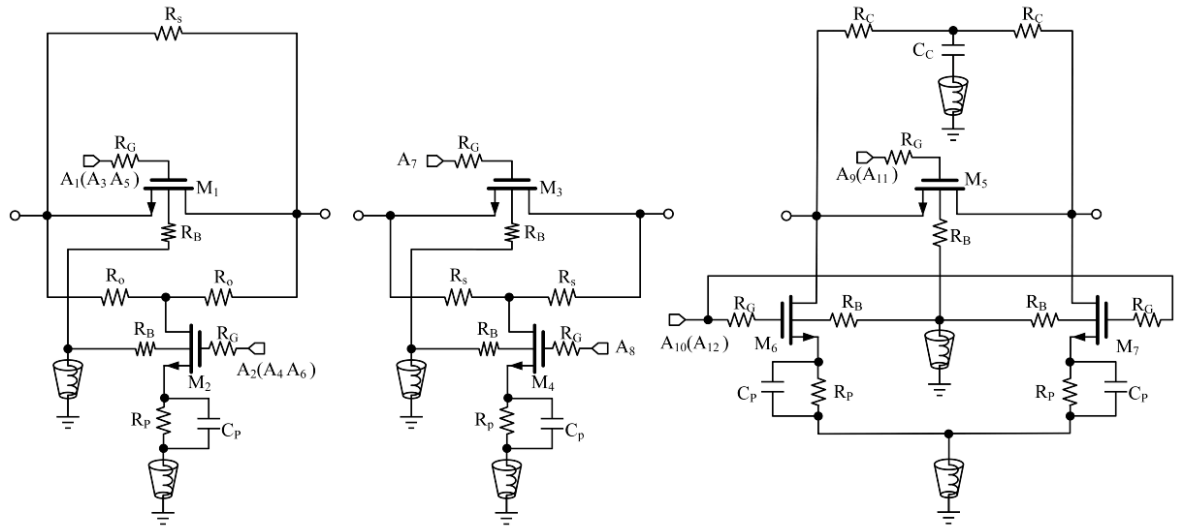


Figure 7. (**a**) The simulation insertion loss results with traditional C_c and proposed $C_c + C_p$ compensation in 16 dB attenuation cell; (**b**) the simulation attenuation, phase difference results with traditional C_c and proposed $C_c + C_p$ compensation in 16 dB attenuation cell.

Through the above theoretical and simulation analysis, in the proposed 6-bit digital control step attenuator circuit, 0.5 db, 1 db, 2 dB and 4 dB attenuation units adopt the proposed parallel capacitor C_p compensation method, which reduces the additional phase shift of attenuation. In the large attenuation unit (8 db, 16 db), we combine the traditional capacitance compensation method with the proposed parallel capacitance C_p compensation method, which reduces the problems of excessive insertion loss and large phase shift fluctuation range in the traditional capacitance compensation method.

The utilized attenuation cell topology in 6-bit CMOS digital control step attenuator is shown in Figure 8. 0.5 dB, 1 dB and 2 dB attenuation cells are configured with switched bridge-T type in Figure 8a. 4dB attenuation cell is configured with switched T-type in Figure 8b. The switched Pi-type topology in Figure 8c is suitable for large attenuation cells, such as 8 and 16 dB cells. The block diagram of the proposed 6-bit digital control step attenuator is shown in Figure 9.



(**a**) Proposed Bridged-T type topology (**b**) Proposed T-type topology (**c**) Proposed Pi-type topology

Figure 8. The utilized attenuation cell topology in 6-bit CMOS digital control step attenuator, (**a**) Proposed Bridged-T type topology, (**b**) Proposed T-type topology and (**c**) Proposed Pi-type topology.

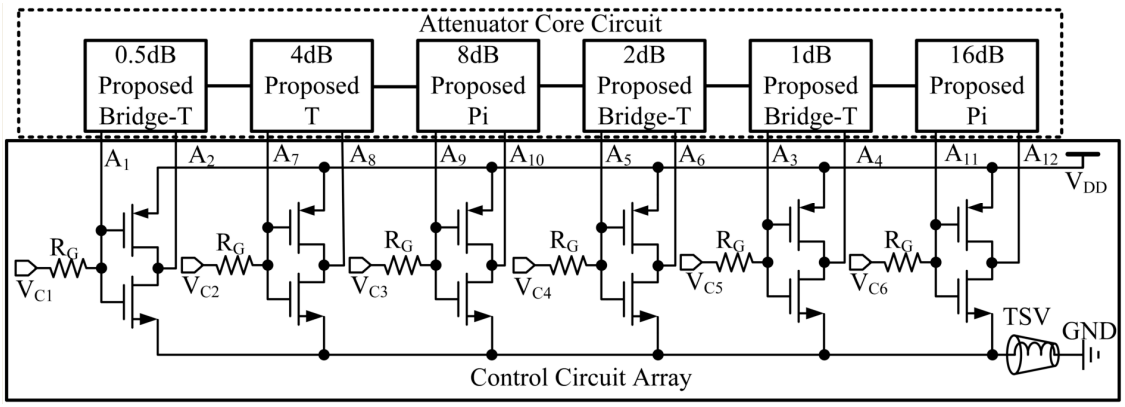


Figure 9. The block diagram of the proposed 6-bit digital control step attenuator.

The component values of each attenuator unit are summarized in Table 2. The 6-bit CMOS digital control step attenuator circuit is optimized in terms of linearity, loading effect and power processing ability. Finally, the bit ordering 0.5-4-8-2-1-16 dB sequence is adopted in this paper. The proposed attenuator is controlled by the 6-bit digital signal control circuit array, V_{c1}, V_{c2}, V_{c3}, V_{c4}, V_{c5}, V_{c6}, which are used to control 0.5 dB, 1 dB, 2 dB, 4 dB, 8 dB, 16 dB attenuation modules, respectively. The layout of series/parallel resistors are the key components in the attenuator design; and the resistance values need to be carefully selected. In particular, small resistance values are realized by parallel connection of large resistance to reduce the influence of process variation effects. The power consumption of the attenuator is extremely low, which is contributed by the dynamic power consumption of inverters in each attenuation module.

Table 2. Component values of each proposed attenuator unit.

Atten. (dB)	Topology	R_s (Ω)	R_o (Ω)	R_p (Ω)	R_c (Ω)	$W_{1,3,5}$ (μm)	$W_{2,4,6,7}$ (μm)	C_c (fF)	C_p (fF)
0.5	Bridge-T	5.92	40.9	368	0	40	15	0	17
1	Bridge-T	15.7	74.1	1293	0	90	20	0	17
2	Bridge-T	20.7	164.6	873	0	80	20	0	83
4	T-type	15.3	0	90.5	0	80	15	0	50.7
8	Pi-type	0	0	91.1	53.7	60	15	84.2	58.1
16	Pi-type	0	0	50.1	70.6	20	15	102.5	152.2

The full chip electromagnetic (EM) simulation of the proposed 6-bit digital control step attenuator except resistors, capacitors and NMOS switch transistors components is realized in ADS Momentum in order to further ensure the performance. The transmission RF lines between the circuits of each attenuation cell are used to connect each module, which improves the matching performance and adjusts the transmission phase characteristics. Both input and output impedances of the proposed attenuator are matched to 50 Ω.

3. Measurement Results

The proposed 6-bit digital control step attenuator has been designed and fabricated in 0.13-μm SiGe BiCMOS technology. The die photograph of the proposed 6-bit digital control step attenuator is depicted in Figure 10. The total chip size is 1×0.9 mm^2. All the DC Pads are bond wired to a PCB for chip testing, and the chip is probed with Cascade's 100 μm ground-signal-ground (GSG) probes at the input and output ports. The power consumption of the proposed attenuator is extremely low and negligible.

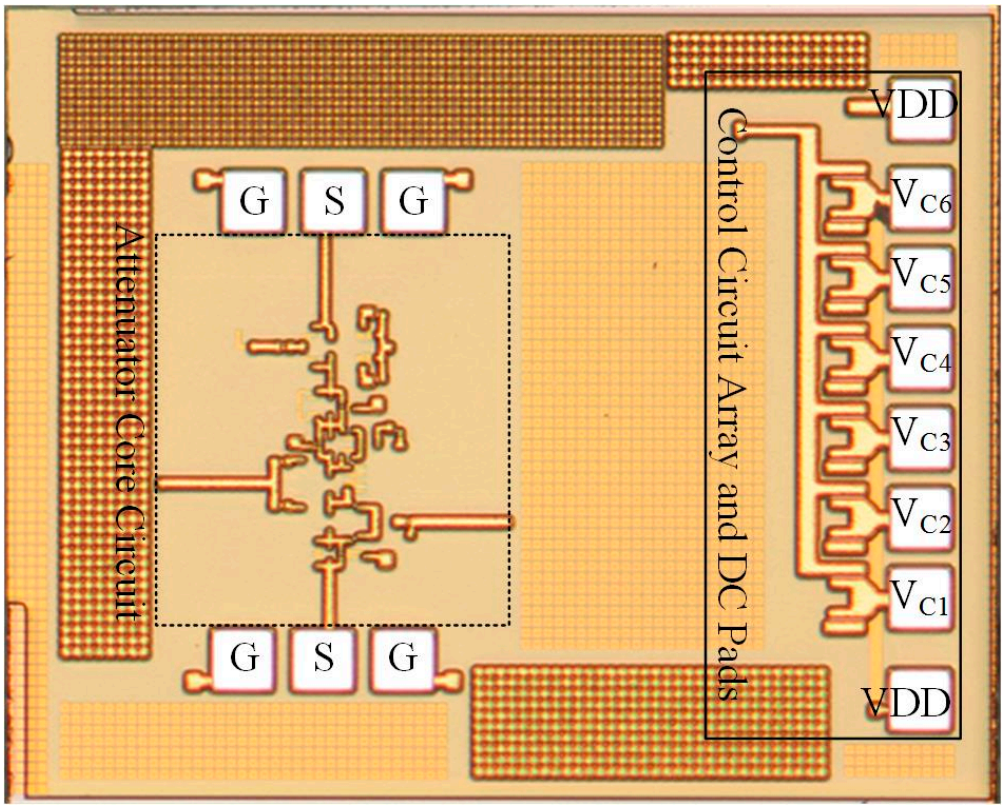


Figure 10. The die photograph of the proposed 6-bit digital control step attenuator.

The input return loss (RL) is >13 dB in Figure 11a and the output return loss is >14.1 dB in Figure 11b at 10–18 GHz for the 64 states. Figure 12 shows the measured insertion loss (of the reference state) is 6.99–9.33 dB and IP_{-1dB} (of the reference state) is 13.6–16.2 dBm at 12–17 GHz. The maximum attenuation relative to that of the reference state is 31.87–30.31 dB with 0.5-dB step (64 states) at 12–17 GHz in Figure 13. The measured results show that the root mean square (RMS) for the amplitude error is 0.58–0.36 dB and the RMS phase error is 2.06–3.46° in the 12–17 GHz frequency range for the 64 states in Figure 14. The RMS for the amplitude error can be defined as:

$$A_{RMS} = \sqrt{\frac{1}{N}\sum_{i=1}^{N}(A_{m\_i} - A_{theo\_i})^2}(dB), \tag{2}$$

where A_{RMS} is the attenuation RMS amplitude error, I is the attenuation state index, N is 64, A_{m_i} is the measured attenuation relative to the reference in a given state, and A_{theo_i} is the theoretical attenuation in a given state. The RMS phase error for the attenuation is calculated using the equation defined as follows:

$$\theta_{RMS} = \sqrt{\frac{1}{M}\sum_{i=1}^{M}\left(\theta_{m\_i} - \theta_{ref\_m}\right)^2}(deg), \tag{3}$$

where θ_{RMS} is the attenuation RMS phase error, i is the attenuation state index, M is 64, θ_{m_i} is the measured attenuation relative phase in a given state, and θ_{ref_m} is the measured attenuation relative phase in the reference state.

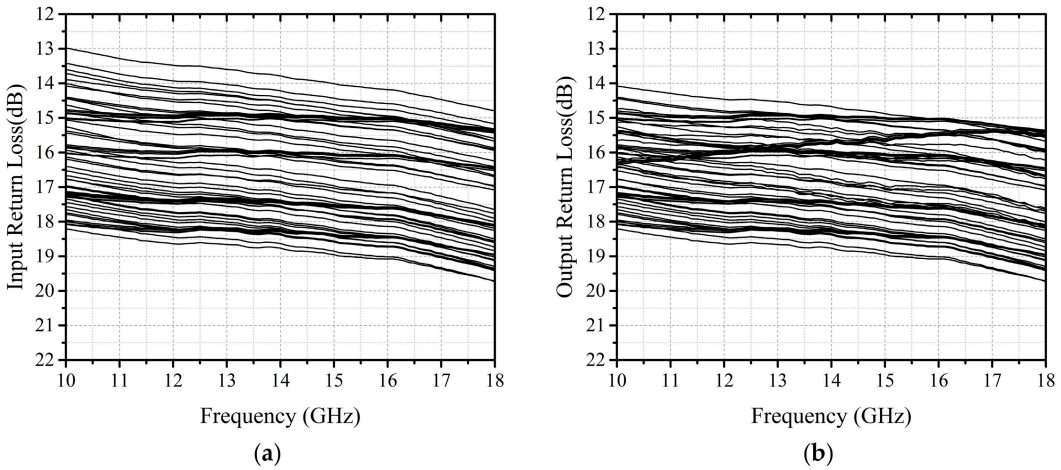


Figure 11. (**a**) The measured input return loss of the proposed attenuator; (**b**) the measured output return loss of the proposed attenuator.

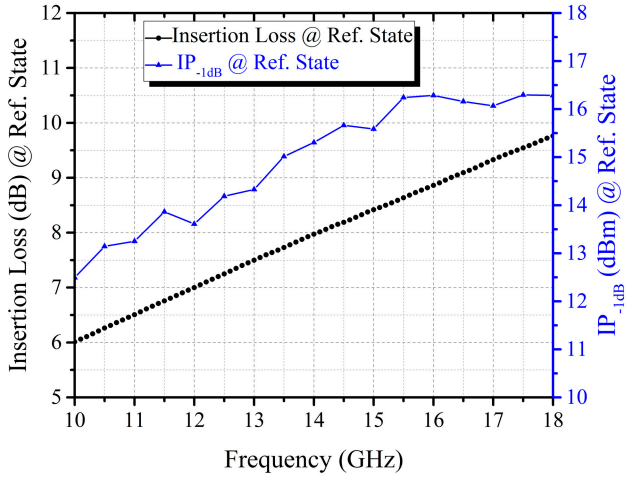


Figure 12. The measured insertion loss and IP_{-1dB} of the proposed attenuator.

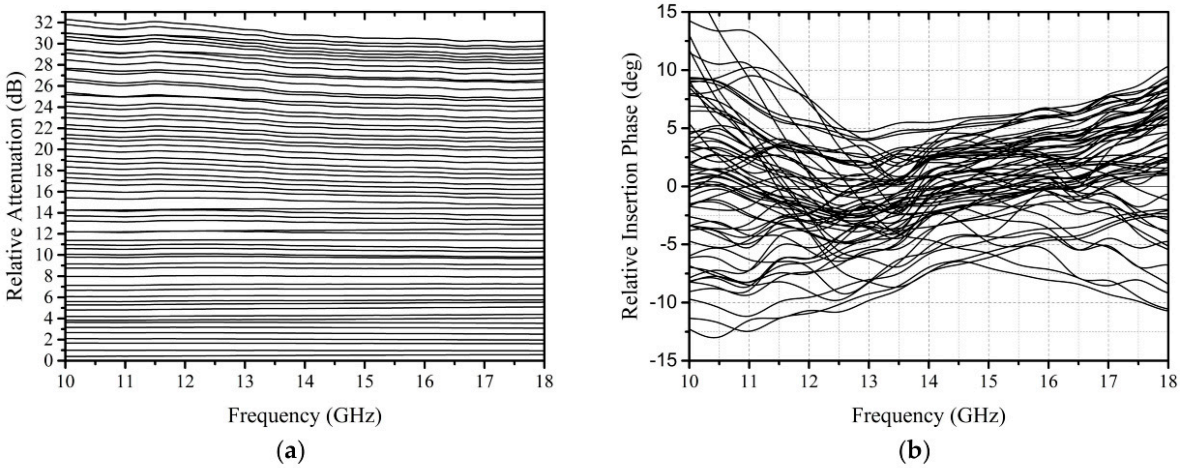


Figure 13. (**a**) The measured 64-state relative attenuation of the proposed attenuator; (**b**) the measured 64-state relative insertion phase of the proposed attenuator.

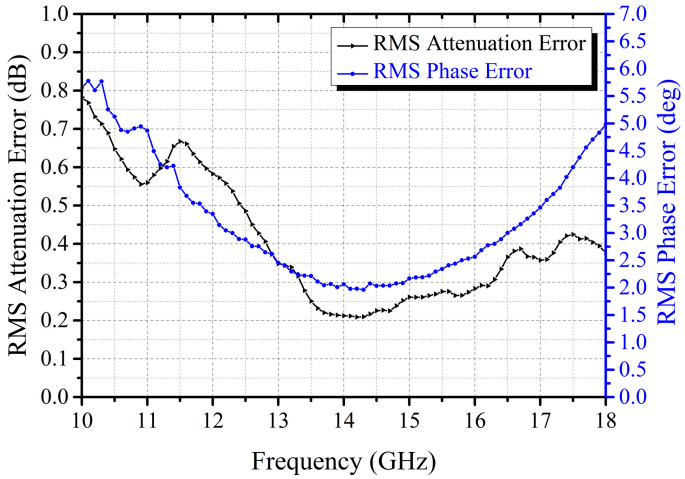


Figure 14. The measured RMS amplitude error and phase error of the proposed attenuator.

4. Comparison with Relevant Digital Control Step Attenuators

This work is compared with other recently published similar digital control step attenuators in Table 3. The proposed 6-bit digital control step attenuator has better insertion loss compared with [16–18] and the higher IP_{-1dB} than [13,16,21]. Compared with [12,13,17], this design has wide frequency coverage. Even compared with all references in Table 3, the RMS phase error of this design has considerable competitive advantage. In this paper, the design of a 6-bit digital attenuator with low insertion loss and small RMS phase error in Ku-band (12–17 GHz) is realized by using substrate floating technology and the proposed capacitance compensation technology.

Table 3. Performance comparison of relevant digital control step attenuators.

Reference	[12] 2017	[13] 2017	[16] 2016	[17] 2018	[18] 2010	[21] 2018	This Work
Frequency (GHz)	19–21	14–18	6–12.5	20–24	DC–14	DC–20	12–17
Technology	0.18 µm CMOS	0.35 µm BiCMOS	0.25 µm BiCMOS	0.13 µm BiCMOS	0.18 µm CMOS	0.13 µm BiCMOS	0.13 µm BiCMOS
Number of Bits	6	6	7	6	6	6	6
Attenuation Rang (dB)	32	31.5	16.51	31.5	31.5	31.5	31.87–30.31
Attenuation Step (dB)	0.5	0.5	0.26	0.5	0.5	0.5	0.5
RL (dB)	>12	>10	>13	>9	>10	>12	>13
IL (dB)	<8	8±0.6	<12.7	20.9–21.95	<10	1.7–7.2	6.99–9.33
RMS Amplitude Error (dB)	N/A	<0.29	<0.26	<0.43	<0.5	<0.37	0.58–0.36
RMS Phase Error (°)	<3.8	<3.9	2.2–3.5	1.6–4.2	<4.2	<4	2.06–3.46
IP_{-1dB} (dBm)	N/A	10	12.5	14	15	10	13.6–16.2
Die area (mm^2)	0.45[1]	0.27[1]	0.29[1]	0.77[2]	0.5[1]	0.98[2]	0.9[2]

[1.] excluding pads [2.] including pads.

5. Conclusions

This paper has presented a 12–17 GHz 6-bit digital control step attenuator with low phase imbalance in 0.13-µm SiGe BiCMOS technology. In this design, a parallel capacitor C_p is added to the attenuation shunt branch of the traditional Pi, T and bridge-T type attenuation cells to form a phase correction network with the parallel resister. Furthermore, in order to study the influence of TSV on phase difference, parasitic parameters of TSV with different sizes can be obtained by an electromagnetic field (EM) simulation. After careful consideration, the TSV size of 2 × 5 was selected in this design. As far as the author knows, this is the first 6-bit digital attenuator designed with TSV. The influence of TSV on attenuator performance is also analyzed and verified. With the help of these techniques, the transmission phase error of the attenuation state can be corrected, thus, leading to a low phase imbalance. Meanwhile, substrate floating technology is adopted to reduce switches insertion loss and

improve linearity. The proposed attenuator achieves the RMS phase error less than 3.46° and amplitude error less than 0.58 dB over 12–17 GHz. It has a maximum attenuation range of 31.87 dB with the approximate 0.5-dB step. In addition, good input/output return loss, high IP_{-1dB}, moderate chip area and wide bandwidth are obtained, which makes it suitable to use in Ku-band phased array systems.

Author Contributions: Formal analysis, L.L., Y.Y. and G.C.; Funding acquisition, Z.L.; Investigation, L.L., Y.Y. and G.C.; Methodology, L.L., Y.Y. and G.C.; Supervision, Z.L.; Writing—original draft, L.L.; Writing—review and editing, Y.Y. and G.C.

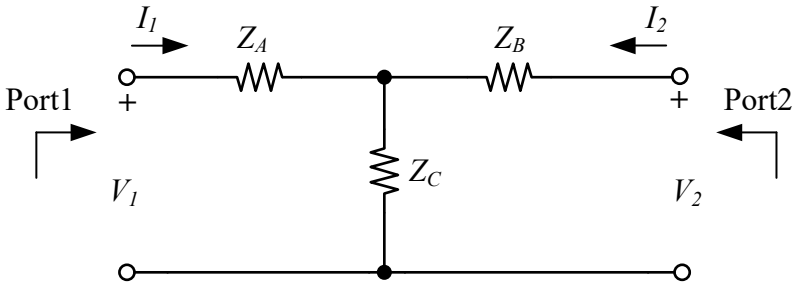
Funding: This research was funded by National Natural Science Foundation of China, grant number 61474021.

Acknowledgments: The authors would like to thank the Global Foundries for the fabrication and Keysight for ADS EM Design support.

Conflicts of Interest: The authors declare no conflict of interest.

Appendix A

For T-network configuration, ABCD-parameters relate the voltages to current in the following form for a two-port network:



$$V_1 = AV_1 - BI_2 \tag{A1}$$

$$I_1 = CV_1 - DI_2 \tag{A2}$$

Which can be put in matrix form as

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_1 \\ -I_2 \end{bmatrix}. \tag{A3}$$

The ABCD parameters in Equation (A3) are defined as

$$\begin{matrix} A = \frac{V_1}{V_2}\big|_{I_2=0} & A = \frac{V_1}{-I_2}\big|_{V_2=0} \\ C = \frac{I_1}{V_2}\big|_{I_2=0} & D = \frac{I_1}{-I_2}\big|_{V_2=0} \end{matrix}. \tag{A4}$$

The ABCD network is useful in finding the voltage or current gain of a component or the overall gain of a network. One of the great advantages of ABCD parameters is their use in cascaded network or components. When this condition exists, the overall ABCD parameter of the network becomes the matrix product of an individual network and a component.

For T-network configuration, Parameters A and C are determined when Port2 is open circuited as

$$A = \frac{V_1}{V_2}\big|_{I_2=0} \rightarrow V_2 = \frac{Z_C}{Z_C + Z_A} V_1 \rightarrow A = \left(\frac{Z_C + Z_A}{Z_C}\right), \tag{A5}$$

and

$$C = \frac{I_1}{V_2}\big|_{I_2=0} \rightarrow I_1 = V_2\left(\frac{1}{Z_C}\right) \rightarrow C = \left(\frac{1}{Z_C}\right). \tag{A6}$$

Parameters B and D are determined when Port2 is short circuited as

$$B = \left.\frac{V_1}{-I_2}\right|_{V_2=0} \rightarrow I_2 = \frac{-V_1}{Z_A + (Z_B//Z_C)}\frac{Z_C}{(Z_B + Z_C)} \rightarrow B = \left(\frac{Z_A Z_B + Z_A Z_C + Z_B Z_C}{Z_C}\right), \tag{A7}$$

and

$$D = \left.\frac{-I_1}{I_2}\right|_{V_2=0} \rightarrow I_2 = -I_1\left(\frac{Z_C}{Z_B + Z_C}\right) \rightarrow D = \left(\frac{Z_B + Z_C}{Z_C}\right). \tag{A8}$$

Therefore, the T-network ABCD matrix is

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \left(\frac{Z_C+Z_A}{Z_C}\right) & \left(\frac{Z_A Z_B+Z_A Z_C+Z_B Z_C}{Z_C}\right) \\ \left(\frac{1}{Z_C}\right) & \left(\frac{Z_B+Z_C}{Z_C}\right) \end{bmatrix}. \tag{A9}$$

Simplified the equivalent circuit of phase correction branch, as shown in Figure 2d, the transmission phase of the network is derived from the transmission (ABCD) matrix for the attenuation state. According to Equation (A9), we can get the Figure 2d ABCD parameters of the network as follows:

$$A = \frac{\left(1 + jR_p\omega C_p\right)(R_{on} + R_s) + R_p}{R_{on}\left(1 + jR_p\omega C_c\right) + R_p}, \tag{A10}$$

$$B = \frac{\left(2R_sR_{on} + R_s^2\right)\left(1 + jR_p\omega C_p\right) + 2R_sR_p}{R_{on}\left(1 + jR_p\omega C_p\right) + R_p}, \tag{A11}$$

$$C = \frac{1 + jR_p\omega C_p}{R_{on}\left(1 + jR_p\omega C_p\right) + R_p}, \tag{A12}$$

$$D = \frac{(R_s + R_{on})\left(1 + jR_p\omega C_p\right) + R_p}{R_{on}\left(1 + jR_p\omega C_p\right) + R_p}. \tag{A13}$$

Assume that the matching impedance of Port 1 and Port 2 is Z_0, according to the theory of microwave network, the insertion phase θ of the T-network can be calculated by the following equation:

$$\theta = \tan^{-1}\frac{\mathrm{Im}\left(AZ_0 + B + CZ_0^2 + DZ_0\right)}{\mathrm{Re}\left(AZ_0 + B + CZ_0^2 + DZ_0\right)}. \tag{A14}$$

Im and Re represent the imaginary part and the real part of the formula, respectively.

$$\begin{aligned} &\mathrm{Im}\left(AZ_0 + B + CZ_0^2 + DZ_0\right) = \\ &-\begin{bmatrix} 2R_s\left(1 + R_p^2\omega^2C_p^2\right)R_p^2\omega C_pZ_0 + R_s^2\left(1 + R_p^2\omega^2C_p^2\right)R_p^2\omega C_p \\ +Z_0^2\left(1 + R_p^2\omega^2C_p^2\right)R_p^2\omega C_p \end{bmatrix} \end{aligned} \tag{A15}$$

Due to $R_p^2\omega^2C_p^2 \ll 1$, the formula can be simplified to (A16)

$$\mathrm{Im}\left(AZ_0 + B + CZ_0^2 + DZ_0\right) = -\left(2R_sR_p^2\omega C_pZ_0 + R_s^2R_p^2\omega C_p + Z_0^2R_p^2\omega C_p\right), \tag{A16}$$

$$\begin{aligned} &\mathrm{Re}\left(AZ_0 + B + CZ_0^2 + DZ_0\right) = Z_0^2\left(R_p + R_{on}\right) + 2Z_0R_s\left(R_p + R_{on}\right) \\ &+R_s^2\left(R_p + R_{on}\right) + 2Z_0\left(R_p + R_{on}\right)^2 + 2R_s\left(R_p + R_{on}\right)^2 + 2\left(R_p^2\omega C_p\right)^2(Z_o + R_s), \\ &+R_p^2\omega C_p(Z_o + R_s)^2 \end{aligned} \tag{A17}$$

$$\theta = \tan^{-1} \frac{-R_p^2 \omega C_p (Z_0 + R_s)}{\left(R_p + R_{on}\right)(Z_0 + R_s) + 2\left(R_p + R_{on}\right)^2 + 2\left(R_p^2 \omega C_p\right)^2 + R_p^2 \omega C_p (Z_0 + R_s)}, \tag{A18}$$

$$\theta = \tan^{-1} \frac{-C_p R_p^2 (Z_0 + R_s)}{(R_p + R_{on})(2R_p + 2R_{on} + Z_0 + R_s)/\omega + 2R_p^4 C_p^2 \omega + R_p^2 C_p (Z_0 + R_s)}. \tag{A19}$$

The appendix gives a detailed derivation of Formula (1) in this paper.

References

1. Sim, S.; Jeon, L.; Kim, J. A compact X-Band Bi-directional phased-array T/R chipset in 0.13 μm CMOS technology. *IEEE Trans. Microw. Theory Tech.* **2013**, *61*, 562–569. [CrossRef]
2. Jeong, J.; Yom, I.; Kim, J.; Lee, W.; Lee, C. A 6–18 GHz GaAs multifunction chip with 8-bit true time delay and 7-bit amplitude control. *IEEE Trans. Microw. Theory Tech.* **2018**, *66*, 2220–2230. [CrossRef]
3. Wagner, J.; Mayer, U.; Wickert, M.; Wolf, R.; Joram, N.; Strobel, A.; Ellinger, F. X-type attenuator in CMOS with novel control linearization, very low phase variations and automatic matching. In Proceedings of the 2013 European Microwave Integrated Circuit Conference, Nuremberg, Germany, 6–8 October 2013; pp. 200–203.
4. Li, D.; Fei, C.; Wu, X.; Yang, Y. A 6-bit digital CMOS variable gain attenuator with large dynamic range and high linearity-in-dB for ultrasound imaging applications. *Microelectron. J.* **2019**, *83*, 32–38. [CrossRef]
5. Koolivand, Y.; Shoaei, O.; Jafarabadi-Ashtiani, S. Linear in dB, sub 0.2 dB gain-step CMOS programmable gain amplifier for ultrasound applications. *Analog Integr. Circuits Signal Process.* **2017**, *93*, 309–318. [CrossRef]
6. Cho, M.; Song, I.; Fleetwood, Z.E.; Cressler, J.D. A SiGe-BiCMOS wideband active bidirectional digital step attenuator with bandwidth tuning and equalization. *IEEE Trans. Microw. Theory Tech.* **2018**, *66*, 3866–3876. [CrossRef]
7. Mikul, A.O.; Zhu, S.; Sun, P.; You, Y.; Sah, S.P.; Heo, D. Compact low phase imbalance broadband attenuator based on SiGe PIN diode. In Proceedings of the 2012 IEEE/MTT-S International Microwave Symposium Digest, Montreal, QC, Canada, 17–22 June 2012; pp. 1–3. [CrossRef]
8. Eom, H.; Yang, K. A 6–20 GHz compact multi-bit digital attenuator using InP/InGaAs PIN Diodes. In Proceedings of the 2008 20th International Conference on Indium Phosphide and Related Materials, Versailles, France, 25–29 May 2008; pp. 1–3. [CrossRef]
9. Zhu, S.; Mikul, A.O.; Sun, P.; You, Y.; Kim, J.H.; Kim, B.S.; Heo, D. Inductor-less SiGe pin diode attenuator with low phase variations. *Electron. Lett.* **2012**, *48*, 1287–1289. [CrossRef]
10. Bae, J.; Lee, J.; Nguyen, C. A 10–67-GHz CMOS dual-function switching attenuator with improved flatness and large attenuation range. *IEEE Trans. Microw. Theory Tech.* **2013**, *61*, 4118–4129. [CrossRef]
11. Min, B.; Rebeiz, G.M. A 10–50-GHz CMOS distributed step attenuator with low loss and low phase imbalance. *IEEE J. Solid State Circuits* **2007**, *42*, 2547–2554. [CrossRef]
12. Zhang, L.; Zhao, C.; Zhang, X.; Wu, Y.; Kang, K. A CMOS K-band 6-bit attenuator with low phase imbalance for phased array applications. *IEEE Access* **2017**, *5*, 19657–19661. [CrossRef]
13. Shi, W.; Ma, K.; Mou, S.; Meng, F. A compact Ku-band 6-bit attenuator in 0.35um SiGe BiCMOS technology. In Proceedings of the 2017 IEEE Electrical Design of Advanced Packaging and Systems Symposium (EDAPS), Haining, China, 14–16 December 2017; pp. 1–3. [CrossRef]
14. Bae, J.; Nguyen, C. A novel concurrent 22–29/57–64-GHz dual-band CMOS step attenuator with low phase variations. *IEEE Trans. Microw. Theory Tech.* **2016**, *64*, 1867–1875. [CrossRef]
15. Kandis, H.; Yazici, M.; Gurbuz, Y.; Kaynak, M. A wideband (3–13 GHz) 7-Bit SiGe BiCMOS step attenuator with improved flatness. In Proceedings of the 2018 18th Mediterranean Microwave Symposium (MMS), Istanbul, Turkey, 31 October–2 November 2018; pp. 139–142. [CrossRef]
16. Davulcu, M.; Caliskan, C.; Kalyoncu, I.; Kaynak, M.; Gurbuz, Y. 7-Bit SiGe-BiCMOS step attenuator for X-Band phased-array RADAR applications. *IEEE Microw. Wirel. Compon. Lett.* **2016**, *26*, 598–600. [CrossRef]
17. Sarfraz, M.M.; Ullah, F.; Wang, M.; Zhang, H. A 6-Bit 0.13 μm SiGe BiCMOS digital step attenuator with low phase variation for K-band application. *Electronics* **2018**, *7*, 74. [CrossRef]
18. Ku, B.; Hong, S. 6-bit CMOS digital attenuators with low phase variations for X-band phased-array systems. *IEEE Trans. Microw. Theory Tech.* **2010**, *58*, 1651–1663. [CrossRef]

19. Ciccognani, W.; Giannini, F.; Limiti, E.; Longhi, P.E. Compensating for parasitic phase shift in microwave digitally controlled attenuators. *Electron. Lett.* **2008**, *44*, 743–744. [CrossRef]
20. Sun, P. Analysis of phase variation of CMOS digital attenuator. *Electron. Lett.* **2014**, *50*, 1912–1914. [CrossRef]
21. Song, I.; Cho, M.; Cressler, J.D. Design and analysis of a low loss, wideband digital step attenuator with minimized amplitude and phase variations. *IEEE J. Solid State Circuits* **2018**, *53*, 2202–2213. [CrossRef]
22. Askari, M.; Kaabi, H.; Kavian, Y.S.; Ajabi, S. A wideband 5-bit switched step attenuator in 0.18 µm CMOS technology. *IETE J. Res.* **2015**, *62*, 295–300. [CrossRef]
23. Jarihani, A.E.; Kocer, F. A phase coherent 7-bit digital step attenuator on 0.18µm SOI. In Proceedings of the 2017 12th European Microwave Integrated Circuits Conference (EuMIC), Nuremberg, Germany, 8–10 October 2017; pp. 167–170. [CrossRef]
24. Dogan, H.; Meyer, R.G.; Niknejad, A.M. Analysis and design of RF CMOS attenuators. *IEEE J. Solid State Circuits* **2008**, *43*, 2269–2283. [CrossRef]
25. Ahn, M.; Kim, B.S.; Lee, C.; Laskar, J. A high power CMOS switch using substrate body switching in Multistack structure. *IEEE Microw. Wirel. Compon. Lett.* **2017**, *17*, 682–684. [CrossRef]
26. Huang, Y.; Woo, W.; Yoon, Y.; Lee, C. Highly linear RF CMOS variable attenuators with adaptive body biasing. *IEEE J. Solid State Circuits* **2011**, *46*, 1023–1033. [CrossRef]