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Three-Phase Five-Level Cascade Quasi-Switched Boost Inverter

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Abstract: This paper presents a three-phase cascaded five-level H-bridge quasi-switched boost inverter (CHB-qSBI). The merits of the CHB-qSBI are as follows: single-stage conversion, shoot-through immunity, buck-boost voltage, and reduced passive components. Furthermore, a PWM control method is applied to the CHB-qSBI topology to improve the modulation index. The voltage stress across power semiconductor devices and the capacitor are significantly lower using improved pulse-width modulation (PWM) control. Additionally, by controlling individual shoot-through duty cycle, the DC-link voltage of each module can achieve the same values. As a result, the imbalance problem of the DC-link voltage can be solved. A detailed analysis and operating principle with the modulation scheme and comprehensive comparison for the CHB-qSBI are illustrated. The experimental and simulation results are presented to validate the operating principle of the three-phase CHB-qSBI.

Keywords: cascaded H-bridge inverter; three-phase inverter; Z-source network; quasi-switched-boost network; shoot-through

1. Introduction

Nowadays, multilevel inverters are attractive for high power high voltage applications due to their well-known properties. The benefits of the multilevel power inverter topologies are as follows: improved output waveforms, low electromagnetic interference (EMI), and small filter size [1–3]. Neutral point clamped (NPC), flying capacitors, and cascaded H-bridge (CHB) inverters [4–14] are three basic multilevel inverter structures. Among these structures, the CHB structures [9–14] have unique merits: higher output voltage, flexibility, and power levels. Furthermore, the CHB inverter can achieve high reliability with modular configuration. The output voltage of each phase in the CHB inverter is achieved by the sum of each output voltage. The CHB structure has some merits in using cascading more H-bridge modules and independent sources. Besides that, the output voltage of the CHB inverter has a high number of levels and reaches medium voltage which results in removing the boost transformer and dropping the size of the output filter. In [14], the low-frequency transformers were used to cascade the H-bridge circuit with a single DC source, but the size of the cascaded system is increased because of using low-frequency transformers.

However, the traditional CHB inverter [9–14] is a buck DC–AC power conversion. In addition, both power switches in the same branch cannot be turned on at the same time. To overcome the

limitation of the traditional CHB inverters, the CHB quasi-Z-source inverters (CHB-qZSI) were discussed in [15–17]. A battery-energy-stored CHB-qZSI-based photovoltaic power generation system was presented in [18]. To enhance the performance of the three-phase five-level CHB-qZSI for grid-connected applications, an innovative modulation technique was introduced in [19] for the voltage stress reduction. A fault-tolerant strategy for the three-phase CHB-qZSI was presented in [20]. In the CHB-qZSI, each module of the three-phase CHB-qZSI topology uses two inductors and two capacitors. As a result, the size, weight, and cost of the cascaded system are increased significantly when the number of output voltage levels is increased. The quasi-switched boost inverter (qSBI) topology had been introduced in [21] to replace the qZSI because it has the same feature as buck-boost voltage and high reliability with shoot-through (ST) immunity. A detailed comparison between qZSI and qSBI topology was discussed in [22]. The comparison results in [22] show that the qSBI topology uses one less capacitor and one less inductor; higher boost factor with the same parasitic effect; lower current rating on switches and diodes; and higher efficiency when compared to qZSI topology. However, with a simple boost control method, the modulation index is low when a voltage gain is required. To improve the modulation index, a novel pulse-width modulation (PWM) scheme for qSBI was proposed in [23]. The single-phase grid-connected CHB-qSBI was discussed in [24]. In CHB-qSBI [24], each module of the CHB-qSBI topology only uses one inductor and one capacitor. A three-phase CHB-qSBI has been proposed in [25] with only some simulation results. Besides that, with using a simple boost method, the CHB-qSBI in [24,25] must use a small modulation index to be able to achieve a high voltage gain. Consequently, the voltage stress across power semiconductor devices and capacitor is high.

To explore more features of the three-phase CHB-qSBI, this paper presents the operating theories, circuit analysis, and experimental verification of the three-phase CHB-qSBI in detail. Furthermore, a PWM control method in [23] is applied to the CHB-qSBI topology to improve the modulation index. The stress voltage across power semiconductor devices and the capacitor is significantly dropped in comparison to CHB-qSBI with using conventional PWM control. To solve the imbalance problem of the DC-link voltage, ST duty cycle of each module is controlled individually. As a result, the DC-link voltage of each module can obtain the same values. The simulation and experimental results are provided to validate the operating principle of the three-phase CHB-qSBI under improved PWM method.

2. Conventional Three-Phase CHB Inverter Topologies

Figure 1 illustrates the traditional three-phase five-level CHB inverter. Two H-bridge circuits were used in each phase to generate a five-level output voltage. Each H-bridge module was connected to the isolated DC voltage source. In the conventional CHB inverter, both upper and lower switches of the H-bridge leg cannot be switched on at the same time. The dead-time between upper and lower switches should be employed to avoid the ST phenomenon in the H-bridge circuit.

Figure 2 presents the three-phase CHB-qZSI topology, where each quasi-Z-source network module used two pair of inductor and capacitor. By adding the ST time interval to the H-bridge switches, the DC-link voltage of each H-bridge module in the CHB-qZSI was boosted to a higher value than the DC source voltage. The CHB-qZSI has the buck-boost voltage function, single-stage conversion, and ST immunity.

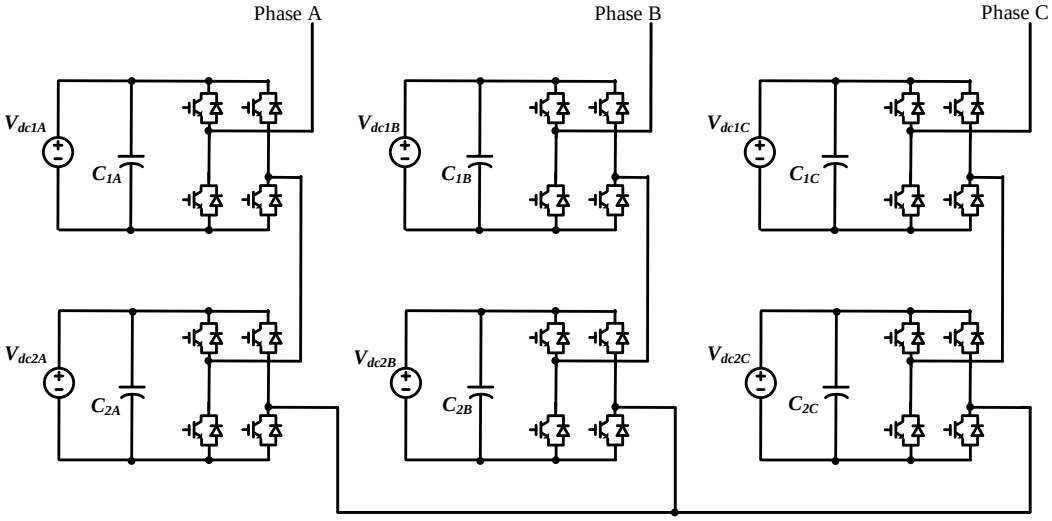

Figure 1. Construction of traditional three-phase cascaded H-bridge (CHB) inverter topology.

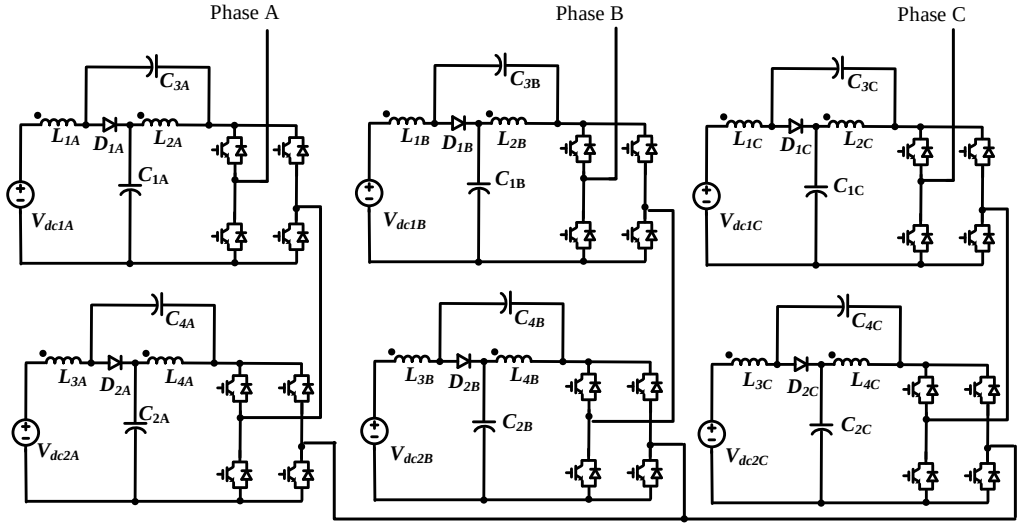

Figure 2. Construction of three-phase CHB quasi-Z-source inverters (CHB-qZSI) topology.

3. Three-Phase CHB-qSBI

The three-phase CHB-qSBI topology is indicated in Figure 3. Similar to conventional CHB inverter topology, each phase of the CHB-qSBI consists of two qSBI modules. The proposed cascaded system consists of six qSBI modules, three filter inductors, six separate DC sources, and a three-phase load. Compared to the conventional CHB module, a qSBI module includes one capacitor, one inductor, two diodes, and one active switch is added.

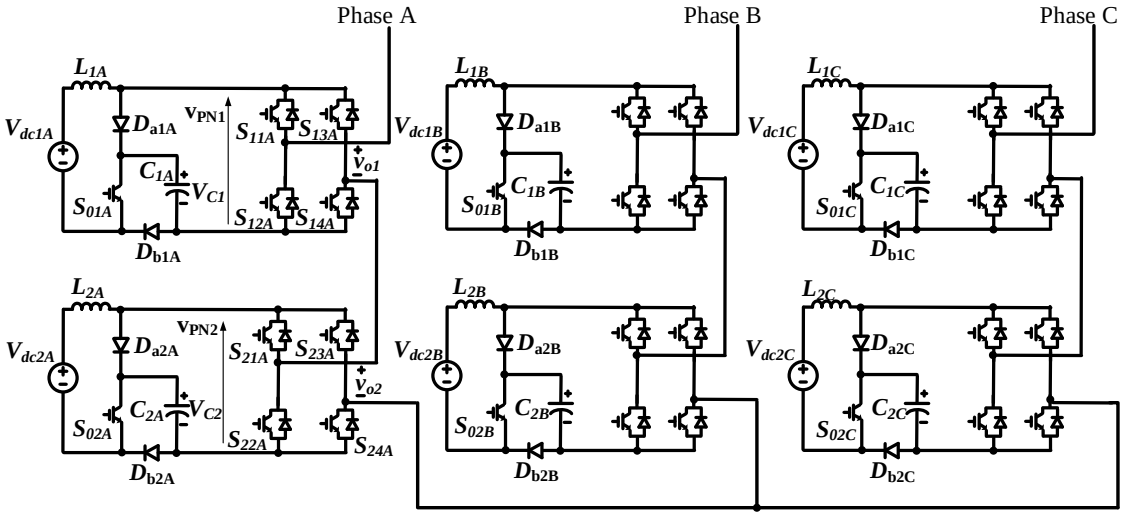

Figure 3. Proposed three-phase CHB quasi-switched boost inverter (CHB-qSBI) topology.

3.1. Operating Principle

As an example, the module 1 in the introduced system is used to analyze the circuit. As shown in Figure 4, there were three operating states: the non-shoot-through (NST) 1 state, the NST 2 state, and the shoot-through (ST) state.

In NST 1 state as shown in Figure 4a, switch S_0 is switched on. During this state, diode D_{a1} conducts while diode D_{b1} is blocked. As a result, the capacitor is discharged while the inductor stores energy. The time interval in this state is $(0.5 - D_1/2).T$, where D_1 is the duty cycle of each cycle of module 1; T is a switching period. We obtain:

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = V_{dc1} \\ C_1 \frac{dv_{C1}}{dt} = -I_{PN1}, \end{cases} \tag{1}$$

where I_{PN1} is the equivalent DC-link current at load side.

In ST state as shown in Figure 4b, both 4 switches on the H-bridge circuit and switch S_0 are switched on at the same time. During this state, two diodes D_{a1} and D_{b1} are blocked. As a result, the capacitor is discharged, while the inductor stores energy. The time interval in this state is $D_1.T$. We obtain:

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = V_{dc1} + V_{c1} \\ C_1 \frac{dv_{C1}}{dt} = -I_{in}, \end{cases} \tag{2}$$

where I_{in} is the average value of the input current (inductor current).

In NST 2 state as shown in Figure 4c, switch S_0 is switched off and the inverter has two active states and two zero states of the inverter main circuit for single-phase topology. During the NST state, D_{a1} and D_{b1} are turned on. As a result, the capacitor is charged from V_{dc1}, while the inductor transfers energy from the DC voltage source to the main circuit. The time interval in this state is $(0.5 - D_1/2).T$. We obtain:

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = V_{dc1} - V_{c1} \\ C_1 \frac{dv_{C1}}{dt} = I_{in} - I_{PN1}. \end{cases} \tag{3}$$

Applying the volt-second balance and ampere-second balance principles to L and C in steady state, Equations (1), (2), and (3) yield:

$$\begin{cases} V_{c1} = \frac{2}{1-3D_1} V_{dc1} \\ I_{in} = \frac{2(1-D_{1)}}{1-3D_1} I_{PN1}. \end{cases} \tag{4}$$

The peak value of DC-link voltage that crosses the inverter of module 1 can be expressed in the NST states as:

$$V_{PN1} = V_{c1} = \frac{2}{1-3D_1} V_{dc1} \quad (5)$$

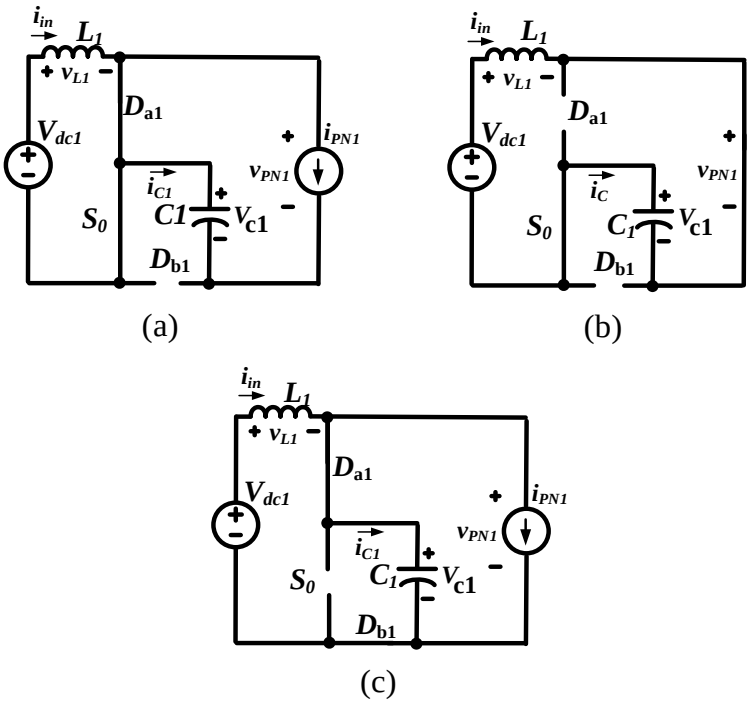

Figure 4. Operating states of qSBI module 1: (**a**) non-shoot through (NST) 1, (**b**) shoot-through (ST), and (**c**) NST 2 states.

3.2. Improved PWM Control for Three-Phase CHB-qSBI

A PWM technique for the single-phase qSBI to improve modulation index was presented in [23]. In this section, the PWM technique in [23] will be extended to the three-phase CHB-qSBI. The PWM strategy for the cascaded system for phase A with the modulation in Figure 4 is illustrated in Figure 5. For module 1, a fixed voltage V_{SH1} was compared to the triangle waveform (dashed line) with double frequency and half of the amplitude of that of V_{tri} to generate the ST state in the inverter bridge. Besides that, a square pulse signal with the same frequency as the triangle waveform (dashed line) and 50% duty cycle was used to control the S_0 switch. Two control waveforms, $V_{control}$ and $-V_{control}$, were compared to a triangle waveform, V_{tri}, to generate control signals for H-bridge switches. The additional switch S_0 signal was produced by comparing between the saw-tooth waveform, v_{saw} and V_{SH1}. Table 1 describes a truth table of the switching states of the switches in module 1. The switching status 0 and 1 in Table 1 represents the turning off and turning on of the switches, respectively.

The output voltage v_{o1} of H-bridge module 1 has three levels: $-V_{PN1}$, 0, and V_{PN1}. For module 2, the high-frequency triangle waveform, V_{tri}, was shifted in 90° and the high-frequency triangle waveform *v_{tri} was shifted in 180° to generate the output voltage v_{o2} of H-bridge module 2. The output voltage of the cascaded system is total v_{o1} and v_{o2}. As a result, the 5-level output voltage of the proposed cascaded system was produced.

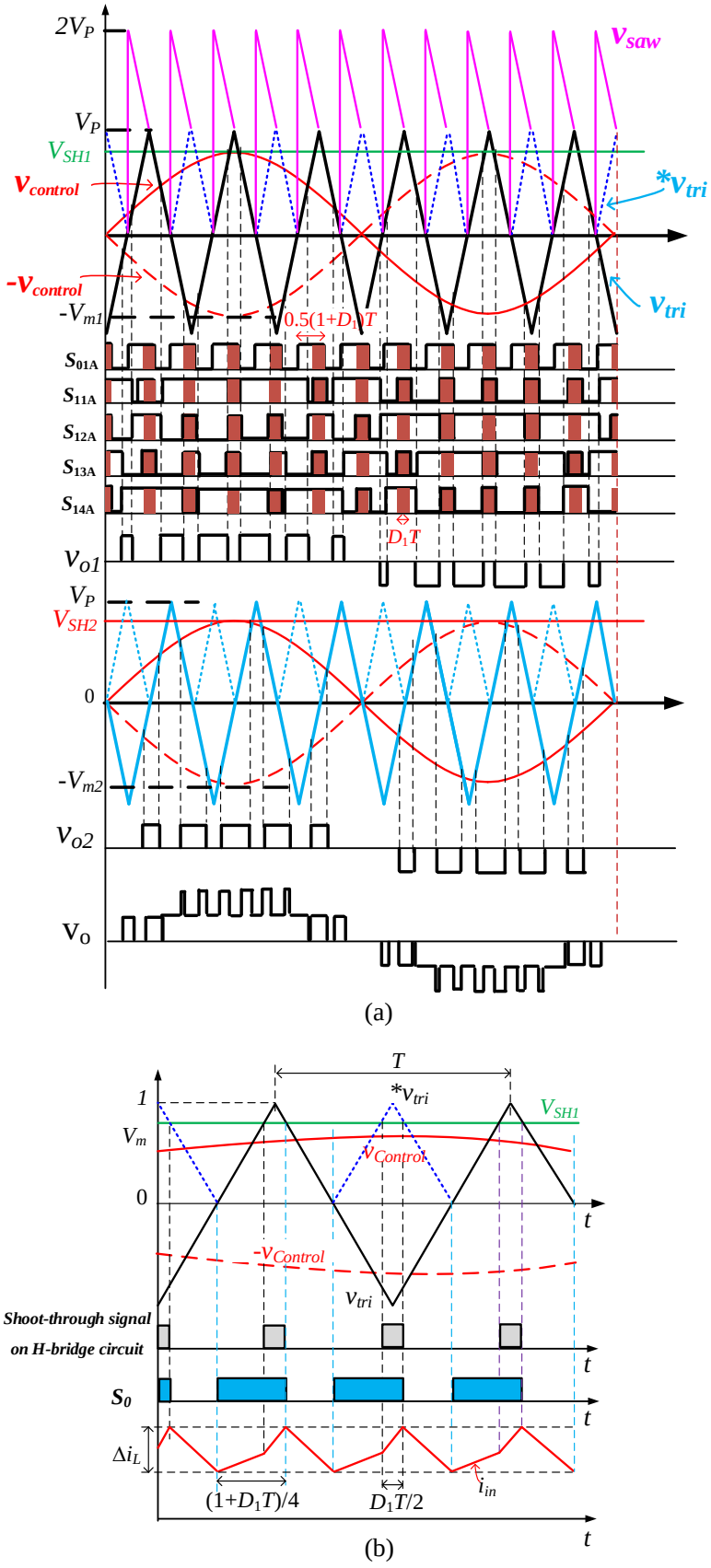

Figure 5. Improved PWM strategy for three-phase CHB-qSBI. (**a**) Improved PWM strategy for phase-A of the CHB-qSBI and (**b**) ST on H-bridge and S_0 signal generation.

Table 1. A truth table of switching signal generation in module 1.

Compared Condition	Status of Switches				
	S_{01A}	S_{11A}	S_{12A}	S_{13A}	S_{14A}
$V_{SH1} \leq {}^{*}v_{tri}$	1	1	1	1	1
$V_{SH1} \leq v_{saw}$	1	-	-	-	-
$V_{SH1} > v_{saw}$	0	-	-	-	-
$v_{control} > v_{tri}$	-	1	0	-	-
$v_{control} \leq v_{tri}$	-	0	1	-	-
$-v_{control} > v_{tri}$	-	-	-	1	0
$-v_{control} \leq v_{tri}$	-	-	-	0	1

"-": Undefinable state.

4. Comparison between Three-Phase CHB-qSBI under Improved PWM Method and Three-Phase CHB-qZSI

Table 2 compares the passive components, semiconductor devices, and the governing equations of the three-phase CHB-qSBI and the three-phase CHB-qZSI. From Table 2, the three-phase five-level CHB-qSBI uses six fewer capacitors, six fewer inductors, six more switches, and six more diodes. Although the three-phase CHB-qSBI reduces the number of passive components, it increases the number of active components. The three-phase CHB-qSBI under the improved PWM method uses a higher modulation index to produce the same voltage gain. Figure 6 compares the voltage stresses on diodes and switches of the CHB-qZSI and CHB-qSBI for the same voltage gain. As shown in Figure 6, the voltage stresses of the CHB-qSBI is lower than those of the CHB-qZSI. Consequently, the stress voltage across power semiconductor devices and the capacitor of the three-phase CHB-qSBI was significantly lower. Therefore, the weight, cost, and size of the three-phase CHB-qSBI under the improved PWM method were reduced in comparison with the three-phase CHB-qZSI topology.

Table 2. Comparison between CHB-qSBI and CHB-qZSI.

Parameter		Three-Phase CHB-qZSI	Three-Phase CHB-qSBI
Number of inductors		12	6
Number of capacitors		12	6
Number of diodes		30	36
Number of switches		24	30
Capacitor voltage	$V_{C1} = V_{C2}$	$\frac{1-D}{1-2D} V_{dc}$	$\frac{2}{1-3D} V_{dc}$
	$V_{C3} = V_{C4}$	$\frac{D}{1-2D} V_{dc}$	NA
DC-Link voltage each module, V_{PN}		$\frac{1}{1-2D} V_{dc}$	$\frac{2}{1-3D} V_{dc}$
Diodes voltage stresses, V_D		$\frac{1}{1-2D} V_{dc}$	$\frac{2}{1-3D} V_{dc}$
Switches voltage stresses, V_S		$\frac{1}{1-2D} V_{dc}$	$\frac{2}{1-3D} V_{dc}$
Voltage gain, G at each module		$\frac{M}{2M-1}$	$\frac{2M}{3M-2}$
ST immunity		Yes	Yes
Input current		Continuous	Continuous

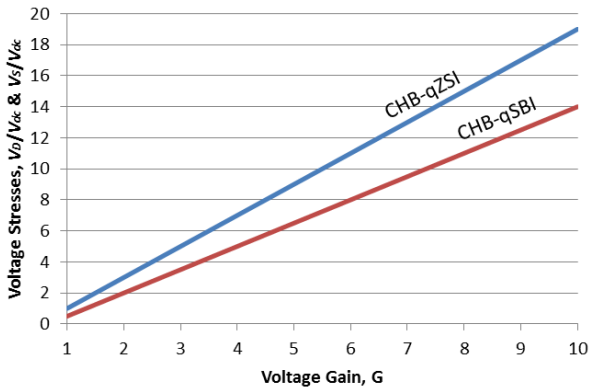

Figure 6. Voltage stress comparison for the same voltage gain.

5. Simulation and Experimental Verifications

5.1. Simulation Verification

To confirm the theoretical discussion of the three-phase CHB-qSBI in this paper, the software for power electronic named PSIM 9.1 was used to simulate the suggested inverter. The major parameters of the simulation are as follow: the output phase voltage is 220 Vrms with five-level; the AC side filter and load are 10 mH and 30 Ω, respectively; the inductor-capacitor and switching frequency for each module are 1 mH, 2200 μF, and 10 kHz. The list of parameters in the simulation is provided in Table 3. It is worth noting that the high valued DC electrolytic capacitors of 2200 μF were used in the simulation and experiment because the double-line-frequency ripple is not suppressed in the CHB-qSBI system. As analyzed in [16,22,26], the single-phase qSBI had a double-line-frequency ripple on the passive element at the DC side. The double-line-frequency ripple caused several problems related to efficiency, lifetime, cost, size, and reliability of the inverter system. To suppress the double-line-frequency ripple on quasi-switched boost network, a feedback controller for qSBI was introduced in [27].

Table 3. Parameters for the three-phase CHB-qSBI inverter.

Parameter		Value
Output voltage		220 Vrms
Output frequency		50 Hz
Inductors		1 mH
Capacitors		2200 uF
Load	Inductor (L_f)	10 mH
	Resistor (R)	30 Ω
Switching frequency		10 KHz

The simulation results for the three-phase CHB-qSBI are noted in Figures 7 and 8. In Figure 7, the input voltages of V_{dc1} and V_{dc2} were set the same value of 50 V. It is clear that both the capacitor voltages in all quasi-switched-boost networks were boosted to 195 V. The DC-link voltages were the square waveform and the peak DC-link voltages were equal to the capacitor voltages, as shown in Figure 7c. The DC-link voltage of two quasi-switched-boost modules was the same with the same ST duty cycle. The root mean square (RMS) value output voltage for each phase was 220 V. The peak output current in each phase was 10.3 A. The total harmonic distortion (THD) of the output phase current was 1.6%. Figure 7e shows the simulation results at the start-up process. The inrush currents have appeared in the inductors at the start-up owing to the existing passive elements in the quasi-switched-boost network. It can be seen in Figure 7a that the proposed three-phase CHB-qSBI operated in a stable state after 0.15 s. Figure 7e shows the simulation results when the load was changed from 30 Ω to 60 Ω at 0.4 s.

Next, the suggested inverter was tested with the unbalanced condition of the input voltage. The input voltage V_{dc1} was 40 V, while V_{dc2} was 50 V. In Figure 8, the simulation results for unbalanced input voltage have been shown. The capacitor voltage and the DC-link voltage are slightly different between the two quasi-switched-boost modules; this is a small insignificant difference in the steady state. Clearly, both of the capacitor voltages in all quasi-switched-boost parts were also boosted to 195 V. The DC-link voltages were the square waveform and the peak DC-link voltages were equal to the capacitor voltages, as shown in Figure 8c. The DC-link voltage of two quasi-switched-boost modules was the same with the same ST duty cycle. The RMS value of the output voltage for each phase was 220 V. The peak output current in each phase was 10.3 A. The THD of the output phase current was 1.7%. The suggested inverter can improve the unbalanced problems in comparison with the conventional CHB inverter.

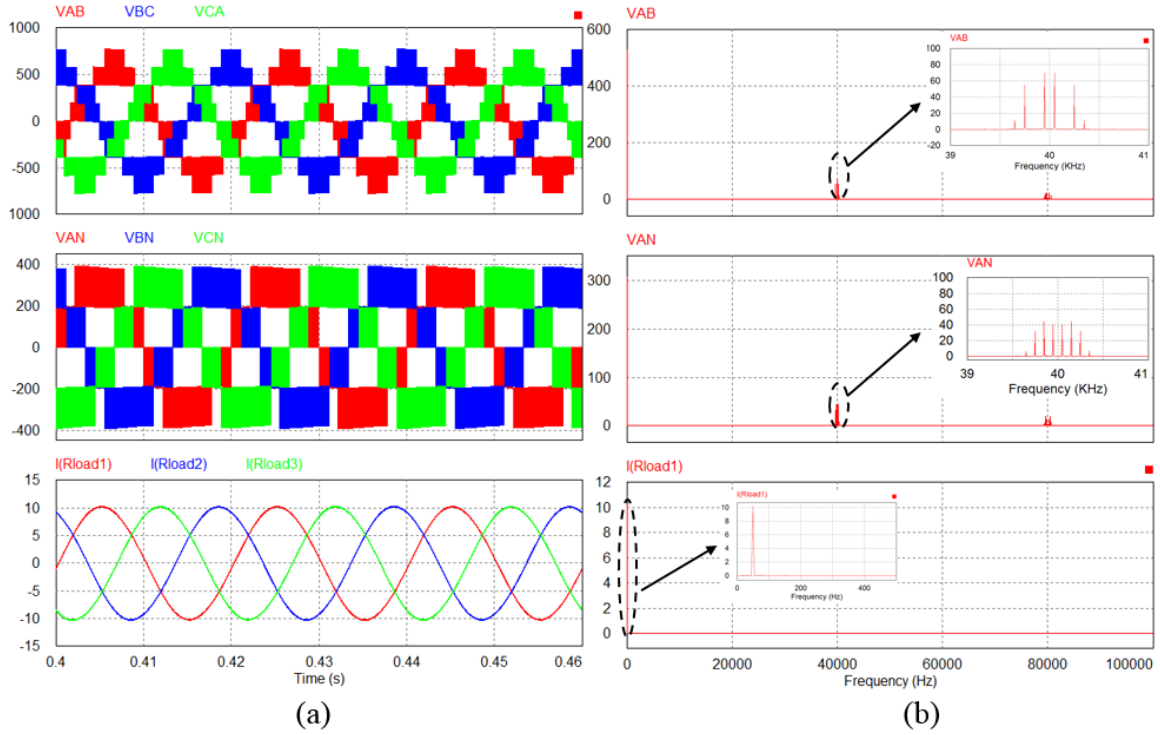

Figure 7. *Cont.*

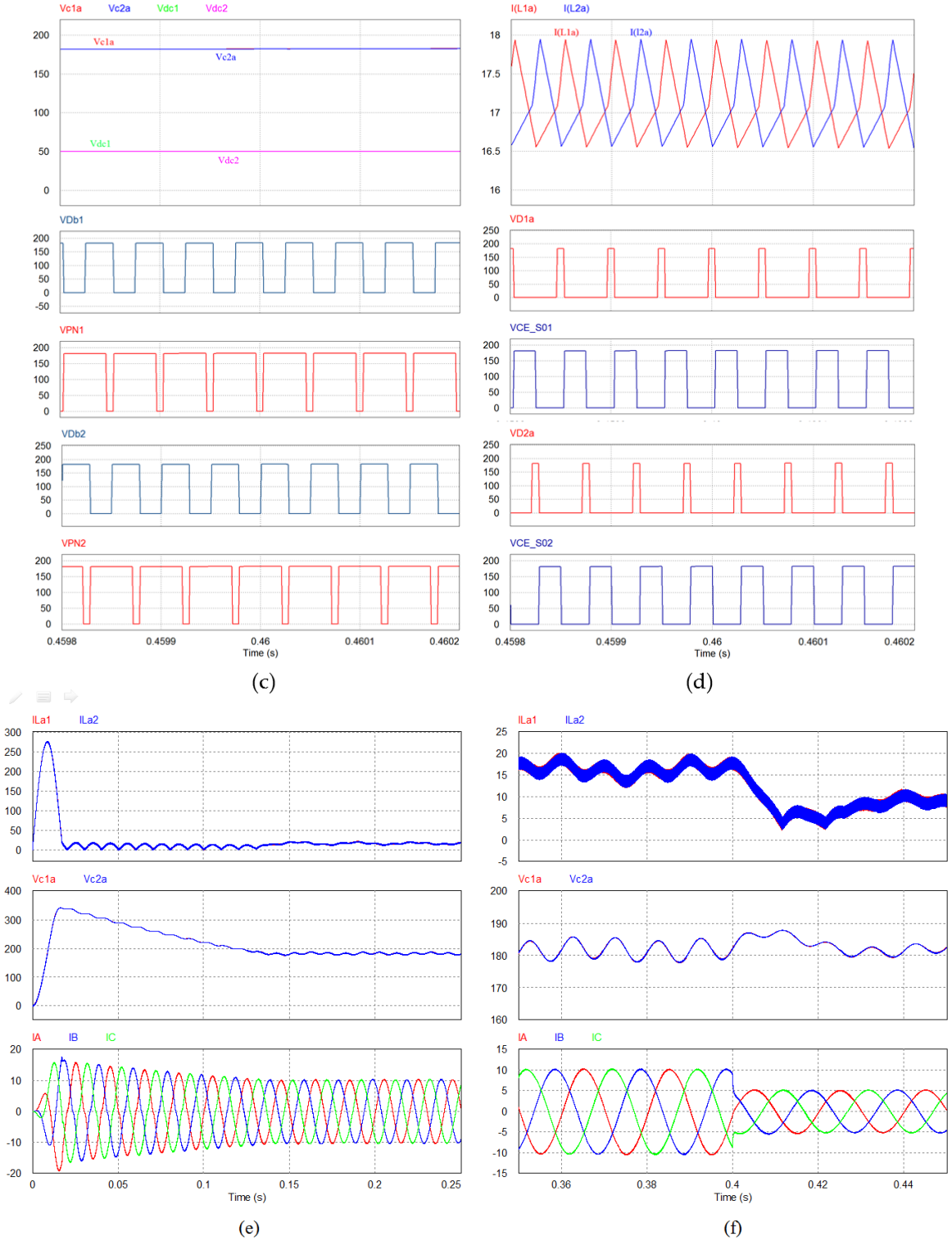

Figure 7. Simulation results for the CHB-qSBI when the input voltage $V_{dc1} = V_{dc2} = 50$ V. From top to bottom: (**a**) output line-to-line voltages, output phase voltages, and phase currents; (**b**) harmonic spectrum of output line-to-line voltages, harmonic spectrum of output phase voltages, and harmonic spectrum of phase currents; (**c**) input voltages, capacitors C_1 and C_2 voltages, diodes D_{b1} and D_{b2} voltages, and DC-link voltages; (**d**) inductor currents, diode D_{a1} voltage, switch S_{01} voltage, diode D_{a2} voltage, and switch S_{02} voltage of phase A; (**e**,**f**) inductor currents, capacitor voltages, and output phase current.

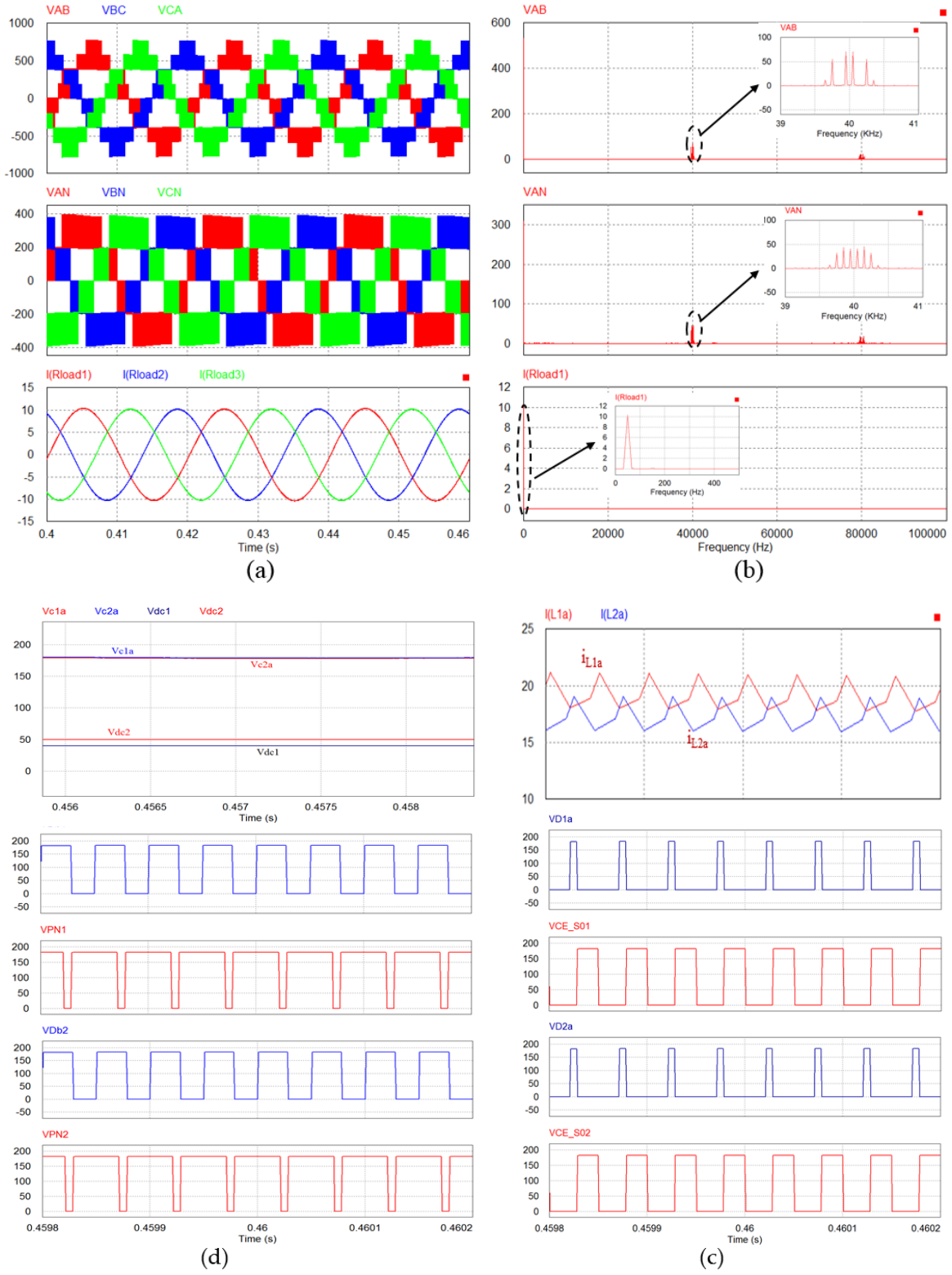

Figure 8. Simulation results for the CHB-qSBI when the input voltage V_{dc1} = 40 V and V_{dc2} = 50 V. From top to bottom: (**a**) output line-to-line voltages, output phase voltages, and phase currents; (**b**) harmonic spectrum of output line-to-line voltages, harmonic spectrum of output phase voltages, and harmonic spectrum of phase currents; (**c**) input voltages, capacitors C_1 and C_2 voltages, diodes D_{b1} and D_{b2} voltages, and DC-link voltages; and (**d**) inductor currents, diode D_{a1} voltage, switch S_{01} voltage, diode D_{a2} voltage, and switch S_{02} voltage of phase A.

5.2. Experimental Verifications

A scaled-down laboratory prototype of the three-phase CHB-qSBI inverter was built as shown in Figure 9. The microcontroller was DSP TMS320F28335. All switches were G40N120 IGBTs. The diodes were DSEI60-06A. The inductors, capacitors, and load parameters in the experiment were the same as the simulation. The switching frequency was 10 kHz. The RMS value of the output voltage for each phase was 110 V.

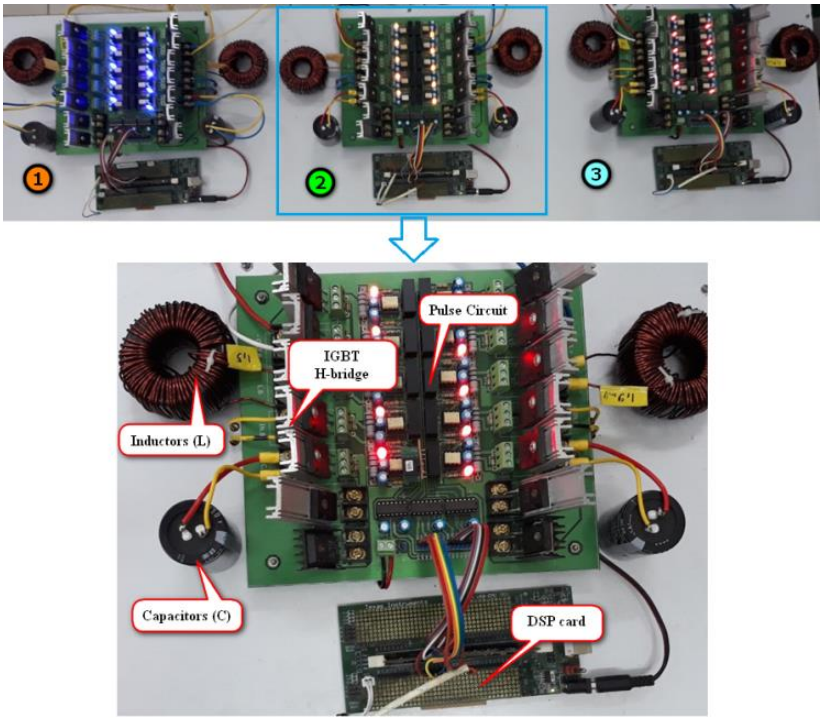

Figure 9. The prototype model with three-phase CHB-qSBI.

The experimental results were tested with the unbalanced input voltage condition. The input voltages V_{dc1} and V_{dc2} were 20 V and 25 V, respectively. The capacitor voltage and DC-link voltage were boosted to the same value of 92 V for all modules, shown in Figure 10a. The DC-link voltage of the two modules was kept on the same value by controlling the ST duty cycle even though the input voltage of the two modules was different. The output phase voltage, V_{AN}, had five levels: −180 V, −90 V, 0, 90 V, and 180 V, as shown in Figure 10b. The maximum output voltage had a lower value than the total voltage of DC-link voltages because of the voltage drop in the H-bridge circuit. The measured output phase voltage after the filter was 110.5 Vrms. The measured output current was 3.68 Arms, as shown in Figure 10e. The three-phase output voltage and harmonic spectrum of phase-A voltage are seen in Figure 10c,d. The THD of output voltage after the filter was 2.67%. The experimental results were consistent with the simulation.

The efficiency of the proposed inverter was measured at the unbalanced condition input voltage, V_{dc1} = 20 V and V_{dc2} = 25 V, as shown in Figure 11. The maximum efficiency of the inverter was 86.8% at the output power of 630 W. The efficiency of the inverter was not high because the selection of semiconductor devices in the experiment was not optimal.

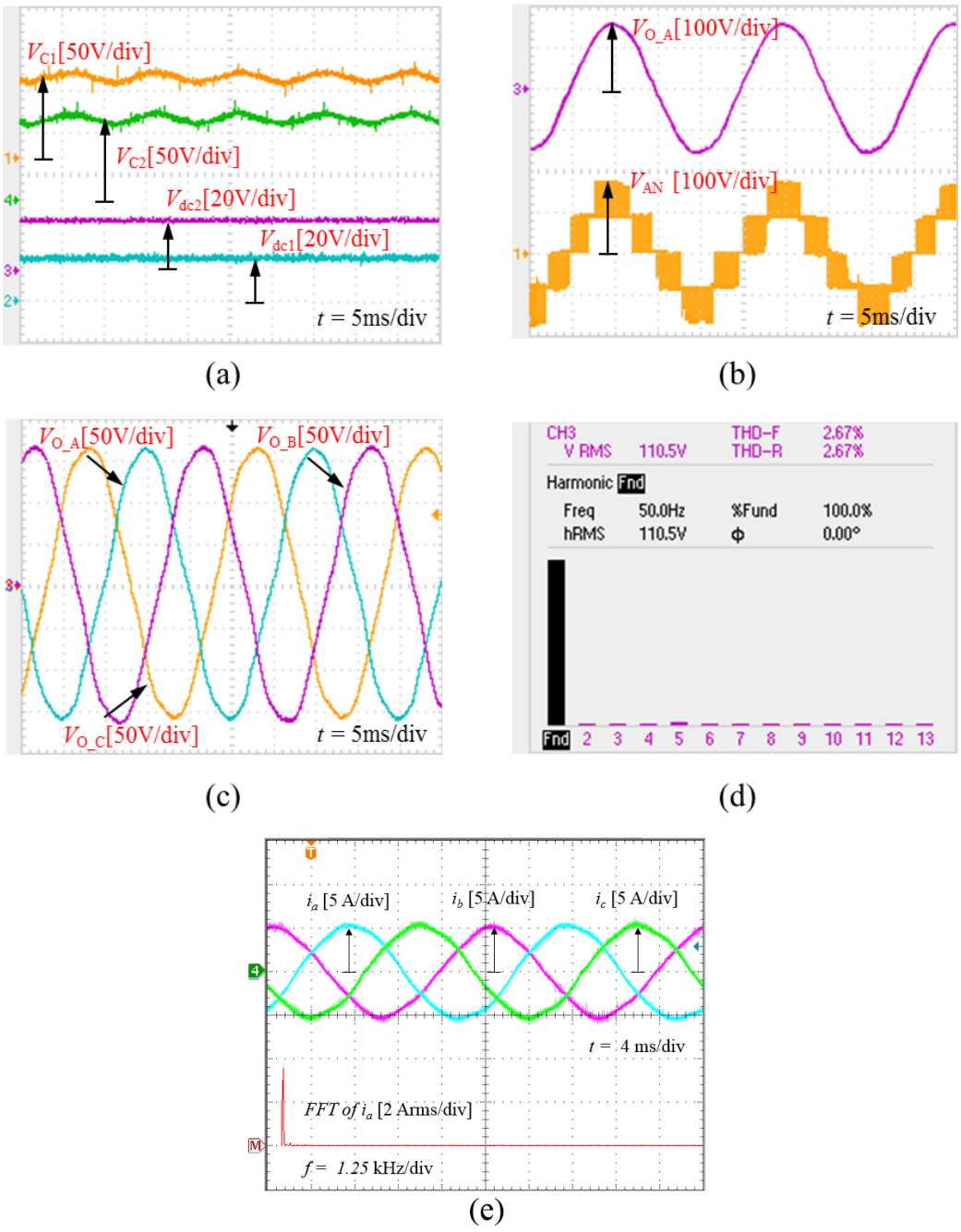

Figure 10. Experimental results for the suggested inverter with the unbalanced condition input voltage, V_{dc1} = 20 V and V_{dc2} = 25 V. (**a**) Input voltage and capacitor voltage in qSBI stages; (**b**) five-level output voltage before and after the filter of phase A (V_{AN}); (**c**) three-phase output voltage; (**d**) harmonic spectrum of output voltage, and (**e**) output currents and harmonic spectrum of output phase-A current.

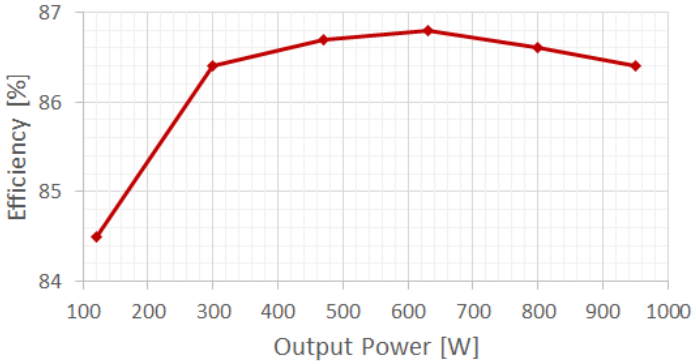

Figure 11. The efficiency of the proposed inverter at the unbalanced condition input voltage, V_{dc1} = 20 V and V_{dc2} = 25 V.

6. Conclusions

The configuration three-phase CHB-qSBI is presented in this paper. The three-phase CHB-qSBI can buck-boost voltage with single-stage power conversion. Furthermore, the three-phase CHB-qSBI immunized the ST phenomenon. In comparison to the three-phase CHB-qZSI, the CHB-qSBI dropped a large number of inductors and capacitors. The DC-link voltage of each module can achieve the same values by controlling the ST duty cycle. The paper describes the circuit analysis, operating theories, and PWM strategy of the introduced topology. Simulation and experimental results prove the validity of the improved PWM strategy for controlling the three-phase CHB-qSBI. The three-phase CHB-qSBI can be applicable.

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Abbreviations

CHB	Cascaded H-bridge
D_1	Shoot-through duty cycle
DSP	Digital signal processing
EMI	Electromagnetic interference
FC	Flying capacitor
NPC	Neutral point clamped
NST	Non-shoot-through
PWM	Pulse-width modulation
qSBI	quasi-switched boost inverter
ST	Shoot-through
T	Period time
qZSI	Quasi-Z-source inverter

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