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A 2.6 GS/s 8-Bit Time-Interleaved SAR ADC in 55 nm CMOS Technology

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Abstract: This paper presents an eight-channel time-interleaved (TI) 2.6 GS/s 8-bit successive approximation register (SAR) analog-to-digital converter (ADC) prototype in a 55-nm complementary metal-oxide-semiconductor (CMOS) process. The channel-selection-embedded bootstrap switch is adopted to perform sampling times synchronization using the full-speed master clock to suppress the time skew between channels. Based on the segmented pre-quantization and bypass switching scheme, double alternate comparators clocked asynchronously with background offset calibration are utilized in sub-channel SAR ADC to achieve high speed and low power. Measurement results show that the signal-to-noise-and-distortion ratio (SNDR) of the ADC is above 38.2 dB up to 500 MHz input frequency and above 31.8 dB across the entire first Nyquist zone. The differential non-linearity (DNL) and integral non-linearity (INL) are +0.93/−0.85 LSB and +0.71/−0.91 LSB, respectively. The ADC consumes 60 mW from a 1.2 V supply, occupies an area of 400 μm × 550 μm, and exhibits a figure-of-merit (FoM) of 348 fJ/conversion-step.

Keywords: analog-to-digital converter; successive approximation register; direct sampling; time-interleaved; channel-selection-embedded bootstrap; segmented pre-quantization and bypass

1. Introduction

High-speed analog-to-digital converters (ADCs) with a moderate resolution of 6–8 bits while maintaining excellent power efficiency for longer battery life are highly demanded for applications such as 802.11 ad (WiGig) radio architectures and the next-generation mobile communication system (5G) [1]. Compared with flash and pipeline ADC, successive approximation register (SAR) ADC has superior energy efficiency and is more suitable for the aggressive downscaling of technology because of its primarily digital nature [2–4]. In order to overcome the speed limitation of a single ADC, time-interleaved (TI) architecture running multiple parallel ADCs is an attractive approach. In general, TI SAR ADC is the most feasible solution to realize both over GHz operation and medium resolution around 8-bit [5]. However, the inter-channel non-ideal factors like offset, gain mismatch, and time skew, will deteriorate the overall performance [6], and can be compensated for by either circuit improvement in the analog domain or special digital calibration. As digital calibration is often complex, it is preferred to minimize these mismatches using on-chip design optimization to relax calibration requirements, especially when the number of interleaved channels is not large.

This paper demonstrates a 2.6 GS/s 8-bit SAR ADC prototype with an eight-channel direct sampling TI architecture. In the sampling front-end, in order to suppress the time skew error among

different channels, the channel-selection-embedded bootstrap switch is used as the sampling switch to ensure the uniformity of sampling times by the master clock. In the sub-channel SAR ADC design, segmented pre-quantization and a bypass switching scheme is employed to avoid unnecessary large capacitors switching, reducing power consumption and non-linearity. Double comparators clocked asynchronously in alternate mode are used to improve the conversion rate, with the background offset calibration function integrated on-chip. This ADC exhibits lower calibration complexity and achieves an acceptable efficiency in terms of area and power consumption.

2. Proposed TI SAR ADC Architecture

TI structures can generally be categorized as hierarchical sampling and direct sampling. In a hierarchical sampling structure, there are at least two sampling switches in series in each sub-channel. In contrast, a direct sampling architecture, wherein all parallel channels have individual sample/hold circuits, provides the shortest signal transmission path from the input to the sampling capacitors, and is very efficient for a small number of parallel channels (usually $\leq$8) [7].

In this design, a direct sampling architecture is adopted to implement the 2.6 GS/s 8-bit TI ADC prototype, which mainly consists of multi-phase clock generator (MPCG), sampling switch, eight-channel 325 MS/s 8-bit SAR ADC, and multiplexer (MUX), as depicted in Figure 1.

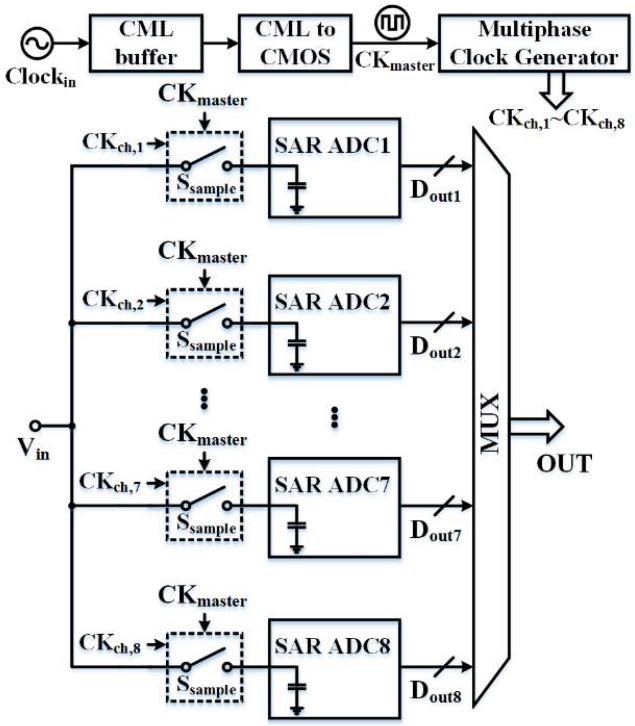

Figure 1. Eight-channel time-interleaved (TI) successive approximation register (SAR) analog-to-digital converter (ADC) architecture.

The current-mode logic (CML) sinusoidal input clock signal is buffered and then transformed to complementary metal-oxide-semiconductor (CMOS) level full-speed master clock CK_{master}. The multi-phase clock pulse signals $CK_{ch,1}$–$CK_{ch,8}$ are generated from CK_{master} using the cascaded D flip-flop (DFF) chain [8–10] and combinational logic circuits using synchronous frequency division, as shown in Figure 2a.

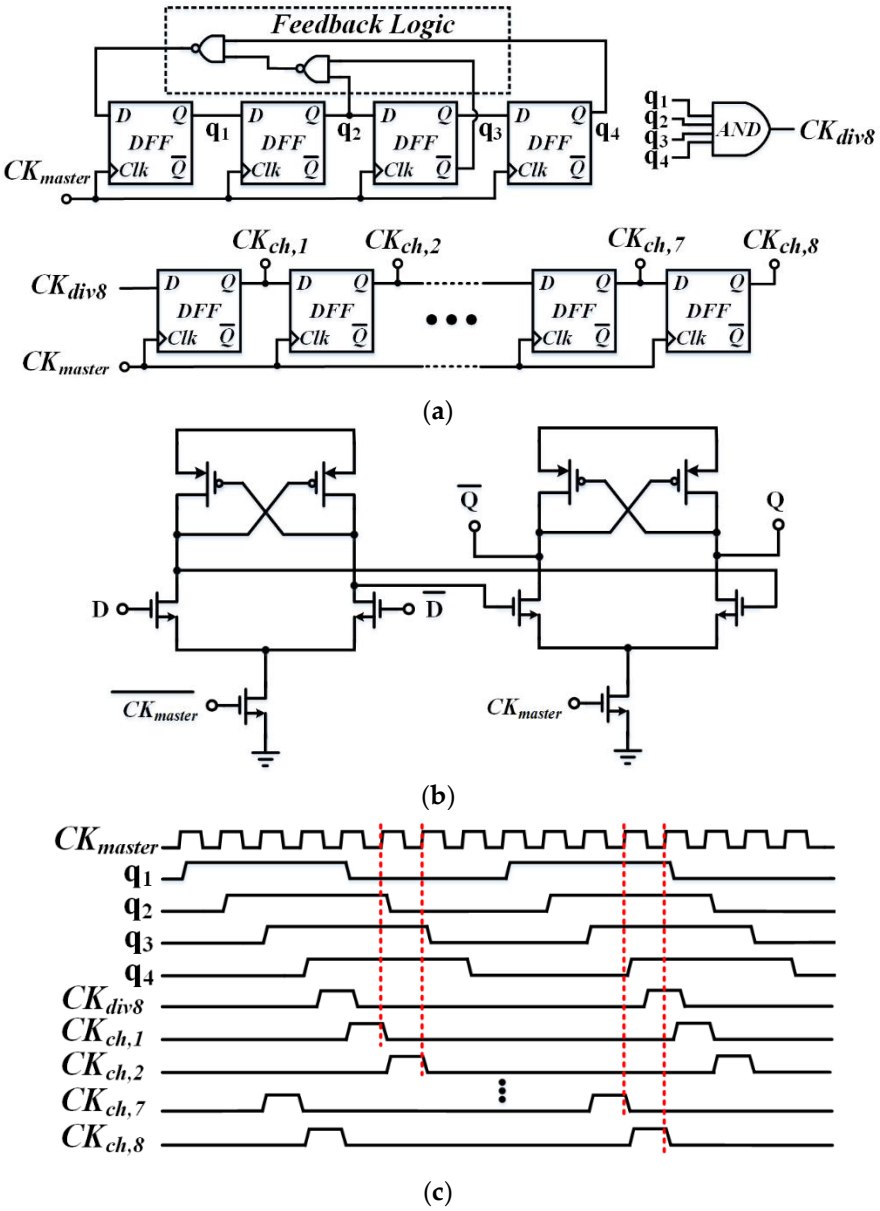

Figure 2. (**a**) Multi-phase clock generator (MPCG), (**b**) D flip-flop (DFF), and (**c**) timing diagram.

The DFF is constructed using two latches [11], as shown in Figure 2b. The internal signals q1, q2, q3 and q4 with a duty cycle of 50% are the divide-by-eight clocks of CK_{master} such that a clock pulse signal CK_{div8} with a duty cycle of 12.5% is obtained through AND logic operation. Since the initial state of the shift registers is uncertain, the feedback logic is added to activate self-starting such that the MPCG can automatically return from the non-ideal state to normal. The shift operation of CK_{div8} is executed to get $CK_{ch,1}$–$CK_{ch,8}$, which have definite phase sequence relationships and the delay between each other is one period of CK_{master}, as shown in Figure 2c. The non-overlapping sampling phases guarantee that only one sampling switch is turned on, thus reducing the channel load at the input. $CK_{ch,1}$–$CK_{ch,8}$ are not only used as the control signals for the sampling switches, but also initiate the conversion process of each channel.

As the input signal is sampled onto the capacitors array of respective sub-ADC sequentially for quantization, the sampling instants are controlled uniformly using CK_{master} to mitigate the time skew between channels. Finally, the multi-path digital outputs from the sub-ADCs array are aggregated into a one-way data stream using MUX.

3. Circuit Implementation Details

3.1. Channel-Selection-Embedded Bootstrap Switch

Time skew refers to the mismatch in the sampling instants among TI channels, which originated from the non-uniform sampling clock edges [12]. Some timing-skew, calibration-free techniques have been proposed to suppress the time skew by circuit design and layout [13–15]. We attempted to realize similar skew tolerance via circuit improvement in the analog domain for design simplicity rather than digital calibration with complex algorithms that will consume extra hardware and power. The channel-selection-embedded bootstrap switch [16] is utilized in the sampling front-end, so that the sampling instants of each channel are aligned to the master clock CK_{master}, while the corresponding TI clock signals $CK_{ch,i}$ (i = 1–8) are used to perform the channel selection, as described in Figure 3.

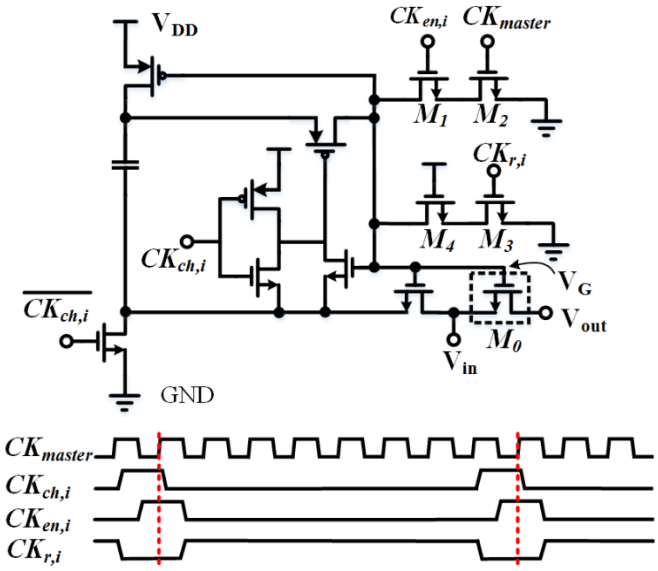

Figure 3. Channel-selection-embedded bootstrap switch.

When $CK_{ch,i}$ becomes high, the switching transistor M_0 is turned on, and the channel begins to track the input signal. $CK_{en,i}$ is a delayed version of $CK_{ch,i}$, used to prepare for sampling synchronization. When $CK_{en,i}$ is high, once the rising edge of CK_{master} comes, M_1 and M_2 are both turned on, and the gate voltage V_G of M_0 is released from V_{in} + V_{DD} to the ground level, thus the sampling instants are determined by the rising edge of CK_{master}. Then, the channel finishes the sampling process and enters the holding phase. As $CK_{en,i}$ goes low, the gate of M_0 is in floating state and vulnerable to the interference of other signals. M_3 from $CK_{r,i}$ provides a discharging path, and the V_G is fixed to the ground level, therefore avoiding the floating node at the holding phase. The inter-channel sampling synchronization that is determined uniformly by CK_{master} ensures the consistency of the sampling instants, and it is beneficial to suppress the time skew among channels.

3.2. Sub-ADC Design

3.2.1. Asynchronous Timing of Alternate Comparators

The sub-ADC is implemented with 325 MS/s 8-bit SAR ADC [17], including fundamental building blocks, such as capacitive digital-to-analog converter (CDAC), comparators and control logic, as illustrated in Figure 4a.

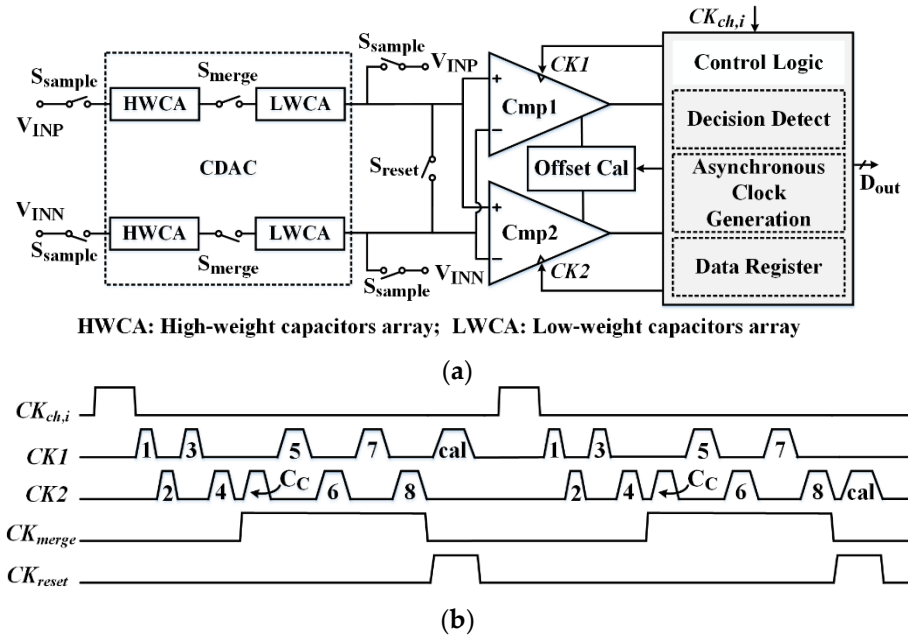

Figure 4. (**a**) SAR ADC overview, and (**b**) asynchronous timing diagram.

If only one comparator is used in the SAR ADC, the comparator needs to be fully reset to avoid the residual effect from the previous conversion process, so the overall conversion speed is slowed down. Double dynamic comparators with cross-coupled latches are used [18], and the preamplifier has been designed for moderate gain to reduce its offset, and more importantly, to limit the kick-back noise from the latch [19]. The two comparators are clocked asynchronously in alternate operation, as shown in Figure 4b. Under the control of *CK1* and *CK2*, when one comparator is in a comparison state, another comparator is reset, reducing the impact of reset time on the critical path, and thus improving the conversion speed [20]. Once the preceding comparison is over, a successful decision is detected as the trigger signal for the following comparison process. This asynchronous conversion process repeats like dominoes until all bits are resolved [21].

The pulse labeled "C_C" corresponds to the operation for the compensation capacitor in the CDAC. At the end of the conversion, the inputs of the comparators are shorted together using CK_{reset} for calibration purposes. With the pulse labeled "cal" the background offset calibration based on the charge pump principle in the analog domain for each comparator is carried out once every two cycles.

3.2.2. The Background Offset Calibration of Comparator

The diagram of comparator's background offset calibration is shown in Figure 5. An auxiliary differential pair is introduced to calibrate the offset voltage of the comparator. Only the generation circuit of V_{calp} is presented. Another calibration voltage V_{caln} can be generated in two ways, one is set to a constant voltage using a resistive voltage divider [20], and the other is similar to the generation of V_{calp}, except that the corresponding control voltage is different. In this design, the latter method is adopted. V_{calp} and V_{caln} change in opposite directions and jointly cancel the impact of the offset.

During the offset calibration phase of the comparator, the input signals V_{ip} and V_{in} of the main differential pair are shorted together. In the case of no offset, $V_{ip} = V_{in}$, then the output voltage of the preamplifier stage is equal, that is, $V_A = V_B$. Finally, the output signal of the comparator $OUTP = OUTN = 0$, and the corresponding complementary output signal $\overline{OUTP} = \overline{OUTN} = 1$. At this time, M5 and M8 are on, the upper capacitor C_p is charged to the power supply, and the lower C_p is discharged to the ground level. Both M6 and M7 are off, and the calibration voltage V_{calp} remains unchanged. There is no calibration effect yet.

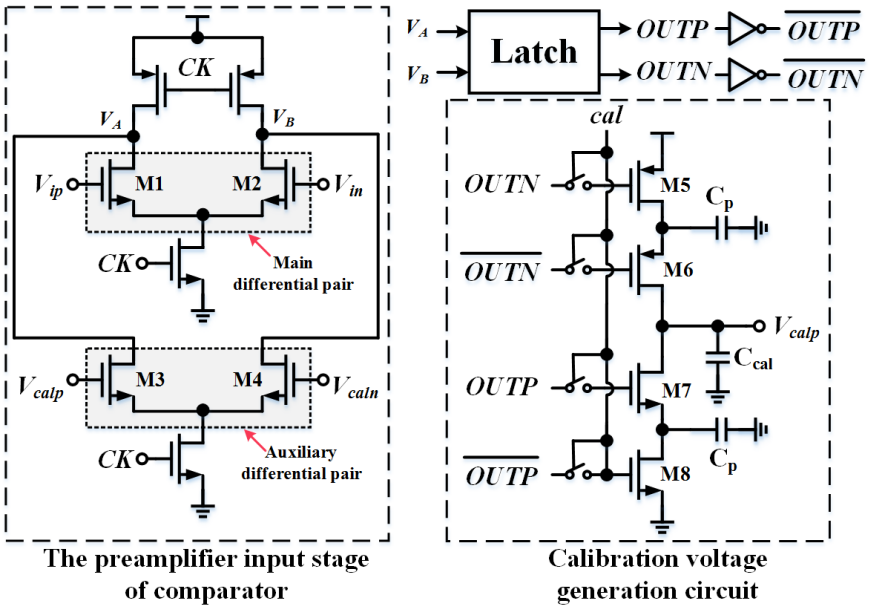

Figure 5. The diagram of comparator's background offset calibration.

If the offset exists, *OUTP* or *OUTN* will change. Usually, the output changes caused by offset can be equivalent to the input changes. Taking an offset output case as an example, if *OUTP* = 0 and *OUTN* = 1, this offset effect is the same as the situation when $V_{ip} < V_{in}$. Note that $V_A > V_B$ now. In the calibration voltage generation circuit, M6 is turned on, the voltage on C_p charges C_{cal}, and V_{calp} is pumped up. Then V_{calp} is fed back to the preamplifier input stage such that V_A decreases to approximate V_B. After a number of calibration cycles, once the decreasing V_A is equal to V_B, *OUTP* = *OUTN*, thereby realizing offset calibration. The calibration step size or accuracy is related to the capacitance values of C_p and C_{cal}. The parasitic capacitor can be used as C_p, which is usually small. The larger the calibration capacitor C_{cal}, the higher the calibration accuracy and the better the calibration effect. However, a large C_{cal} will affect the calibration settling time, and a trade-off between calibration accuracy and settling time is required to determine the value of C_{cal}.

3.2.3. Segmented Pre-Quantization and Bypass Switching Scheme

The control logic is used to generate internal asynchronous clocks, register the decision results of the comparators, and control the switching of the CDAC accordingly [20]. Several typical power-efficient switching sequences for CDAC, such as monotonic [22], splitting monotonic [23], and bypass switching techniques, have been proposed to improve the power efficiency. According to the reference [24], it was observed that the bypass method yields better results with less switching activity [25–27] because of the basic idea to skip the conversion steps for several significant bits when the signal is within a predefined window. Moreover, the skip operation reduces the error accumulation to improve the static performance. In this design, the CDAC is built with a segmented pre-quantization and bypass switching scheme [28], and the actual differential structure is displayed as single-ended for clarity in Figure 6.

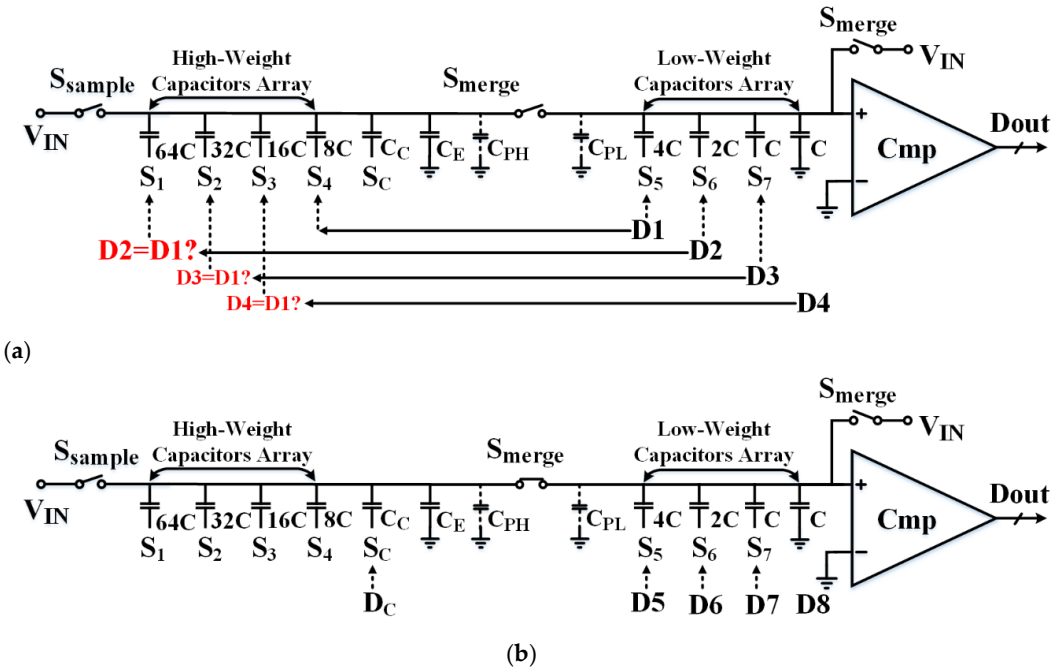

Figure 6. (**a**) Pre-quantization stage, and (**b**) global quantization stage in segmented pre-quantization and bypass switching scheme.

The capacitors array of CDAC is divided into two parts with high and low weight by the switch S_{merge}. To keep the comparator's input common-mode voltage constant, each capacitor is split into two identical small capacitors. The input signal is sampled onto the capacitors array via channel-selection-embedded bootstrap switches.

After sampling, all the switches are turned off, and only the low-weight capacitors array is connected to the comparator, equivalent to a 4-bit ADC. The comparator directly performs the first comparison without switching any capacitors to obtain the first digital code D1 [22], which is fed back to switch the minimum capacitor 8C in the high-weight capacitors array, providing an initial voltage. The subsequent digital codes D2–D4 are compared with D1, as Figure 6a shows. If one of the codes is the same as D1, that means the previous output of the CDAC is not enough, so the associated large capacitor is switched, contributing a corresponding weight output to the CDAC. In case the code is different from D1, it indicates that the last output of the CDAC is excessive, and the relevant large capacitor is bypassed, just maintaining the original state without switching. The monotonic procedure is either upward or downward to avoid unnecessary opposite direction switching of high-weight large capacitors, therefore reducing the power consumption and nonlinearity.

Once the high-weight capacitors are properly set, the switch S_{merge} is turned on, and the two arrays are merged. Meanwhile the low-weight capacitors array is reset to the initial condition. Then, the entire structure is changed back to 8-bit ADC, entering the residual quantization phase for the low 4-bit digital codes D5–D8, as shown in Figure 6b. In the whole conversion process, all quantization is done using the low-weight capacitors array, relaxing the settling constraints of the CDAC.

Ideally, the proportion of 4C in the low-weight capacitors array should be the same as that of 64C in the whole capacitors array, both being 1/2. However, the presence of parasitic capacitance changes the ratio. Since the total capacitance of high-weight capacitors array is much larger than that of low-weight capacitors array, even the same parasitic capacitance will occupy different proportions in different weight capacitor arrays, resulting in gain errors in CDAC output between high 4-bit coarse

quantization and low 4-bit global quantization stages, so it is necessary to insert equilibrium capacitor (denoted as C_E) to balance the parasitic differences between the two capacitor arrays, as shown below:

$$\frac{C_L}{C_L + C_{PL}} = \frac{C_H}{C_H + C_{PH} + C_E} \quad (1)$$

C_H and C_L represent the total capacitance of high and low weight capacitors array, respectively; that is, C_H = 64C + 32C + 16C + 8C = 120C, C_L = 4C + 2C + C + C = 8C. C_{PH} and C_{PL} represent the parasitic capacitance respectively, which can be obtained from the layout parameters extraction.

In order to further solve the potential wrong conversion caused by inaccurate parameter extraction and manufacturing process variation, a compensation capacitor (denoted as C_C) with the weight of 4 is used to provide 1-bit redundancy (corresponding to digital code D_C), whose error correction range is up to 4/128 = 3.125%.

The gain error of TI SAR ADC mainly comes from the parasitic effect and capacitance mismatch of CDAC. When selecting a capacitor size, there are two main factors to consider: thermal noise (kT/C) and matching accuracy [9]. A compact and reasonable CDAC layout is deliberately designed by using full-custom metal-oxide-metal (MOM) capacitors [29] with the unit capacitance of 1.5 fF. Benefiting from 1-bit redundancy, intrinsic capacitor matching, and careful layout routing, the gain error can be minimized to a tolerant level [30].

4. Measured Results

The ADC prototype was manufactured in a 55-nm one-poly nine-metal (1P9M) CMOS process with a core area of 400 μm × 550 μm, and a large number of decoupling capacitors were filled inside the chip to keep the power supply voltage clean and stable. The die micrograph is shown in Figure 7. The static performance of differential non-linearity (DNL) and integral non-linearity (INL) is shown in Figure 8. The measured DNL and INL were +0.93/−0.85 LSB and +0.71/−0.91 LSB, respectively.

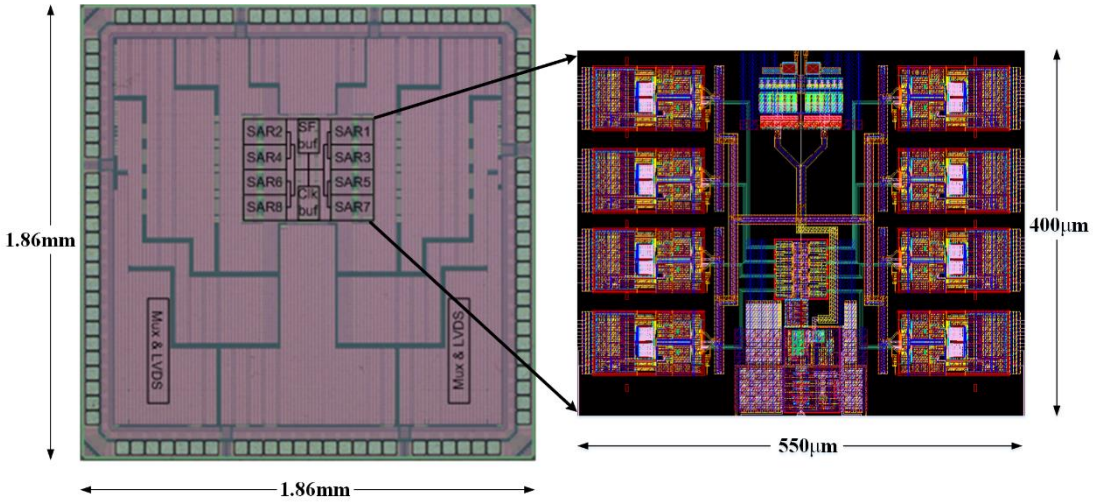

Figure 7. Die micrograph with layout view.

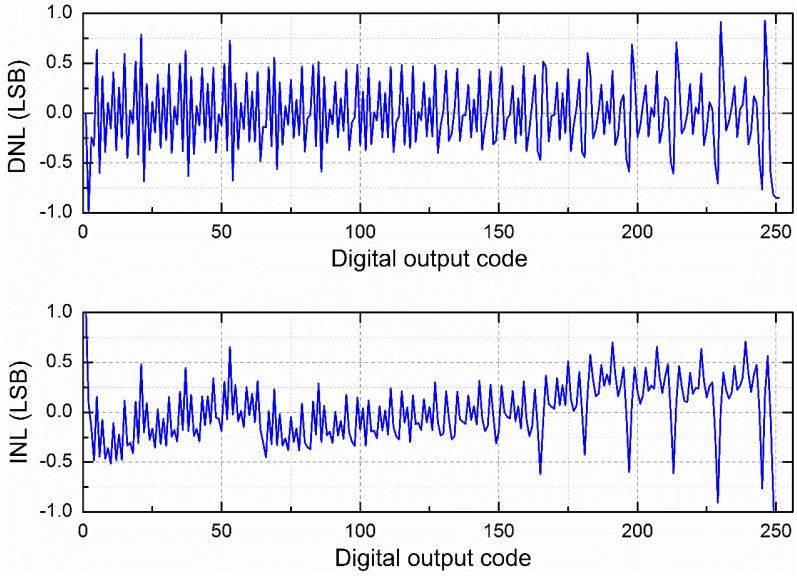

Figure 8. Measured differential non-linearity (DNL) and integral non-linearity (INL).

The output fast Fourier transform (FFT) spectrum is shown in Figure 9 at a 115 MHz input frequency and 2.6 GS/s, with an spurious-free dynamic range (SFDR) of 52.0 dB and signal-to-noise-and-distortion ratio (SNDR) of 41.52 dB. Figure 10 shows SNDR and SFDR versus input frequency at 2.6 GS/s. Within the input frequency range of 500 MHz, the SFDR was greater than 47.9 dB, the SNDR was greater than 38.2 dB, and the effective number of bits (ENOB) was greater than 6-bit. SFDR was above 40.3 dB and SNDR was above 31.8 dB in the first Nyquist zone. However, as the input frequency increased to the Nyquist frequency, the SNDR decreased by about 9 dB, which was much lower than the expected theoretical values. This result reveals that although the proposed method could suppress sample/hold circuit mismatch, the performance was not satisfactory in the high-frequency region due to other non-ideal factors, such as the master clock path mismatch, input signal path mismatch, and so on [5].

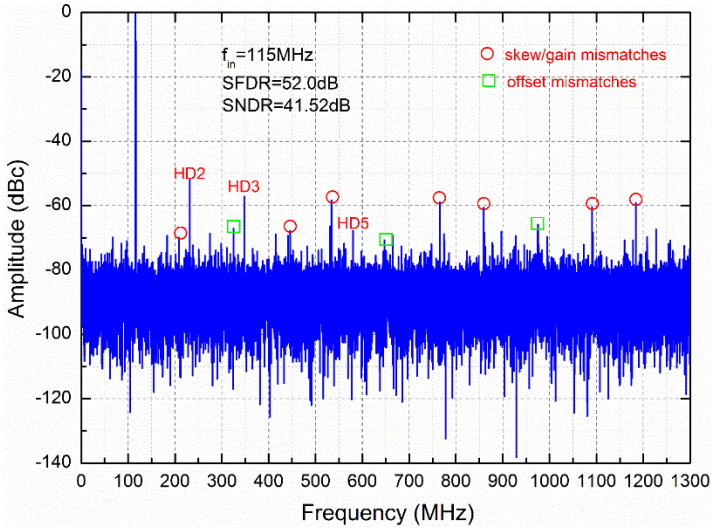

Figure 9. Output fast Fourier transform (FFT) spectrum.

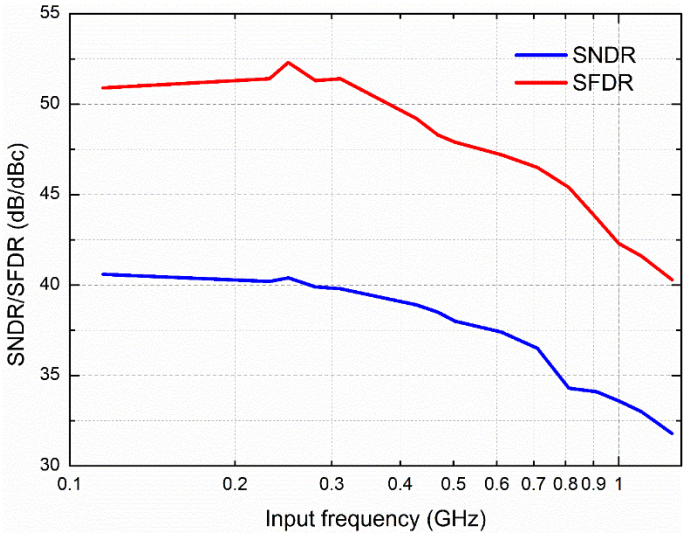

Figure 10. Signal-to-noise-and-distortion ratio (SNDR) and spurious-free dynamic range (SFDR) versus input frequency.

Based on the simulation results, the total power consumption of 60 mW at 1.2 V supply voltage was composed as follows: 12 mW for the clock generation module and 48 mW for the SAR ADCs array (that is, 6 mW/slice for every sub-ADC). The FoM calculated within the 500 MHz input frequency was 348 fJ/conversion-step. The performance summary is shown in Table 1.

Table 1. Performance summary.

Technology	**55-nm 1P9M CMOS**
Architecture	8-channel TI SAR
Sampling Rate	2.6 GS/s
Resolution	8-bit
Power	60 mW
Active Area	0.22 mm^2
DNL	+0.93/−0.85 LSB
INL	+0.71/−0.91 LSB
SFDR	≥50.94 dB (up to115 MHz) ≥47.9 dB (up to 500 MHz) ≥40.3 dB (up to Nyquist)
SNDR	≥40.54 dB (up to115 MHz) ≥38.2 dB (up to 500 MHz) ≥31.8 dB (up to Nyquist)
FoM [1]	348 fJ/conversion-step
Calibration Complexity	On-chip offset calibration only

[1] FoM = Power/(2^{ENOB} × Sampling frequency).

5. Conclusions

A 2.6 GS/s 8-bit SAR ADC prototype with eight-channel direct sampling TI architecture has been presented. The SNDR was above 38.2 dB up to 500 MHz input frequency and above 31.8 dB up to the Nyquist frequency. The DNL and INL were +0.93/−0.85 LSB and +0.71/−0.91 LSB, respectively. The ADC consumed 60 mW, occupied an area of 400 µm × 550 µm, and realized a FoM of 348 fJ/conversion-step. In general, this design is a beneficial attempt of time-skew, calibration-free

technology, which achieves acceptable results in low and medium frequency, and provides a reference for related research and design. If the calibration for time skew is used for future work, better performance can be promised.

Author Contributions: D.W. (Dong Wang) designed the circuits, analyzed the measurement data, and wrote the manuscript. X.Z., J.L., X.G. and L.Z. assisted the circuits implementation and simulation. D.W. (Danyu Wu) and H.L. performed the chip test. J.W. contributed to the technical discussions and reviewed the manuscript. X.L. gave some valuable guidance and confirmed the final version of manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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