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Transformerless Quasi-Z-Source Inverter to Reduce Leakage Current for Single-Phase Grid-Tied Applications

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Abstract: The conventional single-phase quasi-Z-source (QZS) inverter has a high leakage current as it is connected to the grid. To address this problem, this paper proposes a transformerless QZS inverter, which can reduce the leakage current for single-phase grid-tied applications. The proposed inverter effectively alleviates the leakage current problem by removing high-frequency components for the common-mode voltage. The operation principle of the proposed inverter is described together with its control strategy. A control scheme is presented for regulating the DC-link voltage and the grid current. A 1.0 kW prototype inverter was designed and tested to verify the performance of the proposed inverter. Silicon carbide (SiC) power devices were applied to the proposed inverter to increase the power efficiency. The experimental results showed that the proposed inverter achieved high performance for leakage current reduction and power efficiency improvement.

Keywords: quasi-z-source inverter; grid-tied; leakage current; power efficiency

1. Introduction

Quasi-Z-source (QZS) inverters have been widely used for grid-tied applications, due to their advantages over the traditional voltage-source inverters (VSIs) using a DC-DC converter [1–7]. Figure 1 shows the circuit diagram of the QZS inverter for single-phase grid-tied applications [2–4]. It has a QZS circuit (L_1, L_2, C_1, C_2, D_1) and a full-bridge inverter (S_1, S_2, S_3, S_4, L_3, L_4). As it is connected to the grid v_g without an isolation transformer, a leakage current i_p flows through the parasitic capacitance C_p between the inverter and the grid [5]. This leakage current originated from the common-mode voltage v_p, which changes rapidly as the inverter operates with high switching frequency [6]. Due to shoot-through states, the common-mode voltage in the QZS inverter can be higher than that in the conventional VSIs [7]. This leads to a higher leakage current, which decreases the power efficiency of the inverter.

A simple way to reduce the leakage current is to use bipolar pulse-width modulation (PWM) [8]. Power switches are diagonally operated when bipolar PWM is adopted. The common-mode voltage requires only a grid frequency component, yielding a low leakage current. However, as the voltage v_{AB} has two levels V_{PN} and $-V_{PN}$, the output filter inductors L_3 and L_4 should have high current ripples and high core losses. Despite its low leakage current characteristic, a QZS inverter with bipolar PWM is not suitable for grid-tied applications because of its reduced power efficiency.

Another method is to use a decoupling circuit to disconnect the inverter from the grid [9–15]. The decoupling circuit technique has been described for single-phase transformerless inverter applications in [9]. Many advanced transformerless inverters have been developed for voltage source inverters, such as the H5 inverter [10], the highly efficient and reliable inverter concept (HERIC) inverter [11], and the H6 inverter [12]. Many efforts have also been made to develop

transformerless inverters by applying decoupling circuits to the current source inverters [16,17]. To date, however, only a few studies [13–15] have been reported that apply decoupling circuits to ZS inverters. In [13], a symmetric ZS HERIC inverter was proposed. It uses an additional two power switches for maintaining the common-mode voltage constant. In [14,15], a QZS HERIC inverter was suggested. It uses an additional two power switches and two power diodes for clamping the common-mode voltage. The inverters in [13–15] commonly have three distinct switching states, namely powering, freewheeling, and shoot-through states. During powering states, the inverter delivers the DC power into the grid. During shoot-through states, the inverter is decoupled from the grid by turning on all power switches simultaneously in full-bridge inverter legs. After every powering state and shoot-through state, freewheeling states are necessary. During freewheeling states, the grid current circulates through extra power switches, which operate with the grid frequency. However, the previous inverters [13–15] have drawbacks such as (1) they still use the bipolar PWM for power switches in full-bridge inverter legs; and (2) they always need freewheeling states for every powering state and shoot-through state. These drawbacks increase the number of switching times for the power switches, causing high switching power losses.

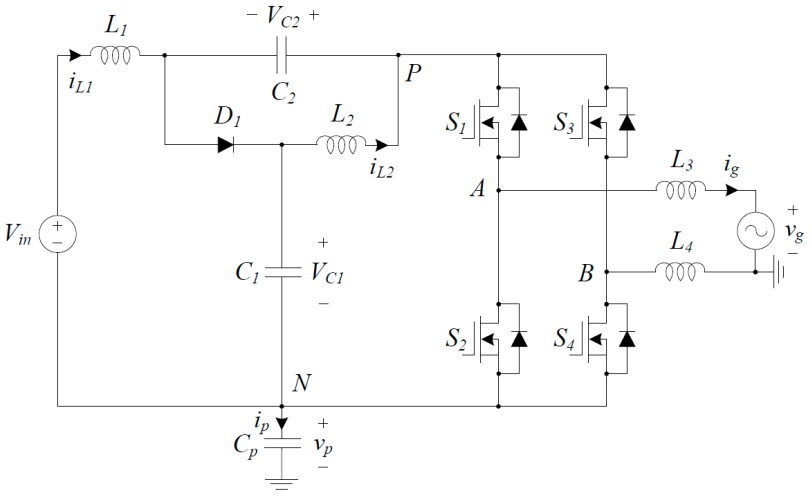


Figure 1. Circuit diagram of the QZS inverter for single-phase grid-tied applications.

To address the above-mentioned drawbacks, this paper proposes a transformerless QZS inverter, which can effectively reduce the leakage current for single-phase grid-tied applications. Figure 2 shows the circuit diagram of the proposed inverter. The idea behind the proposed inverter was to relate two high-frequency switching legs (S_1, S_2 and S_3, S_4) with the grid using a bidirectional switch (S_5, S_6) and two inductors (L_3, L_4). The bidirectional switch operates with the grid frequency, providing a current path for clamping the common-mode voltage v_p to the neutral and the grid voltage v_g, for positive and negative grid cycles, respectively. The leakage current i_p can be reduced due to the absence of high-frequency components for v_p. Shoot-through states are implemented by turning on two power switches simultaneously in only one switching leg. This leads to low switching power losses compared to the previous inverters in [13–15]. A control scheme is suggested for regulating the DC-link voltage V_{PN} and the grid current i_g. Since the peak DC-link voltage is controlled by a voltage controller, the grid current control can be directly implemented to regulate i_g. In this paper, Section 2 describes the operation principle and the control strategy of the proposed inverter. Section 3 presents the experimental results for a 1.0 kW prototype inverter. Silicon carbide (SiC) power devices were applied to the proposed inverter to increase the power efficiency. Section 4 ends the paper by presenting the conclusion.

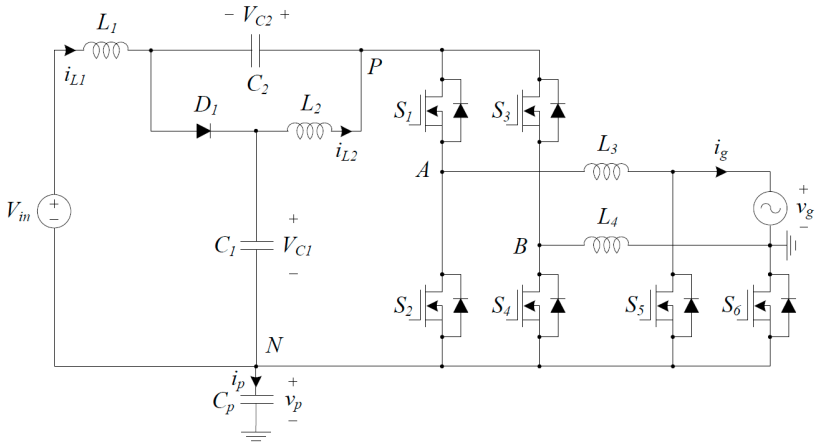


Figure 2. Circuit diagram of the proposed inverter.

2. Proposed Inverter

2.1. Operation Principle

Figure 2 shows a circuit diagram of the proposed inverter. It has a QZS circuit (L_1, L_2, C_1, C_2, D_1), a full-bridge inverter (S_1, S_2, S_3, S_4, L_3, L_4), and a bidirectional switch (S_5, S_6). C_p is modeled as the parasitic capacitance between the inverter and the grid voltage v_g. V_{in} is the DC voltage. V_{PN} is the DC-link voltage. V_{C1} and V_{C2} are the capacitor voltages for C_1 and C_2, respectively. i_{L1} and i_{L2} are the inductor currents for L_1 and L_2, respectively. i_{L3} and i_{L4} are the inductor currents for L_3 and L_4, respectively. $i_{L1} \sim i_{L4}$ are assumed to be continuous. C_1 and C_2 are assumed to have large capacitance so that their ripple components are negligible.

The proposed inverter has three switching states, namely the powering, freewheeling, and shoot-through states. For a positive grid cycle, S_6 is always turned on. S_1 and S_2 operate complementarily during the non-shoot-through states. Figure 3 shows the switching circuit diagrams of the proposed inverter for a positive grid cycle. During the powering state in Figure 3a, S_1 is turned on. The DC voltage source supplies electric power to the grid as D_1 is turned on. i_g flows through v_g, S_6, V_{PN}, S_1, and L_3. The following voltage equation is obtained as in:

$$-V_{PN} + V_{L3} + v_g = 0 \tag{1}$$

i_{L1} flows through L_1, D_{Sb}, C_1, and V_{in}. i_{L2} flows through L_2, C_2, and D_1. The following voltage equations are obtained as in:

$$V_{L1} = V_{in} - V_{C1} \tag{2}$$

$$V_{L2} = -V_{C2} \tag{3}$$

During the freewheeling state in Figure 3b, S_2 is turned on. The energy stored in L_3 is transferred to v_g. i_g freewheels through v_g, S_6, S_2, and L_3. The following voltage equation is obtained as in:

$$V_{L3} + v_g = 0 \tag{4}$$

As L_1 and L_2 are discharged, C_1 and C_2 are charged. During the shoot-through state in Figure 3c, S_1 and S_2 are turned on simultaneously. As D_1 is turned off, L_1 and L_2 are charged. The following voltage equations are obtained as in:

$$V_{L1} = V_{in} + V_{C2} \tag{5}$$

$$V_{L2} = V_{C1} \tag{6}$$

i_g flows through v_g, S_6, S_2, and L_3, as in the freewheeling state.

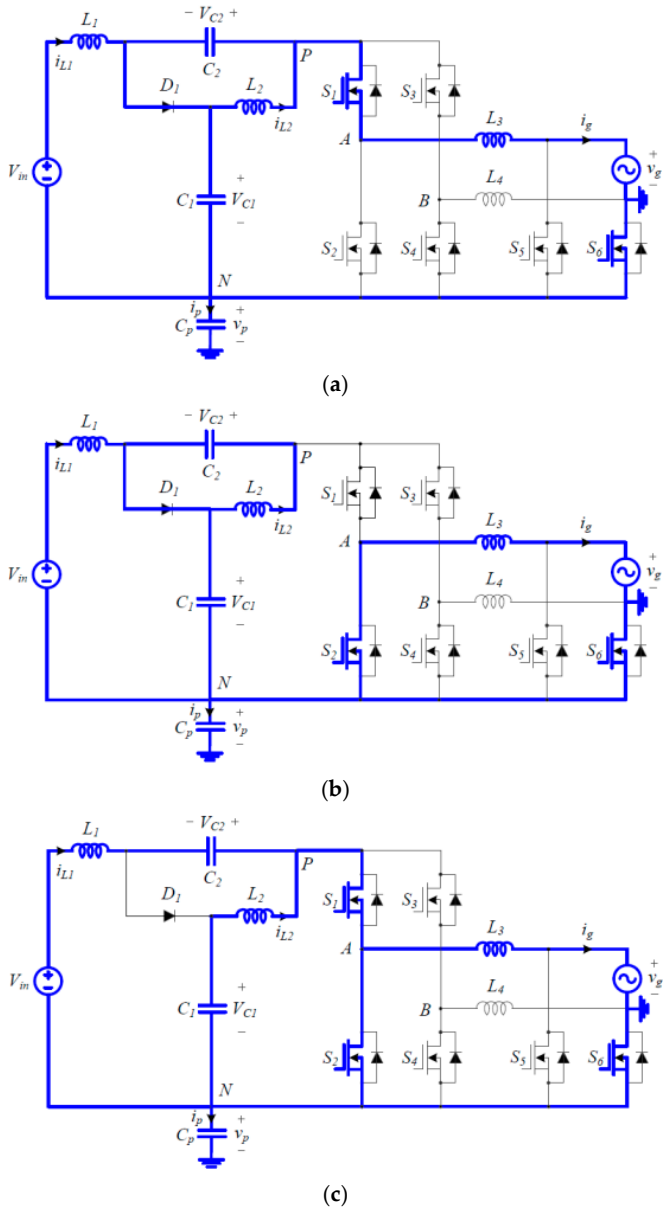


Figure 3. Switching circuit diagrams of the proposed inverter for a positive grid cycle: (**a**) powering state; (**b**) freewheeling state; (**c**) shoot-through state.

Figure 4 shows the switching circuit diagrams of the proposed inverter for a negative grid cycle. S_5 is always turned on for a negative grid cycle. S_3 and S_4 operate complementarily during the non-shoot-through states. The operation principle for a negative grid cycle is not described here because it can be analogously explained as the operation principle for a positive grid cycle.

As shown in Figure 3, S_6 provides a closed path for C_p to be clamped to the zero voltage for a positive grid cycle. On the other hand, as shown in Figure 4, S_5 provides a closed path for C_p to be clamped to the grid voltage for a negative grid cycle for a negative grid cycle. Then, the common-mode voltage v_p can be represented as in:

$$v_p = \begin{cases} 0 & when\ v_g > 0 \\ v_g & when\ v_g \leq 0. \end{cases} \quad (7)$$

The parasitic capacitance C_p can be free from the high-frequency components for both positive and negative grid cycles. This leads to the low leakage current i_p, regardless of the high-frequency switching operation of the inverter.

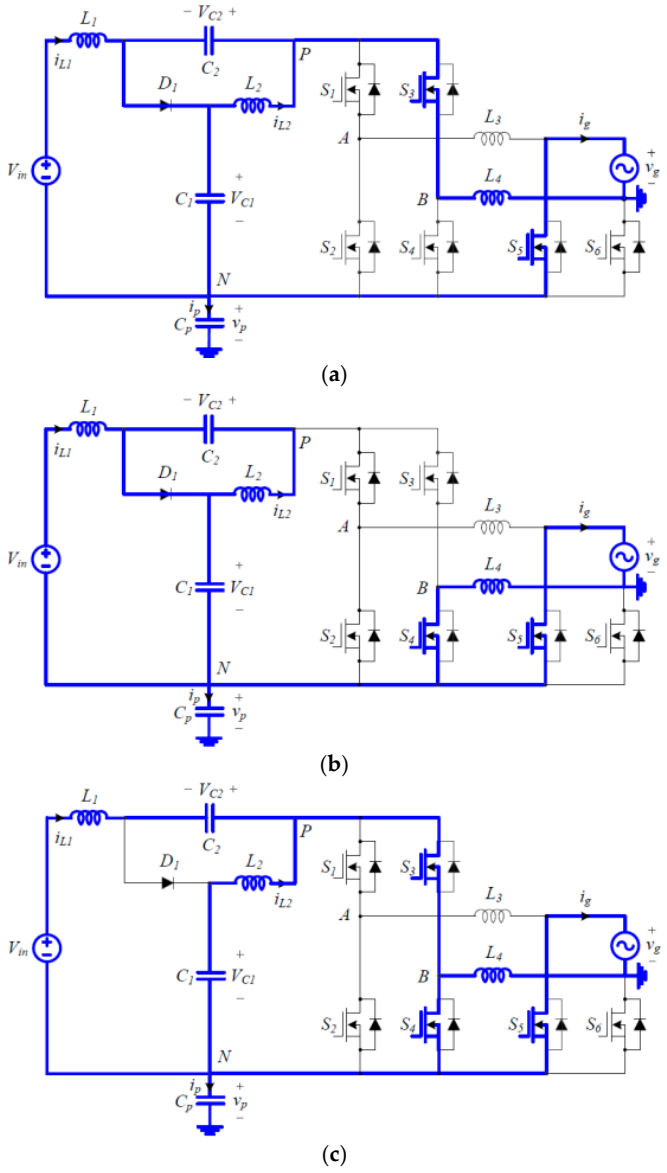


Figure 4. Switching circuit diagrams of the proposed inverter for a negative grid cycle: (**a**) powering state; (**b**) freewheeling state; (**c**) shoot-through state.

Figure 5 shows the signal diagrams for $S_1 \sim S_4$ when they operate with high switching frequency. S_1 and S_3 are the main control switches for positive and negative grid cycles, respectively. S_1 (S_3) and S_2 (S_4) operate complementarily during the non-shoot-through states, respectively. A simple boost modulation scheme is adopted for generating the shoot-through duty cycles [18]. The shoot-through state is equally distributed into two parts adjacent with the on-time of the main control switch. Shoot-through states are implemented by turning on two power switches simultaneously in only one switching leg, which leads to low switching power losses, compared to the previous inverters in [13–15]. Given that the on-time interval for the main control switch is T_{ON} for one switching period T_S, from (1) and (4), the average voltage $V_{L3,avg}$ for L_3 over T_S should be zero, respectively, as in:

$$V_{L3,avg} = \frac{(V_{PN} - v_g)\, T_{ON} - v_g(T_S - T_{ON})}{T_S} = 0. \tag{8}$$

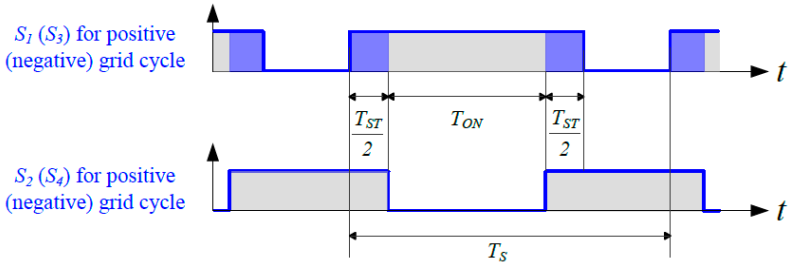


Figure 5. Signal diagrams for S_1 ~ S_4 when they operate with high switching frequency.

The ratio between T_{ON} and T_S is obtained as in:

$$\frac{T_{ON}}{T_S} = \frac{v_g}{V_{PN}} = \frac{V_g|\sin \omega t|}{V_{PN}} \tag{9}$$

where V_g is the positive peak value of v_g, and ω is the angular frequency of v_g. Given that the time interval during the shoot-through state is T_{ST} for T_S, the average voltages $V_{L1,avg}$ and $V_{L2,avg}$ for L_1 and L_2 over T_S should be zero, respectively, as in:

$$V_{L1,avg} = \frac{(V_{in} + V_{C2})\, T_{ST} + (V_{in} - V_{C1})\, (T_S - T_{ST})}{T_S} = 0, \tag{10}$$

$$V_{L2,avg} = \frac{V_{C1} T_{ST} - V_{C2}(T_S - T_{ST})}{T_S} = 0. \tag{11}$$

From Equations (10) and (11), we have:

$$V_{C1} - V_{C2} = V_{in}. \tag{12}$$

From Equation (11), the shoot-through duty cycle D_{ST} is represented as in:

$$D_{ST} = \frac{T_{ST}}{T_S} = \frac{V_{C2}}{V_{C1} + V_{C2}}. \tag{13}$$

From Equations (12) and (13), V_{C1} and V_{C2} are represented as in:

$$V_{C1} = \frac{1 - D_{ST}}{1 - 2D_{ST}} V_{in}, \tag{14}$$

$$V_{C2} = \frac{D_{ST}}{1 - 2D_{ST}} V_{in}. \tag{15}$$

Since $V_{PN} = V_{C1} + V_{C2}$, from Equations (14) and (15), we have:

$$\frac{V_{PN}}{V_{in}} = \frac{1}{1 - 2D_{ST}}. \tag{16}$$

2.2. Control Strategy

As the proposed inverter steps down the DC-link voltage V_{PN} to the level of v_g, it regulates the DC-link voltage and controls the grid current i_g. From Equations (3) and (6), the average voltage for L_2 over T_S is obtained with the inductor current deviation Δi_{L2} as in:

$$L_2 \frac{\Delta i_{L2}}{T_S} = V_{C1} D_{ST} - V_{C2}(1 - D_{ST}). \tag{17}$$

Since $V_{PN} = V_{C1} + V_{C2}$, D_{ST} is derived as in:

$$D_{ST} = \frac{V_{C2}}{V_{PN}} + L_2 \frac{\Delta i_{L2}}{V_{PN} T_S}. \tag{18}$$

Suppose that $L_1 = L_2 = L_i$ and $i_{L1} = i_{L2} = i_i$, D_{ST} can be represented as in:

$$D_{ST} = D_{ST,N} + D_{ST,C} \tag{19}$$

where $D_{ST,N}$ is the nominal shoot-through duty cycle and $D_{ST,C}$ is the controlled shoot-through duty cycle as in:

$$D_{ST,N} = \frac{V_{C2}}{V^*_{PN}}, \tag{20}$$

$$D_{ST,C} = L_i \frac{|\Delta i_i|}{V^*_{PN} T_S}. \tag{21}$$

V^*_{PN} is the reference value for the peak DC-link voltage. To make the peak DC-link voltage to track its reference V^*_{PN}, the following proportional-integral (PI) voltage control is used as in:

$$D_{ST,C} = k_p (V^*_{C2} - V_{C2}) + k_i \int (V^*_{C2} - V_{C2})\, dt \tag{22}$$

where k_p and k_i are the PI control gains, respectively. Here, V^*_{C2} is the reference value for the capacitor voltage V_{C2}, which is utilized for the DC-link voltage control as V_{PN} is a pulsating voltage [19]. V^*_{C2} is given as in:

$$V^*_{C2} = \frac{V^*_{PN} - V_{in}}{2}, \tag{23}$$

which is obtained from the following relations as $V_{PN} = V_{C1} + V_{C2}$ and $V_{in} = V_{C1} - V_{C2}$.

For the positive grid cycle, from Equations (1) and (4), the average voltage for L_3 over T_S is obtained with the grid current deviation Δi_g as in:

$$L_3 \frac{\Delta i_g}{T_S} = (V_{PN} - v_g)\, D_1 - v_g (1 - D_1) = 0 \tag{24}$$

where D_1 is the duty cycle of S_1 without considering D_{ST}. From Equation (24), D_1 is represented as in:

$$D_1 = \frac{v_g}{V_{PN}} + L_3 \frac{\Delta i_g}{V_{PN} T_S}, when\ v_g > 0. \tag{25}$$

Similarly, the duty cycle D_3 of S_3 without considering D_{ST} for a negative grid cycle can be represented as in:

$$D_3 = -\frac{v_g}{V_{PN}} - L_4 \frac{\Delta i_g}{V_{PN} T_S}, when\ v_g < 0. \tag{26}$$

Supposed that $L_3 = L_4 = L_g$, D_1 and D_3 without considering D_{ST} can be represented as the sinusoidal PWM duty cycle D_{SPWM} as in:

$$D_{SPWM} = D_{SPWM,N} + D_{SPWM,C} \tag{27}$$

where $D_{SPWM,N}$ is the nominal sinusoidal PWM duty cycle and $D_{SPWM,C}$ is the controlled sinusoidal PWM duty cycle as in:

$$D_{SPWM,N} = \frac{V_g |\sin \omega t|}{V^*_{PN}}, \tag{28}$$

$$D_{SPWM,C} = L_g \frac{|\Delta i_g|}{V^*_{PN} T_S}. \quad (29)$$

To make the grid current to track its reference i^*_g, the following proportional (P) current control is used as in:

$$D_{SPWM,C} = k_g(i^*_g - |i_g|) \quad (30)$$

where k_g is the P control gain. i^*_g is given as in:

$$i^*_g = I^*_g|\sin \omega t| \quad (31)$$

where I^*_g is the peak magnitude of the current reference. Figure 6 shows the control block diagrams of the proposed inverter. Figure 6a shows the control block diagram for the DC-link voltage control. Figure 6b shows the control block diagram for the grid current control. The phase-locked loop (PLL) control is used for the grid synchronization [20]. The duty cycle for the main control switch can be finally obtained by summing D_{SPWM} and D_{ST}.

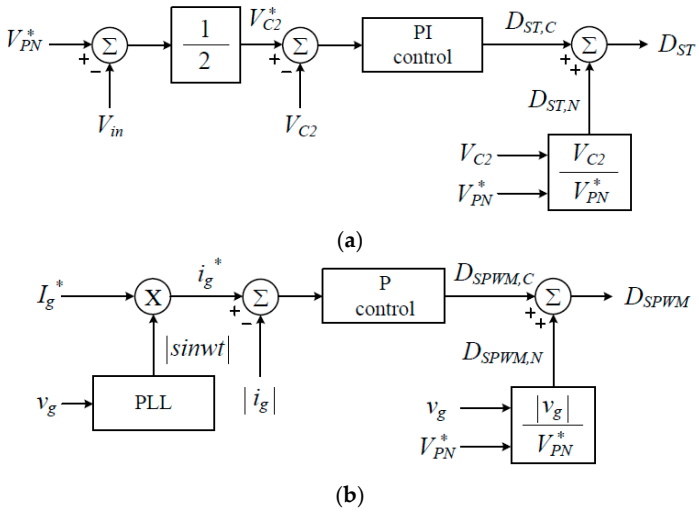


Figure 6. Control block diagrams of the proposed inverter: (**a**) DC-link voltage control; (**b**) grid current control.

3. Experimental Results

A 1.0 kW prototype inverter was designed for the proposed inverter for v_g = 60 Hz/220 V_{rms}. The valve regulated lead-acid batteries were used for the DC voltage V_{in}, the nominal voltage of which was 250 V. The V^*_{PN} was set to 500 V for D_{ST} = 0.25. SiC metal-oxide field-effect transistors (MOSFETs) (C2M0080120D, CREE) were used for S_b. A SiC Schottky diode (C4D20120D, CREE) was used for D_1. A digital signal controller (dsPIC30F6015, Microchip) was used for implementing the DC-link voltage and grid current controllers and for generating the duty cycle signals.

The inverter in Figure 1 and the inverter in [15] were designed using insulated gate bipolar transistors (IGBTs). In the conventional inverter in Figure 1, an IGBT (IKW25T120, Infineon) was used for $S_1 \sim S_4$ with a switching frequency of 10 kHz. A unipolar PWM was adopted for the conventional inverter, due to its better switching performance than a bipolar PWM. In the inverter in [15], IKW25T120 was used for $S_1 \sim S_4$ with a switching frequency of 10 kHz. IKW25T120 and C4D20120D were used for the extra power switches and extra power diodes, respectively. The proposed inverter used IKW25T120 for $S_1 \sim S_4$ with a switching frequency of 10 kHz and for S_5 and S_6 with a switching frequency of 60 Hz, respectively. Figure 7 shows a picture of the prototype inverter. The inductance for $L_1 \sim L_4$ was selected as 1.0 mH. L_3 and L_4 were implemented as a coupled inductor, which simplified the circuit layout. The capacitance for C_1 and C_2 was selected as 560 μF.

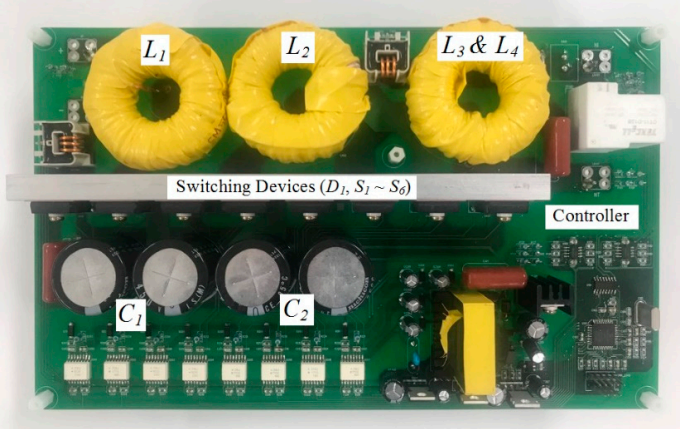


Figure 7. Picture of the prototype inverter.

Figure 8 shows the experimental waveforms of the conventional inverter in Figure 1 and the proposed inverter, respectively. Figure 8a shows v_g and v_p in the conventional inverter. Figure 8b shows v_g and i_p in the conventional inverter. Figure 8c shows v_g and v_p in the proposed inverter. Figure 8d shows v_g and i_p in the proposed inverter. The leakage current in the proposed inverter was greatly reduced compared to that in the conventional inverter.

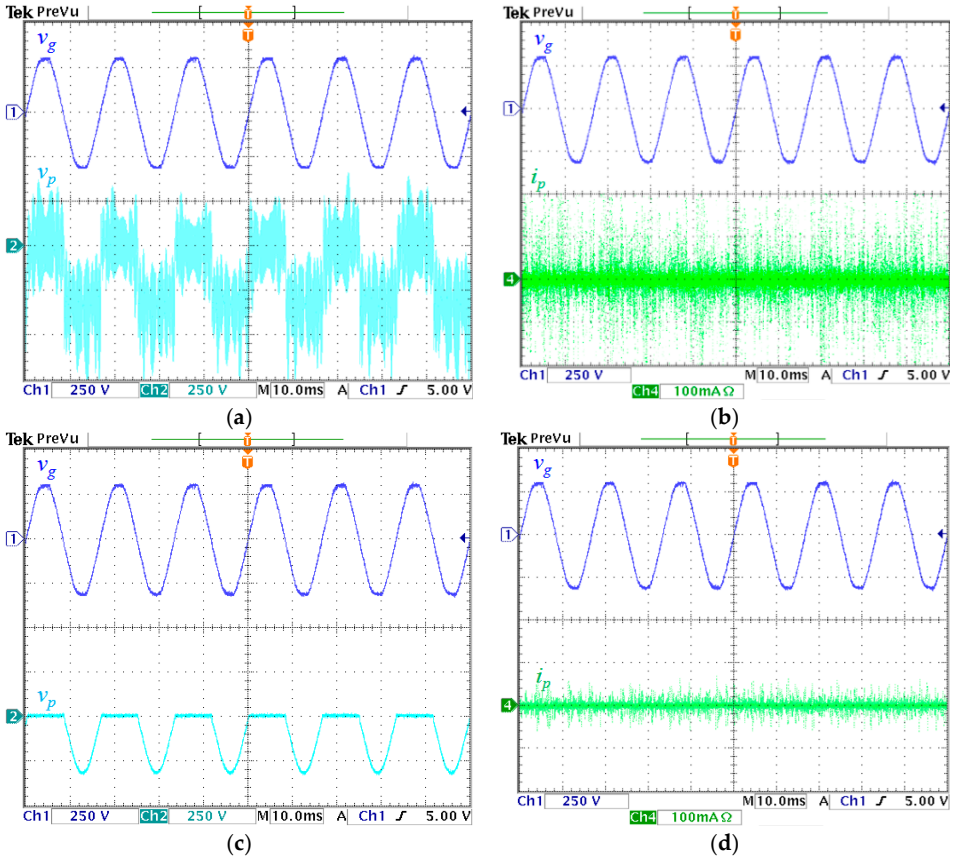


Figure 8. Experimental waveforms: (**a**) v_g and v_p in the conventional inverter; (**b**) v_g and i_p in the conventional inverter; (**c**) v_g and v_p in the proposed inverter; (**d**) v_g and i_p in the proposed inverter.

Figure 9 shows the experimental waveforms of the proposed inverter. Figure 9a shows the V_{in}, V_{PN}, v_g, and i_g. The proposed inverter steps up V_{in} to V_{PN}, and controls i_g with high power factor.

Figure 9b shows the V_{in}, V_{C2}, and V_{PN}. The peak DC-link voltage was regulated and the grid current was controlled in the proposed inverter. Figure 9c shows the V_{in}, V_{C12}, V_{C2}, and i_{L1}. Since the proposed inverter operates in the grid-tied mode, a twice grid frequency DC ripple current was observed on the DC input side. If active power decoupling schemes [17] are adopted, the ripple components as well as the reactive component sizes can be reduced.

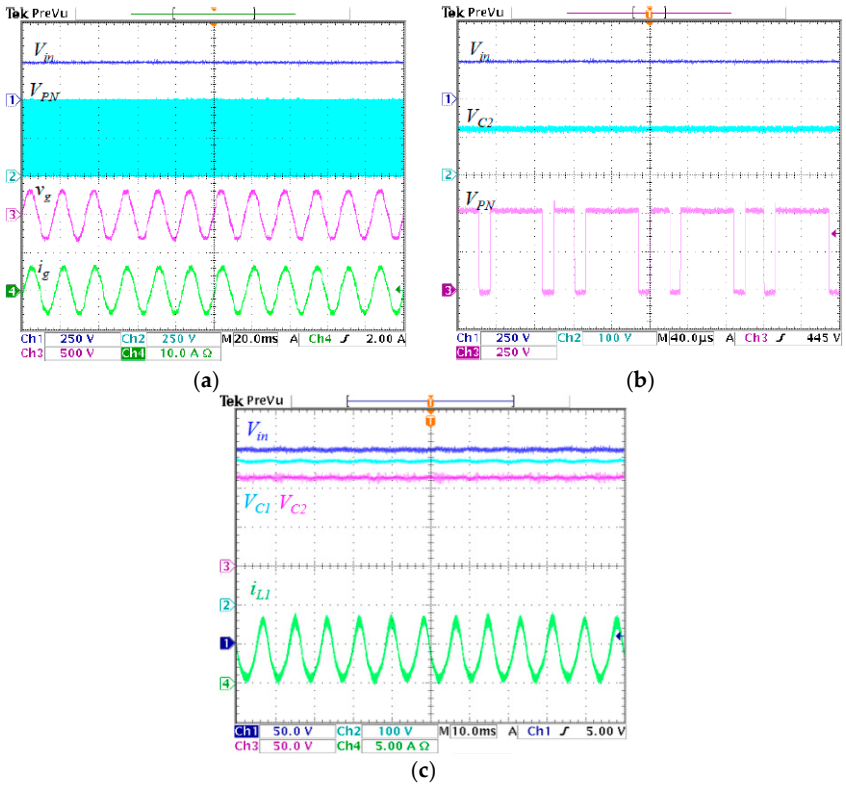


Figure 9. Experimental waveforms of the proposed inverter: (**a**) V_{in}, V_{PN}, v_g, and i_g; (**b**) V_{in}, V_{C2}, and V_{PN}; (**c**) V_{in}, V_{C1}, V_{C2}, and i_{L1}.

Figure 10 shows the power efficiency curves of the inverters. Figure 10a shows the power efficiency curves when the IGBTs have been adopted for the power switches. The inverter in Figure 1 achieved an efficiency of 91.7% at the rated power. The inverter in [15] achieved an efficiency of 92.1% at the rated power. The proposed inverter achieved an efficiency of 92.6% at the rated power, obtaining the highest efficiency of 92.9% at 0.6 kW. The proposed inverter obtained higher power efficiency than the previous inverters. The proposed inverter not only improved the power efficiency by reducing the leakage current, but also alleviated switching power losses by reducing the number of switching times for power switches. Figure 10b shows the power efficiency curves when the SiC MOSFETs were adopted for the power switches. It is observed that the power efficiency was improved when the SiC MOSFETS were used for the power switches. The inverter in Figure 1 achieved an efficiency of 93.6% at the rated power. The inverter in [15] achieved an efficiency of 94.0% at the rated power. The proposed inverter achieved an efficiency of 94.7% at the rated power, obtaining the highest efficiency of 95.1% at 0.6 kW. Regardless of the types of power switches, the proposed inverter achieved higher power efficiency than previous inverters.

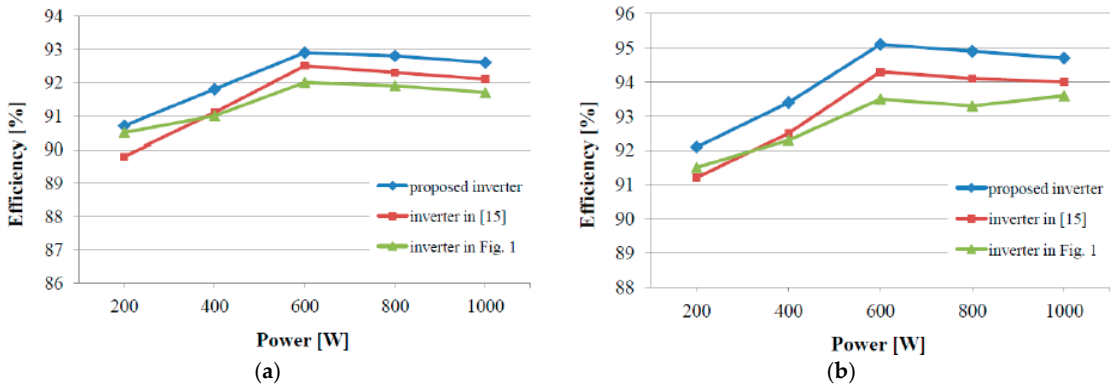


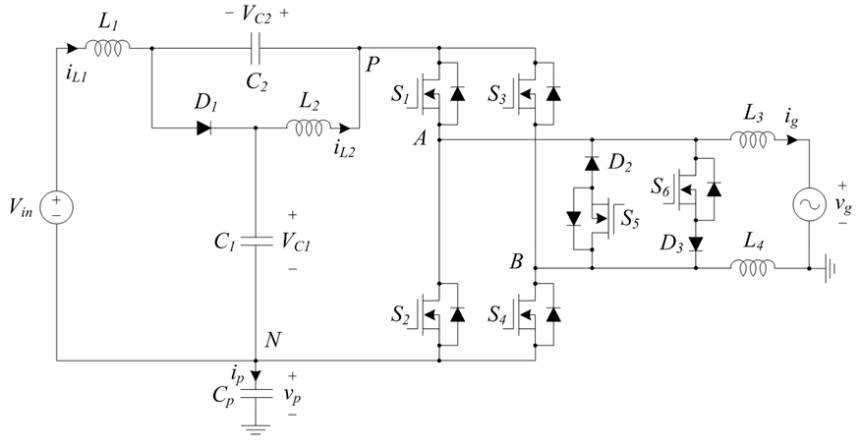
Figure 10. Power efficiency curves: (**a**) when IGBTs were adopted; (**b**) when SiC MOSFETs were adopted.

4. Discussion

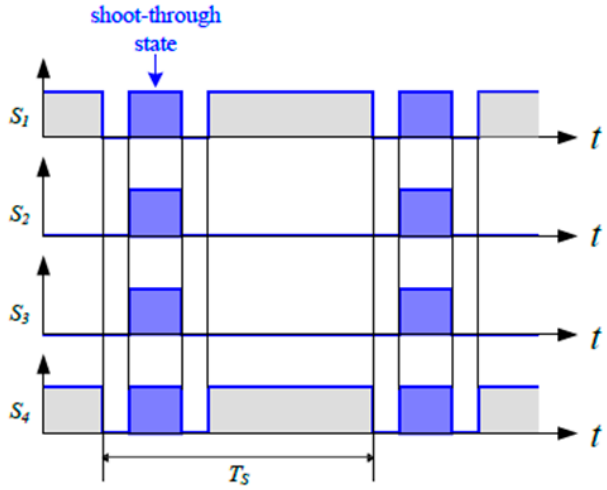
4.1. Power Loss Comparison

A unipolar PWM was used for both the conventional inverter in Figure 1 and the proposed inverter. In both inverters, S_1 and S_2 (S_3 and S_4) had one turn-on switching loss and one turn-off switching loss during one switching period, respectively, for the positive (negative) grid cycle. Both inverters had two turn-on switching losses and two turn-off switching losses during one switching period. The number of switching times was identical during one switching period, as one of the switching legs operated at grid frequency. The number of conducted switching devices was also identical during one switching period. Then, both inverters had identical switching and conduction losses. Even though they had identical power losses for the switching devices, the conventional inverter in Figure 1 had a high leakage current, while the proposed inverter had a low leakage current. This is the reason why the proposed inverter achieved higher power efficiency than the conventional inverter in Figure 1.

Figure 11a shows the circuit diagram of the previous inverter in [15]. Figure 11b shows its switching signal diagrams for $S_1 \sim S_4$ during one switching period. In the previous inverter in [15], S_5 (S_6) was always turned on for the positive (negative) grid cycle. S_1 and S_4 (S_2 and S_3) operated together during one switching period. In order to generate the shoot-through switching states, S_1, S_2, S_3, and S_4 had to be simultaneously turned on during one switching period, as shown in Figure 11b. S_1 and S_4 (S_2 and S_3) had two turn-on switching losses and two turn-off switching losses during one switching period, respectively, for the positive (negative) grid cycle. Meanwhile, S_2 and S_3 (S_1 and S_4) had one turn-on switching loss and one turn-off switching loss during one switching period, respectively, for the positive (negative) grid cycle. Then, the previous inverter in [15] had six turn-on switching losses and six turn-off switching losses during one switching period. Thus, the previous inverter in [15] had higher switching losses than the proposed inverter, even though the additional switches (S_5, S_6) in both inverters operated at the grid frequency. In addition, the conduction losses of the previous inverter in [15] were higher than the proposed inverter because of the use of two additional diodes. This is the reason why the proposed inverter achieved higher power efficiency than the previous inverter in [15]. This is also the reason why the previous inverter in [15] achieved lower power efficiency than the conventional inverter in Figure 1. As the power level decreased, the switching power losses became significant, which reduced the light load efficiency.



(**a**)



(**b**)

Figure 11. Circuit and signal diagrams of the inverter in [15]: (**a**) circuit diagram; (**b**) signal diagram for $S_1 \sim S_4$.

4.2. Topological Investigation

The decoupling circuits for reducing the leakage current can be divided into two concepts, namely AC-based and DC-based decoupling techniques [9]. The proposed inverter can be derived from the AC-based decoupling technique as the bidirectional switch (S_5, S_6) and two inductors (L_3, L_4) provide the current path for clamping the common-mode voltage to the neutral and the grid voltage for the positive and negative grid cycles, respectively. The DC-link voltage between the QZS circuit and the full-bridge inverter pulsates as the shoot-through state is generated. Thus, deriving a DC-based decoupling technique will be quite achievable for the ZS-based inverters. Along with the present state of the art and trend of decoupling circuit techniques [9], the embedded-switch inverter (ESI) [21] and zero-voltage state rectifier (ZVR) [22] concepts can be candidate solutions for extending leakage current reduction schemes to three-phase inverter applications. Furthermore, multilevel inverters using cascaded topologies [23–25] can be advanced approaches for QZS inverters to improve the output power quality.

5. Conclusions

A high-efficiency transformerless QZS inverter was proposed for single-phase grid-tied applications. The proposed inverter effectively reduced the leakage current, providing high power

efficiency. A bidirectional switch operating with the grid frequency was used, which provided a current path to remove high-frequency components for the common-mode voltage. Switching power losses were also alleviated by reducing the number of switching times for power switches. The operation principle of the proposed inverter was described. A control scheme was suggested for regulating the DC-link voltage and the grid current. A 1.0 kW prototype inverter was designed and tested to evaluate the performance of the proposed inverter. SiC MOSFETs were applied to the proposed inverter to increase the power efficiency. The experimental results showed that the proposed inverter achieved high performance in terms of leakage current reduction and power efficiency improvement.

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