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Enhancement of System Stability Based on PWFM

K. I. Hwu [1], C. W. Wang [1] and Y. T. Yau [2,*]

[1] Department of Electrical Engineering, National Taipei University of Technology, Taipei 10608, Taiwan; eaglehwu@ntut.edu.tw (K.I.H.); terrywang@gmail.com (C.W.W.)

[2] Asian Power Devices Inc., Taoyuan City, Taoyuan County 330, Taiwan

* Correspondence: tsmc35@yahoo.com.tw; Tel.: +886-3-799078

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Abstract: In this paper, a pulse width and frequency modulation (PWFM) control strategy is presented, which combines the one-comparator counter-based pulse width modulation (PWM) control with pulse frequency modulation (PFM) control to increase pseudo-1-bit resolution under constant-frequency operation. Accordingly, system stability will be enhanced significantly. As compared with the traditional counter-based PWM control, there is no difference in off-chip circuit complexity except a slight change in on-chip hardware. Finally, a prototype circuit is used to verify the proposed control concept by some experimental results with no limit cycle oscillation.

Keywords: counter-based; one-comparator; PWFM; PWM; PFM

1. Introduction

Up to now, much research on the accuracy of the pulse width modulation (PWM) has been conducted. The reason why the development of the high-resolution PWM is needed is described below. One reason is that the PWM resolution should be higher than the analog-to-digital converter (ADC) resolution to avoid limit cycle oscillation [1–3]. The other reason is that under the fixed system clock, the PWM accuracy is inversely proportional to the switching frequency. However, PWM accuracy should be not too low. Consequently, under this constraint, the more the switching frequency is, the more the system clock, which is proportional to the switching frequency. Accordingly, due to limitations on the integrated circuit (IC) process, the dissipation power will be increased abruptly, including the charging/discharging of the complementary metal-oxide-semiconductor (CMOS) gate and the leakage current due to the miniature process. Based on the above two reasons, the PWM accuracy and the switching frequency are limited to some extent. It is possible that a special process, such as silicon-on-isolator (SOI) [4,5], may reduce the leakage current, and may keep low power dissipation and low temperature under the high-speed system clock of the miniature process. However, the corresponding cost is high, and this special process is usually used in the manufacture of the central processing unit (CPU) or the graphic processing unit (GPU). There is a lot of research on high-accuracy PWM. For example, the literature [6–21] focus on how to reduce the number of digital pulse width modulation (DPWM) steps, where the high-switching clock, e.g., counter-based DPWM, is achieved based on special structures [7,19–21]. Most of these structures are multiple interleaved to achieve high-switching clock or use very short delay elements, e.g., hybrid DPWM [1,22]. Although the delay line based DPWM can achieve high accuracy, the corresponding silicon area is relatively large compared with the traditional counter-based DPWM. In addition, the delay line based DPWM is sensitive to the operating temperature, process, and power interference [12].

On the other hand, some researches increase the effective duty cycle to achieve high-accuracy resolution, for example, digital dither [23], sigma-data [8,10,18], special modulation [24], and PFM [25]. The method taken by the literature [23] may cause the output voltage ripple to be small or large, thereby

influencing the controller performance. The method followed in [24] tends to vary the turn-on and turn-off periods of the switch so the ADC sampling is difficult. As for the method shown in [25], it is restricted to PFM operation.

Based on aforementioned, this paper is an extension of the paper [26]. The latter takes the one-comparator counter-based PWM control, whereas the former takes the one-comparator counter-based PWM control with PFM control. By doing so, the former can increase pseudo-1-bit resolution under constant-frequency operation, so that system stability will be improved greatly. In addition, the difference in on-chip hardware between the two control strategies is slightly small, whereas there is no difference in off-chip circuit complexity between the two control strategies.

2. Problem Description

In many papers, the problem of limit cycle oscillation has been discussed as shown in Figure 1a. Most people say that this is because the resolution of PWM is larger than that of ADC. In fact, the answer to this problem is too brief. This is because the gain of the control loop should be taken into account. The solution of the limit cycle oscillation that is only based on high-resolution DPWM is not enough. Therefore, the detailed overall calculations and the corresponding program flow are discussed. From Figure 1b, it can be seen that although the output voltage V_O keeps up with the voltage reference V_{ref}, V_O swings up and down around V_{ref} due to the DPWM resolution being lower than ADC resolution. From the point of view of control, the difference in oscillation between V_O and V_{ref} is quite small, but V_O cannot keep up with V_{ref}. As the DPWM resolution is higher than the ADC resolution, the feedback error can be kept as small as possible, and hence no limit cycle oscillation occurs. From Figure 1, it gives us a hint that the traditional controller needs an integral gain so as to make V_O approach to V_{ref} as near as possible.

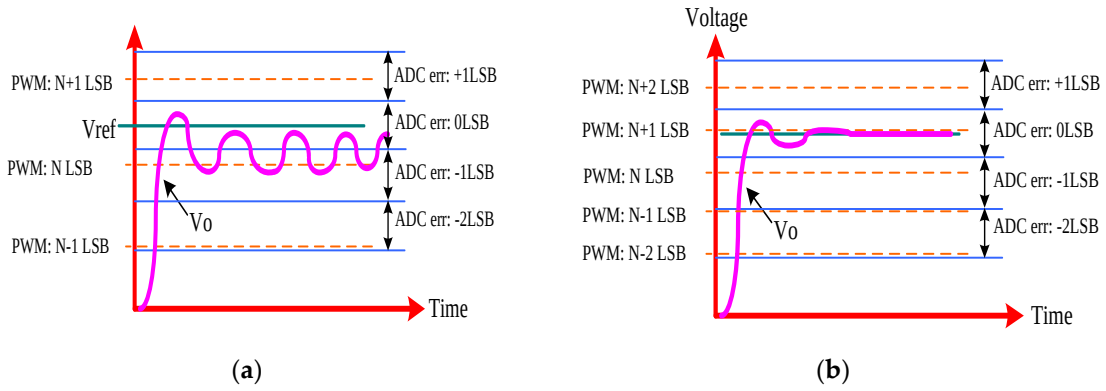


Figure 1. Quantization resolution in a digitally controlled pulse width modulation (PWM): (**a**) with limit cycle oscillation; (**b**) without limit cycle oscillation.

3. Discussion of Compensator Gain

Figure 2 shows the digital closed-loop system block diagram. There are three block diagrams. One is an analog-to-digital converter (ADC) block, another is a compensator block, and the other is a digital-to-analog converter (DAC) block. The last block includes the controlled plant. The gains for the ADC, compensator, and DAC blocks are described as (1), (2) and (3), respectively. In order to avoid limit cycle oscillation, Equation (4) must hold:

$$ADC_{Gain} = \frac{LSB_{ADC}}{Vo} \tag{1}$$

$$DAC_{Gain} = \frac{Vo}{LSB_{DAC}} \tag{2}$$

$$Comp_{Gain} = \frac{LSB_{DAC}}{LSB_{ADC}} \tag{3}$$

$$ADC_{Gain} \times Comp_{Gain} \cdot DAC_{Gain} \leq 1 \tag{4}$$

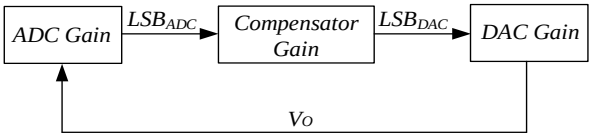


Figure 2. Digital closed-loop system block diagram.

4. ADC Strategy

Figure 3 shows the proposed system configuration, constructed by one synchronously-rectified (SR) buck converter and one feedback control circuit. The latter is built up by the field-programmable gate array (FPGA). Inside the FPGA, there are one proportional-integral-derivative (PID) control block, one DPWM controller, and one feedback control block. Outside the FPGA, there is one voltage divider, one saw-tooth generator, one analog circuit, and one comparator. The saw-tooth generator is constructed by one charging switch Q_3, one constant current source, one capacitor C_{ramp}, one DC-blocking capacitor C_b and one operational amplifier (OPA) with a voltage gain of −1. Furthermore, the feedback counter is a digital counter, which is inside the FPGA. As the output signal from the comparator, named *VFB*, is "1", the counter counts one, whereas the *VFB* signal is reset to zero as synchronized with the *PWM* signal. In addition, the sensed output signal v'_O is obtained by one feedback voltage divider built up by two resistors.

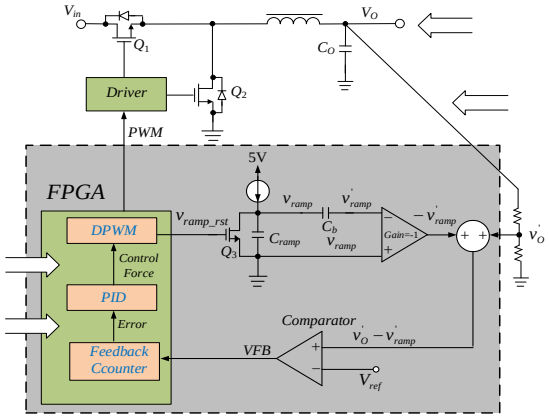


Figure 3. System configuration.

5. Basic Operating Principles

Prior to this section, there are some assumptions and symbol definitions described. It is assumed that the voltage ripple of the output voltage is quite small so the output voltage v_O can be regarded as an average value V_O. The triggering signal for Q_3 is signified by v_{ramp_rst}. The sawtooth waveform is represented by v_{ramp} which has a minimum value of zero and a peak value of V_{ramp_pp}. The signal v_{ramp} after the AC coupling capacitor C_b is signified by v'_{ramp}. Therefore, the signal $-\frac{1}{2}V_{ramp\_pp}$ is the minimum value of v'_{ramp} whereas the signal $\frac{1}{2}V_{ramp\_pp}$ is the maximum value of v'_{ramp}. The signal v'_{ramp} is changed to $-v'_{ramp}$ after the OPA with gain= −1. Afterwards, the sum of $-v'_{ramp}$ and v'_O has a minimum value of $\left(v'_O - \frac{1}{2}V_{ramp\_pp}\right)$ and a maximum value of $\left(v'_O + \frac{1}{2}V_{ramp\_pp}\right)$. Finally, the output of the comparator is a digital signal, determined by $\left(v'_O - v'_{ramp}\right)$ and V_{ref}. If the $\frac{v'_O}{v_O} = G_{fb}$, then the voltage range of V_O can locate between $\left(V_{ref} - \frac{1}{2}V_{ramp\_pp}\right)/G_{fb}$ and $\left(V_{ref} + \frac{1}{2}V_{ramp\_pp}\right)/G_{fb}$. Figure 4

shows the associated circuit waveforms, which are described based on the time sequence, that is, the operating states. There are four operating states in this circuit, to be shown below:

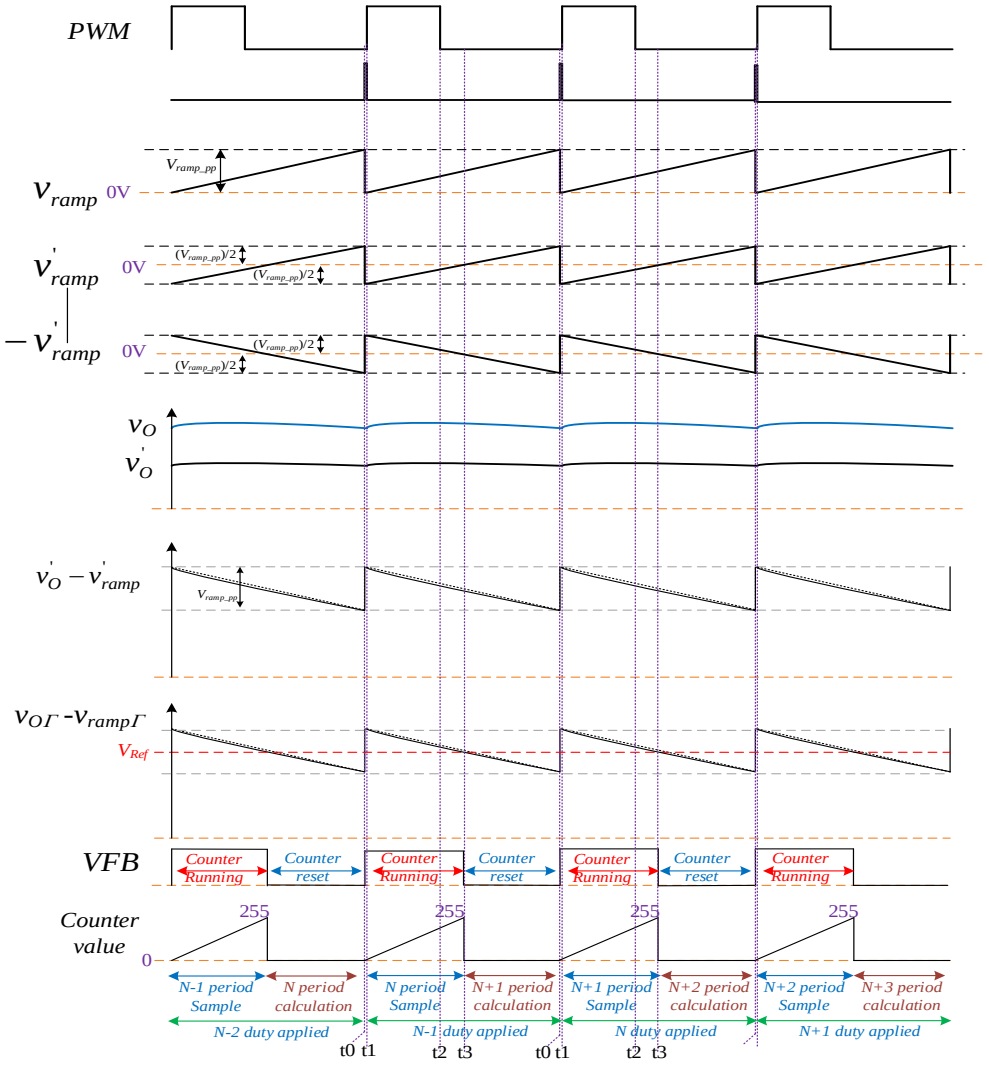


Figure 4. Waveforms relevant to sampling sequence.

(1) State 1 [t0~t1]: Let the voltage V_{ramp_rst} be high, thereby making the switch Q_3 turned on and the voltage across C_{ramp} zero. At the same time, the PWM is high, causing Q_1 to be turned on and Q_2 to be turned off. This time interval is short, smaller than 1% of the PWM switching period. The signal v_{ramp} is blocked by the DC-blocking capacitor C_b, and after the OPA with a gain of −1, the resulting signal $-v'_{ramp}$, which is added to v'_O so as to obtain $\left(v'_O - v'_{ramp}\right)$, which is subtracted from V_{ref} to obtain the signal VFB.

(2) State 2 [t1~t2]: The signal PWM keeps high. Let V_{ramp_rst} be low, thereby making Q_3 turned off and C_{ramp} is linearly charged. If $\left(v'_O - v'_{ramp}\right) > V_{ref}$, then VFB = "high", thereby making the counter value increased by one. As the preset turn-on time in the N period is reached, the operating state proceeds to state 3.

(3) State 3 [t2~t3]: At the time instant of t2, let the signal PWM be "low." If $(v'_O - v'_{ramp}) > V_{ref}$, then VFB = "high", thus rendering the counter value keeping increased by one. If $v'_O - v'_{ramp} < V_{ref}$, then the operating state goes to state 4.

(4) State 4 [t3~t0]: At the time instant of t3, VFB = "low," the corresponding counter value will be saved in the feedback register, and then the counter value is set to zero. During this state, the PID

calculates the control force for the next period, according to the information in the feedback register. At the same time, the duty cycle information is downloaded to the DPWM. At the time of t0, the next cycle begins. In addition, from Figure 4, it can be seen that as $v'_O = V_{ref}$, the counter value is 50%, which is a full scale.

Under the ideal condition, if the counter value locates within the sampling range of the comparator, *VFB* is linearly proportional to v'_O. For example, in Figure 4, if the range of the counter value is *n*-bit, the sampling resolution can be represented by $\frac{V_{ramp\_pp}}{counter\ value}$, that is, $\frac{V_{ramp\_pp}}{n\ bits}$ is the sampling resolution of the least significant bit (LSB). The smaller the V_{ramp_pp} is or the larger the bit number of the counter value is, the more the resolution. It is suggested that in order to enhance the linearity, $V_{ramp_{pp}} > 10 \times v_{O\_ripple}$ should hold in design.

If the sensed output voltage v'_O is out of the sampling range of the comparator, the sampled data will be saturated. For example, as $v'_O \geq V_{ref} + \frac{1}{2}V_{ramp\_pp}$, the comparator keeps *VFB* = "high", and hence the counter value keeps the maximum error. By the same way, as $v'_O \leq V_{ref} - \frac{1}{2}V_{ramp\_pp}$, the comparator keeps *VFB* = "low", and hence the counter value keeps the minimum error.

6. Resolution Design

6.1. Requirements of Resolution of DPWM and ADC

In the traditional buck converter with digital control, if the DPWM has N_{DPWM} bits, then the resolution of DPWM can be expressed by

$$Resolution_{DPWM} = \frac{V_{in}}{2^{N_{DPWM}}} \tag{5}$$

Each bit in DPWM causes a voltage variation to be $\Delta V_{DPWM} = \frac{V_{in}}{2^{N_{DPWM}}}$.. By the same way, if ADC has N_{ADC} bits, then ADC resolution can be represented by

$$Resolution_{ADC} = \frac{V_{ramp\_pp}}{2^{N_{ADC}}} \tag{6}$$

Each LSB in ADC causes a voltage variation to be $\Delta V_{ADC} = \frac{V_{ramp\_pp}}{2^{N_{ADC}}}$.

According to the literature [20], the resolution of DPWM and ADC is mainly influenced by the limit cycle oscillation. This is because when the DPWM resolution is lower than the ADC resolution, the DPWM cannot satisfy the sampled value of the ADC for any operating point such that the feedback error is not zero. Therefore, the controller outputs a keeping-jumping control force to the DPWM, to force the average output voltage to satisfy the voltage reference. However, such a keeping-jumping PWM control force will cause the output voltage to oscillate. When the DPWM resolution is higher than the ADC resolution, the DPWM can find some operating point to satisfy the sampled value of the ADC and to make the feedback error zero. By doing so, the limit cycle oscillation phenomenon can be avoided.

Therefore, the minimum requirement for the limit cycle oscillation is shown in (7):

$$Resolution_{DPWM} = \frac{V_{in}}{2^{N_{DPWM}}} = \frac{V_{ramp_{pp}}}{2^{N_{ADC}}} \tag{7}$$

Accordingly, the minimum value of V_{ramp_pp} is $V_{ramp\_pp\_min} = V_{in} \times \frac{2^{N_{ADC}}}{2^{N_{DPWM}}}$.
Based on $I_{ramp} \times T_s = C_{ramp} \times v_{ramp}$, $V_{ramp\_pp\_min}$ can be signified by

$$V_{ramp\_pp\_min} = V_{in} \times \frac{2^{N_{ADC}}}{2^{N_{DPWM}}} = \frac{I_{ramp} \times T_s}{C_{ramp}} \tag{8}$$

6.2. Calculation of VFB Duty

From Figure 5, it can be seen that the relationship between the comparator output signal and the feedback counter value are as shown in (9):

$$Duty_{(VFB)} = \frac{T_{VFB\_Hi}}{T_S} = \frac{ADC_{VFB}}{ADC_{fullscale}} \tag{9}$$

where

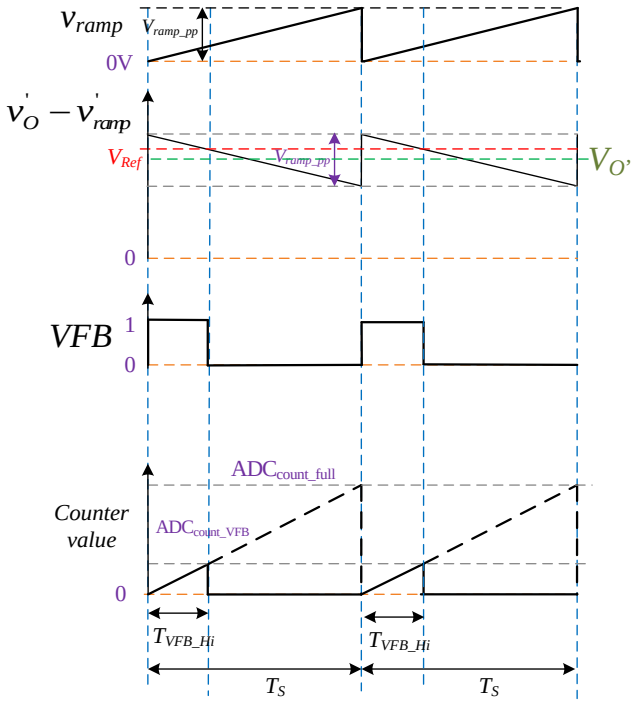
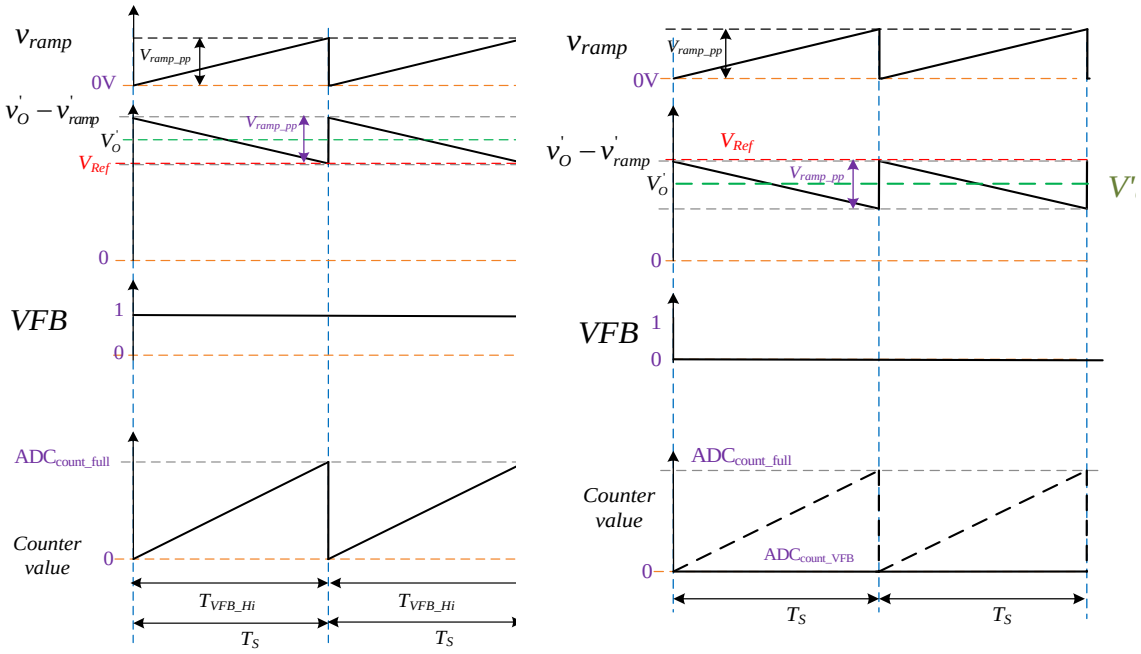


Figure 5. $\left(V_{ref} - \frac{V_{ramppp}}{2}\right) < v_O' < \left(V_{ref} + \frac{V_{ramp\_pp}}{2}\right)$.

$ADC_{fullscale}$: Full-scale value of feedback counter.
ADC_{VFB}: Feedback value of N period
T_{VFB_Hi}: High level of the VFB signal
$Duty_{(VFB)}$: Duty cycle of the VFB signal

On the other hand, Figure 6a is under the condition that $Duty_{(VFB)}$ is 100%. In this case, $V_{O'_{max}} = V_{ref} + \frac{V_{ramp\_pp}}{2}$. Figure 6b is under the condition that $Duty_{(VFB)}$ is 0%. In this case, $v'_{Omin} = V_{ref} - \frac{V_{ramppp}}{2}$. Thus, based on the geometry theory, it can be found that any value of $Duty_{(VFB)}$ within the interval of $\left(V_{ref} - \frac{V_{ramp\_pp}}{2}\right) < v'_O < \left(V_{ref} + \frac{V_{ramp\_pp}}{2}\right)$ can be expressed as

$$Duty_{(VFB)} = \frac{v'_O - V_{ref} + \frac{V_{ramppp}}{2}}{v'_{Omax} - v'_{Omin}} = \frac{\left(v'_O - V_{ref} + \frac{V_{ramp\_pp}}{2}\right)}{V_{ramp\_pp}} = \frac{\left(v'_O - V_{ref}\right)}{V_{ramp\_pp}} + \frac{1}{2} \tag{10}$$



(**a**) (**b**)

Figure 6. (**a**) $v'_O = \left(V_{ref} + \frac{V_{ramp\_pp}}{2}\right)$; (**b**) $v'_O = \left(V_{ref} - \frac{V_{ramp\_pp}}{2}\right)$.

Combining (9) and (10) yields

$$Duty_{(VFB)} = \frac{ADC_{VFB}}{ADC_{fullscale}} = \frac{\left(v'_O - V_{ref}\right)}{V_{ramp\_pp}} + \frac{1}{2} \tag{11}$$

Taking the output voltage divider transfer function into account, (11) can be rewritten to be

$$Duty_{(VFB)} = \frac{ADC_{VFB}}{ADC_{fullscale}} = \frac{\left(V_O \times G_{fb} - V_{ref}\right)}{V_{ramp\_pp}} + \frac{1}{2} \tag{12}$$

Substituting $V_{ramp\_pp\_min}$ shown in (8) into (12) yields

$$Duty_{(VFB)} = \frac{ADC_{VFB}}{ADC_{fullscale}} = \frac{\left(V_O \times G_{fb} - V_{ref}\right)}{V_{ramp\_pp\_min}} + \frac{1}{2} = \frac{\left(V_O \times G_{fb} - V_{ref}\right)}{\left(\frac{I_{ramp} \times T_s}{C_{ramp}}\right)} + \frac{1}{2} \tag{13}$$

7. Gain Analysis of Digital Compensator

Figure 7 shows the block diagram of the PID compensator. Inside this compensator, there is one rounded number block, one anti-saturation block, and one right z shift block beside the PID calculation.

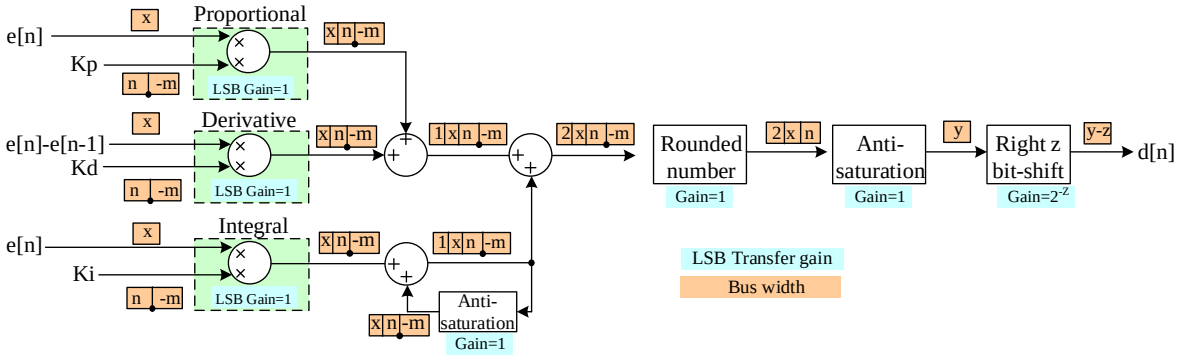


Figure 7. Proportional–integral–derivative (PID) compensator block diagram.

7.1. PID Calculation

The proportional gain *Kp*, the integral gain *Ki*, and the derivative gain *Kd* all have the data register form. This form implies an n-bit integer and an m-bit decimal fraction. For example, if $n = 5$, $m = 3$ and $Kp = 1$, then the corresponding digital value is "00001.000". If the bus width of e[*n*] is (*x*) and the bus widths of *Kp*, *Ki*, and *Kd* are all the same (*n.m*), then after PID calculation, the corresponding bus width is ($x + n.m$).

7.2. Rounded Number Block

The decimal bits are removed without any conditions, but there is no change of LSB gain, implying that the corresponding output bus width is still ($x + n.m$).

7.3. Anti-Saturation Block

This block is used as a protection of the arithmetic overflow of the register. There is no change of LSB gain and the corresponding output bus width is ($2 + x + n$).

7.4. Right z-Bit Shift Block

As the division is operated, redundant bits are removed. This is because the DPWM does not need so many bits. The right shift number is expressed by the symbol z. For each shift, the corresponding LSB gain is divided by two. The output bus width of this block is (y-z) and the corresponding LSB gain is 2^{-z}.

Accordingly, if $Kp = 2$ and $z = 1$, then the total LSB gain is one. If $Kp = 4$ and $z = 0$, then the total LSB gain is four. The LSB gain of the PID calculation is determined by the minimum value of {*Kp*, *Ki*, *Kd*}. For example, if $Kp = 2$, $Ki = 0.01$ and $Kd = 3$, then the LSB gain of the PID block is two. This is because the decimal fraction, created from the integrator, will be removed directly.

8. PWFM Control Concept

The PWFM strategy, combining the pulse width modulation (PWM) and the pulse frequency modulation (PFM), can improve 1-bit resolution. This strategy does not need to change the original control structure and circuit. In the following, one example, together with Table 1, is given. The first two columns are associated with traditional duty cycles and periods, respectively. There are three cases with duty cycles of 30%, 50%, and 80%. According to the traditional PWM, the jumping interval is about 0.195%. The last two columns are associated with the proposed duty cycles and periods, respectively. Under the condition of the period of 512 clocks (CLK), both the corresponding duty cycle for the PWM and PFWM are the same, whereas, under the condition of the period of 511 CLK, the corresponding duty cycle for the PFWM is larger than that for the previous PWM but smaller than that for the next PWM. By doing so, the resolution of the DPWM strategy is larger than that of the PWM strategy. In other words, a higher resolution can be achieved and expressed by ($n + 0.5$) CLK,

which is different from the PWM strategy with a resolution expressed by n CLK. From Table 1, it can be seen that there are no errors in the duty cycle of around 50%, but there are some errors in the duty cycle of 30% and 80%. Whether these errors are useful or not depends on actual applications. For an example of a buck converter, it normally works with the duty cycle locating between 15% and 85%, so a little large error in duty cycle calculation is OK. Furthermore, the extreme duty cycle is used in a large transient response so the duty cycle linearity is not so important. From Figure 8, both the curves of duty cycle versus control force for the PWFM and PWM are almost the same. In Figure 9, it shows that the errors in the duty cycle locating between zero and 100%, where not all points have errors. For n CLK, there are no errors in duty cycle calculation if n CLK is activated, whereas, for (n + 0.5) CLK, there are some errors in duty cycle calculation if (n + 0.5) CLK is activated. From Figure 9, it can be seen that the maximum error is within 0.1%, showing that the proposed strategy possesses industrial applications to some extent.

Table 1. Duty cycle comparison between (PWM) and pulse width and frequency modulation (PWFM).

Traditional PWM	PWM Period	Duty (%)	Proposed PWFM	PWFM Period	Duty (%)
154	512	30.08	154	512	30.08
			154	511	30.14
155	512	30.27	155	512	30.27
			155	511	30.33
156	512	30.47	156	512	30.47
			156	511	30.53
157	512	30.66	157	512	30.66
			157	511	30.72
158	512	30.86	158	512	30.86
			158	511	30.92
159	512	31.05	159	512	31.05
			159	511	31.12
160	512	31.25	160	512	31.25
256	512	50.00	256	512	50.00
			256	511	50.10
257	512	50.20	257	512	50.20
			257	511	50.29
258	512	50.39	258	512	50.39
			258	511	50.49
259	512	50.59	259	512	50.59
			259	511	50.68
260	512	50.78	260	512	50.78
410	512	80.08	410	512	80.08
			410	511	80.23
411	512	80.27	411	512	80.27
			411	511	80.43
412	512	80.47	412	512	80.47
			412	511	80.63
413	512	80.66	413	512	80.66
			413	511	80.82
414	512	80.86	414	512	80.86
			414	511	81.02
415	512	81.05	415	512	81.05
			415	511	81.21
416	512	81.25	416	512	81.25

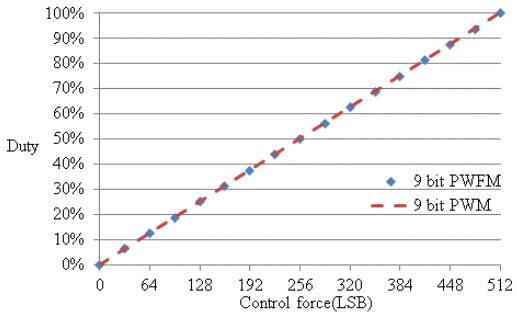


Figure 8. Curves of duty cycle versus control force for the PWFM and PWM strategies.

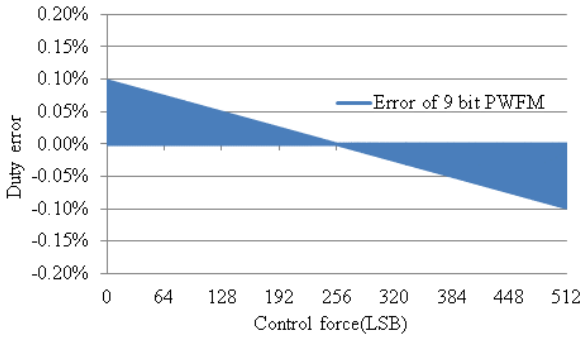


Figure 9. Curves of duty cycle error versus control force for the PWFM strategy.

9. PWFM Procedure

Figures 10 and 11 show the program flow charts for the traditional PWM strategy and the proposed PWFM strategy, respectively. From Figure 10, since the traditional 9-bit PWM has a period of 512 CLK, the 11-bit control force will be saved in a register with the last two bits cut off. At the same time, there is an up counter to be activated as PWM is equal to one, counting from zero. As soon as the counter value is equal to the duty cycle value, this counter will be set to zero. As for the PWFM shown in Figure 11, the 11-bit control force will be saved in a register with the last bit cut off. The first nine bits are integral values, similar to 9-bit PWM but the last bit is not an integral value, called 0.1bit, which will be finely modulated according to the PFM. The first nine bits will be put into a register and compared with the value of the up counter, and at the same time, the last bit will be checked. If the 0.1bit is equal to one, the accompanying period is 511 CLK, leading to the resolution of $(n + 0.5)$; otherwise, the integral bit information is obtained and the duty cycle is 512 CLK.

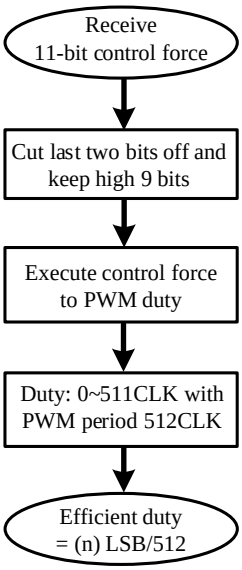


Figure 10. Program flow chart for the traditional PWM strategy.

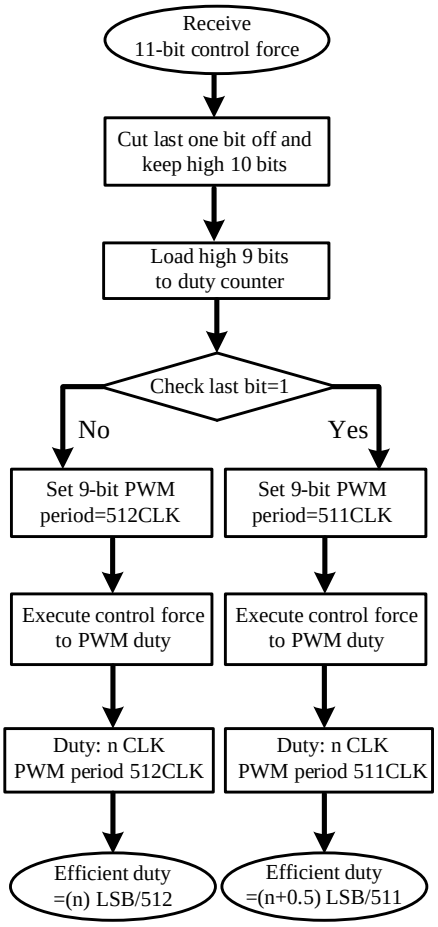


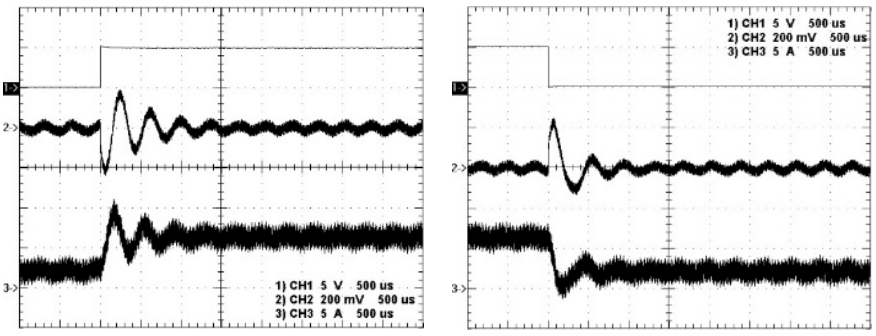
Figure 11. Program flow chart for the proposed PWFM strategy.

10. Experimental Results

Prior to this section, some specifications for a buck converter are given as follows: (i) The input voltage is 12 V; (ii) The output voltage is 5 V; (iii) The rated output current is 8 A; (iv) The switching frequency is 195 kHz; (v) The ADC is 9-bit with a peak-to-peak voltage of 1.7 V; (vi) The PWM is 9-bit

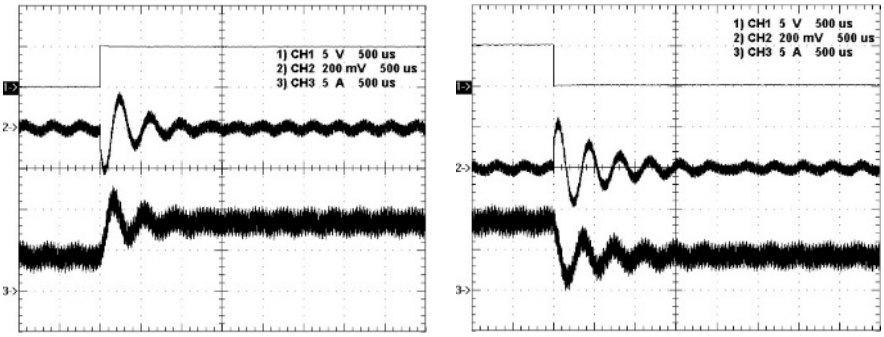
and PWFM is 9-bit plus 1-bit; (vii) The value of the output inductor is 5 μH; (viii) The output capacitor is constructed by two 470 μF electrolytic capacitors and two 10 μF multilayer ceramic capacitors (MLCC), with all capacitors paralleled together; (x) The part names of the main switch Q_1 and synchronous rectifier Q_2 are the same, called IRL8113; (xi) The FPGA, belonging to Altera Cyclone 3 with operating clock of 100 MHz, has the part name of EP34C5T44.

Figures 12 and 13 show the waveforms relevant to the traditional PWM control strategy and the proposed PWFM control strategy under different loads, respectively. The controller is not well designed herein. The purpose of the controller is to show the limit cycle oscillation under the traditional PWM control strategy. Therefore, the transient part is not so important. As for the proportional gain k_p, it may affect the experimental results but may not be needed. As for the integral gain k_i, it must be needed to make the DC output voltage stable at a given value. In the following experiments, the value of k_i is 0.0625. From Figures 14 and 15, the limit cycle oscillation is removed, and the transient parts are almost the same as those shown in Figures 12 and 13. The features of the proposed PWFM control strategy are the same as those of the traditional PWM control strategy except that both the resolutions are different. Figures 16–19 show the zoom-in waveforms for Figures 12–15, respectively. From these figures, it can be seen that due to the switching frequency, the output voltages have high-frequency ripples, and the inductor currents also have high-frequency ripples.



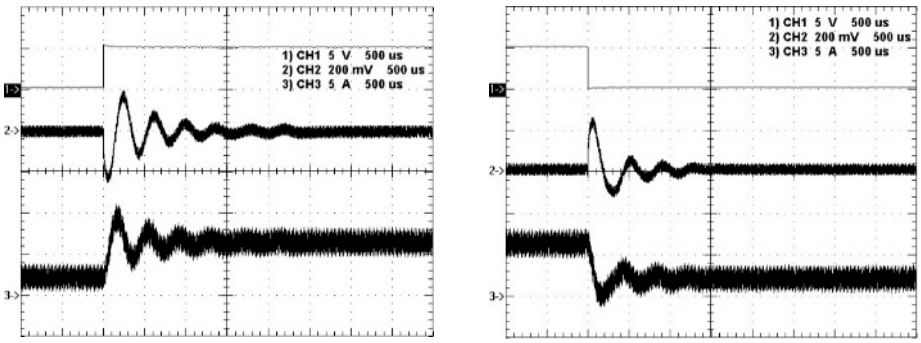
(**a**) (**b**)

Figure 12. Waveforms based on the traditional PWM control strategy: (1) load enable; (2) AC output voltage; (3) inductor current, due to (**a**) from 25% to 75%; (**b**) from 75% to 25%.



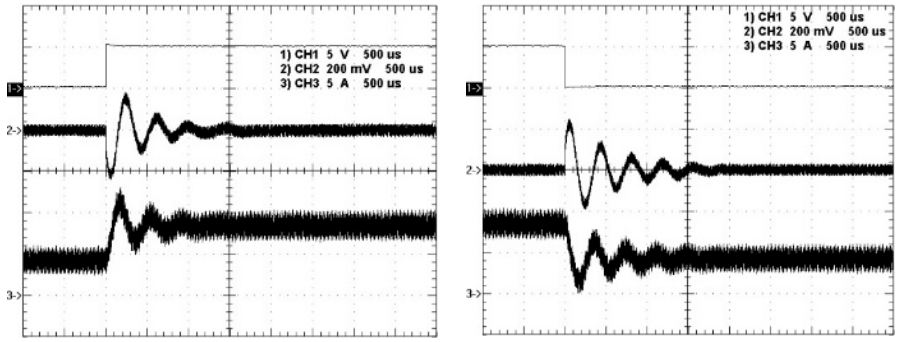
(**a**) (**b**)

Figure 13. Waveforms based on the traditional PWM control strategy: (1) load enable; (2) AC output voltage; (3) inductor current, due to (**a**) from 50% to 100%; (**b**) from 100% to 50%.



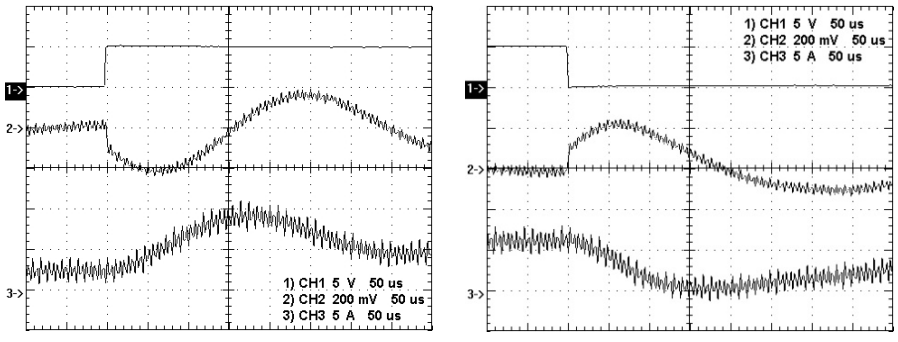
(**a**) (**b**)

Figure 14. Waveforms based on the proposed PWFM control strategy: (1) load enable; (2) AC output voltage; (3) inductor current, due to (**a**) from 25% to 75%; (**b**) from 75% to 25%.



(**a**) (**b**)

Figure 15. Waveforms based on the proposed PWFM control strategy: (1) load enable; (2) AC output voltage; (3) inductor current, due to (**a**) from 50% to 100%; (**b**) from 100% to 50%.



(**a**) (**b**)

Figure 16. Zoom-in waveforms based on the traditional PWM control strategy: (1) load enable; (2) AC output voltage; (3) inductor current, due to (**a**) from 25% to 75%; (**b**) from 75% to 25%.

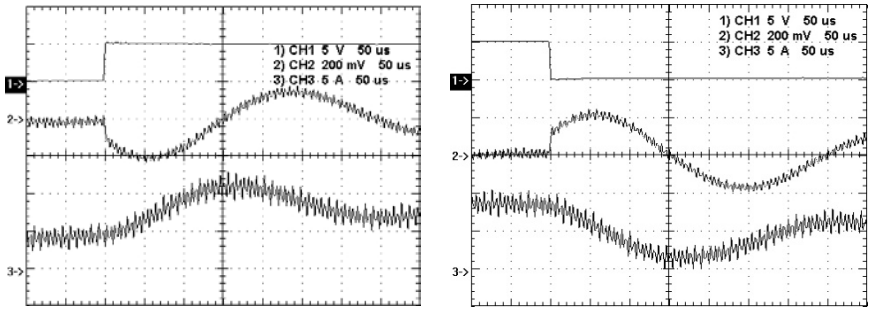


Figure 17. Zoom-in waveforms based on the traditional PWM control strategy: (1) load enable; (2) AC output voltage; (3) inductor current, due to (**a**) from 50% to 100%; (**b**) from 100% to 50%.

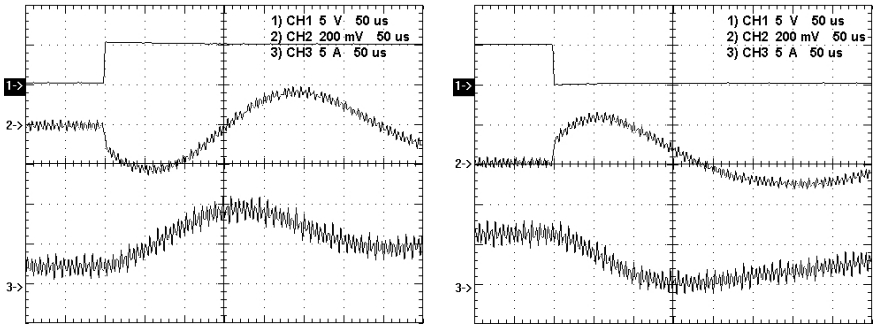


Figure 18. Zoom-in waveforms based on the proposed PWFM control strategy: (1) load enable; (2) AC output voltage; (3) inductor current, due to (**a**) from 25% to 75%; (**b**) from 75% to 25%.

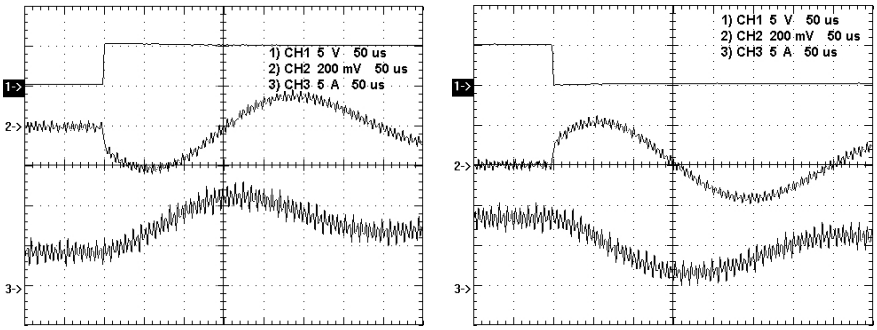


Figure 19. Zoom-in waveforms based on the proposed PWFM control strategy: (1) load enable; (2) AC output voltage; (3) inductor current, due to (**a**) from 50% to 100%; (**b**) from 100% to 50%.

11. Conclusions

A PWFM control strategy is presented herein by combining the one-comparator counter-based DPWM control with PFM control to increase pseudo-1-bit resolution under constant-frequency operation. By doing so, as compared with the traditional PWM control strategy, system stability will be enhanced, including no limit cycle oscillation although both have almost the same transient responses. Above all, the difference in internal structure between the two is quite small, and the circuit complexity and chip area are not altered. In the future, the number of bits for DPWM and PFM will be investigated to shorten the transient time.

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Conflicts of Interest: The authors declare no conflict of interest with commerce.

References

1. Peterchev, A.V.; Sanders, S.R. Quantization resolution and limit cycling in digitally controlled PWM converters. *IEEE Trans. Power Electron.* **2003**, *18*, 301–308. [CrossRef]
2. Peng, H.; Prodic, A.; Alarcon, E.; Maksimovic, D. Modeling of quantization effects in digitally controlled DC-DC converters. *IEEE Trans. Power Electron.* **2007**, *22*, 208–215. [CrossRef]
3. Prodic, A.; Maksimovic, D.; Erickson, R.W. Design and Implementation of a digital PWM controller for a high-frequency switching DC-DC power converter. In Proceedings of the 27th Annual Conference of the IEEE Industrial Electronics Society, Denver, CO, USA, 29 November–2 December 2001.
4. Bernstein, K.; Rohrer, N.J. *SOI circuit design concepts*; Springer: New York, NY, USA, 2007; pp. 6–9.
5. Curran, B.; Fluhr, E.; Paredes, J.; Sigal, L.; Friedrich, J.; Chan, Y.H.; Hwang, C. Power-constrained high-frequency circuits for the IBM POWER6 microprocessor. *IBM J. Res. Dev.* **2007**, *51*, 715–731. [CrossRef]
6. Dancy, A.P.; Chandrakasan, A.P. Ultra low power control circuits for PWM converters. In Proceedings of the 28th Annual IEEE Power Electronics Specialists Conference, Saint Louis, MO, USA, 27 June 1997.
7. Foley, R.; Kavanagh, R.; Marnane, W.; Egan, M. Multiphase digital pulsewidth modulator. *IEEE Trans. Power Electron.* **2006**, *21*, 842–846. [CrossRef]
8. Lukic, Z.; Wang, K.; Prodic, A. High-frequency digital controller for DC-DC converters based on multi-bit sigma-delta pulse-width modulation. In Proceedings of the Twentieth Annual IEEE Applied Power Electronics Conference and Exposition, Austin, TX, USA, 6–10 March 2005.
9. Foley, R.F.; Kavanagh, R.C.; Marnane, W.P.; Egan, M.G. An area efficient digital pulsewidth modulation architecture suitable for FPGA implementation. In Proceedings of the Twentieth Annual IEEE Applied Power Electronics Conference and Exposition, Austin, TX, USA, 6–10 March 2005.
10. Malley, E.O.; Rinne, K. A programmable digital pulse width modulator providing versatile pulse patterns and supporting switching frequencies beyond 15 MHz. In Proceedings of the Nineteenth Annual IEEE Applied Power Electronics Conference and Exposition, Anaheim, CA, USA, 22–26 February 2004.
11. Wang, K.; Rahman, N.; Lukic, Z.; Prodic, A. All-digital DPWM/DPFM controller for low-power DC-DC converters. In Proceedings of the Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition, Dallas, TX, USA, 19–23 March 2006.
12. Yousefzadeh, V.; Takayama, T.; Maksimovic, D. Hybrid DPWM with digital delay-locked loop. In Proceedings of the 2006 IEEE Workshops on Computers in Power Electronics, Troy, NY, USA, 16–19 July 2006.
13. Peterchev, A.V.; Xiao, J.; Sanders, S.R. Architecture and IC implementation of a digital VRM controller. In Proceedings of the 2001 IEEE 32nd Annual Power Electronics Specialists Conference, Vancouver, BC, Canada, 17–21 June 2001.
14. Lukic, Z.; Blake, C.; Huerta, S.C.; Prodic, A. Universal and fault tolerant multiphase digital PWM controller IC for high-frequency DC-DC converters. In Proceedings of the Twenty-Second Annual IEEE Applied Power Electronics Conference and Exposition, Anaheim, CA, USA, 25 February–1 March 2007.
15. Zhang, J.; Sanders, S.R. A digital multi-mode multi-phase IC controller for voltage regulator application. In Proceedings of the Twenty-Second Annual IEEE Applied Power Electronics Conference and Exposition, Anaheim, CA, USA, 25 February–1 March 2007.
16. Huerta, S.C.; de Castro, A.; Garcia, O.; Cobos, J.A. FPGA based digital pulse width modulator with time resolution under 2 ns. *IEEE Trans. Power Electron.* **2008**, *23*, 3135–3141. [CrossRef]
17. Syed, A.; Ahmed, E.; Maksimovic, D.; Alarcon, E. Digital pulse width modulator architectures. In Proceedings of the 2004 IEEE 35th Annual Power Electronics Specialists Conference, Aachen, Germany, 20–25 June 2004.

18. Kelly, A.; Rinne, K. High resolution DPWM in a DC-DC converter application using digital sigma-delta techniques. In Proceedings of the 2005 IEEE 36th Power Electronics Specialists Conference, Recife, Brazil, 16 June 2005.
19. de Castro, A.; Todorovich, E. DPWM based on FPGA clock phase shifting with time resolution under 100 ps. In Proceedings of the 2008 IEEE Power Electronics Specialists Conference, Rhodes, Greece, 15–19 June 2008.
20. Carosa, T.; Zane, R.; Maksimovic, D. Scalable digital multiphase modulator. *IEEE Trans. Power Electron.* **2008**, *23*, 2201–2205. [CrossRef]
21. Batarseh, M.G.; Al-Hoor, W.; Huang, L.; Iannello, C.; Batarseh, I. Segmented digital clock manager-FPGA based digital pulse width modulator technique. In Proceedings of the 2008 IEEE Power Electronics Specialists Conference, Rhodes, Greece, 15–19 June 2008.
22. Foley, R.F.; Kavanagh, R.C.; Marnane, W.P.; Egan, M.G. A versatile digital pulsewidth modulation architecture with area-efficient FPGA implementation. In Proceedings of the 2005 IEEE 36th Power Electronics Specialists Conference, Recife, Brazil, 16 June 2005.
23. Li, P.; Kang, Y.; Pei, X.; Chen, J. A novel PWM technique in digital control. *IEEE Ind. Electron.* **2007**, *54*, 338–346. [CrossRef]
24. Qiu, Y.; Li, J.; Xu, M.; Ha, D.S.; Lee, F.C. Proposed DPWM scheme with improved resolution for switching power converters. In Proceedings of the Twenty-Second Annual IEEE Applied Power Electronics Conference and Exposition, Anaheim, CA, USA, 25 February–1 March 2007.
25. Li, J.; Qiu, Y.; Sun, Y.; Huang, B.; Xu, M.; Ha, D.S.; Lee, F.C. High resolution digital duty cycle modulation schemes for voltage regulators. In Proceedings of the Twenty-Second Annual IEEE Applied Power Electronics Conference and Exposition, Anaheim, CA, USA, 25 February–1 March 2007.
26. Yau, Y.T.; Hwu, K.I. One-comparator sampling design for digital power converters. In Proceedings of the 2018 7th International Symposium on Next Generation Electronics, Taipei, Taiwan, 7–9 May 2018.