electronics

MDPI

Design Architectures of the CMOS Power Amplifier for 2.4 GHz ISM Band Applications: An Overview

Mohammad Arif Sobhan Bhuiyan [1],* , **Md Torikul Islam Badal [2,3], Mamun Bin Ibne Reaz [3], Maria Liz Crespo [4] and Andres Cicuttin [4]**

[1] Electrical and Electronics Engineering, Xiamen University Malaysia, Bandar Sunsuria, Sepang 43900, Selangor, Malaysia

[2] Electronic and Telecommunication Engineering, RMIT University, Melbourne, VIC 3000, Australia; torikul.uniten@gmail.com

[3] Electrical, Electronic and Systems Engineering, Universiti Kebangsaan Malaysia, Bangi 43600, Selangor, Malaysia; mamun.reaz@gmail.com

[4] International center for Theoretical Physics (ICTP), Via Beirut 31, 34100 Trieste, Italy; mcrespo@ictp.it (M.L.C.); cicuttin@ictp.it (A.C.)

* Correspondence: arifsobhan.bhuiyan@xmu.edu.my; Tel.: +60-182851-271

check for updates

Abstract: Power amplifiers (PAs) are among the most crucial functional blocks in the radio frequency (RF) frontend for reliable wireless communication. PAs amplify and boost the input signal to the required output power. The signal is amplified to make it sufficiently high for the transmitter to propagate the required distance to the receiver. Attempted advancements of PA have focused on attaining high-performance RF signals for transmitters. Such PAs are expected to require low power consumption while producing a relatively high output power with a high efficiency. However, current PA designs in nanometer and micrometer complementary metal–oxide semiconductor (CMOS) technology present inevitable drawbacks, such as oxide breakdown and hot electron effect. A well-defined architecture, including a linear and simple functional block synthesis, is critical in designing CMOS PA for various applications. This article describes the different state-of-the art design architectures of CMOS PA, including their circuit operations, and analyzes the performance of PAs for 2.4 GHz ISM (industrial, scientific, and medical) band applications.

Keywords: CMOS; ISM band; PA; transmitter; WSN

1. Introduction

At present, wireless communication systems are experiencing a rapid growth because of the advancement of complementary metal–oxide semiconductor (CMOS) technology [1,2] which provides more advantages over Gallium Arsenide (GaAs) and Gallium Nitride (GaN) technologies. CMOS technology enables operation at a lower power supply, resulting in a reduced power dissipation in the circuit [3,4] and a minimized fabrication cost because of the compact chip size. CMOS offers the prospect of integrating radiofrequency (RF)/digital/analog functions on a single chip in a low-cost manner [5–7]. The CMOS power amplifier (PA) is a promising solution for modern wireless devices to satisfy the demand of a low-power and low-cost design. Over the years, CMOS PA has been widely used in various wireless communication applications, including home automation, Radio Frequency Identification (RFID), industrial consumer electronics, TV transmissions, phones, and medical instruments [8–10]. It has been integrated in high-frequency medical ultrasonic applications to amplify high-voltage excitation signals to activate ultrasonic transducers, because ultrasonic imaging requires a higher contrast resolution, which can be produced by a highly linear PA [4].

The PA is the key component of RF transmitters. An RF transmitter is composed of functional blocks, such as a digital-to-analog converter (DAC), an up-conversion mixer, an oscillator, a PA, and a band pass filter (BPF), [11–13], as shown in Figure 1. Among all of these modules, the PA is the most vital block because its performance significantly affects the overall performance of the transmitter [14–16]. The PA can be defined as an electronic amplifier that converts a low-power RF signal into a high-power RF signal [1]. The PA receives the RF signal from the mixer and then sends it to the antenna after amplifying and passing it through the band pass filter [17–19]. In addition, the PA reduces the voltage swing to obtain a higher output power according to the system's requirement.
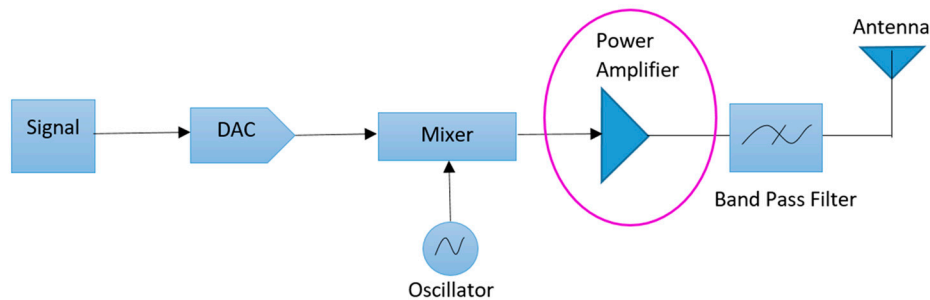
Figure 1. Basic block diagram of radio frequency (RF) transmitter.

Figure 2 describes the basic block diagram of the CMOS PA. The block diagram consists of two main stages, namely, the driver and power stages. Both stages are biased with individual bias voltages. Different configurations are applied to the driver and power stages to operate the PA properly [20–23]. Input and output matching networks are used to minimize the return losses to obtain a high gain and output power. However, inter-stage matching is also required between the driver and power stages.
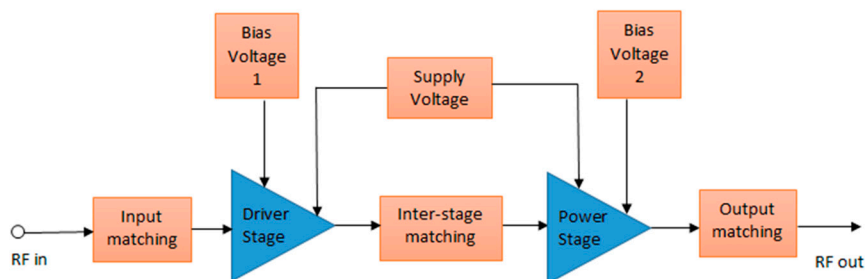
Figure 2. Block diagram of complementary metal–oxide semiconductor (CMOS) power amplifier (PA) [20].

In the past decade, different PA design architectures have been proposed to achieve the desired performances. These architectures suffer from high power consumption, nonlinearity, circuit complexity, low output power, low gain, and low efficiency. Thus, a high-performance PA must urgently be designed to satisfy the rising demands for ISM band applications. This article is aimed to evaluate the various aspects of the designs and performances of PA for 2.4 GHz ISM band applications and review their recent advances in terms of key performance parameters. This comparative study is expected to guide future works on 2.4 GHz RF devices.

2. Performance Parameters

The performance of CMOS PA was evaluated in terms of several parameters. The most important aspects of a PA design are output power, power consumption, power gain, linearity, and power added efficiency (PAE). Inevitable trade-offs exist among these factors, and these trade-offs make PA design challenging at CMOS downscaling. The key factors for assessing transmitter performance were determined as follows:

2.1. Output Power

Output power (P_{out}) refers to the amount of power that must be delivered to the load (antenna) [24] and is considered the most important aspect of a PA design [25]. Power gain and efficiency have a trade-off with output power. To generate output power, the energy supply in the device should exceed the required output power because some power dissipates as heat [25]. When the supply voltage has a constant value, the amount of current is critical in obtaining the output power. The output power is proportional to the efficiency of the PA and therefore, determines the performance of the PA. It is expressed in dB$_m$ by Equation (1) as follows:

$$P_{out} = \frac{V_{out}^2}{2R_L} \tag{1}$$

where V_{out} is the output voltage, and R_L is the resistance load.

2.2. Power Consumption

Power consumption is another important performance parameter of a PA. The increasing demand for portable operation must be addressed without consuming excessive power to ensure the maximum run time of the device. The total power consumption (P_{Total}) of a PA is the sum of the dynamic and static power consumption, as shown in Equation (2). Static power consumption (P_S) results from the leakage current (ICC), whereas dynamic power consumption (P_D) occurs when switching at high frequency [26]. Equations (3) and (4) show the derivation of the static and dynamic power consumption, respectively. Static power significantly affects the overall power consumption. A reduction in power consumption generates less heat in the device. Consequently, the temperature stress on the device will decrease, and the reliability of the system will be increased. High power consumption reduces the lifetime of PAs. Thus, PAs should be designed such that power consumption is minimized for a longer battery life.

$$P_{Total} = P_S + P_D \tag{2}$$

$$P_S = V_{DD} \times I_{CC} \tag{3}$$

$$P_D = \left[\left(C_{pd} \times f_I \times N_{SW} \right) + \sum \left(C_{Ln} \times f_{On} \right) \right] \times V_{DD}^2 \tag{4}$$

where C_{pd} is the capacitance of the power consumption (F), f_I is the input frequency (Hz), f_{On} is the sum of different output frequencies at each output (Hz), N_{SW} is the total number of outputs switching, V_{DD} is the supply voltage (V), and C_{Ln} is the sum of different load capacitances at each output.

2.3. Power Gain

Power gain (G) is the ratio of the output and input power, as expressed in Equation (5). This parameter describes how well the power amplifier can deliver a significantly higher power signal to the load compared to the input power [24]. The gain indicates the extent of the increase in the amplitude of a signal. A power amplifier enhances the output power to provide improved efficiency and sensitivity [25].

$$G = 10 \log_{10} (P_{out}/P_{in}) \text{ [dB]} \tag{5}$$

where P_{out} is the output power, and P_{in} is the input power.

2.4. Efficiency

The efficiency of the PA can be classified into two categories, namely drain efficiency (DE) and power-added efficiency (PAE). DE is the ratio of the RF output power to the DC power dissipation, as described in Equation (6) [27]. PAE is defined as the output power gained subtracted by the input power and then divided by the DC power dissipation, as shown in Equation (7) [24]. PAE evaluates how

efficiently the PA converts the DC power into AC power signal when the input power is considered [12]. High output power leads to high PAE.

$$DE= P_{out}/P_{(DC,drain)} \tag{6}$$

$$PAE= (P_{out} - P_{in})/P_{(DC,drain)} \tag{7}$$

2.5. Linearity

Linearity is defined as the scenario in which the output of the device varies linearly with respect to the variations of the input [28]. Linearity has become increasingly important in current RF communication structures. In general, the value of the third-order intercept point (IP3) determines the linearity. The intercept point is obtained by plotting the graph of the output power with respect to the input power on a logarithmic scale [28]. A high linearity means that the output power gained is linear to the input power [25].

Therefore, to satisfy the current demand, PAs should be designed to have low power consumption, high output power, high power gain, high PAE, and high linearity. The output power delivered by a PA and PAE play important roles in the design of an efficient power amplifier.

3. PA Design Classes

PA can be classified based on the power classes of A, B, C, D, E, F, AB, and so on [29]. Power classes are classified based on the types of bias applied to the RF transistors. Classes A, B, and AB are labeled as linear amplifiers, whereas classes C, D, E, and F are categorized as non-linear amplifiers [12]. For linear amplifiers, a class-A amplifier is biased such that the output device of the amplifier conducts 360° throughout the full cycle and as a consequence, the power loss is also increased which in turn leads to have less efficiency [14]. By contrast, the class-B amplifier is operated similarly to the class-A amplifier, but its output device conducts only a half (i.e., 180°) of the sinusoidal cycle (either a positive or a negative cycle [15]. Therefore, the power loss is decreased, and the efficiency is improved compared with its class-A counterpart. On the other hand, the class-AB amplifier is the combination of class-A and class-B amplifiers, in which both amplifiers can be on at the same time for a very short time [12] and thus improves the efficiency further.

For non-linear amplifiers, the class-C amplifier, conducts less than a half cycle, and experiences higher distortion and noise effects [30]. Although the efficiency of class-C PA is good, it suffers from poor dynamic range. The class-D amplifier, which is also known as the switching amplifier, has a low power loss because the active devices are kept either fully on or fully off [31]. The class-E amplifier is preferred for the design of RF PAs because class E has a higher theoretical efficiency than classes D and F [12]. The class-F amplifier operates in a unique manner by implementing the output network such that the drain voltage and current do not overlap with each other [32]. Aside from the classes in PA, an accurate architecture of PA must be selected to design an application-specific CMOS PA.

4. Advancement of 2.4 GHz CMOS PA

The PA design has emerged rapidly and has become more advanced. The rapid growth of 2.4 GHz ISM band devices demands a low-cost and low-power consumption solution. Although considerable achievements have been attained in CMOS, realizing this goal remains challenging for system-on-chip designers. The literature review shows that few design architectures are available for PAs, such as general cascode, self-biased cascode, differential cascode, and power-combining technique. The advancement of CMOS PAs operating at 2.4 GHz frequency are described in this study in terms of circuit architecture and performance point of view.

4.1. General Cascode Architecture

In the PA design in CMOS technology, two main issues must be addressed: Oxide breakdown and the hot carrier effect [16]. The gate-oxide breakdown is caused by a high voltage drop across the gate oxide, which results in an irreversible shortage of gate-to-channel capacitance. The oxide breakdown degrades the performance and the efficiency of the PA. Hot carrier effect refers to the acceleration of an electron by a high electric field in the MOS device, which generates a high kinetic energy [4]. This effect increases the threshold voltage and degrades the performance of the device. To overcome these problems, the general cascode circuit configuration was introduced in the PA design [17].

Ding and Harjani (2005) proposed a general cascode parallel class-AB CMOS PA by integrating a linear power control technique, as shown in Figure 3 [33]. In this design, two amplifiers operate in parallel to improve the dynamic range and power efficiency. The input transistor M1 was biased with a fixed voltage of 1.2 V. The cascode configuration was formed by the CS transistors M1, M2, M3, and M4, and the CG transistors M5 and M6. The CS transistors form the transconductance of the class-A and the class-B PAs in order to provide more linear transconductance, which led to high power gain of 12 dB. At low input levels, the class-A amplifier contributed the majority of the gain, and the class B amplifier had a very low gain. As the input level increased, the gain of the class- B amplifier increased, and its contribution to the overall gain increased proportionately. The outputs from both amplifiers were combined in the current domain with a slight overhead, thereby producing an improved isolation property and high power efficiency of 44%. AC coupling capacitors and the matching network were used for the output impedance matching [33].
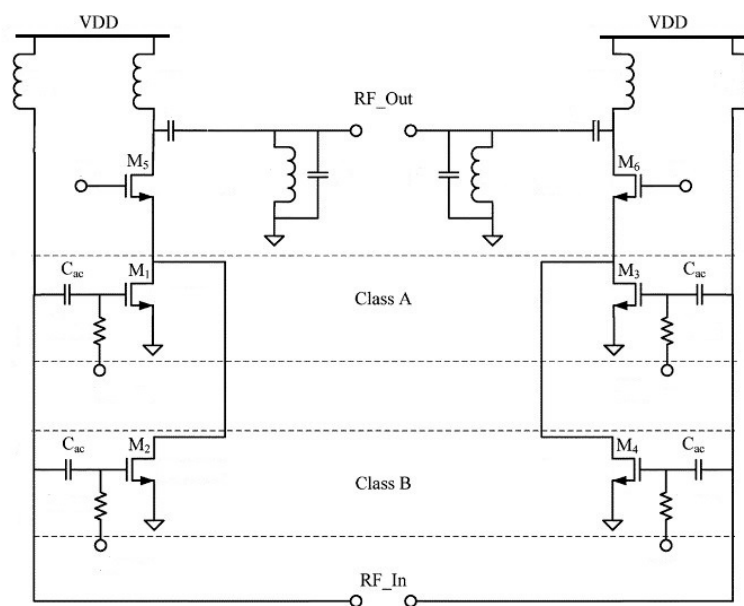
Figure 3. Circuit schematic for the CMOS parallel class-AB amplifier [33].

Saari et al. (2005) proposed an integrated cascode class-E PA (Figure 4) [34]. A cascode transistor M2 was inserted at the drive stage to increase the output power (21.3 dB) and stability. The switch on-resistance was minimized by integrating the transistor M3 as a switch. Both the driver and power stages were biased with NMOS current mirrors to prevent bias oscillations. The proposed design achieved a gain of up to 14.3 dB and a 40% PAE with a 3.3 V supply voltage. The input high-pass LC network degraded the gain performance. The source inductance LB4 reduced the gain by inducing the negative feedback. Although the gain was reduced, the overall stability of the proposed design was improved.
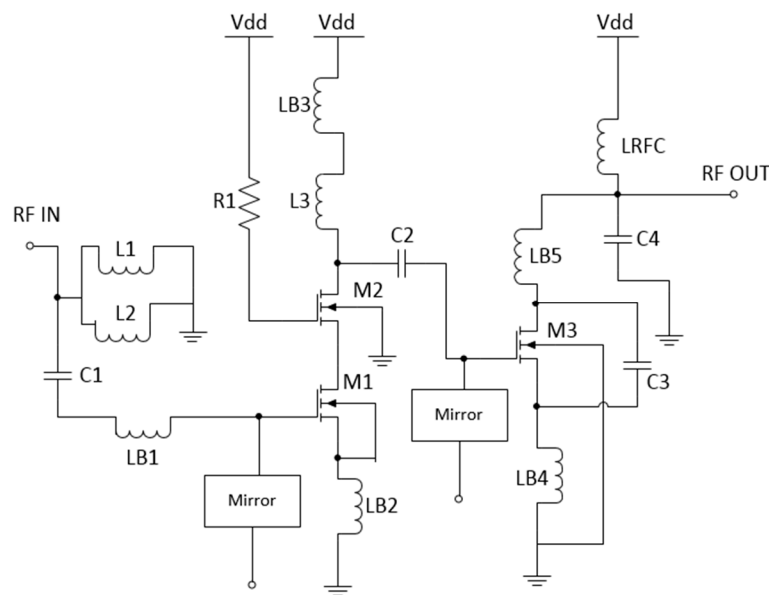
Figure 4. Schematic of a two-stage class-E PA [34].

Sira et al. (2011) presented a cascode modulated class-E PA that used 0.13 μm CMOS technology (Figure 5) [35]. In this design, the transistor M3 was cascoded with the transistor M2, and the power control signal was utilized at the gate of the transistor M3. The Vcasc dictated whether the cascode transistor M3 operated in the saturation or linear region. If the Vcasc value increased from zero, then M3 operated in the saturation region. If the Vcasc was further increased to 1.3 V, then M3 entered the linear region. The advantages of this proposed cascode modulated design are the 35-dB output power dynamic range. The power dynamic range refers to the maximum range over which the PA average output power can be controlled. This design obtained approximately 35% PAE and a 14.8 dB gain with a supply voltage of 1.6 V and a chip area of only 1.2 mm × 1.0 mm. This design had a low output power of 18 dBm, which was limited by the input power feed-through to the PA output because of the Miller capacitance between the gate and drain of the switching transistor. The feed-through effect was significant at low Vcasc levels, at which the cascode transistor was in saturation. At high Vcasc levels, M3 was in the linear region, but it did not affect the dynamic range.
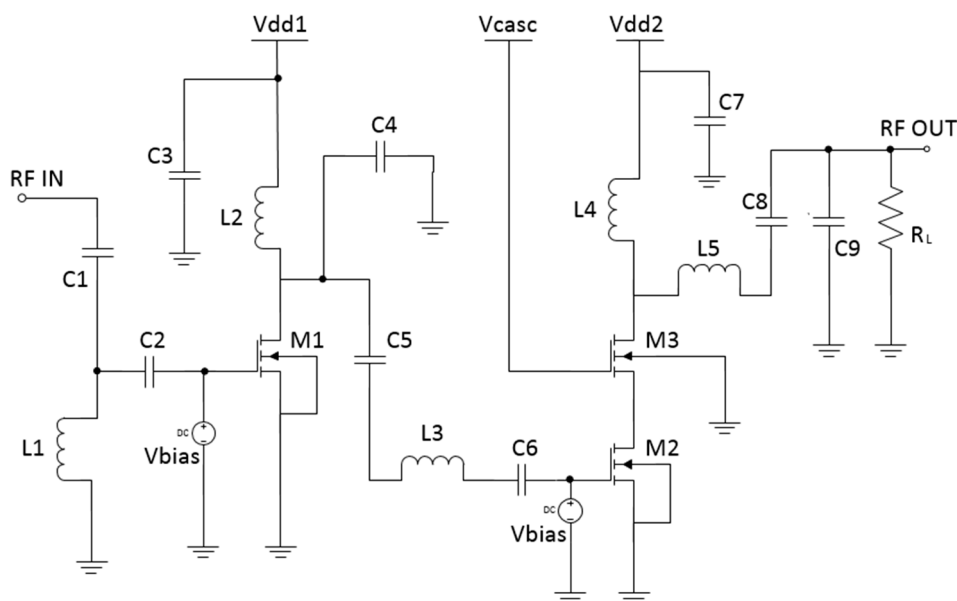

Figure 5. Cascode-modulated CMOS PA [35].

Bameri et al. (2011) proposed another general cascode class-E PA that utilized an advanced linear power control technique, as shown in Figure 6 [16]. The gate voltage of the transistor M4 was used to control the voltage of the output power. The significant improvement offered by this design was the wide power control range of 155 dB from −136 dBm to +19 dBm. However, this design suffered from a low output power because the output power was reduced as the control voltage was decreased. The reduced output power operates the PA from a switching mode to a linear mode, thereby producing a higher slope of AM-AM characteristic for the cascode power control technique. At high control voltage levels, the driver output power also increased. An increase in the driver output power reduced the Ron, thereby increasing its PAE and gain.
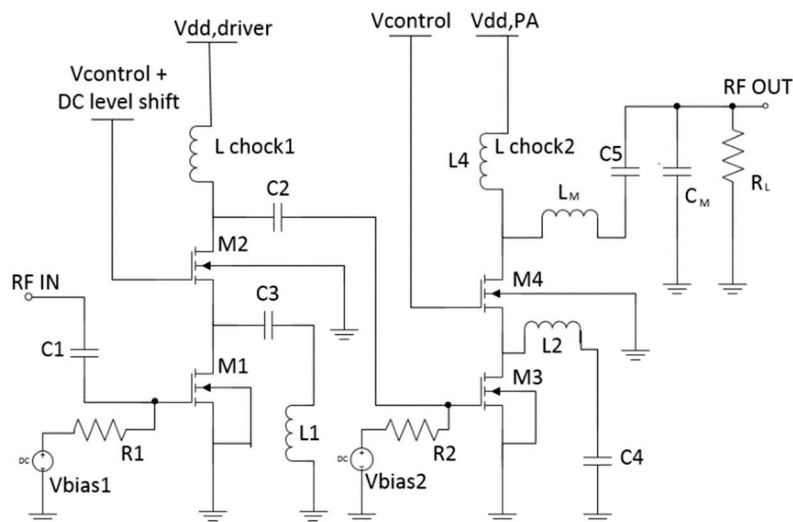

Figure 6. Linear power control cascode PA circuit [16].

Sahu and Deshmukh (2013) introduced another PA that was operated with a 2.5 V supply, as depicted in Figure 7 [20]. In this PA, the driver stage used the cascode topology, whereas the power stage utilized the basic power topology. Two types of bias circuits were tested in this circuit. Both the driver stage and the power stage used the Metal Oxide Semiconductor Field Effect Transistor (MOSFET)-only bias in order to reduce total DC current up to 0.0901 A. The input and output matching networks reduced the input and output return losses, resulting in a low power consumption of 0.2253 W and a high PAE of 44.67% for a 1 dB compression point.

Cai et al. (2016) reported a class-D PA for medical applications in 0.18 μm CMOS technology [31]. The PA was designed with two active switches. The switches are alternatively turned on and off depending on the driver stage output signal. A LC band pass filter was also utilized to control the frequency of operation which exhibits the advantage of no power dissipation for out of band signal. At 2.4 GHz, the PA reported less than −10 dB S_{11} to transmit a maximum of 15 dBm output power to a 50 Ω load with 50% PAE.

However, the cascode configuration experienced additional power losses. In practical cases, two cascode devices cannot be switched on or off simultaneously. Thus, a greater power loss is always present between them, which diminishes the efficiency performance of the PA [27].
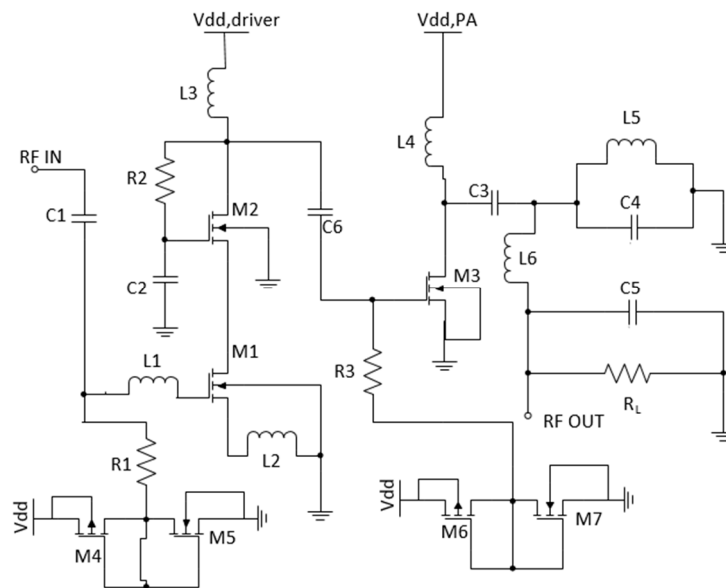
Figure 7. Schematic of two-stage CMOS PA [20].

4.2. Self-Biased Cascode Architecture

For the general cascode topology, the breakdown voltage of the common gate (CG) transistor limits the supply voltage of a design. Thus, a self-biased technique allows an RF signal to swing at the CG to increase the biasing voltage above V_{DD}. The maximum drain to the gate voltage is the same for both cascode transistors. A larger signal swing can be delivered at the output before oxide breakdown occurs. By applying this technique, the gate of the NMOS was boosted above V_{DD}, and the power consumption was minimized [36].

The design presented in Figure 8 proposed by Sowlati and Leenaerts (2003) is the first PA that can operate at 2.4 V without oxide breakdown or hot carrier degradation [17]. The self-biased cascode topology was applied at both driver and power stages to swing the RF signal at gate of M2. An additional bond pad was not required to connect through gate of M2, as the bias at this point was provided by Rb–Cb network. Both gate and drain of M2 operated at the same DC voltage. Bias voltages of 0.55 and 0.8 V were used for the gates of the driver and power stages. The simulation results revealed that the proposed design provided a 24.5 dBm output power for a gain of 31 dB by utilizing the sliding bias technique. This technique is a de-biasing technique applied at low and intermediate power levels to obtain the same gain as that at maximum power. The gain variation was reduced by applying the sliding bias technique.

Murad et al. (2009) designed a 0.18 µm single-ended class-E PA for WLAN applications, as shown in Figure 9 [37]. In this design, the bias for CS gate is provided by R3 and C3, for which no extra bond pad is required. The dc voltage applied to the CS gate is the same as that applied to CS drain. As shown in Figure 9, all inductors were replaced with bond wire inductors to increase the quality factor (Q) and to minimize losses. The high Q contributed to obtaining a higher PAE. The design used 2- and 5-mm bond wires, which were equivalent to 2.0 and 4.1 nH, respectively. This PA design achieved a 44.5% PAE and a 23 dBm output power delivered with a supply voltage of 3.3 V [37]. Although it had a high PAE, a significantly high supply voltage was needed to operate it. However, this work adopted a class-E PA with a cascode topology, which reduced the stress on the device due to the high supply voltage.
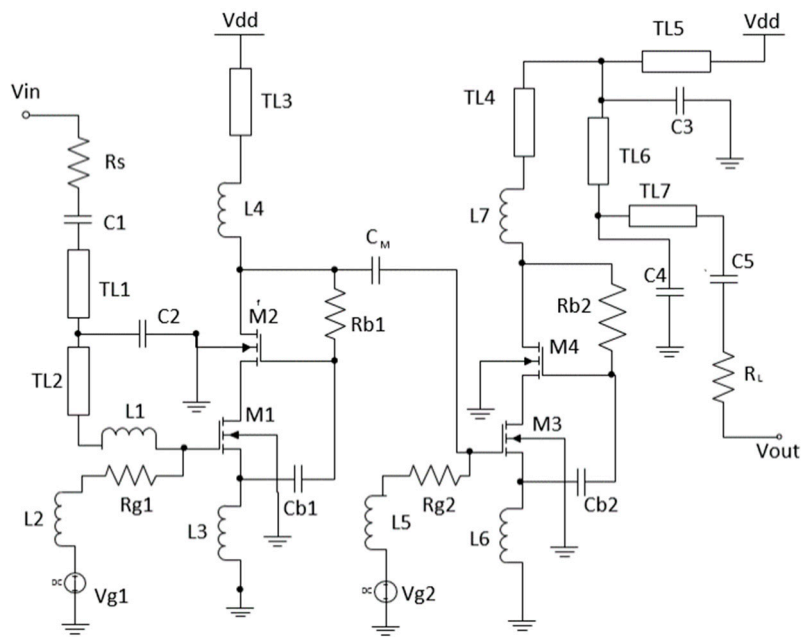
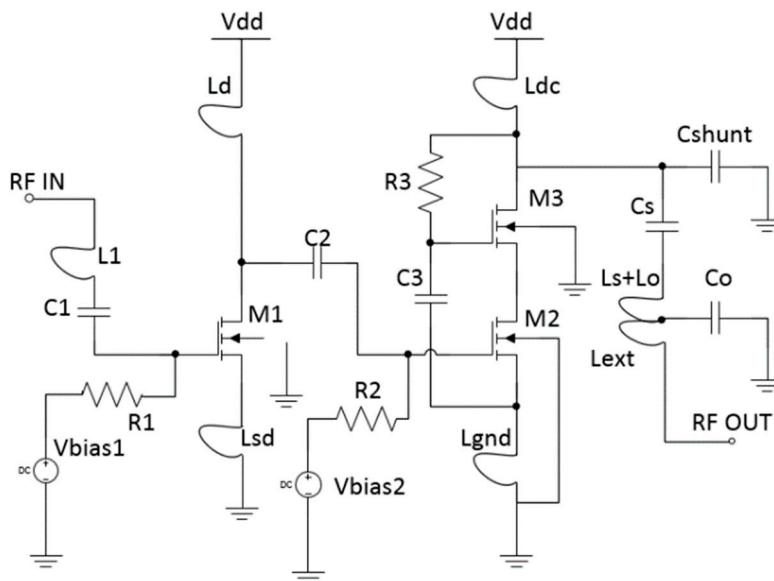**Figure 8.** Two-stage self-biased cascode PA [17].

Figure 9. Schematic of class-E self-biased cascode PA [37].

Hong et al. (2010) introduced a new self-biased cascode PA design with a capacitive cross-coupling technique, as shown in Figure 10 [38]. The first amplifier stage employed a general cascode class-A PA, whereas the second stage implemented a self-biased cascode class-AB PA. Given that thick gate-oxide transistors were used, the large size of the transistors resulted in a large gate-drain capacitance. Capacitive cross-coupling was implemented to decrease the gate-drain capacitance and the layout area of the bypass capacitance. Thus, the PA covered a small chip area of 1.0 mm × 1.6 mm and improved the reverse isolation. A transformer was integrated at the output to improve the output power. The transformer had a turn ratio of 2:1, which reduced the output impedance from 50 Ω to 12.5 Ω. At a supply voltage of 3.3 V, the PA achieved a 34.3% maximum PAE, a 25.2 dBm output power, and a 26.5 dB power gain [38].
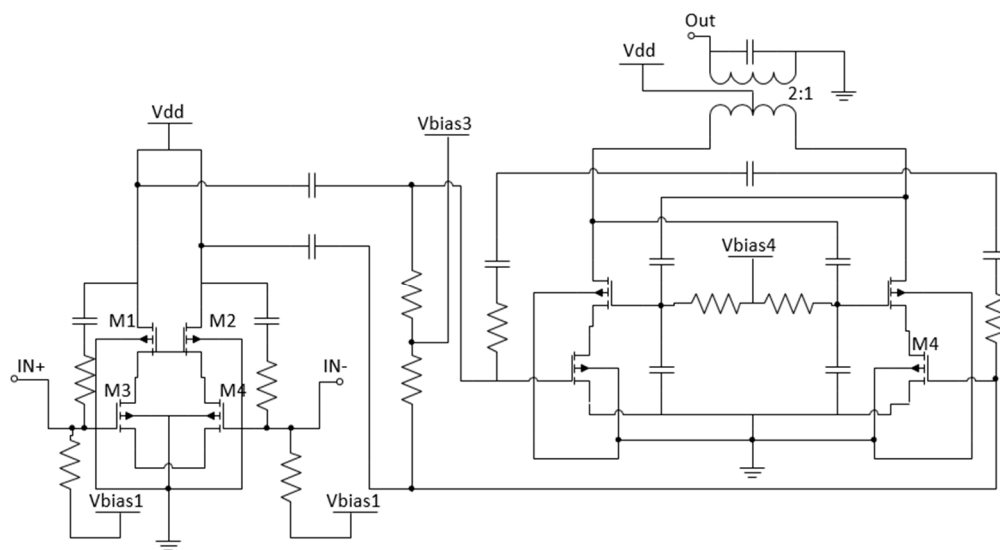
Figure 10. Schematic of proposed capacitive-cross-coupled CMOS PA [38].

The objective of the self-biased cascode architecture was to provide a circuit that did not require external bias supplies to minimize the use of resistor networks. Operational flexibility can be achieved by not providing a bias voltage directly from the power supply. Consequently, a simple, compact, efficient, and economical circuit was formed [39]. This design eliminated the requirement of additional bond pads and overcame the device stress.

4.3. Differential Cascode Architecture

Differential cascode topology is mainly composed of CG and CS amplifiers [40]. The differential configuration minimizes the common mode noise and the substrate coupling. Compared with other designs, this architecture presents less impedance matching losses. In addition, the problem of low breakdown voltage can easily be overcome by implementing this architecture.

Ho and Luong (2003) introduced a differential class-E PA with a low supply voltage of 1 V, as shown in Figure 11 [41]. This architecture displayed a large capacitive loading when it used millimeter-size transistors because of the low supply voltage. This issue was solved by utilizing bond wire inductor and a cross-coupled pair. By doing so, a positive feedback was formed for the preamplifier. The positive feedback provided an optimum driving signal to the output to maintain high efficiency and output power. The bond wire inductors generated a high-quality factor, which resulted in a 33% PAE and an 18 dBm output power. However, the bond wire inductor was challenging to predetermine in this design, thereby reducing the accuracy within 5% to 10%.

Lee and Park (2014) proposed a modified mode-locking differential cascode PA to minimize the time delay, as shown in Figure 12 [42]. This design was focused on improving the high power gain. The input of the cross-coupled transistor was connected to the drain voltage of the CS transistor. This design overcame the low breakdown voltage problems of CMOS devices. The time delay between the CS and the cross-coupled transistors was reduced by this method, thereby maximizing the advantage of the mode-locking technique and reducing the harmonics. An excessive time delay produces harmonics, which distorts the signal. Although the parameters for this design are moderate, the power gain is considerably high. The measured power-added efficiency for the proposed design was 34.9%, whereas the saturated output power was 23.32 dBm.
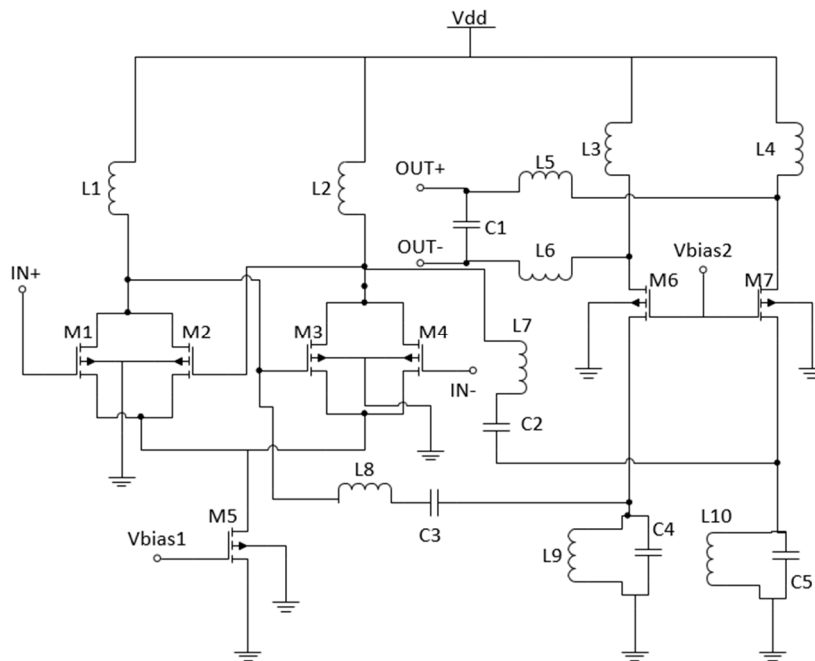
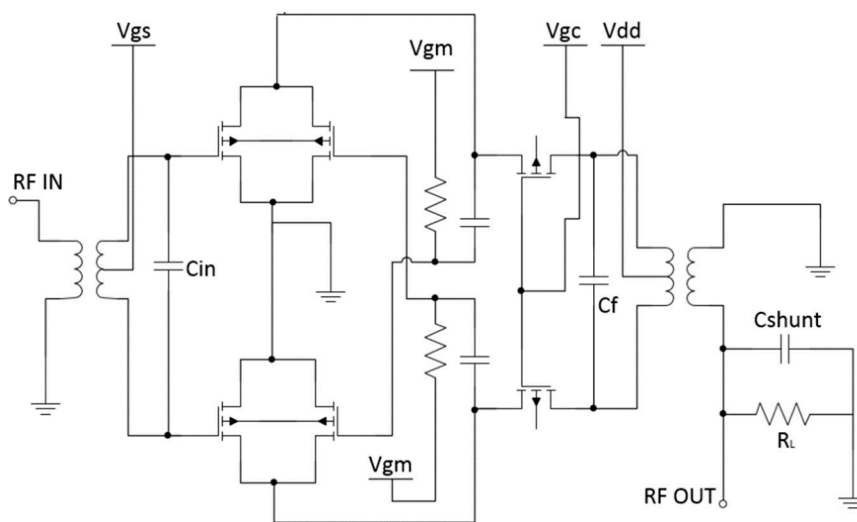**Figure 11.** Schematic of proposed differential PA [41].

Figure 12. Schematic of mode-locking technique PA [42].

Ghorbani and Ghoushchi (2016) proposed a class-E differential PA by implementing capacitive cross-coupling neutralization, as shown in Figure 13 [43]. This design applied a complementary CMOS cross-coupled pair with transistors M1–M4 to decrease the transistor size and, in turn, reduce the inductor loss. The transconductance of the transistors was increased by the cross-coupling capacitor technique [44,45]. Consequently, the power gain increased because it was proportional to the transconductance value. Such capacitor cross coupling improved the stability of the PA. The simulation results indicate that a high gain of 35.6 dB was obtained with a supply voltage 1.8 V. This design produced a very high power gain and a high output power (28.5 dBm). However, the PAE performance was moderate because it was optimized by the changing the cross-coupling capacitance with the input power.
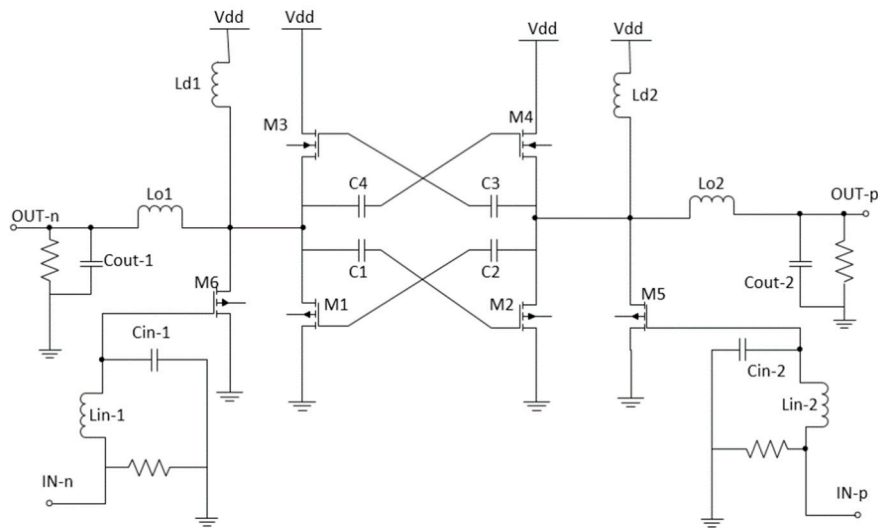
Figure 13. Class-E differential PA with cross-coupling pair [43].

4.4. Power Combining Architecture

If the output power requirement for a transmitter is very high and a single stage PA cannot fulfil the demand, power combining methods are very useful where multiple stages of PA are added to achieve the desired overall output power. Transformers are the commonly utilized components for implementing a fully integrated high-power power amplifier (PA) as a power combiner which also serve the purpose of impedance transformation in order to maximize the efficiency.

An et al. (2009) proposed a different architecture of the class-AB PA design that consisted of an input balun and a parallel combining transformer (PCT), as depicted in Figure 14 [46]. Cascode topology was applied at the driver and power stages to prevent excessive voltage stress on the device, as it undergoes breakdown at high voltages under an excessive voltage stress [46]. The PCT concept was applied by combining the three identical PAs in parallel for the layout of the transformers, which was more compact but displayed an average chip size of 2 mm² [47]. LC baluns were applied because they can be effectively exploited for matching and power combining [25]. With this design, the authors achieved a maximum output power of 31 dBm, a power gain of 35 dB, and a PAE of 27% at a current consumption of 650 mA with a power supply of 3.3 V [46]. This design generated a very high output power with less PAE. However, this design was bulky and had a complex circuitry.
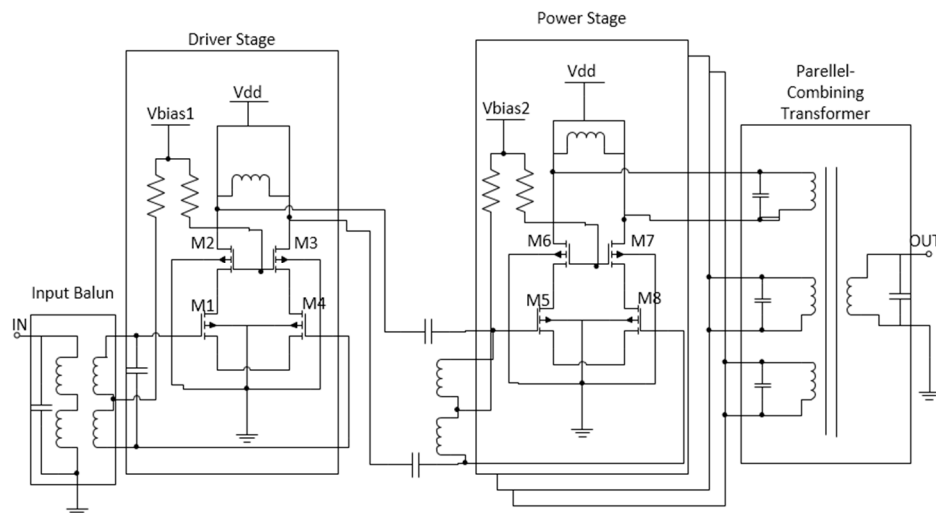

Figure 14. Proposed differential class-AB PA with parallel combining transformer (PCT) [46].

Ren et al. (2015) designed another 2.4 GHz PA using PCT technique, as shown in Figure 15 [48]. The driver stage uses class-A biasing, whereas the power stage follows class-AB biasing. Three identical PAs were combined in parallel to form the PCT design. The self-biased cascode technique was implemented inside the PA. This PA design delivered an output power of 30.7 dBm and a high gain of 33.2 dB [48], but its PAE was 29%.
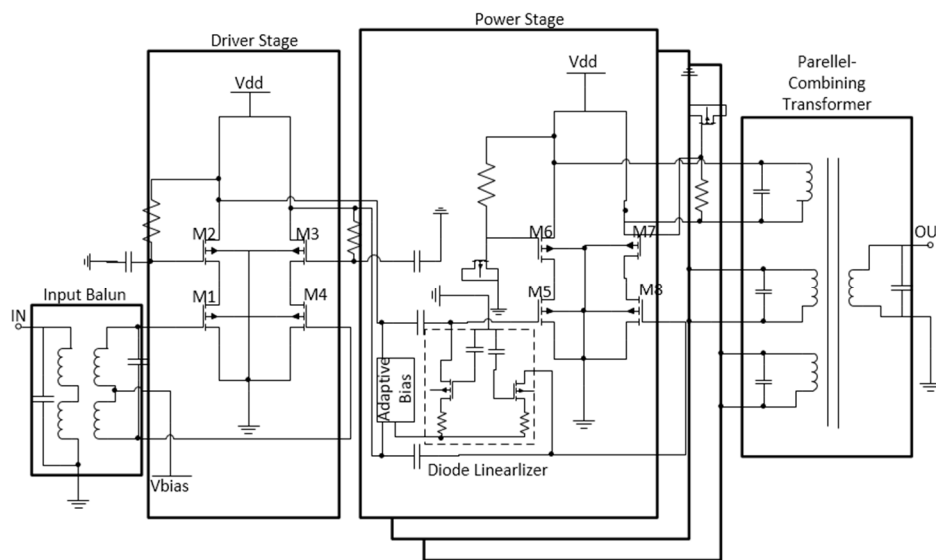

Figure 15. Schematic of 2.4 GHz PCT PA [48].

PSCT is another method that performs parallel and series combining simultaneously inside a single structure [49]. Ezzulddin and Jasim (2015) introduced another class-AB PA for wireless local area network (WLAN) applications by integrating the hybrid-type parallel-series power-combining transformer (PSCT) method, as shown in Figure 16 [50]. The design consisted of a single-ended class-AB PA connected in series to the PSCT with three other identical PAs combined in parallel to the PSCT. In class AB, the DC bias voltage of the gate-to-source slightly exceeded the threshold voltage, and the transistor was biased at a small drain current. The LC tank circuit was designed to block higher harmonics from reaching the load. This PA simulated a very high output power of 30 dBm, a gain of 30 dB, and moderate PAE of 40% at 2.5 V supply voltage.
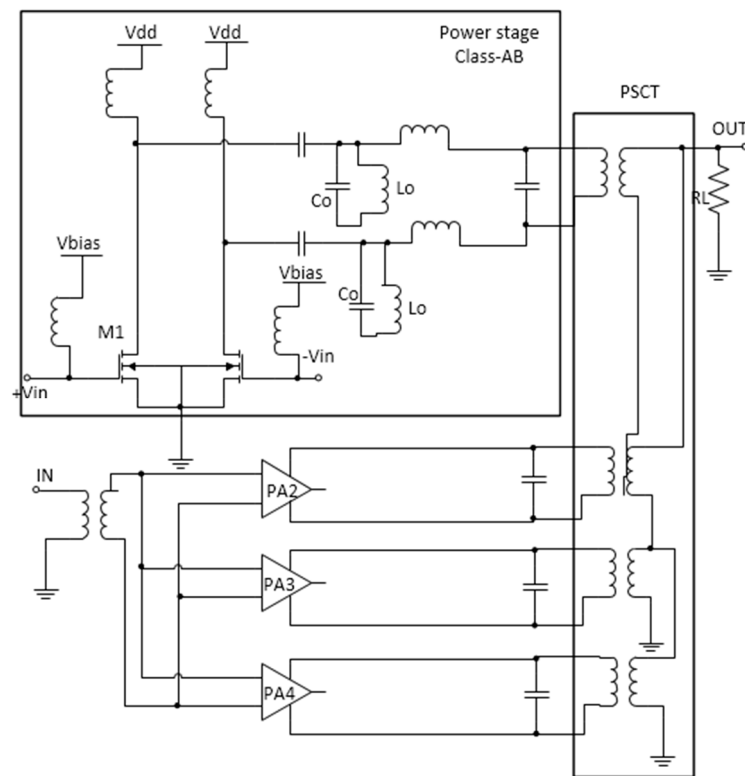
Figure 16. Schematic class-AB PA based on parallel-series power-combining transformer (PSCT) [50].

5. Discussion

In modern wireless communication systems, different classes of CMOS PAs have been implemented successfully. The CMOS process has become much more popular because of its simple integration, low power consumption, and low cost of design. However, these PAs are hindered by oxide breakdown and hot electron effect. The reason is that the CMOS technology is mostly optimized for low voltage, whereas power amplifiers operate at high voltage. The low breakdown voltages of CMOS transistors lead to the reliability problem in PAs. Thus, further investigations are needed to overcome the limitations of the PA design in CMOS technology.

Different architectures have been proposed to satisfy the desired performance of the PA. The pie chart and bar graph in Figures 17 and 18, which have been generated from the literature considered for this study, present the outcomes of the PA design architectures and classes in state-of-the-art works in the past 18 years (2000 to 2018). The plotted graph shows that the dominant choice is the general cascode architecture, which accounts for 33.33% of the overall PA design architectures. Compared with the rest, this type of architecture produces a higher power-added efficiency and a higher power gain at a lower power consumption. The second most dominant choice is the power combining architecture, which accounts for 26.67% of the overall design architectures. This architecture is characterized by a high output power and balanced parameter values. Both the self-biased and differential cascode architectures have the lowest percentage coverage of 20%. Among all classes of PA, class-E biasing has the highest percentage coverage of 53.33%. The high PAE allows the extensive integration of that class in the PA design. Class-D biasing has the second highest coverage of 25.34%, whereas class-AB biasing has the lowest coverage of 21.33%.
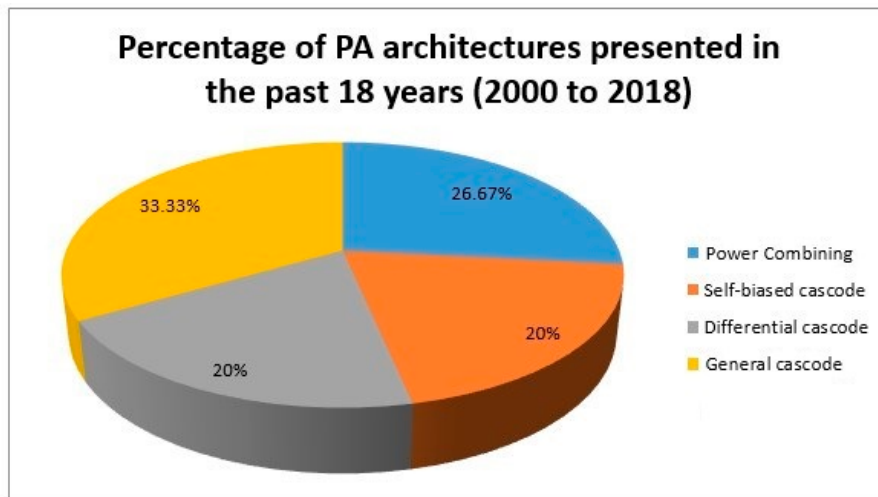
Figure 17. Pie chart of PA architectures in the past 18 years (2000 to 2018).
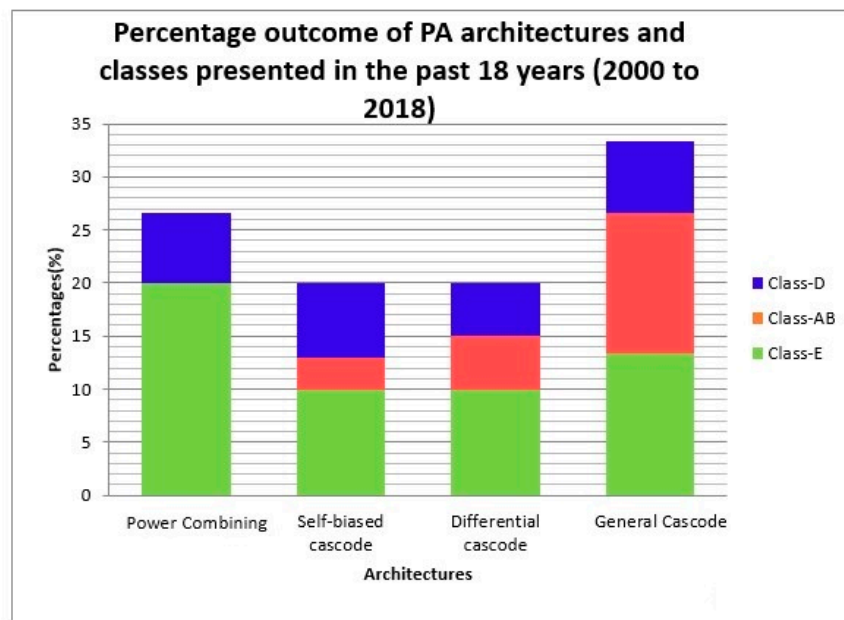

Figure 18. Bar graph of PA architectures and classes in the past 18 years (2000 to 2018).

Several PA design architectures achieved high parameter performance, whereas some did not. Table 1 summarizes the design techniques, advantages, and disadvantages of each PA architecture.

As shown in Table 1, the general cascode configuration eliminated the problem of oxide breakdown and hot carrier effect. The drawbacks of this architecture were additional power losses caused by the parasitic inductance. Integrating an inductor with a high-quality factor can linearly decrease the power losses. However, the breakdown voltage of the CG transistor limits the supply voltage in cascode PAs. Thus, a strategy for device staking in series was introduced to reduce the voltage stress of each device without decreasing the supply voltage [51]. In comparison, a self-biased cascode does not require external bias, minimizes the use of resistor networks, and overcomes the device stress. Given that no additional bond pads were required, a simpler circuit was produced, which reduced the fabrication cost. However, the self-biased cascode is hindered by its low slew rate [52], which causes the amplifier to respond more slowly to the rapid changes at the input level.

Table 1. Performance analysis between different PA design techniques.

Architectures	Design Techniques of Architectures	Advantages	Disadvantages
General Cascode	- The source terminal of the transistor is connected to cascode with the drain of another transistor - The gate of transistors is biased with DC voltages.	- Eliminates oxide breakdown and hot carrier effect - Circuit simplicity - Low power consumption - High power gain and PAE - Small chip size	- Additional power losses in CG transistor - Moderate output power
Self-Biased Cascode	- A resistor and a capacitor produce bias for the transistor to reduce the extra DC voltage supply needed - Allow RF signal swing at the common gate of two cascaded transistors to improve the biasing voltage.	- No external bias supplies needed - Can overcome the device stress - Simpler circuit and low-cost circuit - High power gain - Reduced power consumption	- Required high supply voltage - Low slew rate with slow react time of PA to the input level - The supply voltage is limited by the breakdown voltage of CG
Differential Cascode	- Cross-coupling capacitors are used to decrease the power dissipation of PA with increasing transconductance. - The cross-coupling transistors form a positive feedback on driver stage is used to obtain a high efficiency	- Minimized common mode noise and substrate coupling - Minimized impedance matching losses - No low breakdown voltage problem	- Considerably less PAE - More complex circuitry - Average output power
Power Combining Architecture	- Three identical PAs are combined in parallel to form a transformer - LC balun is used as the input balun for an effective input matching.	- Reduction of secondary inductor losses - Generate high output power - High power gain	- Large chip size and high cost - Complex circuitry - High power consumption - Poor PAE performance

In a differential configuration, the current is discharged to the ground twice per cycle, thereby reducing the common mode noise and the substrate coupling. Removing the substrate noise component twice in the circuit diminishes the interference problem [53]. In addition, the output power was doubled from that under a single-ended configuration, and the optimum load was reduced. Consequently, the matching losses were reduced [41]. The size of the transistors and the current flowing can be reduced by using a differential configuration. The drain output voltage can be spread over both transistors; thus, nearly twice of the supply voltage can be handled, which resolves the low breakdown voltage. Moreover, the power combining architecture reduces the secondary inductor losses, thereby minimizing the current flowing through it [50]. The power combiner generates a higher output power by combining several units of power cells [49]. However, this kind of structure is more complex and bulkier, and it consumes larger chip area, leading to a high manufacturing cost.

Table 2 shows a chronological summary of empirical results for PAs, which were extracted from studies on differential topologies involving CMOS process, supply voltage, architectures, classes, power consumption, power gain, PAE, and output power.

As shown in Table 2, the highest output power performances of the PA design were 31, 30.7, and 30 dBm obtained from References [46,48,50], respectively, and all of these works used powers combining method, suggesting that this method provides a higher output power compared with that in other architectures. Although Reference [46] has a high output power of 31 dBm and a high-power gain of 35 dB, its PAE performance was poor at 27%.

The highest PAE of 57% was achieved in Reference [16], which implemented a general cascade architecture. The reason is that dissipation of the charge and discharge of parasitic capacitance was reduced. Although its efficiency was high, the output power was only 19 dBm. It used a supply voltage of 2.0 V, which was considerably low and resulted in a low power consumption. The design proposed by Sahu and Deshmukh [20] achieved the highest power gain of 42.73 dB and the second highest PAE of 44.7%. It attained a moderate output power of 20 dBm.

The PA based on the differential cascode designed by Ghorbani and Ghaznavi [38] achieved the lowest power consumption of 0.225 W by implementing cross coupling capacitor technique, whereas the method in Reference [46] consumed a large amount of power (2.1450 W) because of the vast parasitic capacitances at the gates of the PCT. In addition, it had the lowest power gain. A significant power gain of 35.6 dB was obtained in Reference [43]. It had a low supply voltage and a considerably high output power. The PAE of this design was also quite high (43%). However, its other parameters were low, displaying an output power of 18 dBm and a PAE of 33%. Thus, this design exhibited an

average performance for all parameters. Hence, this design would be ideal for a moderate performance with a low power consumption.

Table 2. Performance comparison of 2.4 GHz CMOS PA.

Reference (Year)	CMOS Technology (µm)	Supply Voltage (V)	Architectures	Classes	Power Consumed (W)	Power Gain (dB)	PAE (%)	Output Power (dBm)
[34] (2005)	0.18	3.3	General cascode	Class-E	-	14.3	40	21.3
[35] (2011)	0.18	1.6	General cascode	Class-E	-	14.8	35	18
[16] (2011)	0.13	2.0	General cascode	Class-E	-	17	57	19
[20] (2013)	0.13	2.5	General cascode	-	0.2283	42.73	44.7	20
[14] (2018)	0.18	2.4	General cascode	Class-F	-	25.8	34.6	27.6
[17] (2003)	0.18	2.4	Self-biased cascode	-	0.5208	31	49	24.5
[37] (2009)	0.18	3.3	Self-biased cascode	Class-E	-	13	44.5	23
[38] (2010)	0.18	3.3	Self-biased cascode	Class-A	-	26.5	34.3	25.2
[41] (2003)	0.35	1.0	Differential cascode	Class-E	-	-	33	18
[42] (2014)	0.18	3.3	Differential cascode	-	-	13.2	34.9	23.3
[43] (2016)	0.18	1.8	Differential cascade	Class-E	0.2250	35.6	43	28
[46] (2009)	0.18	3.3	Power combining	Class-AB	2.1450	35	27	31
[48] (2015)	0.18	3.3	Power combining	Class-AB	0.8382	33.2	29	30.7
[50] (2015)	0.13	2.5	Power combining	Class-AB	-	30	40	30
[54] (2016)	0.065	3.3	Power combining	-	-	26.5	40.3	26.9
[55] (2017)	0.18	3.3	Spiral-type output transformer	-	-	26.6	23.5	21.28
[12] (2018)	0.18	2.5	Proportional series combining transformer	Class-AB	-	28	31	26.8
[31] (2016)	0.18	1.8	Switched mode	Class-D	0.9040	-	50	15

Among the classes of PA architectures, the class-E PA was generally selected as the most. For the general cascode architecture, References [16,34,35] were designed with a class-E PA. In self-biased cascode cases, Reference [33] applied class-E biasing, whereas Referencs [41,42] adopted a differential cascode topology. Their PAE values were very high, with one reaching up to 57%. Class-AB PAs in power combining architecture has high output power of more than 30 dBm and a high power gain of more than 30 dB in References [46,49,50]. However, the PAE performances of these designs were unsatisfactory. Thus, the class-E PA had a higher PAE, whereas the class-AB PA had a higher

output power and power gain. The class-E PA achieved a high efficiency, and a lower supply voltage was needed.

Comparison of Tables 1 and 2 indicate that in the case of the output power, the power combining architecture was the ideal selection. It combined several power cell units, which can endure more force and in turn can produce a higher output power. In terms of gain, the general cascode and the self-biased cascode were considered the most suitable architectures because they can achieve a high gain of 42.73 and 35.6 dB, respectively [20,43]. In terms of circuit complexity, the general cascode was the best architecture with the simplest circuitry, whereas the power combining architecture had the highest circuit complexity. Both the general and differential cascode architectures can operate at a lower supply voltage compared that for the self-biased and power combining architectures.

Overall, the key advantage of the general cascode architecture is its high efficiency and gain while maintaining the performance of the other parameters under the standard requirements. For low-power and highly efficient applications, this architecture is considered the best. Among all types of PA architectures, the general cascode was identified as the most suitable for full system integration. Besides, class-E PA provided the best performance, and it can be easily integrated with the general cascode architecture. Therefore, studies in this field will continue to be extremely active and vigorous for the development of RF devices operating in a high-frequency range, such as 2.4 GHz with optimum power.

6. Conclusions

This article comprehensively discussed the different architectures of the CMOS PA design. These architectures are for Industrial, Scientific and Medical (ISM) band applications with design concerns and performance analysis. Several techniques have been implemented by different researchers to improve the performance of 2.4 GHz RF PAs in CMOS technology. Several researchers have attempted to maximize the transmitter output power, and several others have worked to reduce the leakage of current and power consumption to obtain ultra-low power. A few studies have improved the power gain. In designing a CMOS PA, the required performance of the specific parameters must be identified and concentrated on. Output power, power efficiency, and power consumption are the main performance parameters of PA that must be considered. Comparison showed that the general cascode architecture is highly suitable for designing a 2.4 GHz CMOS PA and can address the demand for high power gain, PAE, output power, and low-cost solutions by modern wireless communication systems. The class biasing for the PA would be class-E if high efficiency is highly demanded for the desired PA. The procedures of PA designing, and the relevant discussions presented in this study, are expected to aid researchers in designing CMOS PAs and contribute to realizing small, low-cost, wireless communication terminals at the 2.4 GHz ISM band.

Author Contributions: All authors have contributed equally in this review article.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Bhuiyan, M.; Reaz, M.; Jalil, J.; Rahman, L.; Chang, T. Design Trends in Fully Integrated 2.4 GHz CMOS SPDT Switches. *Curr. Nanosci.* **2014**, *10*, 334–343. [CrossRef]
2. Ali, S.N.; Agarwal, P.; Gopal, S.; Mirabbasi, S.; Heo, D. A 25–35 GHz Neutralized Continuous Class-F CMOS Power Amplifier for 5G Mobile Communications Achieving 26% Modulation PAE at 1.5 Gb/s and 46.4% Peak PAE. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2019**, *66*, 834–847. [CrossRef]
3. Badal, T.I.; Reaz, M.B.I.; Bhuiyan, M.A.S.; Kamal, N. CMOS Transmitters for 2.4-GHz RF Devices: Design Architectures of the 2.4-GHz CMOS Transmitter for RF Devices. *IEEE Microw. Mag.* **2019**, *20*, 38–61. [CrossRef]

4. Bhuiyan, M.A.S.; Chew, J.X.; Reaz, M.B.I.; .Kamal, N. Design of an active inductor based LNA in Silterra 130 nm CMOS process technology. *Inf. Midem* **2015**, *45*, 188–194.

5. Bhuiyan, M.A.; Zijie, Y.; Yu, J.S.; Reaz, M.B.; Kamal, N.; Chang, T.G. Active inductor based fully integrated CMOS transmit/receive switch for 2.4 GHz RF transceiver. *Anais da Academia Brasileira de Ciências* **2016**, *88*, 1089–1098. [CrossRef]

6. Badal, M.T.I.; Reaz, M.B.I.; Jalil, Z.; Bhuiyan, M.A.S. Low Power High-Efficiency Shift Register Using Implicit Pulse-Triggered Flip-Flop in 130 nm CMOS Process for a Cryptographic RFID Tag. *Electronics* **2016**, *5*, 92. [CrossRef]

7. Schmiedeke, P.; Bhuiyan, M.A.S.; Reaz, M.B.I.; Chang, T.G.; Crespo, M.L.; Cicuttin, A. A fully integrated high IP1dB CMOS SPDT switch using stacked transistors for 2.4 GHz TDD transceiver applications. *Sadhana* **2018**, *43*, 94. [CrossRef]

8. Issa, A.H.; Ghayyib, S.M.; Ezzulddin, A.S. Toward a fully integrated 2.4GHz differential pair class-E power amplifier using on-chip RF power transformers for Bluetooth systems. *AEU Int. J. Electron. Commun.* **2015**, *69*, 182–187. [CrossRef]

9. Kamerman, A.; Monteban, L.; Zysman, G.I. WaveLAN®-II: A high-performance wireless LAN for the unlicensed band. *Bell Labs Tech. J.* **2002**, *2*, 118–133. [CrossRef]

10. Kumar, R.; Kumar, M.; Balrajb, M. Design and Implementation of a High Efficiency CMOS Power Amplifier for Wireless Communication at 2.45 GHz. In Proceedings of the 2012 International Conference on Communication Systems and Network Technologies (CSNT 2012), Gujarat, India, 11–13 May 2012; pp. 804–807.

11. Rostomyan, N.; Özen, M.; Asbeck, P. 28 GHz Doherty Power Amplifier in CMOS SOI With 28% Back-Off PAE. *IEEE Microw. Wirel. Compon. Lett.* **2018**, *28*, 446–448. [CrossRef]

12. Wu, H.; Li, B.; Hu, Y.; Wang, K.; Liang, Z.; Wu, Z.; Liu, Y. Fully-integrated linear CMOS power amplifier with proportional series combining transformer for S-Band applications. *IEICE Electron.* **2018**, *15*, 20171100. [CrossRef]

13. Roy, P.; Dawn, D. Fully integrated CMOS power amplifier using resistive current combining technique. *IET Microwav. Anten. Propag.* **2018**, *12*, 826–832. [CrossRef]

14. Kim, J. Linear CMOS power amplifier using continuous gate voltage control. *Microw. Opt. Technol. Lett.* **2018**, *60*, 337–341. [CrossRef]

15. Kim, K.; Ko, J.; Nam, S.; Lee, S. A Two-Stage Broadband Fully Integrated CMOS Linear Power Amplifier for LTE Applications. *IEEE Trans. Circuits Syst. II Briefs* **2016**, *63*, 533–537. [CrossRef]

16. Bameri, H.; Hakimi, A.; Movahhedi, M. A linear-high range output power control technique for cascode power amplifiers. *Microelectron. J.* **2011**, *42*, 1025–1031. [CrossRef]

17. Sowlati, T.; Leenaerts, D. A 2.4-ghz 0.18-μm cmos self-biased cascode power amplifier. *IEEE J. Circuits* **2003**, *38*, 1318–1324. [CrossRef]

18. Bhuiyan, M.A.S.; Reaz, M.B.I.; Jalil, J.; Rahman, L.F. Design of a nanoswitch in 130 nm CMOS technology for 2.4 GHz wireless terminals. *Bull. Pol. Acad. Sci. Tech. Sci.* **2014**, *62*, 399–406. [CrossRef]

19. Van Praet, C.; Spiessens, P.; Tubbax, H.; Stubbe, F.; Li, Z.; Torfs, G.; Bauwelinck, J.; Yin, X.; Vandewege, J. A 2.45-GHz +20-dBm fast switching class-E power amplifier with 43% PAE and an 18-dB-wide power range in 0.18-um CMOS. *IEEE Trans. Circuits Syst. II Briefs* **2012**, *59*, 224–228. [CrossRef]

20. Sahu, S.R.; Deshmukh, A.Y. Design of High Efficiency Two Stage Power Amplifier in 0.13 μM RF CMOS Technology for 2.4GHZ WLAN Application. *Int. J. VLSI Des. Commun. Syst.* **2013**, *4*, 31–40. [CrossRef]

21. Santana, D.B.; Klimach, H.; Fabris, E.; Bampi, S. CMOS RF class-E power amplifier with power control. In Proceedings of the 2016 IEEE 7th Latin American Symposium on Circuits & Systems (LASCAS), Florianopolis, Brazil, 28 February–2 March 2016; pp. 371–374. [CrossRef]

22. Yen, C.-C.; Chuang, H.-R. A 0.25-μm 20-dBm 2.4-GHz CMOS power amplifier with an integrated diode linearizer. *IEEE Microw. Wirel. Compon. Lett.* **2003**, *13*, 45–47. [CrossRef]

23. Zhang, X.; Yan, J.; Shi, Y.; Dai, F.F. A 2.4GHz Power Amplifier Driver used in a WLAN IEEE 802.11b/g Transmitter Front-End. In Proceedings of the 2008 4th IEEE International Conference on Circuits and Systems for Communications (ICCSC 2008), Shanghai, China, 26–28 May 2008; pp. 55–59. [CrossRef]

24. Fritzin, J. Power Amplifier Circuits in CMOS Technologies. Ph.D. Thesis, Linköping University, Linköping, Sweden, 2009.

25. An, K.H. CMOS RF Power Amplifiers for Mobile Wireless Communications. Ph.D. Thesis, Georgia Institute of Technology, Atlanta, GA, USA, 2009.

26. Sarwar, A. *CMOS power Consumption and CPD Calculation*; Texas Instruments Incorporated: Dallas, TX, USA, 1997.

27. Lee, O. High Efficiency Switching CMOS Power Amplifiers for Wireless Communications. Ph.D. Thesis, Georgia Institute of Technology, Atlanta, GA, USA, 2009.

28. Choi, H.; Jung, H.; Shung, K.K. Power Amplifier Linearizer for High Frequency Medical Ultrasound Applications. *J. Med. Boil. Eng.* **2015**, *35*, 226–235. [CrossRef]

29. Sokal, N.O. RF power amplifiers, classes A through S-how they operate, and when to use each. In Proceedings of the IEEE Professional Program Proceedings. Electronic Industries Forum of New England, Boston, MA, USA, 6–8 May 1997; pp. 179–252. [CrossRef]

30. Samal, L.; Mahapatra, K.K.; Raghuramaiah, K. Class-C power amplifier design for GSM application. In Proceedings of the 2012 International Conference on Computing, Communication and Applications, Tamilnadu, India, 22–24 February 2012; pp. 1–5. [CrossRef]

31. Cai, W.; Huang, L.; Wang, S. Class D Power Amplifier for Medical Application. *Inf. Eng. Int. J.* **2016**, *4*, 9–15. [CrossRef]

32. Ma, L.; Zhou, J.; Yu, Z. Design of a class-F power amplifier with expanding bandwidth. In Proceedings of the 2015 Asia-Pacific Microwave Conference (APMC), Nanjing, China, 6–9 December 2015; pp. 1–3. [CrossRef]

33. Ding, Y.; Harjani, R. A high-efficiency CMOS +22-dBm linear power amplifier. *IEEE J. Circuits* **2005**, *40*, 1895–1900. [CrossRef]

34. Saari, V.; Juurakko, P.; Ryynänen, J.; Halonen, K. Integrated 2.4 GHz class-E CMOS power amplifier. In Proceedings of the IEEE Radio Frequency Integrated Circuits Symposium, Long Beach, CA, USA, 12–14 June 2005; pp. 645–648. [CrossRef]

35. Sira, D.; Thomsen, P.; Larsen, T. A cascode modulated class-E power amplifier for wireless communications. *Microelectron. J.* **2011**, *42*, 141–147. [CrossRef]

36. Fouad, H.; Zekry, A.H.; Fawzy, K. Self-Biased 0.13 μm CMOS 2.4-GHz Class E Cascode Power Amplifier. In Proceedings of the 26th National Radio Science Conference, New Cairo, Egypt, 17–19 March 2009; pp. 1–12.

37. Murad, S.A.Z.; Pokharel, R.K.; Kanaya, H.; Yoshida, K.; Nizhnik, O. A 2.4-GHz 0.18-μm CMOS Class E single-ended switching power amplifier with a self-biased cascode. *AEU Int. J. Electron. Commun.* **2010**, *64*, 813–818. [CrossRef]

38. Hong, J.; Imanishi, D.; Okada, K.; Matsuzawa, A. A 2.4 GHz fully integrated CMOS power amplifier using capacitive cross-coupling. In Proceedings of the 2010 IEEE International Conference on Wireless Information Technology and Systems, Honolulu, HI, USA, 28 August–3 September 2010; pp. 1–4. [CrossRef]

39. Luo, S.; Potomac, M. Simple Self-Biased Cascode Amplifier Circuit. U.S. Patent Application Publication US20040085130A1, 6 May 2004.

40. Kiumarsi, H.; Mizuochi, Y.; Ito, H.; Ishihara, N.; Masu, K. A Three-Stage Inverter-Based Stacked Power Amplifier in 65 nm Complementary Metal Oxide Semiconductor Process. *Jpn. J. Appl. Phys.* **2012**, *51*, 2. [CrossRef]

41. Ho, K.-W.; Luong, H.C. A 1-V CMOS power amplifier for bluetooth applications. *IEEE Trans. Circuits Syst. II Briefs* **2003**, *50*, 445–449. [CrossRef]

42. Lee, C.; Park, C. 2.4 GHz CMOS Power Amplifier with Mode-Locking Structure to Enhance Gain. *Sci. J.* **2014**, *2014*, 5–10. [CrossRef]

43. Ghorbani, A.R.; Ghaznavi-Ghoushchi, M.B. A 35.6dB, 43.3% PAE class E differential power amplifier in 2.4GHz with cross coupling neutralization for IoT applications. In Proceedings of the 24th Iranian Conference on Electrical Engineering (ICEE), Shiraz, Iran, 10–12 May 2016; pp. 490–495. [CrossRef]

44. Zhuo, W.; Li, X.; Shekhar, S.; Embabi, S.; De Gyvez, J.; Allstot, D.; Sanchez-Sinencio, E. A capacitor cross-coupled common-gate low-noise amplifier. *IEEE Trans. Circuits Syst. II Briefs* **2005**, *52*, 875–879. [CrossRef]

45. Asada, H.; Matsushita, K.; Bunsen, K.; Okada, K.; Matsuzawa, A. A 60GHz CMOS power amplifier using capacitive cross-coupling neutralization with 16% PAE. In Proceedings of the 41st European Microwave Conference (EuMC 2011), Manchester, UK, 10–13 October 2011; pp. 1115–1118.

46. An, K.H.; Lee, D.H.; Lee, O.; Kim, H.; Han, J.; Kim, W.; Lee, C.-H.; Kim, H.; Laskar, J. A 2.4 GHz Fully Integrated Linear CMOS Power Amplifier With Discrete Power Control. *IEEE Microw. Wirel. Compon. Lett.* **2009**, *19*, 479–481. [CrossRef]

47. Lee, T.H. *The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd ed.; Cambridge University Press (CUP): Cambridge, UK, 2003.

48. Ren, Z.; Zhang, K.; Liu, L.; Li, C.; Chen, X.; Liu, D.; Liu, Z.; Zou, X. On-chip power-combining techniques for watt-level linear power amplifiers in 0.18 μm CMOS. *J. Semicond.* **2015**, *36*, 95002. [CrossRef]

49. An, K.H.; Lee, O.; Kim, H.; Lee, D.H.; Han, J.; Yang, K.S.; Kim, Y.; Chang, J.J.; Woo, W.; Lee, C.-H.; et al. Power-Combining Transformer Techniques for Fully-Integrated CMOS Power Amplifiers. *IEEE J. Circuits* **2008**, *43*, 1064–1075. [CrossRef]

50. Ezzulddin, A.S.; Jasim, S.H. Design of RF Power Amplifiers using Parallel-Series Power Combining Transformers. *Eng. Technol. J.* **2015**, *33*, 294–307.

51. Mazzanti, A.; Larcher, L.; Brama, R. Analysis of reliability and power efficiency in cascode class-E Pas. *IEEE J. Solid-State Circ.* **2006**, *41*, 1222–1229. [CrossRef]

52. Mandal, P.; Viisvanathan, V. A Self-Biased High Performance Folded Cascode CMOS Op-Amp. In Proceedings of the 10th International Conference on VLSI Design, Hyderabad, India, 4–7 January 1997; pp. 429–434. [CrossRef]

53. Tsai, K.C.; Gray, P.R. A 1.9GHz 1W CMOS Class-E Power Amplifier for Wireless Communications. *IEEE J. Solid-State Circ.* **1999**, *34*, 962–970. [CrossRef]

54. Baek, S.; Ryu, H.; Nam, I.; Jeong, M.; Kim, B.; Lee, O. A 2.4-GHz CMOS Power Amplifier with Parallel-Combined Transistors and Selective Adaptive Biasing for Wireless Lan Applications. *Microw. Opt. Technol. Lett.* **2016**, *58*, 1374–1377. [CrossRef]

55. Yoo, J.; Lee, C.; Kang, I.; Son, M.; Sim, Y.; Park, C. 2.4-GHz CMOS Linear Power Amplifier for IEEE 802.11N WLAN Applications. *Microw. Opt. Technol. Lett.* **2017**, *59*, 546–550. [CrossRef]