

Article

A High-Efficiency K-band MMIC Linear Amplifier Using Diode Compensation

Heng Zhu, Wei Chen *, Jianhua Huang, Zhiyu Wang and Faxin Yu

School of Aeronautics and Astronautics, Zhejiang University, Hangzhou 310027, China; hzhu_zju@zju.edu.cn (H.Z.); oscarhua@zju.edu.cn (J.H.); zywang@zju.edu.cn (Z.W.); fxyu@zju.edu.cn (F.Y.)

* Correspondence: cwydl@zju.edu.cn; Tel.: +86-1876-847-9949

Received: 12 April 2019; Accepted: 29 April 2019; Published: 30 April 2019



Abstract: This paper describes the design and measured performance of a high-efficiency and linearity-enhanced K-band MMIC amplifier fabricated with a 0.15 μm GaAs pHEMT processing technology. The linearization enhancement method utilizing a parallel nonlinear capacitance compensation diode was analyzed and verified. The three-stage MMIC operating at 20–22 GHz obtained an improved third-order intermodulation ratio (IM3) of 20 dBc at a 27 dBm per carrier output power while demonstrating higher than a 27 dB small signal gain and 1-dB compression point output power of 30 dBm with 33% power added efficiency (PAE). The chip dimension was 2.00 mm \times 1.40 mm.

Keywords: high-efficiency; K-band; linearity enhancement; power amplifier; GaAs pHEMT; diode compensation

1. Introduction

GaAs MMIC is regarded as the premier power device for the microwave communication system [1] and phase array radar system [2] witnessed in recent decades. However, when facing high peak-to-average ratio (PAR) modulation schemes such as QPSK and OFDM, the nonlinearity of the power amplifier causes spectral reproduction and intermodulation distortion. When multi-signals are amplified within a single channel, the beat between carriers generates amplitude modulation [3].

To meet the linearity requirements in the point-to-point radio or satellite communications which usually operate with a high PAR and inconstant enveloped input signal, conventional designs have to work at a back-off output point compared to their saturated power level. Thus, several techniques have been employed to improve the efficiency in the low power region, such as the linear Doherty design, feed-forward technique, and envelop feedback. Some linear Doherty amplifier [4] and feed-forward designs [5] show a high linearity at an acceptable efficiency; however the complexity and cost of chips are not low. Class-J [6] was also reported to achieve a high linearity in the back-off region. Those technologies usually generate a high circuit complexity. Some literature has also reported on the possibility of inner chip nonlinear compensation methods based on diodes [7]. However, no concrete MMIC design has been proposed.

This paper presents a high-efficiency K-band MMIC linear power amplifier fabricated with a 0.15 μm GaAs pHEMT processing technology. A kind of linearizer circuit of diode nonlinear compensation was accomplished. The Y-parameter matrix method was used to analyze and deduce the dynamic characteristic of the parallel diode and FET network. Both simulation and measurement results show the linearity improvement of the circuit. As a result, the proposed linear amplifier achieved an excellent performance with more than a 1 W output power and 33% power-added efficiency at the 1-dB compression point while maintaining an IM3 better than 20 dBc at an output power of 27 dBm per carrier over a 20–22 GHz band.

2. Nonlinear Analysis and Diode Compensation

Table 1 shows the main parameter of the 0.15 μm GaAs pHEMT process. The equivalent circuit models of pHEMT and a diode are shown in Figure 1.

Table 1. The parameters of the 0.15 μm GaAs pHEMT process.

Parameter	Value	Parameter	Value
V_{TH} (V)	-1.2	f_t (GHz)	85
V_{BDG} (V)	10	Gm_Peak (mS/mm)	495
I_{dmax} (mA/mm)	650	$P_{density}$ (W/mm)	0.8
I_{dss} (mA/mm)	500	C_{MIM} (pF/mm ²)	400

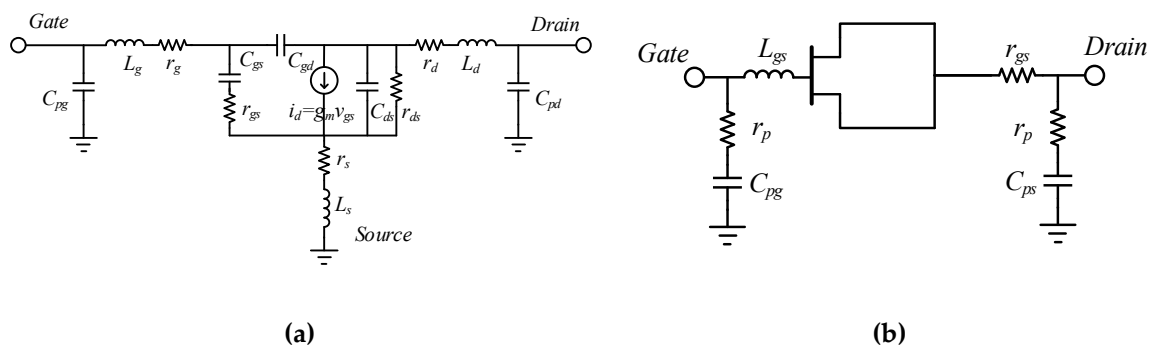


Figure 1. (a) The equivalent circuit model of pHEMT; (b) the equivalent circuit model of a diode.

Using a diode depletion capacitance model [8], the values of C_{gs} and C_{gd} can be derived as

$$C_{gs}(v_{gs}) = \frac{C_{gsb}}{\sqrt{1 - \frac{v_{gs}}{v_{bi}}}} \tag{1}$$

$$C_{gd}(v_{gd}) = \frac{C_{gdb}}{\sqrt{1 - \frac{v_{gd}}{v_{bi}}}} \tag{2}$$

The functional model of a single-stage pHEMT amplifier can be represented by Figure 2.

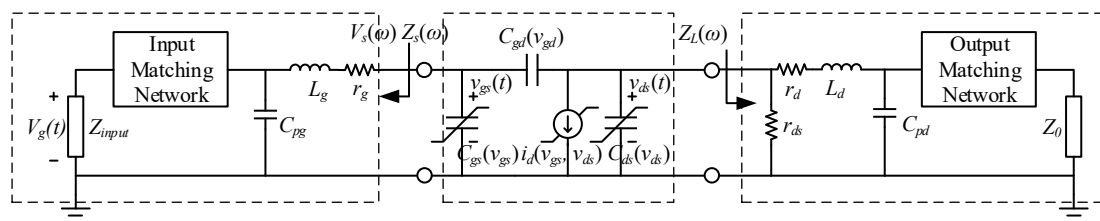


Figure 2. Single-stage pHEMT amplifier model.

In this model, $V_S(\omega)$ and $Z_S(\omega)$ constitute the Thevenin equivalent of the excitation source and the input matching network, and $Z_L(\omega)$ is the load impedance of the pHEMT. Assuming that the pHEMT is excited by a voltage, $v_{gs}(A, t)$:

$$v_{gs}(A, t) = \sum_0^n V_{gsk}(A, \omega) \cdot \cos(k\omega_0 t) \tag{3}$$

where V_{gsk} represents the Fourier components of v_{gs} and A is the amplitude. By setting the dynamic charge between the gate and source determined by v_{gs} as Q_{gs} , i_{gs} can be derived as

$$i_{gs}(t) = \frac{\partial Q_{gs}[v_{gs}]}{\partial t} = C_{gs}[v_{gs}] \cdot \frac{\partial v_{gs}}{\partial t} \tag{4}$$

Then, we get the frequency domain representation of i_{gs} as

$$I_{gs} = \left[\frac{1}{2} \sum_{-n}^n C_{gsk}(V_{gs}, \omega) \right] \cdot \left[\frac{1}{2} \sum_{-n}^n jk\omega_0 V_{gsk} \right] \tag{5}$$

where C_{gsk} is the Fourier components of C_{gs} :

$$C_{gsk} = \frac{\omega}{2\pi} \int_{-\pi/\omega}^{\pi/\omega} C_{gs}[v_{gs}] \cdot e^{-jk\omega t} dt \tag{6}$$

Substituting (R4) into (R3), the fundamental component of i_{gs} would be

$$I_{gs1} = j\omega_0 C_{gs0} V_{gs1} + \frac{1}{2} j2\omega_0 C_{gs1}^* \cdot V_{gs2} - \frac{1}{2} j\omega_0 C_{gs2} \cdot V_{gs1}^* + \dots \tag{7}$$

As a result, the fundamental $v_{gs}(t)$ voltage V_{gs1} (A) can be derived as

$$V_{gs1} = V_S(\omega) - j\omega Z_s(\omega) \{ C_{gs0} \cdot V_{gs1} + C_{gs1}^* \cdot V_{gs2} - \frac{1}{2} C_{gs2} \cdot V_{gs1}^* + \dots \} \tag{8}$$

and solving (8) leads to

$$V_{gs1} = \frac{V_s(\omega)}{1 + j\omega Z_s(\omega) \cdot C_{gs0}} \tag{9}$$

The term involving C_{gs2} and V_{gs2} is neglected as it is significantly smaller than the others. Incorporating the feedback capacitor C_{gd} into (9), we get

$$V_{gs1} = \frac{V_s(\omega)}{1 + j\omega Z_s(\omega) \cdot [C_{gs0} + C_{gd}(1 - A_v)]} \tag{10}$$

(10) reveals that C_{gs} and C_{gd} influence the phase of fundamental $v_{gs}(t)$, which leads to AM/PM distortion. Using a similar method, we can derive the fundamental $v_{ds}(t)$ voltage V_{ds1} (A) as

$$V_{ds1}(A) \approx \frac{Z_L(\omega) \cdot I_{d1}(A)}{1 + j\omega Z_L(\omega) \cdot [C_{ds0}(A) + C_{gd}(\frac{A_v - 1}{A_v})]} \tag{11}$$

The term involving C_{ds2} is neglected as it is significantly smaller than the others. Since the denominator of (11) is approximately equal to unity [9], as a result, there is no significant impact on AM/PM brought about by C_{ds} . From (10) and (11), it can be derived that the main contributors to the AM/PM distortion are the variations of C_{gs} and C_{gd} . According to the barrier capacitance effect, the value of C_{gs} is usually much bigger than that of C_{gd} . Therefore, the nonlinear characteristic of pHEMT is mainly contributed by C_{gs} , which approximately equals C_{in} . As shown in Figure 3, a Schottky diode is parallel in the gate and the drain of the output stage FET to compensate for the nonlinearity of C_{gs} .

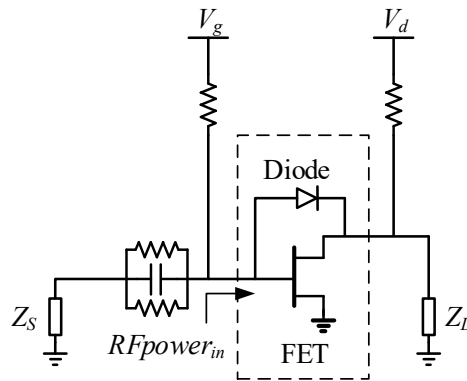


Figure 3. Paralleled Shottky diode linearizer.

The voltage between the reverse diode is

$$v_{diode} = v_{ds} - v_{gs} \tag{12}$$

The two-port Y-parameter matrix can be utilized to analyse the parallel network composed of the FET and diode. The matrix form of FET is as follows:

$$\begin{bmatrix} i_g \\ i_d \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} v_{gs} \\ v_{ds} \end{bmatrix} \tag{13}$$

where

$$y_{11} = \frac{j\omega C_{gs}}{1 + j\omega C_{gs} r_{gs}} + j\omega C_{gd} \tag{14}$$

$$y_{12} = -j\omega C_{gd} \tag{15}$$

$$y_{21} = \frac{g_m}{1 + j\omega C_{gs} R_{gs}} - j\omega C_{gd} \tag{16}$$

$$y_{22} = \frac{1}{r_{ds}} + j\omega(C_{ds} + C_{gs}) \tag{17}$$

Incorporating the diode barrier capacitance into the matrix,

$$y_{11}' = \frac{j\omega C_{gs}}{1 + j\omega C_{gs} r_{gs}} + j\omega(C_{gd} + C_{diode}) \tag{18}$$

$$C_{in}' = -\frac{1}{\omega \text{Im}\left(\frac{1}{y_{11}'}\right)} \tag{19}$$

C_{in}' represents the input capacitance of the network. According to the previous analysis, the state of input capacitance mainly determines the nonlinear characteristics of the network. Thus, it is possible to perform distortion compensation utilizing the high-frequency C-V characteristic of the diode. As $v_{diode} < 0$, C_{diode} is dominated by depletion layer capacitance C_j , where

$$C_j = \frac{C_{j0}}{\sqrt{1 - \frac{v_{diode}}{\Phi_B}}} \tag{20}$$

where Φ_B is the junction built-in potential, so

$$C_{in}' = \frac{[\omega C_{gs} R_{gs} (C_{gd} + C_j)]^2 + (C_{gs} + C_{gd} + C_j)^2}{(\omega C_{gs} R_{gs})^2 (C_{gd} + C_j) - (C_{gs} + C_{gd} + C_j)} \tag{21}$$

As the input RF power increases, the electric field within the FET channel is enhanced, which makes the swing of both v_{gs} and v_{ds} become higher. However, the negative swing of v_{ds} is limited by the knee voltage (V_{knee}) and the positive swing of v_{gs} is limited by the diffusion barrier voltage (V_{diff}). As a result, \bar{v}_{ds} grows higher while \bar{v}_{gs} grows lower. Consequently, \bar{v}_{diode} (3) becomes higher while \bar{v}_{gs} becomes lower. The voltage waveform versus input RF power is shown in Figure 4.

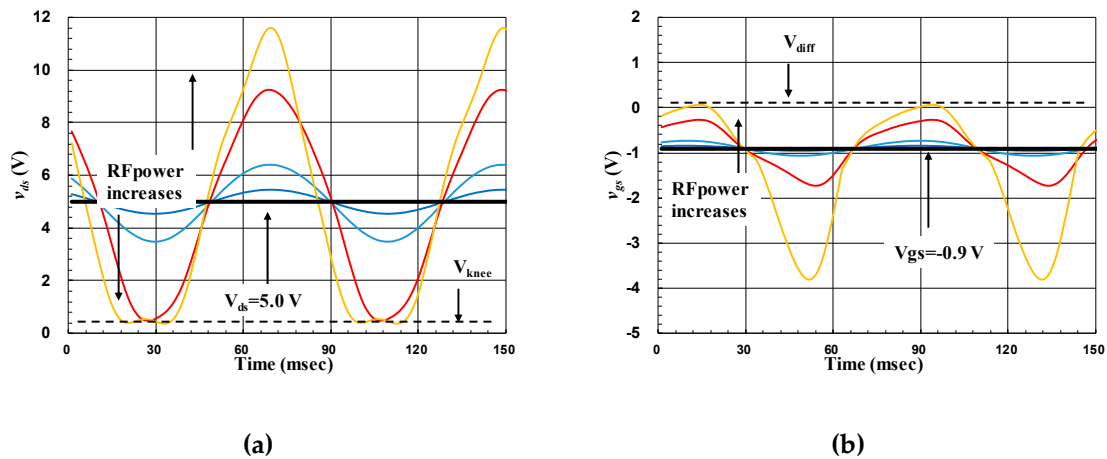


Figure 4. (a) Voltage waveform of v_{ds} ; (b) voltage waveform of v_{gs} .

Therefore, substituting (1), (2), and (20) into (21) and combining the voltage analysis above, the characteristics of input capacitance can be shown as the curve in Figure 5.

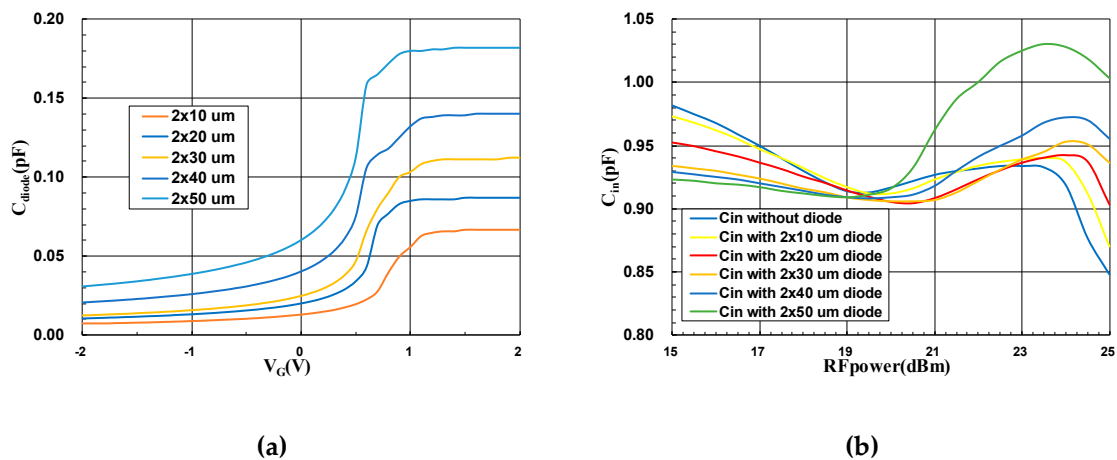


Figure 5. (a) C-V characteristics of the two-finger diode; (b) input capacitance of the network versus RF power.

The principles for the choice of diode periphery are as follows.

1. The size of the diode should be large enough to compensate for the input capacitance of the pHEMT as the input power increases;
2. The barrier capacitance of the diode should not be too large to over change the input characteristics of the HMET and generate excessive feedback between drain and gate.

Figure 6 shows that as the size of diode increases, the additional feedback becomes stronger. As a result, the MaxGain of the network decreases, which leads to lower linear gain. Therefore, combined with the C-V characteristics of the diode shown in Figure 5a, we gradually adjusted the diode size so that it could effectively compensate for the input capacitance of pHEMT while reducing the effect

on the gain. The C-V characteristics of the selected $2 \times 20 \mu\text{m}$ diode and the input capacitance of the network versus RF power are shown in Figure 7.

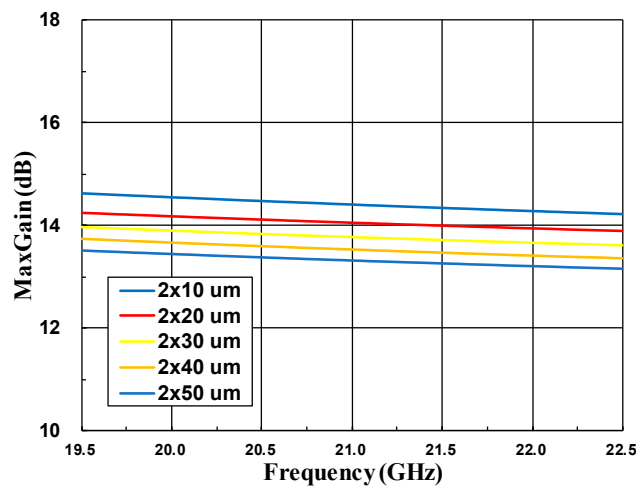


Figure 6. The influence of the diode size on the MaxGain of the network.

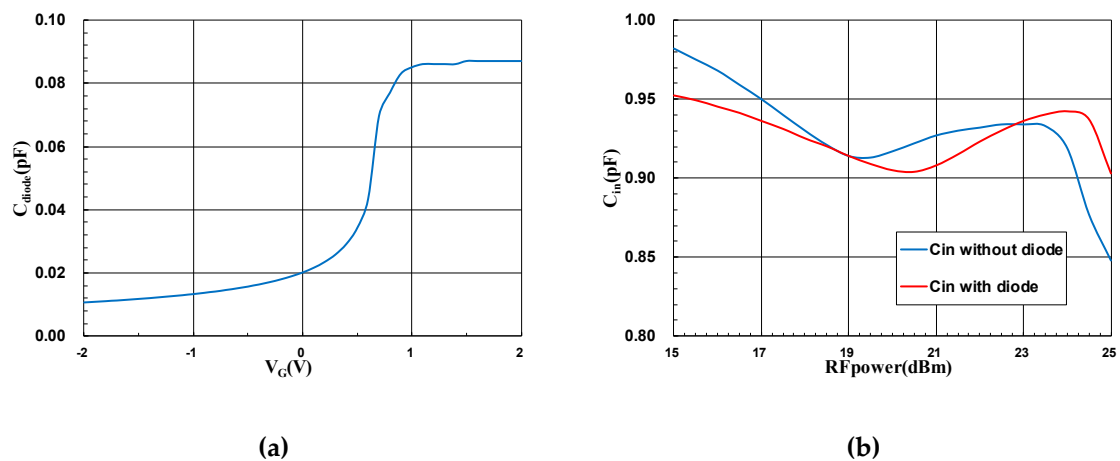


Figure 7. (a) C-V characteristics of the $2 \times 20 \mu\text{m}$ diode; (b) input capacitance of the network versus RF power (Behavior of $2 \times 20 \mu\text{m}$ diode and $8 \times 100 \mu\text{m}$ FET).

The parasitic parameter value of the selected pHEMT and diode is shown in Tables 2 and 3, respectively.

Table 2. The parasitic parameter value of the $8 \times 100 \mu\text{m}$ pHEMT

Parameter	Value	Parameter	Value
$r_g (\Omega)$	1.5	$L_d (\text{pH})$	8.5
$r_d (\Omega)$	1.2	$L_s (\text{pH})$	0.7
$r_s (\Omega)$	0.2	$C_{pg} (\text{fF})$	9.5
$L_g (\text{pH})$	9.5	$C_{pd} (\text{fF})$	17.5

Table 3. The parasitic parameter value of the $2 \times 20 \mu\text{m}$ diode

Parameter	Value
$r_{gs} (\Omega)$	41.5
$C_{pg} (\text{fF})$	89.0
$C_{ps} (\text{fF})$	33.5
$L_{gs} (\text{pH})$	55.0

Converting (7) to the S-parameter matrix:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \quad (22)$$

where

$$S_{11} = \frac{(1 - Z_0 y_{11})(1 + Z_0 y_{22}) + y_{12} y_{21} Z_0^2}{\Psi} \quad (23)$$

$$S_{12} = \frac{-2Y_{12}Z_0}{\Psi} \quad (24)$$

$$S_{21} = \frac{-2Y_{21}Z_0}{\Psi} \quad (25)$$

$$S_{22} = \frac{(1 + Z_0 y_{11})(1 - Z_0 y_{22}) + y_{12} y_{21} Z_0^2}{\Psi} \quad (26)$$

$$\Psi = (1 + Z_0 y_{11})(1 + Z_0 y_{22}) - y_{12} y_{21} Z_0^2 \quad (27)$$

Using the S-parameter to derive the stability factor of the network:

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}||S_{21}|} \quad (28)$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \quad (29)$$

The factor $k > 1$ is a necessary and sufficient condition for network stability. Since the diode compensation method generates additional feedback between the gate and drain, the stability of the network is enhanced compared with single FET. The conclusion can be verified by calculation or simulation. The simulation result of the stability factor is shown in Figure 8.

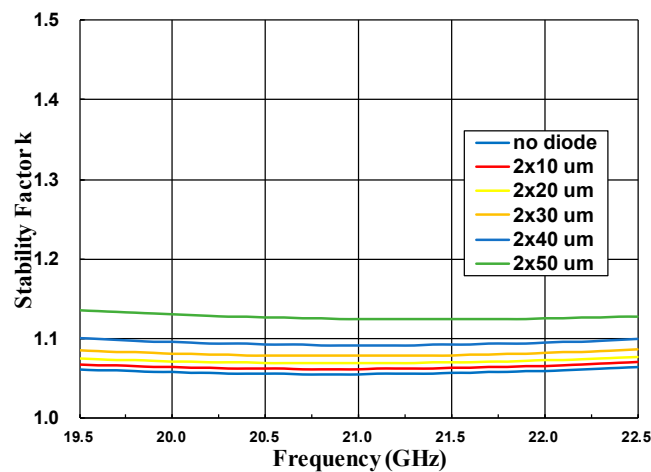


Figure 8. The influence of the diode size on the stability factor of the network.

Consequently, because of the nonlinear effect of the diodes, the input capacitance of the network is compensated for as the input power increases, thus avoiding the degradation of linearity. As the diode is operated in an inverted connection, there is nearly no additional current or power loss in the circuit.

3. Circuit Design

The K-band MMIC linear amplifier is composed of three-stage FETs fabricated with a 0.15 μm gate length AlGaAs/GaAs pHEMT technology. The process exhibits a gate-drain breakdown voltage of 16.5 V and a cutoff frequency (f_T) of 90 GHz. The FETs for the power stage are $8 \times 100 \mu\text{m}$. Source-pull and load-pull simulations using a large signal model at a center frequency were taken to

determine the optimal input and output impedances that lead to a higher output power and efficiency. The output matching network combining two FETs matches the fundamental load impedance based on the load-pull simulation. The interstage and input matching networks are designed to match the conjugated impedance and were optimized for low loss. The circuit of the amplifier configuration is shown in Figure 9. The simulation result of the amplifier is shown in Figures 10 and 11.

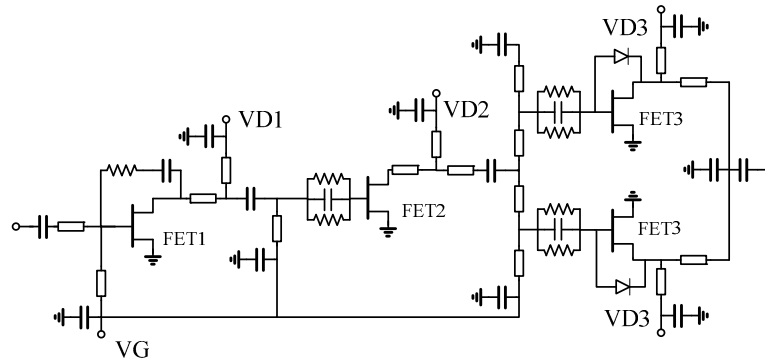


Figure 9. Schematic of the MMIC linear amplifier.

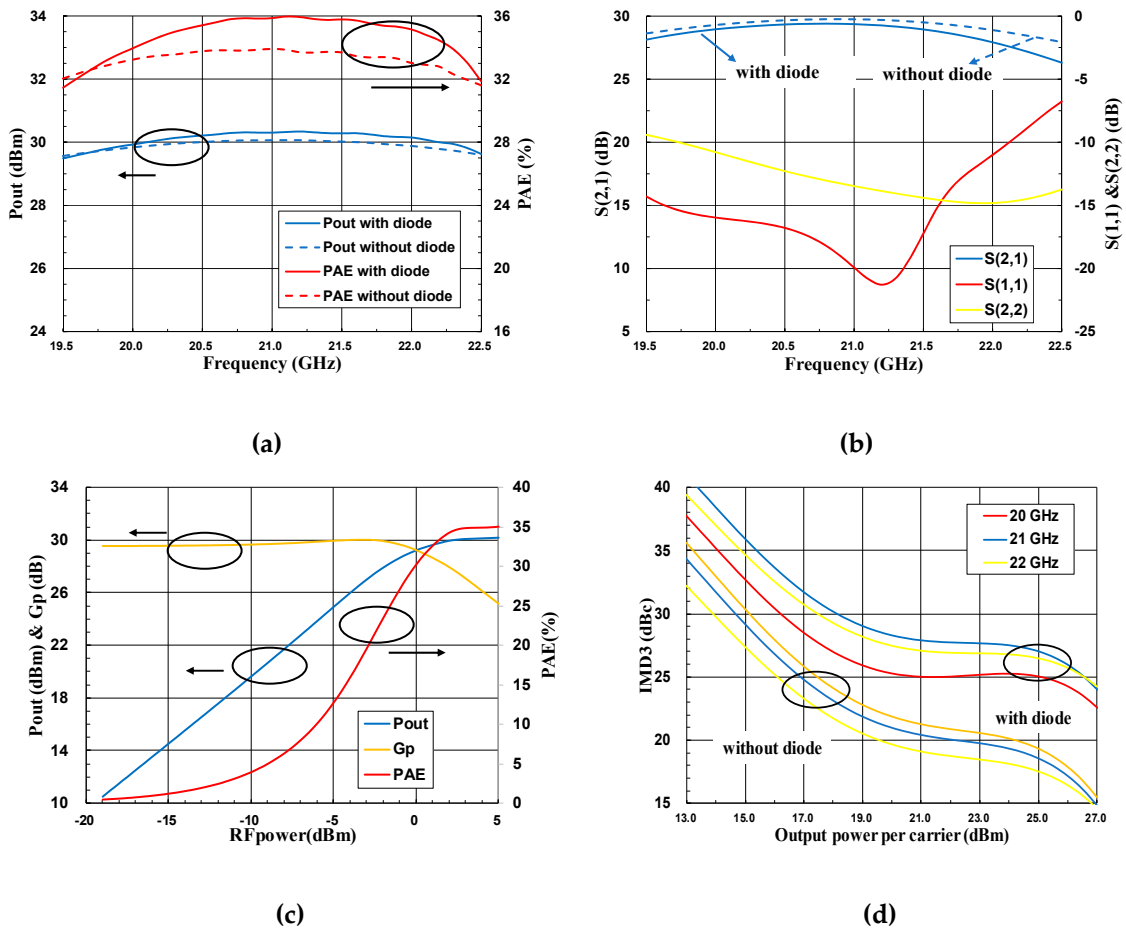


Figure 10. (a) Simulated output power and PAE versus frequency at a 3 dBm input power; (b) simulated S-parameter versus frequency; (c) simulated output power, gain, and PAE versus input power at a 21 GHz frequency; (d) simulated IMD3 and PAE versus output power.

Figures 10 and 11 show the improvement of the amplifier linearity performance generated by the parallel diode circuit design.

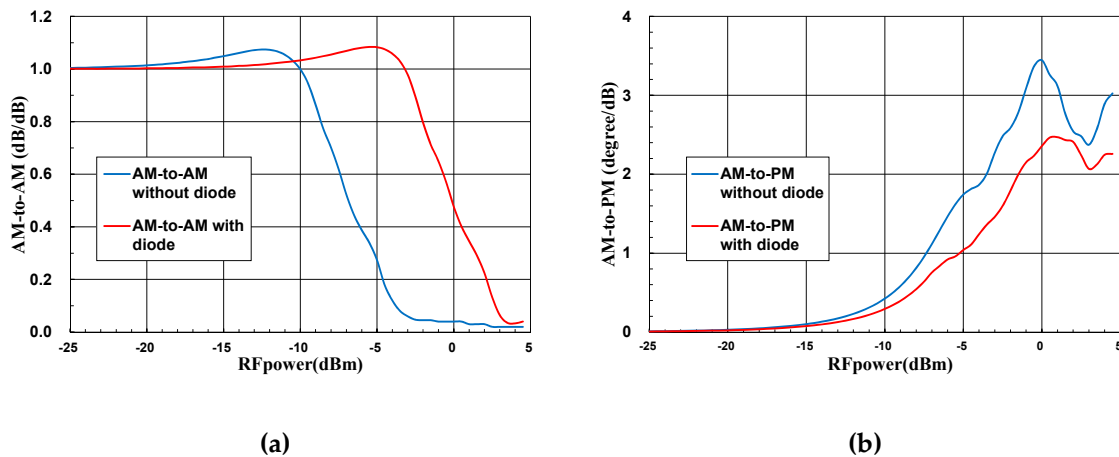


Figure 11. (a) Simulated AM-to-AM versus input power at 21 GHz; (b) simulated AM-to-PM versus input power at 21 GHz.

4. Measurement Results

The fabricated three-stage K-band linear amplifier MMIC is shown in Figure 12. The MMIC size is as small as $2.00 \times 1.40 \text{ mm}^2$ with a GaAs substrate thickness of $50 \mu\text{m}$. Linear S-parameter and large signal measurements were performed at a drain voltage of 5 V and gate voltage of -0.8 V on a wafer. Figure 13 shows the measured S-parameter of the MMIC from 19.5 GHz to 22.5 GHz. The design has achieved higher than a 26 dB small signal gain and better than a 10 dB input return loss. Figure 14 illustrates the measured output power and PAE for the amplifier at fixed input drive levels of +3.5 dBm under a continuous wave (CW). At the nominal supply of $V_D = 5 \text{ V}$ and $V_G = -0.8 \text{ V}$, the amplifier demonstrates higher than 30 dBm P1dB with 33–35% PAE over a 20–22 GHz frequency. Very flat power and gain characteristics were achieved for this design. Further PAE improvement should be possible with a more precise power match by the result of a load-pull test.

Two-tone measurement of the amplifier has been performed with 10 MHz tone spacing under the drain voltage of 5 V and gate voltage of -0.8 V . The intermodulation distortion was measured on a wafer with 10 MHz two-tone spacing. The two carrier sources were connected to the chip through a power combiner with an isolator in order to reduce the intermodulation contributions of the setup. As shown in Figure 15, IMD3 better than 20 dBc and PAE higher than 33% were measured at an output power of 27 dBm per carrier over a 20–22 GHz band. Compared to the design without an inner paralleled diode configuration, there is more than a 5dB improvement of IMD3. Table 4 summarizes the performance comparison of this work with other published linear amplifiers working in close frequency ranges. The characteristics of the amplifier, including power, gain, efficiency, and IMD3, are better than the previously reported ones.

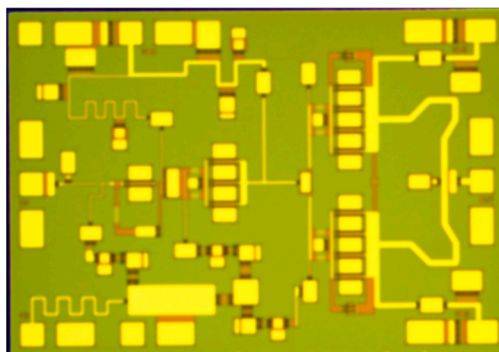


Figure 12. Photograph of the fabricated K-band linear amplifier.

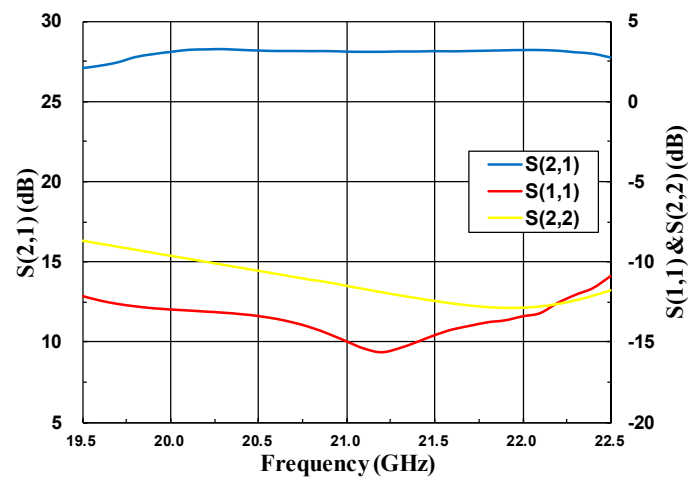


Figure 13. Measured small-signal performance of the amplifier under the bias of $V_D = 5$ V and $V_G = -0.8$ V at 25 Celsius.

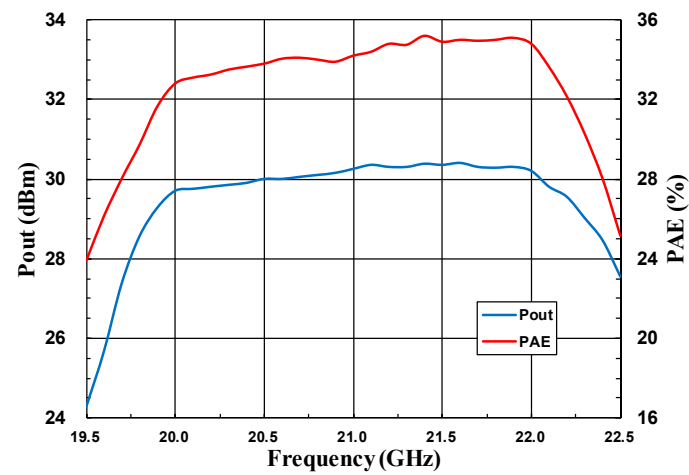


Figure 14. Measured output power and PAE at 1 dB compression.

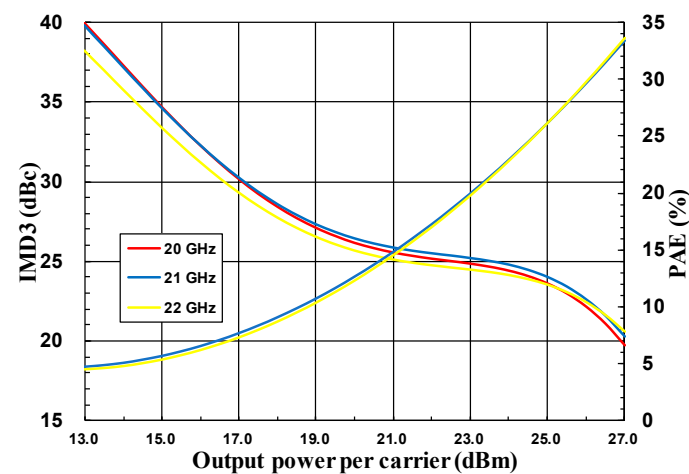


Figure 15. Measured IMD3 and PAE versus output power under a two-tone test with different frequencies.

Table 4. Performance comparison of linear amplifiers.

Reference	Process	Frequency (GHz)	P _{-1dB} (dBm)	PAE (%)	Gain (dB)	IMD3 (dBc)	Size (mm ²)
[10]	0.15 μ m GaAs	20–23	31	24	9.5	-	-
[11]	0.25 μ m GaAs	22.8–23.5	28	15.3	25	-	2.52
[12]	0.25 μ m GaAs	18–27	31.4	27	14	18	3.91
[13]	0.15 μ m GaAs	17–20	28	30	21	14	2.96
[14]	0.15 μ m GaAs	24–28	28	21	21	15	4.50
This work	0.15 μ m GaAs	20–22	30	34	27	20	2.80

5. Conclusions

In this paper, a three-stage K-band 20–22 GHz high-efficiency linear MMIC power amplifier using 0.15 μ m GaAs pHEMT technology is reported. The design utilizes an optimum paralleled diode circuit for inner chip linear compensation. The MMIC generates an output power of 30 dBm and PAE of 33% at -1 dB gain compression under CW operation and delivers a lower than -20 dBc IMD3 performance with 10 MHz tone spacing. The MMIC has a smaller size and more than a 5dB improvement of IMD3 was observed.

Author Contributions: Methodology, H.Z.; Software, J.H.; Validation, J.H.; Data Curation, H.Z.; Writing: Original Draft Preparation, H.Z.; Writing: Review and Editing, W.C.; Supervision, W.C.; Project Administration, Z.W.; Funding Acquisition, F.Y.

Funding: This research was funded by the National Natural Science Foundation of China grant number 61604128 and the Fundamental Research Funds for the Central Universities grant number 2017QN81002.

Acknowledgments: The authors would like to thank the Institute of Aerospace Electronics Engineering of Zhejiang University for providing the research platform and technical support.

Conflicts of Interest: The authors declare no conflict of interest.

References

- Camarchia, V.; Guerrieri, S.D.; Ghione, G.; Pirola, M.; Quaglia, R.; Rubio, J.M.; Loran, B.; Palomba, F.; Sivverini, G. A K-band GaAs MMIC Doherty power amplifier for point-to-point microwave backhaul applications. In Proceedings of the 2014 International Workshop on Integrated Nonlinear Microwave and Millimetre-wave Circuits (INMMiC), Leuven, Belgium, 2–4 April 2014. [\[CrossRef\]](#)
- Lane, A.; Jenkins, J.; Green, C.; Myers, F. S and C band GaAs multifunction MMICs for phased array radar. In Proceedings of the 11th Annual Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, San Diego, CA, USA, 22–25 October 1989; pp. 259–262. [\[CrossRef\]](#)
- Simons, K.A. The decibel relationships between amplifier distortion products. *Proc. IEEE* **1970**, *58*, 1071–1086. [\[CrossRef\]](#)
- Cho, K.-J.; Kim, W.-J.; Kim, J.-H.; Stapleton, S.P. Linearity optimization of a high power Doherty amplifier based on post-distortion compensation. *IEEE Microw. Wireless Compon. Lett.* **2005**, *15*, 748–750. [\[CrossRef\]](#)
- Roy, M.K. Distortion cancellation performance of miniature delay filters for feed-forward linear power amplifiers. *IEEE Trans. Ultrason. Ferroelectr. Freq. Control* **2002**, *49*, 1592–1595. [\[CrossRef\]](#)
- Wright, P.; Lees, J.; Benedikt, J.; Tasker, P.J.; Cripps, S.C. A methodology for realizing high efficiency class-J in a linear and broadband PA. *IEEE Trans. Microw. Theory Techn.* **2009**, *57*, 3196–3204. [\[CrossRef\]](#)
- Mrunal, A.K.; Shirasgaonkar, M.; Patrikar, R.M. Power amplifier linearization using a diode. In Proceedings of the MELECON 2006–2006 IEEE Mediterranean Electrotechnical Conference, Malaga, Spain, 16–19 May 2006; pp. 173–176. [\[CrossRef\]](#)
- Wren, M.; Brazil, T.J. The effect of the gate Schottky diode on pHEMT power amplifier performance. In Proceedings of the 2003 High Frequency Postgraduate Student Colloquium, Belfast, Ireland, 8–9 September 2003; pp. 52–55. [\[CrossRef\]](#)
- Nunes, L.C.; Cabral, P.M.; Pedro, J.C. A Physical Model of Power Amplifiers AM/AM and AM/PM Distortions and Their Internal Relationship. In Proceedings of the 2013 IEEE MTT-S International Microwave Symposium Digest (MTT), Seattle, WA, USA, 2–7 June 2013. [\[CrossRef\]](#)

10. Fersch, T.; Quaglia, R.; Pirola, M.; Camarchia, V.; Ramella, C.; Khoshkholgh, A.J.; Ghione, G.; Weigel, R. Stacked GaAs pHEMTs: design of a K-band power amplifier and experimental characterization of mismatch effects. In Proceedings of the 2015 IEEE MTT-S International Microwave Symposium, Phoenix, AZ, USA, 17–22 May 2015; pp. 1–4. [[CrossRef](#)]
11. Koo, B.; Park, C.; Lee, K.A.; Chun, J.H.; Hong, S. A 28-dBm pHEMT Power Amplifier Using Voltage Combiner for K-Band Applications. In Proceedings of the 38th European Microwave Conference, Amsterdam, Netherlands, 27–31 October 2008. [[CrossRef](#)]
12. Brown, S.A.; Carroll, J.M. Compact, 1 Watt, power amplifier MMICs for K-band applications. In Proceedings of the GaAs IC Symposium, Seattle, WA, USA, 5–8 November 2000.
13. Bessemoulin, A.; McCulloch, M.G.; Alexander, A.; McCann, D.; Mahon, S.J.; Harvey, J.T. Compact K-band watt-level GaAsPHEMT power amplifier MMIC with integrated ESD protection. In Proceedings of the 2006 European Microwave Integrated Circuits Conference, Manchester, UK, 10–13 September 2006.
14. Wang, K.; Yan, Y.; Liang, X. A K-band power amplifier in a 0.15-um GaAs pHEMT process. In Proceedings of the 2018 IEEE MTT-S International Wireless Symposium (IWS), Chengdu, China, 6–10 May 2018; pp. 1–3.



© 2019 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<http://creativecommons.org/licenses/by/4.0/>).