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A CMOS W-Band Amplifier with Tunable Neutralization Using a Cross-Coupled MOS–varactor Pair

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Abstract: This paper presents a CMOS W-band amplifier adopting a novel neutralization technique for high gain and stability. The W-band amplifier consists of four common-source differential gain cells that are neutralized by a cross-coupled MOS–varactor pair. Contrary to conventional neutralizations, the proposed technique enables tunable neutralization, so that the gate-to-drain capacitance of transistors is accurately tracked and neutralized as the varactor voltage is adjusted. This makes the neutralization tolerant of capacitance change caused by process–voltage–temperature (PVT) variation or transistor model inaccuracy, which commonly occurs at mm-wave frequencies. The proposed tunable neutralization is experimentally confirmed by measuring gain and stability of the W-band amplifier fabricated in a 65-nm CMOS process. The amplifier achieves a measured gain of 17.5 dB at 79 GHz and a 3-dB bandwidth from 77.5 to 84 GHz without any stability issue. The DC power consumption is 56.7 mW and the chip area is 0.85 mm^2.

Keywords: CMOS W-band amplifier; tunable neutralization; MOS–varactor; transformer-based impedance matching

1. Introduction

Over the last years, wireless communication technology based on the CMOS process was widely developed in the W-band frequencies. Wireless point-to-point links at 71–76 GHz and 81–86 GHz enable high-speed communication with a data rate of tens of Gbps [1]. In addition to wireless communication, there are several significant W-band applications, such as 77-GHz automotive radar for collision avoidance [2] and 94-GHz imaging for surveillance, security, and medical purposes [3,4]. Currently, owing to the CMOS scaling and advanced device modeling [5,6], silicon-based integrated circuits became popular at millimeter-wave (mm-wave) frequencies [7]. Compared to compound semiconductor technologies, the CMOS technology offers a highly integrative solution with a low cost. However, as frequency increases toward the W-band, CMOS transistors suffer from low gain and poor stability. Several g_m-boosting techniques were proposed to increase gain at mm-wave frequencies [8,9].

Neutralization is one of the most popular techniques for improving both gain and stability [10–14]. An unwanted feedback through gate-to-drain capacitance (C_{gd}) of transistors is canceled by externally connecting a neutralization capacitor that offsets C_{gd} [10–12]. However, since C_{gd} can be changed with process−voltage−temperature (PVT) variation and transistor model inaccuracy, the neutralization capacitor should also be made tunable to track the change of C_{gd} for an optimum neutralization effect. Previously, tunable neutralization was implemented using a varactor [13] and a switched

inductor [14] at 60 GHz and 28 GHz, respectively. Nonetheless, they would suffer from high loss, transistor mismatch, and large chip area consumption.

In this paper, we propose a new tunable neutralization technique using a cross-coupled MOS–varactor pair. A triple-well MOS structure with a body terminal tied to source is employed to have a high Q and excellent matching with main transistors. The neutralization capacitance can be tuned by varying the source terminal voltage. Therefore, the proposed technique is suitable for tunable neutralization at the W-band, showing low loss, good transistor matching, and a small chip area. In Section 2, conventional and proposed neutralization techniques are described in detail. In Section 3, a CMOS W-band amplifier is designed with the proposed tunable neutralization technique. The measurement results are presented in Section 4, followed by conclusions in Section 5.

2. Conventional and Proposed Neutralization Techniques

The maximum available gain (MAG) of a 2 × 12 μm transistor in a bulk 65-nm CMOS technology is shown in Figure 1. The MAG rapidly decreases with frequency and reaches below 7.5 dB at the W-band. One of the main reasons for gain reduction is the degraded reverse isolation of transistors. The MAG and Rollett stability factor (K) are expressed with respect to S-parameters as follows [15]:

$$MAG = \frac{|S_{21}|}{|S_{12}|}(K - \sqrt{K^2 - 1}) \quad (1)$$

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{12}S_{21}|} \quad (2)$$

As reverse isolation decreases, i.e., reverse gain (S_{12}) increases, MAG is lowered in Equation (1). The stability factor in Equation (2) also decreases with larger S_{12}. Therefore, S_{12} should be minimized to improve the MAG and stability. Neutralization is a well-known technique that minimizes S_{12} by canceling out a transistor feedback capacitance (C_{gd}) which is the main cause of S_{12}.

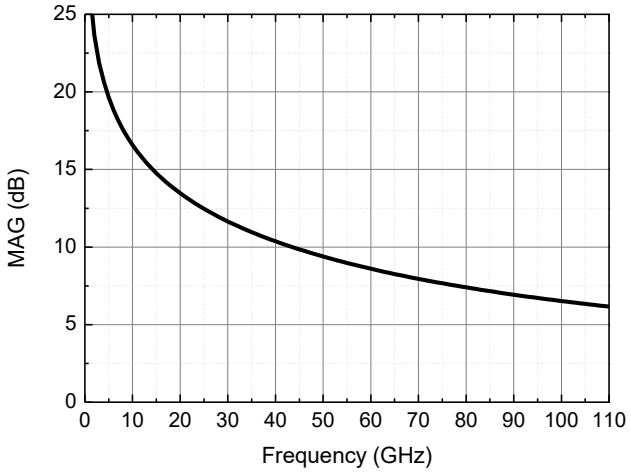


Figure 1. Simulated maximum available gain (MAG) of a 2 × 12 μm transistor in a bulk 65-nm CMOS technology.

2.1. Conventional Neutralization Techniques

A structure of the most conventional neutralization technique is shown in Figure 2. A common-source (CS) differential pair is neutralized by cross-connecting neutralization capacitors (C_n). The transistor feedback capacitance (C_{gd}) is canceled by C_n because the signals across C_{gd} and C_n are out of phase with respect to each other. The improvement of MAG and stability at 79 GHz is shown in Figure 3. Without neutralization (C_n = 0), MAG is only 7.4 dB and K is 0.75, meaning that the transistor pair is conditionally unstable. On the other hand, with neutralization, both MAG and K

increase. The optimum value of C_n is determined in between the peaks of MAG and K, i.e., C_n = 7.5 fF. This leads to MAG of 10.4 dB and K of 1.3, such that the transistor pair becomes unconditionally stable while achieving high gain. The neutralization capacitor is usually implemented in a metal-oxide-metal (MOM) capacitor [10,11] or an MOS capacitor [12]. However, in those conventional cases, C_n is fixed to a single value and, thus, neutralizes only a particular value of C_{gd}.

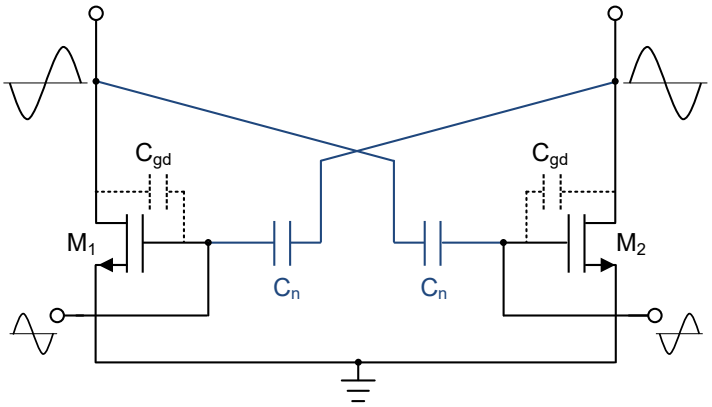


Figure 2. Conventional neutralization technique for compensating C_{gd}.

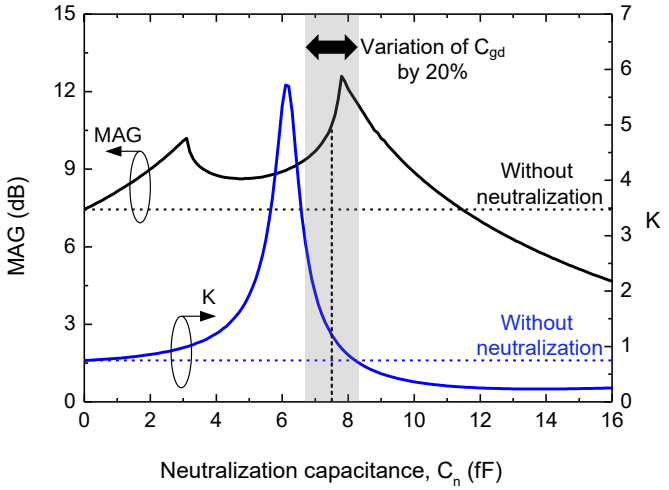


Figure 3. Improvement of the maximum available gain (MAG) and stability factor (K) at 79 GHz by a neutralization capacitor (C_n).

However, if C_{gd} is changed due to PVT variation or inaccurate transistor modeling, which commonly occurs at mm-wave frequencies, the effect of neutralization by a fixed C_n is diminished. For example, if C_{gd} varies by 20% from the original value in Figure 3 (indicated by a shaded region), both MAG and K decrease to 9.3 dB and 0.75, respectively. This leads the transistor to be conditionally unstable again despite the use of neutralization. Therefore, it is necessary to make C_n tunable, so that C_n tracks the variation of C_{gd}. In Reference [13], two-terminal varactors were used to implement the tunable neutralization. However, four DC-block capacitors were additionally required to feed the varactor control voltages. Those additional capacitors not only occupied an extra chip area, but also imposed additional loss, thus lowering the neutralization effect. In Reference [14], a switched inductor was employed for tunable neutralization. However, the inductor presented substantial parasitic capacitance, substrate loss, and chip area consumption. Furthermore, this technique was vulnerable to PVT variation because C_{gd} was neutralized by an inductor rather than an MOS capacitor. To overcome these issues, a new tunable neutralization technique is proposed in this work, as described in Section 2.2.

2.2. Proposed Tunable Neutralization Technique

Figure 4 shows a CS differential pair (M_1 and M_2) to which the proposed tunable neutralization technique was applied. A cross-coupled MOS–varactor pair (M_{v1} and M_{v2}) was connected to the CS pair for neutralization. The gate-to-drain capacitance ($C_{gd,n}$) of M_{v1} and M_{v2} was employed to neutralize C_{gd} of M_1 and M_2. Since the transistors used for the CS and MOS–varactor pairs had a similar dimension to each other, the neutralization effect was robust to PVT variation. To make the neutralization tunable, $C_{gd,n}$ was varied with the varactor control voltage (V_c) applied to the source terminal of M_{v1} and M_{v2}. Thus, $C_{gd,n}$ could track the undesirable change of C_{gd} caused by PVT variation and transistor model inaccuracy. The varactor control voltage should be varied within a range that keeps M_{v1} and M_{v2} turned off to avoid extra DC power consumption.

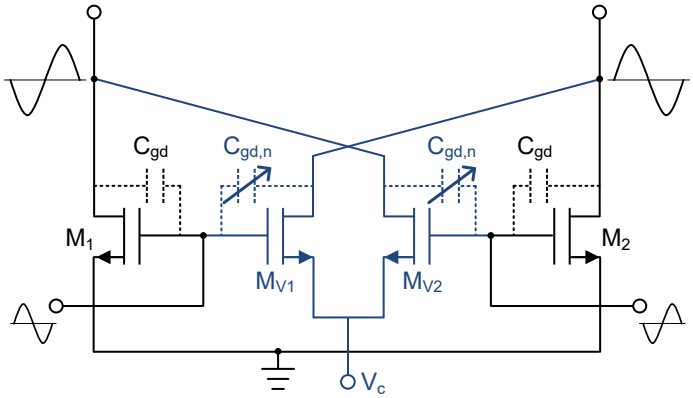


Figure 4. Proposed tunable neutralization technique using a cross-coupled MOS–varactor pair.

The proposed tunable neutralization technique has several advantages over conventional techniques. Firstly, compared to fixed neutralization [10–12], the neutralization capacitance was made tunable. Hence, the neutralized amplifier can be experimentally tuned for optimum performance even after chip fabrication. Secondly, unlike Reference [13], no additional DC-block capacitors are required, because the varactor control voltage is applied to the source terminal while the neutralization signal flows between the gate and drain. Therefore, the neutralization does not suffer from capacitor loss, which tends to increase at high frequencies such as the W-band. Thirdly, the MOS–varactor occupies significantly less chip area and has a higher Q-factor at the W-band than the switched inductor employed in Reference [14]. Finally, since the MOS–varactor uses a similar structure and dimension as the main transistors, the neutralization is immune to mismatch caused by PVT variation.

3. Design of CMOS W-Band Amplifier with Tunable Neutralization

3.1. Implementation of MOS−Varactor

To implement an MOS–varactor for tunable neutralization, three different MOS transistor structures were considered according to the body termination type. As shown in Figure 5, the body terminal can be connected to the source, grounded, or floated. Figure 6 exhibits the simulated Q-factor and C_{gd} of each structure at 79 GHz as a function of the varactor control voltage (V_c). For fair comparison, an identical transistor size was used with a same bias condition of V_{GG} = 0.8 V and V_{DD} = 1.2 V. It can be observed that the body tied to the source exhibited the highest Q, while the variation of C_{gd} was 1.4 fF. The high Q would present a low series resistance and, thus, a high gain increase by neutralization. Therefore, a transistor with body tied to source was chosen as an optimum MOS–varactor structure in this work.

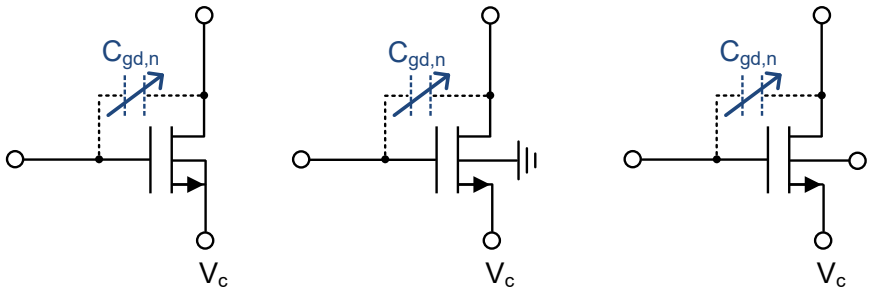


Figure 5. Three different MOS–varactor structures for tunable neutralization: (**a**) body tied to source; (**b**) body grounded; (**c**) body floated.

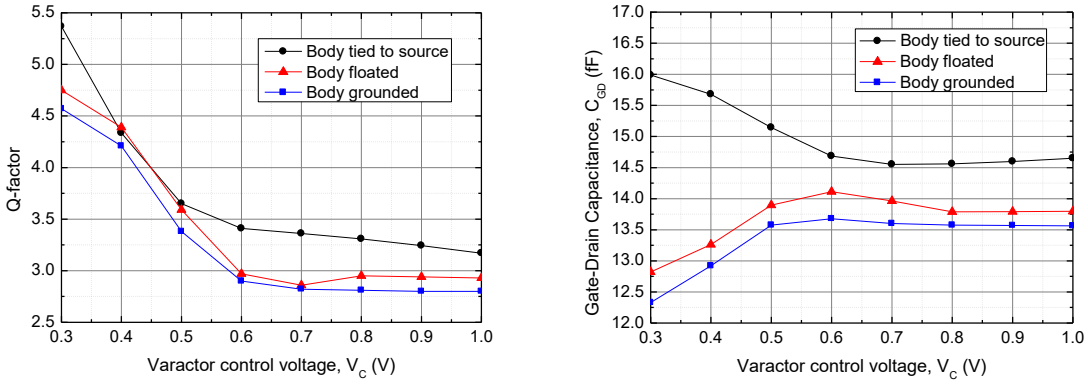


Figure 6. Simulation of MOS–varactors at 79 GHz: (**a**) Q-factor; (**b**) C_{gd}.

A schematic of the MOS–varactor employed in the W-band amplifier is depicted in Figure 7. A triple-well MOS transistor (M_v) was used because the body terminal must be isolated and connected to the source. The dimension of M_v was determined to be 12 × 2.2 µm considering the capacitance required for neutralization of a CS differential pair with 12 × 2 µm transistors. The control voltage at the source (V_c) was varied from 0.3 to 1 V, which kept the transistor turned off. Therefore, no additional DC-block capacitor was needed at the gate and drain. A quarter-wave transmission line and a bypass capacitor (C_{byp}) were connected at the source to choke the RF signal. The neutralization effect on the W-band CS differential pair is shown in Figure 8. With the proposed MOS–varactor neutralization, MAG increased by 1.8 dB at 79 GHz, and K became greater than unity over the full frequency span from DC to the W-band.

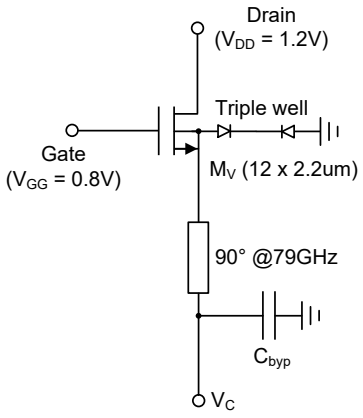
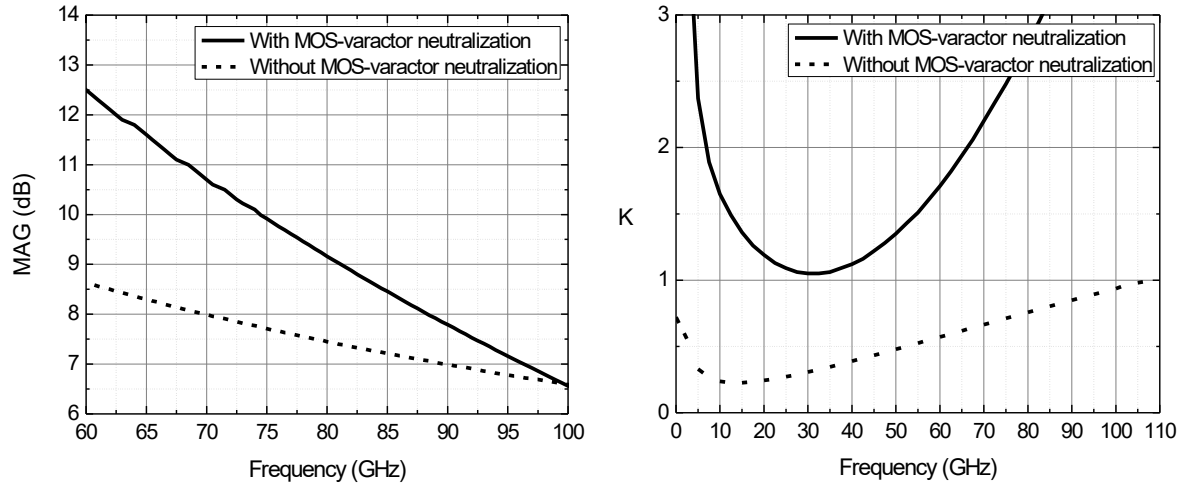


Figure 7. Schematic of the MOS–varactor used in the W-band amplifier.



(a) (b)

Figure 8. Neutralization effect on the W-band CS differential pair: (**a**) MAG; (**b**) K.

3.2. W-Band Amplifier Design with Tunable Neutralization

A complete schematic of the W-band amplifier with tunable neutralization is shown in Figure 9. The amplifier consisted of four cascaded stages of a CS differential pair which was neutralized by the proposed MOS–varactors described in Section 3.1. The impedance matching was fulfilled by transformers (T_1–T_5), which enabled wideband matching performance. In addition, the transformers eliminated the need for additional DC-block capacitors and DC-feed network, which are quite lossy at the W-band. Bias voltages were applied to the center tap of the transformers. Furthermore, the input and output transformers (T_1 and T_5) served as on-chip baluns required for the differential amplifier topology.

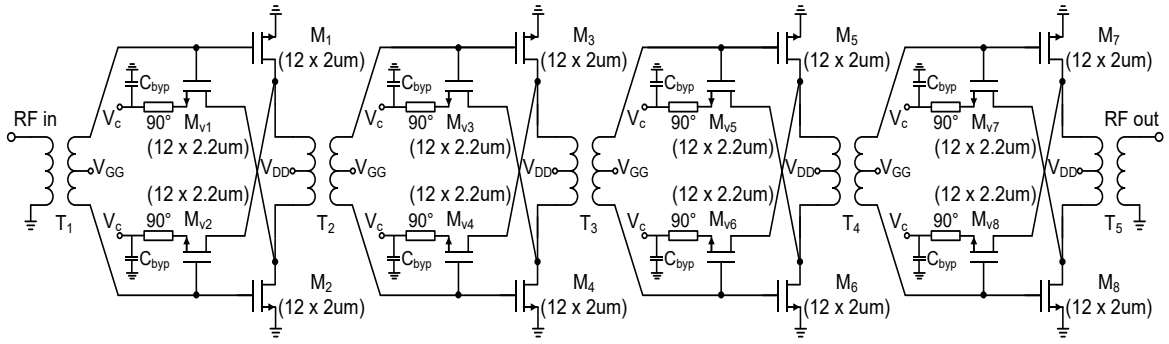


Figure 9. Complete schematic of the W-band amplifier with tunable neutralization.

The S-parameters and K of the amplifier were simulated at two different varactor control voltages (V_c = 0.3 and 0.7 V), as shown in Figure 10. It can be observed that the effect of neutralization on the gain and stability changed with V_c, and the optimum neutralization was fulfilled at V_c = 0.7 V. The gain and K were varied from 16.5 to 18.5 dB and from 30 to 62, respectively, at 79 GHz.

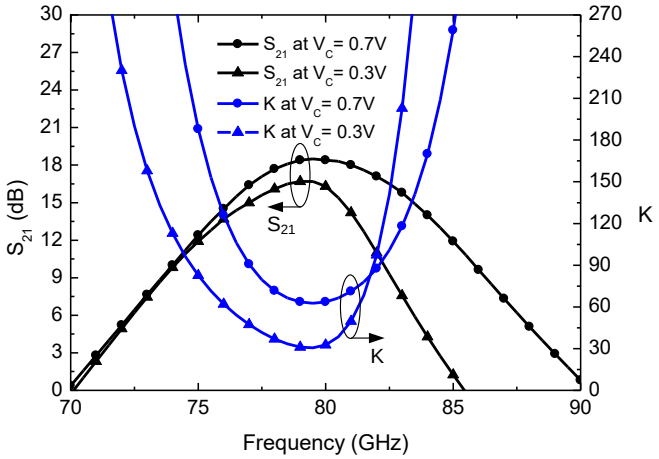


Figure 10. Simulated S-parameters and K of the W-band amplifier at two different varactor control voltages (V_c = 0.3 and 0.7 V).

4. Experimental Results

The W-band neutralized amplifier was fabricated in a bulk 65-nm CMOS process. The chip microphotograph is shown in Figure 11. The total chip area including all probing pads was 0.85 mm^2. The DC power consumption was 56.7 mW. The S-parameter measurement was performed up to 110 GHz using an Anritsu MS4647A network analyzer, Anritsu 3739B switch box, and Anritsu 3743A 110 GHz module through on-wafer probing.

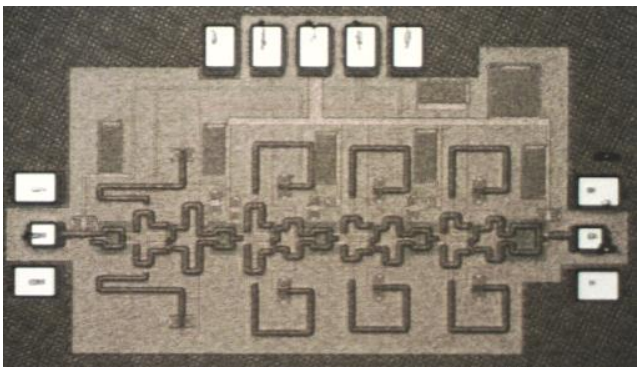


Figure 11. Chip microphotograph of the W-band amplifier.

The measured S-parameters are shown in Figure 12. The varactor control voltage (V_c) was fixed to 0.7 V. The peak gain was measured to be 17.5 dB at 79 GHz with a 3-dB bandwidth of 6.5 GHz from 77.5 to 84 GHz. The input and output return loss were better than 10 dB from 78.8 to 97.4 GHz and from 82.2 to 98 GHz, respectively. The reverse isolation was greater than 39 dB in the whole W-band. A difference between the simulation and measurement was believed to be due to additional model inaccuracy of varactors. To confirm the tunable neutralization by the MOS–varactor, the gain (S_{21}) and stability factor (K) were measured as V_c was varied. As shown in Figure 13, the gain and stability at 79 GHz exhibited their peaks at the optimum V_c around 0.7 V as expected from Section 3.2. It can also be observed that the amplifier performance can be experimentally tuned with the proposed neutralization if the feedback capacitance undesirably deviates from the nominal value after chip fabrication.

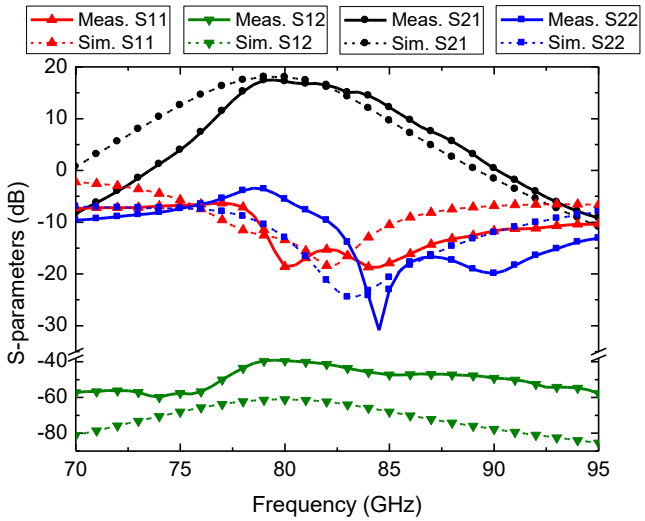


Figure 12. Measured S-parameters of the W-band amplifier.

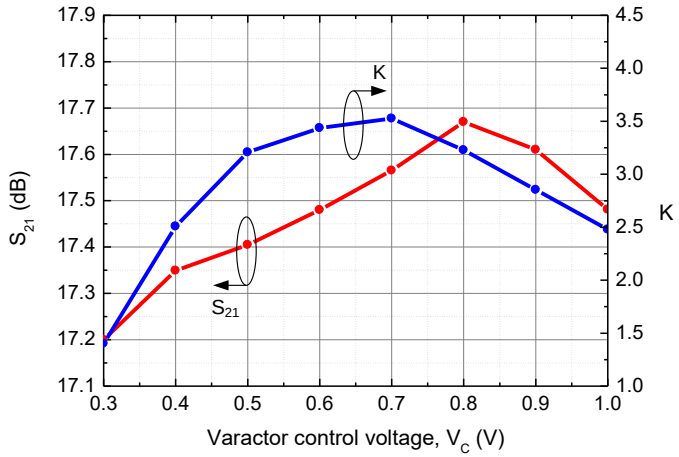


Figure 13. Measured gain (S_{21}) and stability factor (K) versus varactor control voltage at 79 GHz.

In Table 1, the W-band neutralized amplifier is compared with previously reported CMOS W-band amplifiers in the same technology node. The amplifier performance is comparable to others. However, the amplifier in this work employed tunable neutralization for the first time at the W-band, which allows for precise experimental tuning of gain and stability after chip fabrication.

Table 1. Performance summary and comparison.

Ref.	Technology	Frequency (GHz)	Gain (dB)	3-dB BW (GHz)	P_{DC} (mW)	Chip size (mm^2)	Neutralization
[16]	65-nm CMOS	77	17.5	-	30	-	-
[17]	65-nm CMOS	77	11	3 *	25.8	0.3	-
[18]	65-nm CMOS	80	13.5	19	47	-	-
[19]	65-nm CMOS	84	22	20	21	0.45	-
[3]	65-nm CMOS	86	15	12	42	-	-
[20]	65-nm CMOS	79	9.4	15	9.7	0.38	Fixed
[12]	65-nm CMOS	99	11	11	94	0.87	Fixed
[21]	65-nm CMOS	107 **	10.2 **	16 **	28.2 **	-	Fixed
This work	65-nm CMOS	79	17.5	6.5	56.7	0.85	Tunable

* Estimated from the article; ** simulated result.

5. Conclusions

A W-band amplifier employing a new tunable neutralization technique was demonstrated in a bulk 65-nm CMOS technology. The proposed neutralization employs a cross-coupled MOS–varactor pair. Therefore, the amount of neutralization was made tunable without suffering from high loss, transistor mismatch, and large chip area consumption. The amplifier exhibited a measured gain of 17.5dB at 79 GHz and a 3-dB bandwidth from 77.5 to 84 GHz. The gain and stability can be tuned toward the optimum performance by varying the varactor control voltage. The proposed tunable neutralization is useful for precise performance tuning of amplifiers under the existence of PVT variation and transistor modeling inaccuracy.

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Conflicts of Interest: The authors declare no conflicts of interest.

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