The Study of the Operational Characteristic of Interleaved Boost Converter with Modified Coupled Inductor

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Abstract: In this article, design, analysis, and experimental testing of a dual interleaved boost converter with coupled inductor including demagnetizing winding are presented. Proposed topology uses the specific design of boost coils placed within the side parts of the EE core together with a demagnetizing coil located on the center part of the core. Paper describes principles of operational scenarios and characteristics. Through modification of turns ratio between boost coils and demagnetizing coil is possible to achieve high voltage gain. Consequently, the functional performance of this perspective topology is realized experimentally. For that purpose, the physical sample of converter is designed and tested in terms of efficiency considering the change of transferred power or the change of input voltage. Through modification of turns ratio between boost coils and demagnetizing coil is possible to achieve high voltage gain, therefore these dependencies are also evaluated considering also the change of the duty cycle. At the end of the paper basic operational properties are compared to standard boost topologies. It was discovered that even due to higher complexity of the proposed converter oppose to selected topologies, the operational performance is much better considering ripple of the electrical variables, efficiency, or the size of circuit components.

Keywords: interleaved boost converter; high gain boost converter; high efficiency; switching frequency; the planar inductor

1. Introduction

Nowadays, in many power conversion applications, the boost converters (isolated or non-isolated) are used. The most important parameter of every power converter is high efficiency, low costs, and low volumes [1–3].

Due to the limited resources of fossil fuels and also their serious environmental impacts including greenhouse gas emissions, global warming, and environmental pollution, the renewable technologies such as photovoltaic (PV) systems, fuel cells have received extensive attention as a clean source of energy [4–9] similarly current trends in automotive applications are characterized by a common rule-green energy, or blue energy [10–13]. High gain DC/DC (direct current to direct current) converters are the key part of renewable energy systems. The designing of high gain DC/DC converters is imposed by severe demands. Designers face contradictory constraints such as low cost and high reliability. First of all, the inverters must be safe in terms of further maintenance as well as in relation to the environment [14–17].

For almost all industrial and commercial applications the power consumption increases continuously thus it becomes impossible for a single-phase converter to withstand the high current

stress [18–20]. One of the ways how to optimize this negative characteristic is a connection of converter cells in parallel instead of paralleling switching devices of a single cell [21]. The multiphase interleaved converters thus have benefits related to better transient response, power scalability, and better light load efficiency [22–24]. The single-phase converter uses large inductance, which limits the dynamics of the energy transfer within the main circuit [25]. To increase the transient response of the inductor, the value of inductance needs to be reduced significantly. On the other side, small inductance results in large current ripple. The large current ripple usually causes a large turn-off loss and generates large voltage ripple on the input capacitor that is comparable to transient voltage spikes [25–29]. Due to above-mentioned facts the use of the interleaved technique with several converter cells whose inductance value is reduced results in quick and efficient power transfer from input to the output. Improvements of some properties have been achieved in dual interleaved boost (DIB) converters with coupled inductors [30–32], or with voltage lift technique have been proposed.

Electrical behavior of power stage of switched-mode power supplies based on interleaved solution still provides several disadvantages. Those are mostly related to power limitations and voltage gain limitations. High power levels are mostly problematic, because of the increase of conduction losses within the circuit together with a high increase of magnetic components losses, which are related to the DC biasing and consequently components saturation [32–34]. Careful attention shall be paid on the magnetic component design, while there are several proposals how to overcome the negative consequences of the interleaved topologies [35–37].
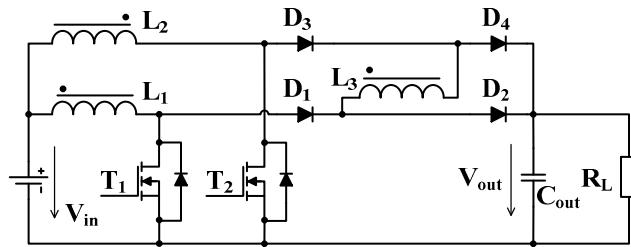
Anyway, within presented research approach attention is given on further optimizations of the magnetically coupled inductor, which is one of the main parts of double-interleaved boost inductor. The investigated topology consists of two interleaved boost converters whose operation is shifted by 180° phase delay. Boost inductors are placed on side parts of the ferrite core. Together with boost inductors additional two SiC diodes are being used for connection with a demagnetizing inductor. The output capacitor is then supplied through another two diodes, thus 4 diodes are required for proper operation of the converter. Due to the addition of demagnetizing inductor, it is possible to achieve voltage gain whose value can be adjusted also by the turn's ratio between boost and demagnetizing inductors. This topology is primarily suited for the applications, where high efficiency, adjustable voltage gain and low dimensions are required, while galvanic isolation between input and output is not required.

Within the presented paper, the analysis of the main circuit operation is being shown, while the focus is given on the operational intervals for various scenarios of the duty cycle value. Consequently, magnetic circuit of coupled inductor with demagnetizing coil is described, while identification of coupling coefficient is done for the needs of the simulation experiments. At the end of the paper, more detailed analysis is provided on the experimental sample of proposed converter (500 W), while the dependency of voltage gain on duty cycle and turns ration is given. Also, efficiency performance is being investigated within various operational conditions. Finally, critical comparison to other standard DIB and boost converters is given.

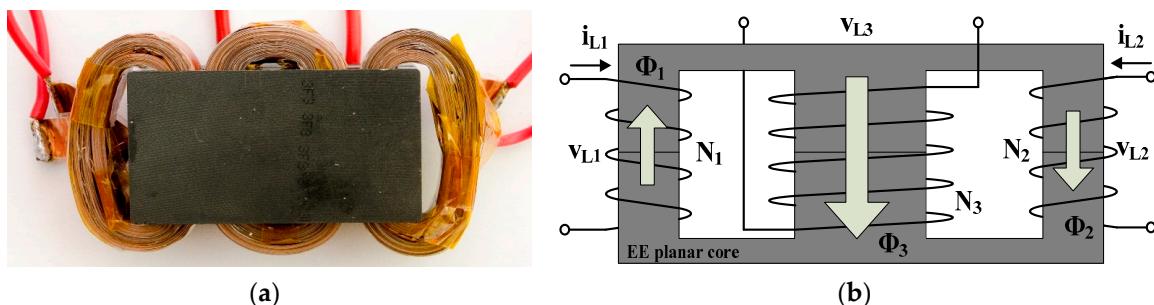## 2. Dual Interleaved Boost with Coupled Inductors

Figure 1 shows a schematic diagram of the proposed interleaved converter with a coupled inductor. The proposed converter consists of T_1, T_2 transistors, coupled L_1, L_2, and demagnetizing L_3 inductors, filtering capacitor C_{OUT} and diodes D_1–D_4. The proposed converter is derived from standard interleaved boost converter by adding third inductor and two rectifiers diode. Coil L_3 is magnetically coupled with L_1 and L_2 on the common magnetic core. The reason for the use of L_3 is related to the possibility of DC flux reset of the ferrite core. Switching of the transistors is similar to standard interleaved boost converter, thus 180° phase shift between gate drive impulses applies. On the other side, the duty cycle range can be extended for both transistors up to D = 100%. The benefit of the proposed topology compared to the standard is that the inductors L_1 and L_2 are periodically

demagnetized during operation, so the saturation of the core is reduced. This effect is made by the presence of L_3 within the converter´s main circuit.

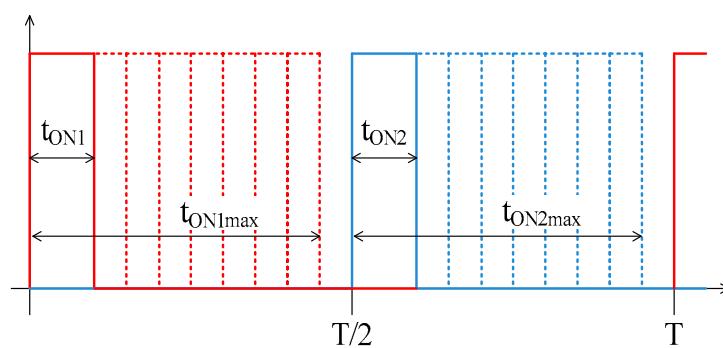**Figure 1.** An electrical schematic of the proposed converter.

Main circuit component i.e. coupled inductor is wound on the common ferrite core E43 which is planar type. The windings of individual coils are made of copper foil. Figure 2 shows the designed component together with its equivalent circuit and winding directions of L_1, L_2, L_3. The equivalent magnetic circuit shown in Figure 2b shows also the direction of the magnetic fluxes Φ_1–Φ_3, which are caused by the inductor currents i_{L1}–i_{L3}.
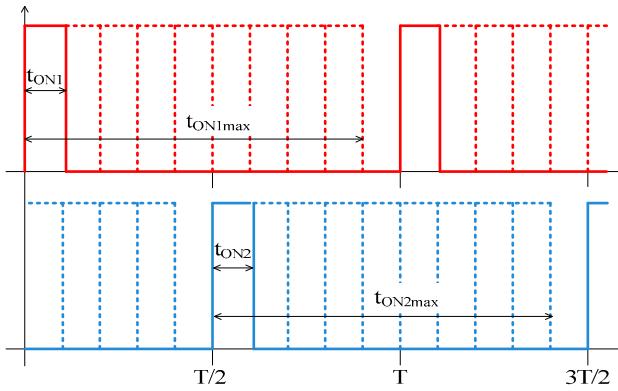

(**a**) (**b**)

Figure 2. Physical sample of the coupled inductor with the demagnetizing coil (**a**) and its equivalent circuit (**b**).

2.1. Analysis of the Operational Intervals

As was mentioned the converter operation can be realized with various duty cycle range, i.e. for D < 50% and for D > 50%. Gate drive impulses during both states are shown in Figures 3 and 4 respectively. Within this paper two situations are analyzed for converter operation, D = 35% and for D = 65%. It is expected that the converter behavior for both operational states will be different.
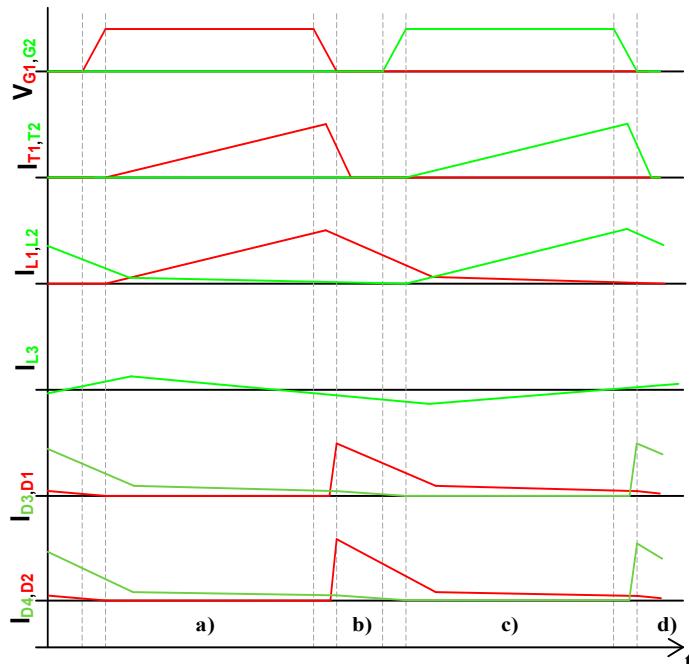

Figure 3. Gate drive impulses for converter operation when the duty cycle of the transistor is below 50%.

Figure 4. Gate drive impulses for converter operation when the duty cycle of the transistor is above 50%.

The proposed converter operates within four main intervals of conduction while the duty cycle is below 50% (Figure 5). These intervals repeat periodically every switching period.

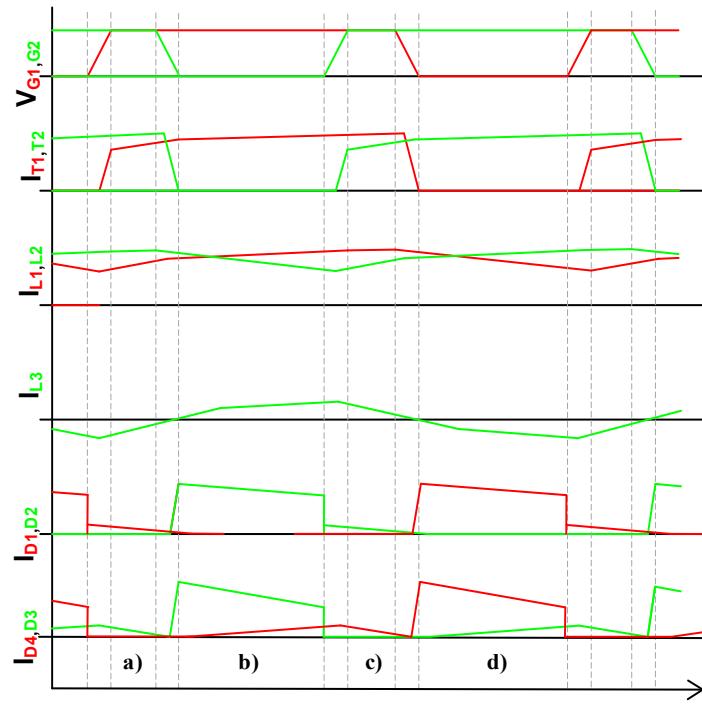**Figure 5.** Working intervals of proposed converter, D < 50% (35%).

a) Interval: Transistor T_1 is ON, T_2 is OFF, The T_1 and L_1 currents are linearly increasing, The L_3 and D_3, D_4 currents are linearly decreasing.

b) Interval: Transistor T_1 is OFF, T_2 is OFF, The L_1 current is linearly decreasing and energy from L_1 are sinking to the load trough the D_1 and D_2.

c) Interval: Transistor T_1 is OFF, T_2 is ON, The T_2 and L_2 currents are linearly increasing, The L_3 and D_1, D_2 currents are linearly decreasing.

d) Interval: Transistor T_1 is OFF, T_2 is OFF, The L_2 current is linearly decreasing and energy from L_2 is sinking to the load trough the D_3 and D_4.

Figure 6 shows the principal waveforms of the converter variables for the situation when the value of the duty cycle exceeds 50%. For this case D = 65% was used.

Figure 6. Working intervals, Duty > 50% (65%).

a) Interval: Transistor T_1 is ON, T_2 is ON, the L_1 and L_2 currents are linearly increasing, the L_3 current are linearly increasing and D_1 current is linearly decreasing.

b) Interval: Transistor T_1 is ON, T_2 is OFF, the L_1 current is linearly increasing and energy from L_2 is sinking to the load trough the D_2 and D_3.

c) Interval: Transistor T_1 is ON, T_2 is ON, the L_1 and L_2 currents are linearly increasing, the L_3 current are linearly decreasing and D_2 current is linearly decreasing.

d) Interval: Transistor T_1 is OFF, T_2 is ON, the L_2 current is linearly increasing and energy from L_1 are sinking to the load trough the D_1 and D_4.

The induced voltage in each of the three windings is defined as follows:

$$
\begin{aligned}
v_{L1} &= N_1 \frac{d\Phi_1}{dt} \\
v_{L2} &= N_2 \frac{d\Phi_2}{dt} \\
v_{L3} &= N_3 \frac{d\Phi_3}{dt}
\end{aligned}
\tag{1}
$$

where: v_{L1}, v_{L2} and v_{L3} are the winding voltages; N_1, N_2, and N_3 are the numbers of turns of each winding L_1, L_2, and L_3, respectively, and Φ_1, Φ_2, and Φ_3 are the magnetic fluxes interlinking with the windings L_1, L_2, and L_3, respectively. Moreover, for the symmetry between the two phases, we assume $N_{12}=N_1=N_2$. Additionally, according to Figure 2 we have:

$$
\Phi_3 = \Phi_1 - \Phi_2
\tag{2}
$$

the induced voltage in the central winding:

$$
v_{L3} = \frac{N_3(v_{L1} - v_{L2})}{N_{12}}
\tag{3}
$$

Next, we introduce N as the ratio of the number of turns of the central winding and the number of turns of L_1 or L_2:

$$
N = \frac{N_3}{N_{12}}
\tag{4}
$$

Finally, substituting (4) into (3), we can get the induced voltage in the central winding in the function of the voltage of L_1 and L_2:

$$v_{L3} = N(v_{L1} - v_{L2}) \tag{5}$$

2.2. Steady-State Analysis

The steady-state analysis is performed for both situations of the converter operation, i.e. when duty – cycle operation is considered below and above 50% (Figures 3–6). For these purposes just, equivalent circuits are selected which are cyclically repeated.

2.2.1. 1st Mode (1st Conduction Interval)

T_1 is turned ON and T_2 is turned OFF. During this interval, the energy is accumulated within the magnetic core of L_1, while the L_2 supports the output current flow through D_3-L_3-D_2. The value of the current flowing through L_2-D_3- L_3-D_2 is decreasing and its maximal value is limited by the value of magnetizing current, which is determined by the mutual relationship between L_2-L_3. This interval ends when dead-time between switching of T_1 and T_2 is applied.
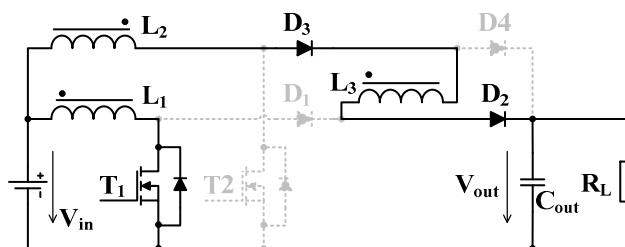
Considering this operational interval, we can define the input voltage of the converter as follows:

$$v_{IN} = N_{12} \frac{\Delta \Phi_1}{T_1} \tag{6}$$

Under the assumption of (1) and (2) and based on the situation given by the equivalent circuit from Figure 7 the input and output voltage dependency can be defined by (7).

$$v_{IN} = N_{12} \frac{\Delta \Phi_2}{T_1} - N_3 \frac{\Delta \Phi_3}{T_1} + V_{out} \tag{7}$$

where and $\Delta\Phi1$, $\Delta\Phi2$ and $\Delta\Phi3$ are the magnetic flux variations in the windings L_3, L_2 and L_3 and T_1 is the time duration of Mode 1, v_{IN} is input voltage, V_{out} output voltage.

Figure 7. Equivalent circuit schematics of the converter during 1st operational interval.

2.2.2. 2nd Mode (2nd Conduction Interval)

T_1 turned OFF and T_2 is turned ON. The beginning of this interval is characterized by the current i_{L1} decrease to the value of the magnetizing current. From this point the visible increase of i_{L2} is evident. L_1 is supporting the output with current flow through D_1-L_3-D_4. The current direction of the i_{L3} is opposite to i_{L1} thus the demagnetizing ability of the proposed magnetic component is clear. The interval ends similarly as 1st Mode of operation, i.e. before dead-time.
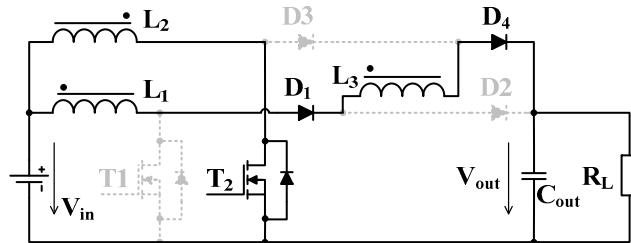
Considering this operational interval (Figure 8), we can define the value of input voltage of the converter based on the (7), while the end of the 1st interval represents initialization of the 2nd interval:

$$v_{IN} = N_{12} \frac{\Delta \Phi_1}{T_2} - N_3 \frac{\Delta \Phi_3}{T_2} + V_{out} \tag{8}$$

Under the assumption of (1) and (2) the value of the input voltage can be expressed by (9).

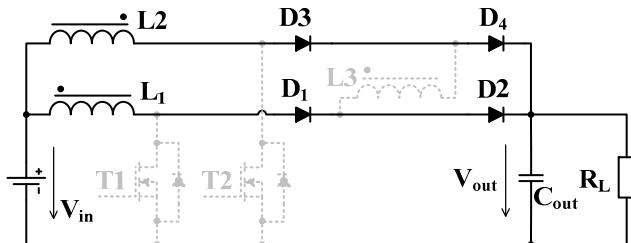$$v_{IN} = N_{12} \frac{\Delta \Phi_2}{T_2} \tag{9}$$

where T_2 is the time duration of Mode 2.

Figure 8. Equivalent circuit schematics of the converter during 2nd operational interval.

2.2.3. 3rd Mode (Dead-Time)

T_1 and T_2 are turned OFF (Figure 9). This interval is the so-called dead-time and is valid just and only during operation if the duty cycle is below 50%. During this interval, the commutation between the transistor and diodes is occurring. Also, one of the main inductances (L_1, L_2) is de-energized to the value of the magnetizing current, while supporting the output current.

Figure 9. Equivalent circuit schematics of the converter during 3rd operational interval.

Similar to the previous situation from 2nd operational interval, the value of the input voltage, or the dependency between input–output situation shall be expressed under the assumption of (3) and (4) as follows:

$$v_{IN} = N_{12} \frac{\Delta \Phi_1}{T_3} + V_{out} \tag{10}$$

$$v_{IN} = N_{12} \frac{\Delta \Phi_2}{T_3} + V_{out} \tag{11}$$

where T_3 is the time duration of Mode 3.

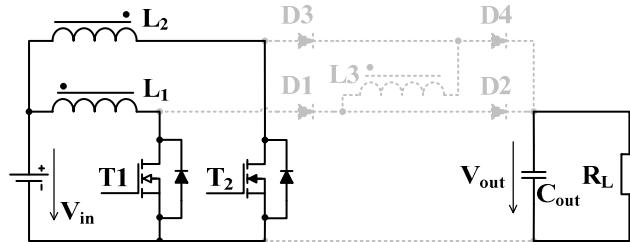### 2.2.4. 4th Mode (Valid Only for Duty > 50%)

T_1 and T_2 are turned ON and the inductors L_1 and L_2 are accumulating the energy within their magnetic circuits. The output is supported just by the energy stored in C_{OUT}.

The condition within this operational interval can be described by the situation which is valid from 3rd operational interval while considering the equivalent circuit from Figure 10 is given by the next equations:

$$v_{IN} = N_{12} \frac{\Delta \Phi_1}{T_4} \tag{12}$$

$$v_{IN} = N_{12} \frac{\Delta \Phi_2}{T_4} \tag{13}$$

where T4 is the time duration of Mode 4.

Figure 10. Equivalent circuit schematics of the converter during 4th operational interval.

2.3. Voltage Gain Calculation

The voltage gain M, defined as the ratio of the output and input of voltage in dependence on the value of the duty cycle D when it is lower than 50% can be obtained from (6), (8), and (10) and is derived as follows:

$$M_{D \leq 0.5} = \frac{1 + N}{(1 + N) - D(1 + 2N)} \tag{14}$$

The voltage gain when the duty cycle is higher than 50% is expressed as:
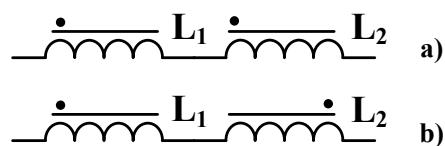
$$M_{D \geq 0.5} = \frac{1 + N}{(1 - D)} \tag{15}$$

2.4. Determination of Coupling Coefficients Between the Coils

For the purposes of simulation investigation as well as for optimization purposes of the magnetic design of coupled inductor with the demagnetizing coil, the coupling coefficients of the converter shall be determined. The process of the identification was realized experimentally, initially through measurement of parasitic DC resistance and inductance of individual coils—Table 1.

Table 1. Inductance and DC resistance values of coils.

	L1 [µH]	L2 [µH]	L3 [µH]
Inductance [µH]	297	298	573
DC resistivity [mΩ]	41	43	80

Consequently, mutual inductances have been measured between coils L_1 and L_2 for coincident and anti-coincident directions of the coil windings (Figure 11). The measured values of mutual inductances are listed in Table 2.

Figure 11. Coincident (**a**) and anti-coincident directions of the coil's windings (**b**).

Table 2. Value of mutual inductances between coils.

	L12 [µH]	L13 [µH]	L23 [µH]
Positive config (a)	730	1206	1200
Negative config (b)	409	440	438

Measured values of the mutual inductances have been used for the determination of the coupling coefficients, what is given by (16)–(18).

$$M_{12N} = \frac{L_1 + L_2 - L_{12N}}{2} \tag{16}$$

$$M_{12P} = \frac{L_{12P} - L_1 - L_2}{2} \tag{17}$$

$$k_{12} \frac{M_{12}}{\sqrt{L_1 * L_2}} \tag{18}$$

Based on the (18) including individual values of inductances, the coupling coefficients have been determined (Table 3).

Table 3. Table of inductance couplings coefficients between coils.

k_{12}	k_{13}	k_{23}
0.27	0.46	0.46

3. Experimental Verification

Experimental measurements have been realized on the converter prototype sample (Figure 12), whose main circuit parameters are listed below. Main circuit parameters were selected for the application use within photovoltaic systems, where proposed converter solutions shall be used as MPPT converter, which shall distribute energy within other power semiconductor converter subsystems or shall operate as energy charger for storage components (Figure 12). Also, these parameters have been selected due to the ability of photovoltaic panels which are connected in series, while their output voltage is reaching 120 V [38]. Since the converter system considers microgrid operation its power rating was initially set to 500 W, while it is not excluded that other variations of input/output parameters are not possible.
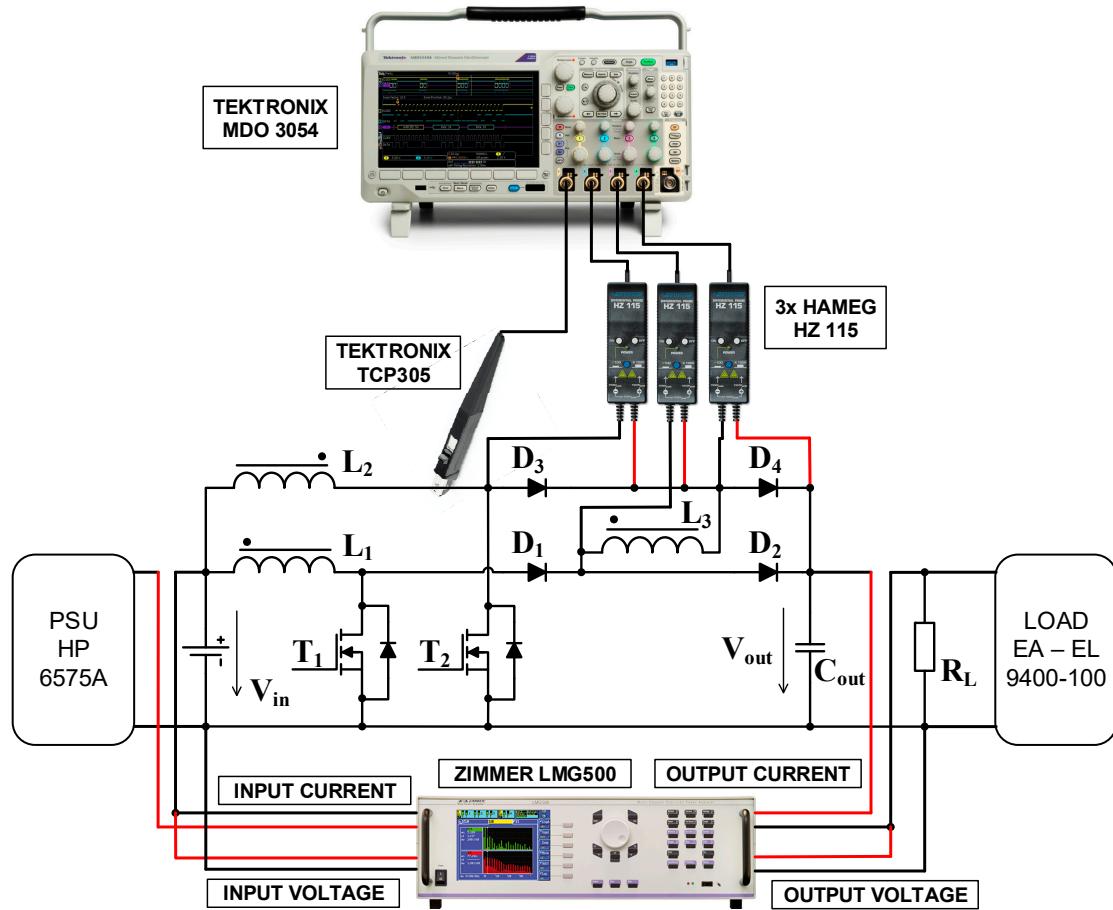

Figure 12. Proposed converter prototype.

The focus was given on the investigation of the converter operation with a duty cycle above and below 50%. For the operation D < 50%, value of the duty cycle was set to 35% and for D > 50% value of the duty cycle was 65%. Initially, the time waveforms on the inductors were investigated due to verification of the existence of AC magnetic flux of the L_3, which serves for the core demagnetization. Finally, the focus was given on the evaluation of the efficiency and voltage gain performance for the selected duty cycle values [39–42]. At this point the turns ratio between L_1 and L_2 is equal to 1:1, while the turns ratio between L_1 and L_3 and L_2 and L_3 is 1:1,7.

- Input voltage = 100 V

- Switching frequency (f_{SW}) = 200kHz
- Output voltage = 300 V
- Output power = 500 W
- Duty cycle = D_1 = D_2 = range 0–95%
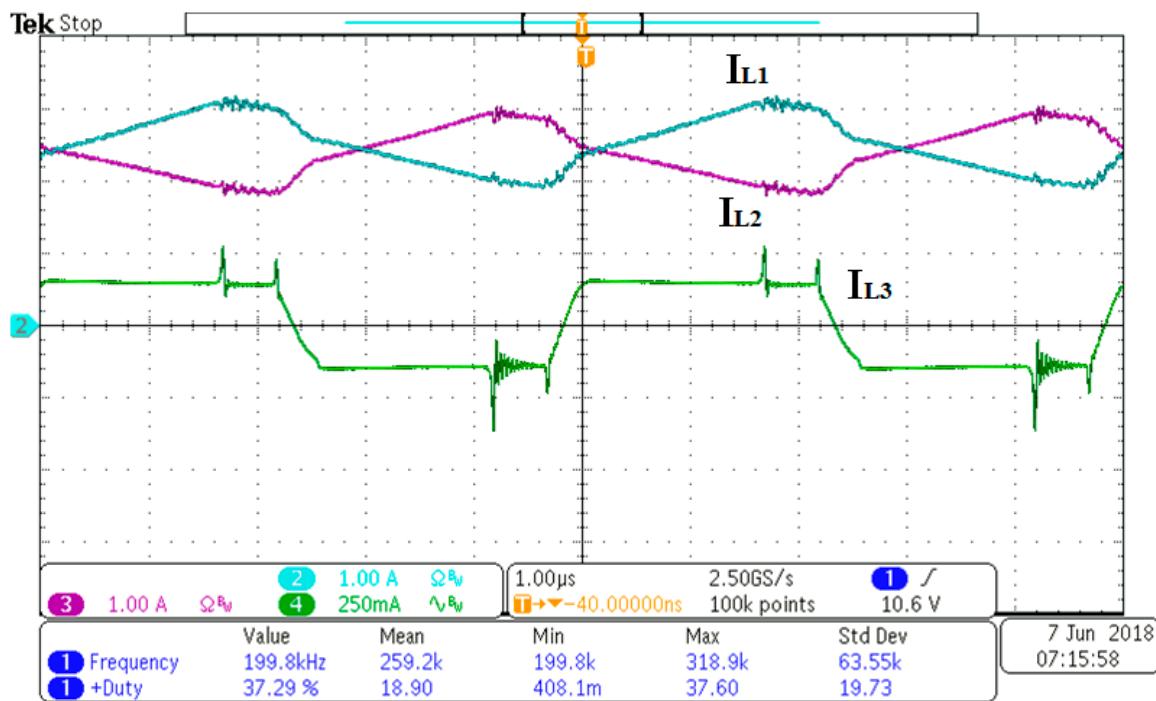- Turns ratio = 3.6 ($N_1 = N_2$ = 6, $N_3 = 10$ => TR = 1:1.7)

Figure 13 shows the arrangement of the experimental set-up, which was prepared for the individual measurements. For the time-waveform measurement of the circuit components, the oscilloscope MDO3054 was used, while evaluation of the efficiency and other circuit variables (input–output voltages) for the purpose of graphical dependencies were recorded with the use of spectral analyzer Zimmer LMG500.

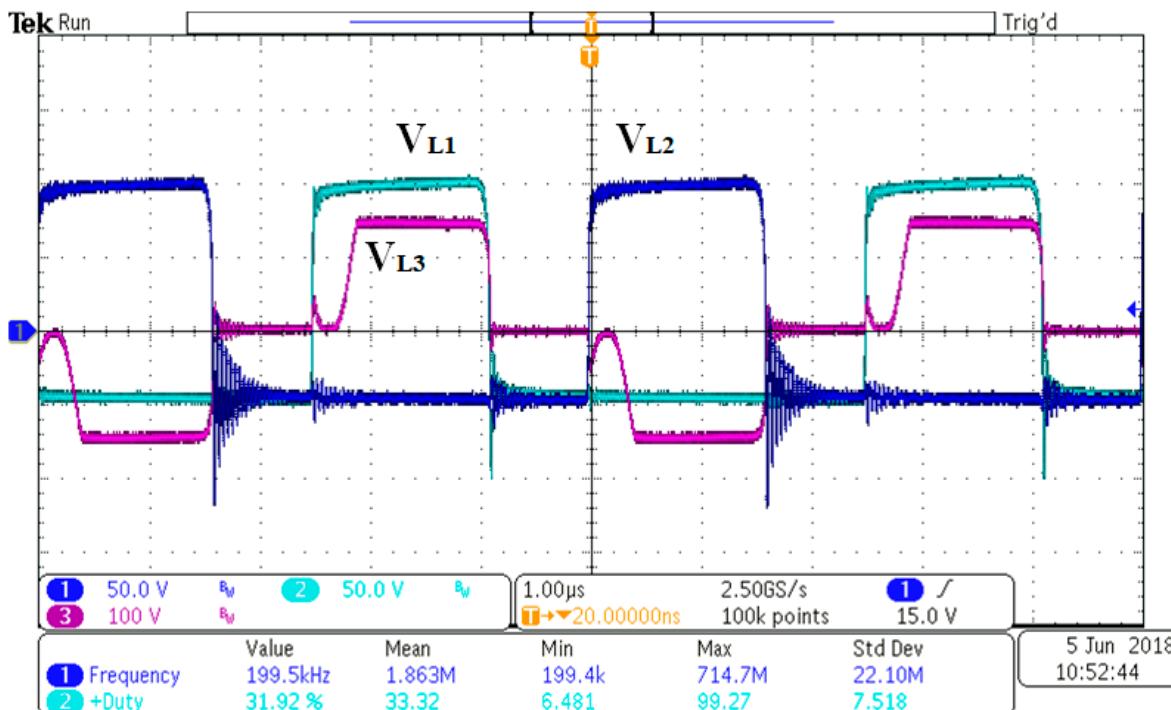**Figure 13.** Experimental set-up with measuring equipment.

3.1. Measurement Results for D < 50% (35%)

Figure 14 shows the time-waveforms of the inductors currents during the operation when D = 35%. It is seen, that the current of the L_3 coil has an AC character within the selected operating range. Dead-time is visible through the waveform of I_{L1} and I_{L2} when the character of these currents is decreasing. The received waveforms correspond to the theoretical operation described in Figure 5.

Figure 14. Time–waveforms of the inductors currents. D = 35% Vin = 100V in Pout = 500 W.

Figure 15 shows the time waveforms of the inductance voltages and the character of voltage V_{L3} is exhibiting alternating shape. The small valleys at the begin of each period are caused due to the dead-time existence during operation.
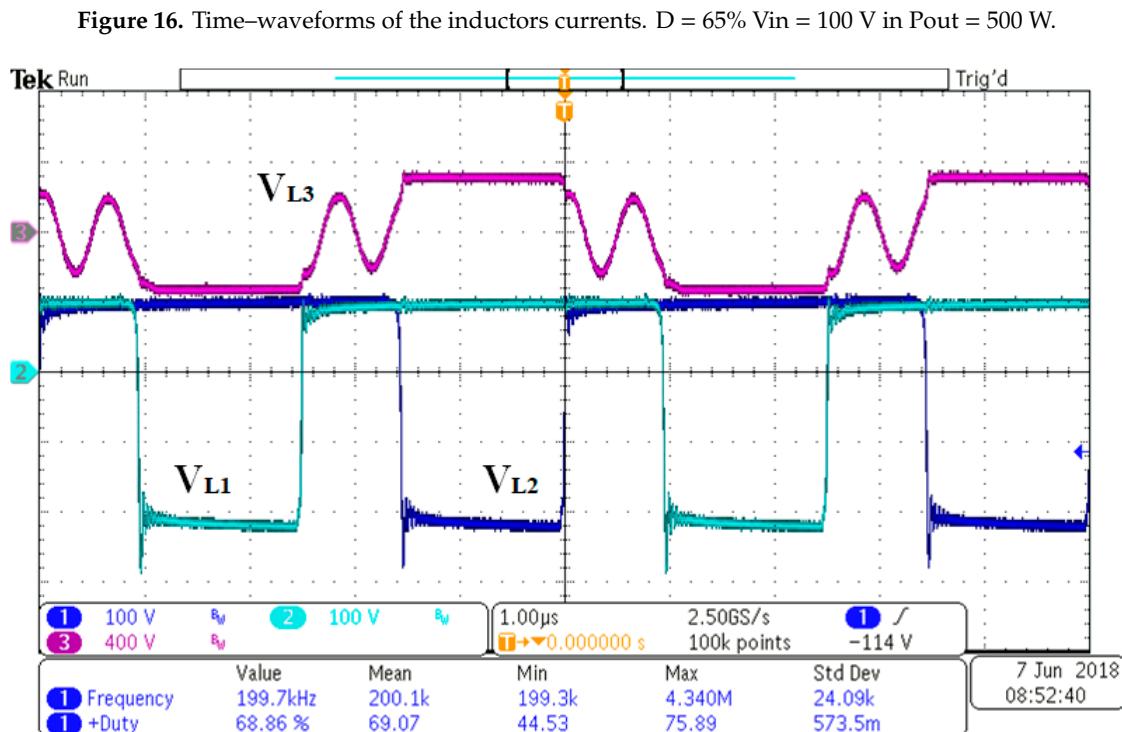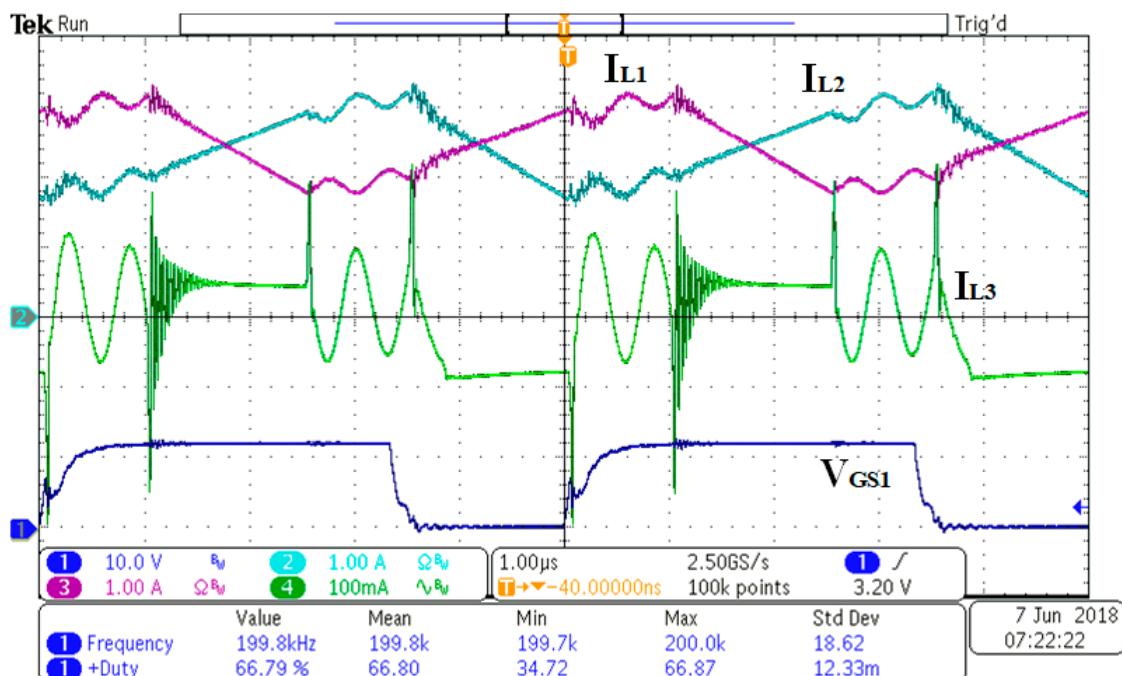

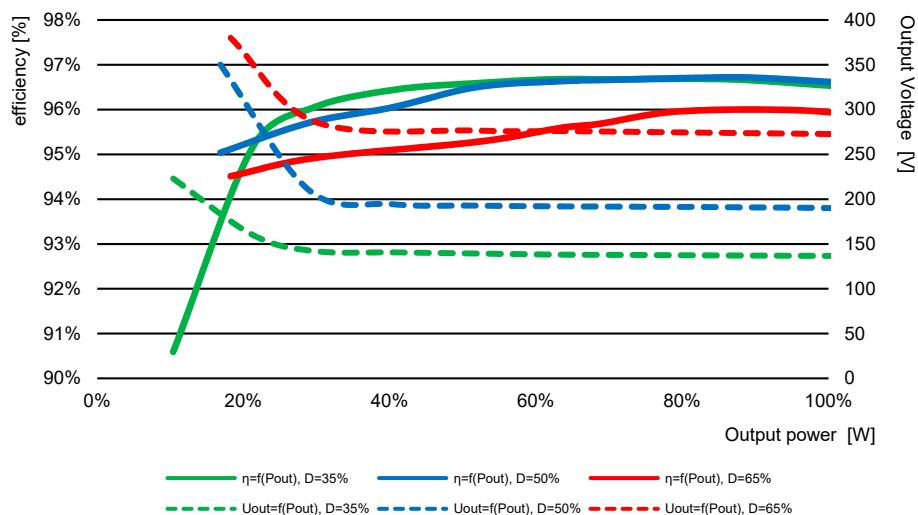**Figure 15.** Time–waveforms of the inductors voltages. D = 35% Vin = 100V in Pout = 500 W.

Based on the results from Figures 14 and 15 is seen, that the shapes of the waveforms are without significant disturbances thus the converter operation acts stable.

3.2. Measurement Results for D > 50% (65%)

Similar verifications as those from Figures 14 and 15 were done for duty cycle value above 50% (Figures 16 and 17). Figure 16 shows the current waveforms of the inductances together with one of the transistor's gate drive signal. It is seen that compared to waveforms from Figure 14, the shape is more distorted mostly for the current L_3. Amplitudes for the variables on L_1 and L_2 are the same and the only change for this operating condition is the change of the output voltage value (Figure 18) and the change of the AC current flowing through L_3, which exhibits much more distortion and lower values.

Figure 16. Time–waveforms of the inductors currents. D = 65% Vin = 100 V in Pout = 500 W.

Figure 17. Time–waveforms of the inductors voltages. D = 65% Vin = 100 V in Pout = 500 W.
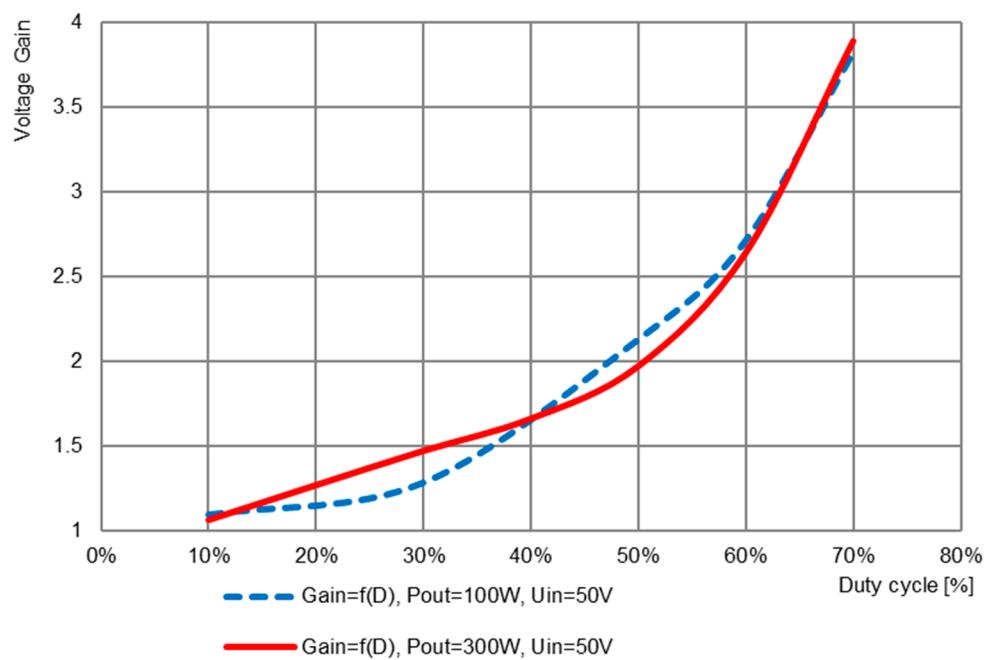
Efficiency performance investigation was done for three operating conditions, which have been defined by the value of the operational duty cycle, whereby dependency on the output power delivery was evaluated. From Figure 18 is seen that the converter exhibits efficiency between 94.5% and 96.7% within 20% up to 100% of output power considering selected values of the duty cycle. From Figure 18 is seen that more efficient operation is for the duty cycle D = 50%, while whole operation region of the output power is considered, i.e. from 20% to 100% of nominal P_{OUT}. Efficiency decrease for the highest selected value of duty cycle (D = 65%) is caused by the distorted operation (Figure 16), by higher conduction losses in the main circuit due influence of the L_3 inductance, and by the higher voltage difference between input–output part of the converter.

Figure 18. Efficiency and output voltage in dependence on the value of the duty cycle and output power.

On the other side, it can be seen, that output voltage is able to increase directly with the increase of the duty cycle value (Figure 19) or by the change of the ration between inductances L_1, L_2, and L_3, while ration between L_1 and L_2 is always considered to be 1:1.
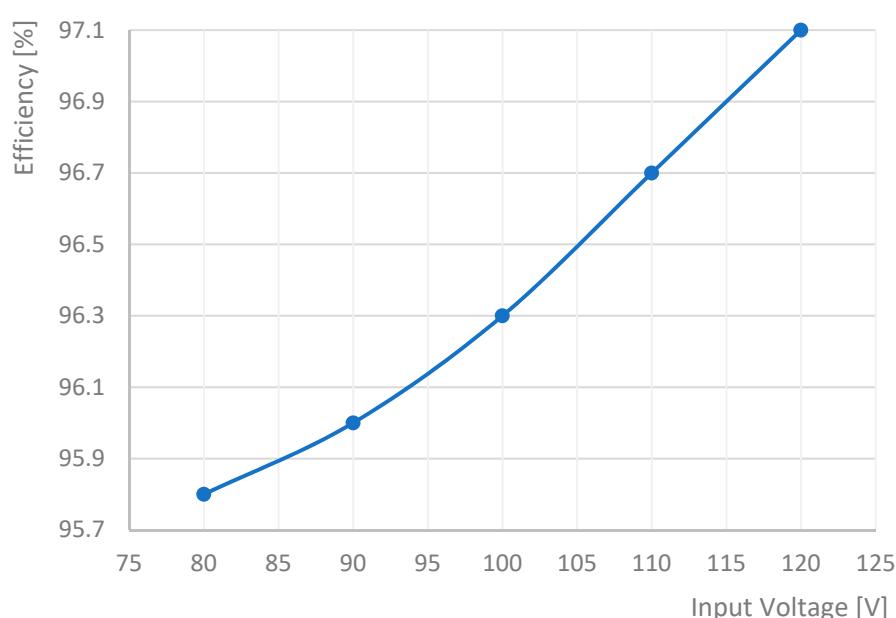

Figure 19. Voltage gain dependency on duty cycle and output power.

Figure 20 shows the dependency of the voltage gain for investigated values of the duty cycle, while the dependency is evaluated on the turns ration change between the L1, L2, and L3, while as was already mentioned, the ratio between L1 and L2 shall always be 1:1 if the proper operation is expected. The ratio range is selected for the values, a which the operational waveforms of the currents and voltages are on the acceptable level considering efficiency performance.

Figure 20. Voltage gain dependency on duty cycle and turns ration between L_1, L_2, and L_3, while $L_1 = L_2$.

Figure 21 shows the experimental evaluation of the influence of the input voltage variance on the efficiency for the operational condition when the output power is at its maximum, and duty cycle is at the worst selected condition (65%) from Figure 17. It is seen, that the input voltage variance has direct impact on the efficiency while considering the difference of 40 V at the input voltage causes 1.2% efficiency fluctuation.

Figure 21. Efficiency performance in dependency on input voltage at $P_{OUT} = 100\%$ and D = 65%.

3.3. Performance Comparisons to Other Topologies

For the performance analysis of presented converter to commercially used alternatives was realized in the way experimental measurements, while the proposed converter is compared to the standard dual-interleaved boost (DIB) type converter and to the classic boost converter [43]. The parameters of converters related to the output power, input voltage and switching frequency have been the same. It means each of converter operates at the maximum power of 500 W, at input voltage 100 VDC, with switching frequency 200 kHz. The voltage gain of all converters was set to the same level, i.e. Gain = 3.6. The results from the analysis related to the operational parameters/characteristics are listed in next table.

Table 4 shows that the proposed converter has the best efficiency from the investigated alternatives and it is also even the number of semiconductor switches is doubled oppose to standard alternatives. It is related to the type of magnetic component being used while the proposed converter uses much lower magnetic core and utilizes reset winding that is eliminating saturation of the core oppose to compared solutions. Due to very low output voltage ripple, the output electrolytic capacitors can be reduced, i.e. their value shall be much lower compared to standard topologies. In this way, the optimization is done also in the way of reduction of ESR and, thus, of other parts of losses. This is second issue related to the efficiency improvements of proposed converters. The proposed magnetic design of inductor is beneficial also due to fact, that it operates as stiff voltage transformer with the given transformer ratio. Existence of the visible AC component within the circuit secures, that the input current ripple is minimized. The only visible disadvantage of proposed converter to investigated one is the limitation of the voltage gain. With given turns ratio of inductor, it can achieve maximum value of 4. Anyway, if the ratio is modified, also higher values can be reached, but the performance of other variables can be then reduced [43].

Table 4. Comparisons of the proposed converter to other circuit alternatives.

	Proposed Converter	DIB Converter	Boost Converter
Output power	500 W	500 W	500 W
Output voltage ripple	19 mV	180 mV	364 mV
Input ripple current	4.4 A	17 A	14 A
Output capacitor	66 uF	470 uF	470 uF
Inductor Volumes	E 43 PLT	E50/27/15	ETD59
Efficiency Pout=100%	96.7%	91%	90%
Maximum achievable voltage gain	1:6	1:19	1:10

A more comprehensive comparison can be done within future works, where the focus will be given also on the investigation of the semiconductor used and variant solutions of the main circuit with the possibility of resonant switching.

4. Conclusions

In this paper, the dual interleaved converter with coupled inductors and additional flux reset circuit was introduced and investigated. Principally the interleaved topologies offer several advantages to standard solutions, while mostly performance related to the lowered values of the output voltage ripple, and input current ripple are improved. Also, the efficiency is optimized through the wide operational range of input–output variances. However, there are still design considerations which negatively influence characteristics of the interleaved solutions. Since the boost coils work with DC magnetization, the demagnetizing circuit was introduced and investigated within presented paper. Such approach adds alternating current flow during each interval, thus AC part for the ferrite core is considered in this way. The main outcome is the reduction of the core direct saturation, so the better thermal performance and optimization of the geometrical properties is possible.

Because the analysis of the circuit was performed, several dependencies have been presented. The focus was given on the voltage gain characteristic dependent on the duty cycle change as well as on the turns ratio between boost and demagnetizing inductors. Both techniques were tested experimentally within the selected operational range on the prototype sample. Simultaneously the efficiency was estimated for various operational conditions, mostly for the variable output load at a constant duty cycle, while 3 scenarios were selected. Together with it the output voltage stiffness was also evaluated. The results showed that the most efficient operation is limited for the value of the duty cycle of 50%. On the other side, with low turns ratio between inductances, higher voltage gain is achieved above the 50% value of duty cycle.

Based on these considerations it is concluded, that proposed converter is possible to design for target application area with satisfying parameters from efficiency and voltage gain point of view. The designer just needs to decide, whether use duty cycle modification or turns ratio will be more effective. However, it is expected that the proposed converter topology can achieve 96% of efficiency within the whole operation range even when standard semiconductor devices are being used. A further increase is possible with wide bandgap devices.

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