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Power Efficiency Improvement of Three-Phase Split-Output Inverter Using Magnetically Coupled Inductor Switching

Min-Kwon Yang and Woo-Young Choi *

Division of Electronic Engineering, Chonbuk National University, Jeonju 561-756, Korea
* Correspondence: wychoi@jbnu.ac.kr; Tel.: +82-063-270-4218

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Abstract: The conventional three-phase split-output inverter (SOI) has been used for grid-connected applications because it does not require dead time and has no shoot-through problems. Recently, the conventional inverter uses the silicon carbide (SiC) schottky diodes for the freewheeling diodes because of its no reverse-recovery problem. Nevertheless, in a practical design, the SiC schottky diodes suffer from current overshoots and voltage oscillations. These overshoots and oscillations result in switching-power losses, decreasing the power efficiency of the inverter. To alleviate this drawback, we present a three-phase SOI using magnetically coupled inductor switching technique. The magnetically coupled inductor switching technique uses one auxiliary diode and coupled inductor for each switching leg in the three-phase SOI. By the operation of the coupled inductor, the main diode current is shifted to the auxiliary diode without the reverse-recovery process. The proposed inverter reduces switching-power losses by alleviating current overshoots and voltage oscillations of SiC schottky diodes. It achieves higher power efficiency than the conventional inverter. We discuss experimental results for a 1.0 kW prototype inverter to verify the performance of the proposed inverter.

Keywords: three-phase; split-output inverter; silicon carbide; coupled inductor; switching-power loss; power efficiency

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1. Introduction

The standard three-phase voltage source inverter (VSI) has been widely used for grid-connected applications [1–3]. It has two power switches in same switching-leg that present a shoot-through problem. A dead-time is essentially required for two power switches in same switching-leg to prevent the shoot-through switching state. Dead-time distorts the output waveforms and reduces the pulse-width modulation (PWM) [4]. Even with the dead-time compensation, a shoot-through switching state is the problem of VSI, which reduces the system's reliability [5].

Figure 1 shows the circuit diagram of the conventional three-phase split-output inverter (SOI) [6,7]. It can operate without the above-mentioned shoot-through problem to decouple two series-connected power switches by splitting the inverter switching leg. Recently, SOIs have adopted wide bandgap devices such as silicon carbide (SiC) metal-oxide semiconductor field-effect transistors (MOSFETs) for S_1~S_6 and SiC schottky diodes for D_1~D_6 due to their higher electric-breakdown filed strength, and higher thermal conductivity [6]. The material properties of SiC have made the SiC device the focal point of high temperature, high frequency, and power efficiency [8]. The SiC devices can achieve higher power density, and system efficiency compared with Si devices [9,10]. Especially, the SiC schottky diodes have been used for the freewheeling diodes of the conventional inverter because they do not have reverse-recovery problem [11]. However, in a practical design, the SiC schottky diodes exhibited current overshoots and voltage oscillations due to the resonant *RLC* circuit formed between the diode parasitic resistance, stray inductance, and diode parasitic capacitance [12]. These current overshoots and voltage oscillations cause switching-power losses for the switch and diode, which reduce the power efficiency of the system.

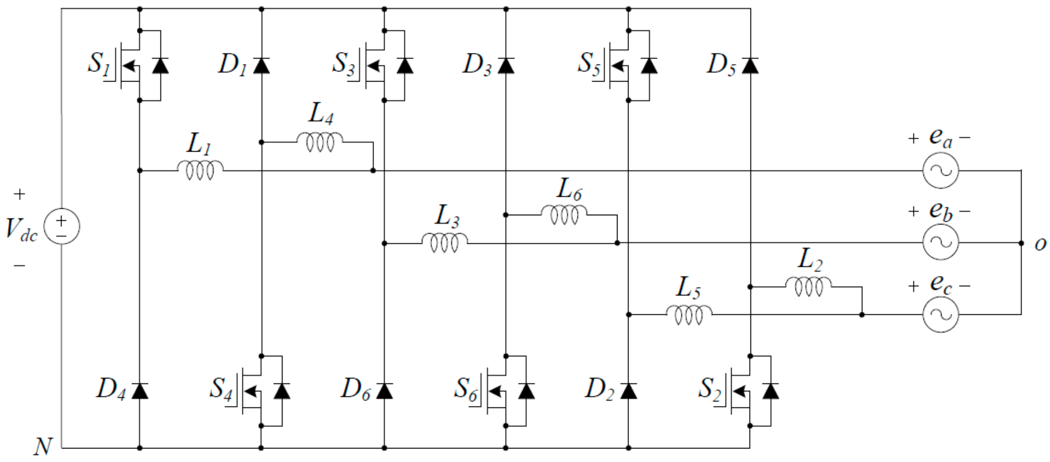


Figure 1. Circuit diagram of the conventional three-phase split-output inverter.

To minimize the switching-power losses, additional snubber circuits are required, as described in [13–16]. They can be classified into two cases—passive snubber circuits [13,14] and active snubber circuits [15,16]. The *RC* snubber circuit presented in [13] dissipates the switching-power losses, reducing the power efficiency of the inverter. The passive lossless snubber circuit presented in [14] employs an *LC* snubber circuit for each switching device to achieve zero-current turn on and zero-voltage turn off. However, the passive lossless snubber circuit requires many passive components and increases system complexity and cost. The snubber circuit in [15] uses a capacitor to store the energy due to switching losses. This solution is attractive because of its simple circuit structure and reduced component count. However, when an inductor is utilized to limit *di*/*dt*, it is inevitable to have an overcurrent through the snubber diodes because of the commutations of the other switching legs. The active-clamping technique has been applied in [16]. Conduction and switching losses are reduced because of the active snubber circuit that provides zero-voltage switching conditions for all switches. However, the voltage stress of power devices is increased higher than the dc-link voltage. Passive snubber circuit and active snubber circuit approaches require many switching devices to reduce switching-power losses. It causes a high cost and complicates the layout design of the inverter. The proposed inverter is compared with the recently presented approaches as well as the conventional approaches. *RCD* snubber can be classified as the switch-side snubber and the bus-side snubber [17]. The *RCD* snubber presented in [17] is used because of its simple topology, high reliability, and low cost. However, the series resistor in the snubber circuit makes contributes to energy loss, similar to the reference [13]. The three-phase quasi-Z-source inverter (qZSI) presented in [18] is used due to effectively reduced number of switch commutations, resulting in reduced switching-power losses. However, modulation methods of the qZSI are more complicated than the standard VSI. The zero-voltage switching (ZVS) three-phase four-wire inverter presented in [19,20] can achieve the zero-voltage switching operation of all switches, including the main switches and the auxiliary switch. However, the voltage stress of power devices is higher than the input dc voltage, similar to the reference [16].

To solve the above-mentioned shortcomings, we present a three-phase SOI using magnetically coupled inductor switching technique. Figure 2 shows the circuit diagram of the proposed inverter. In the proposed inverter, for each switching leg, by using only one auxiliary diode and adding one coupled winding to the inductor, the current through the original diode can be steered to an auxiliary diode and can be reduced to zero before the power switch is turns on. The leakage inductors in the coupled inductor are used for *di*/*dt* control. The proposed inverter mitigates current overshoots and voltage oscillations of SiC schottky diodes, reducing switching-power losses. It achieves higher power efficiency than does the conventional inverter. Also, the advantages of the proposed inverter are compared with not only conventional inverter but also other approaches [13–16]. The proposed inverter is better than others in respect of the number of components, switching-power loss, and efficiency. Section 2 describes the configuration, operation, control, and modulation of the proposed inverter. Section 3 discusses the simulation results, experimental results, and power-loss analysis for a 1.0 kW prototype inverter. Finally, the conclusion is presented in Section 4.

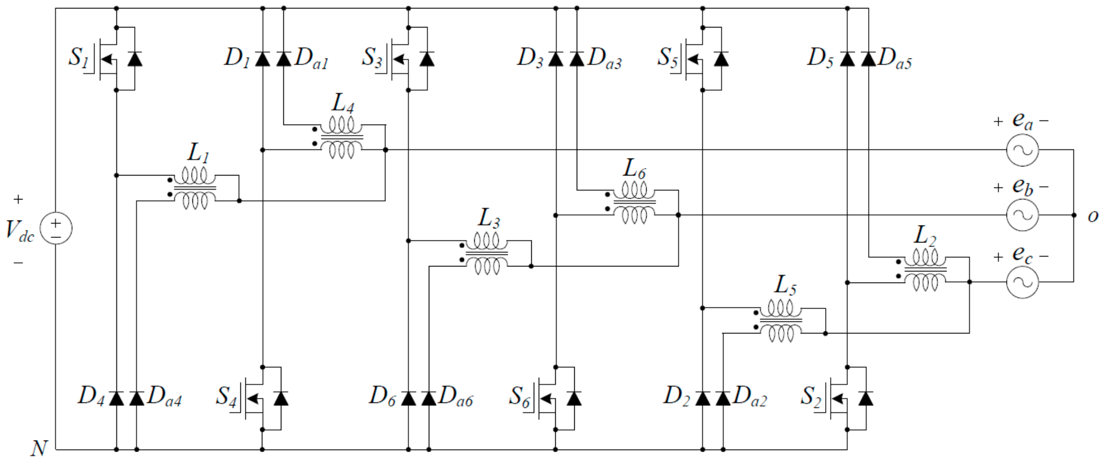
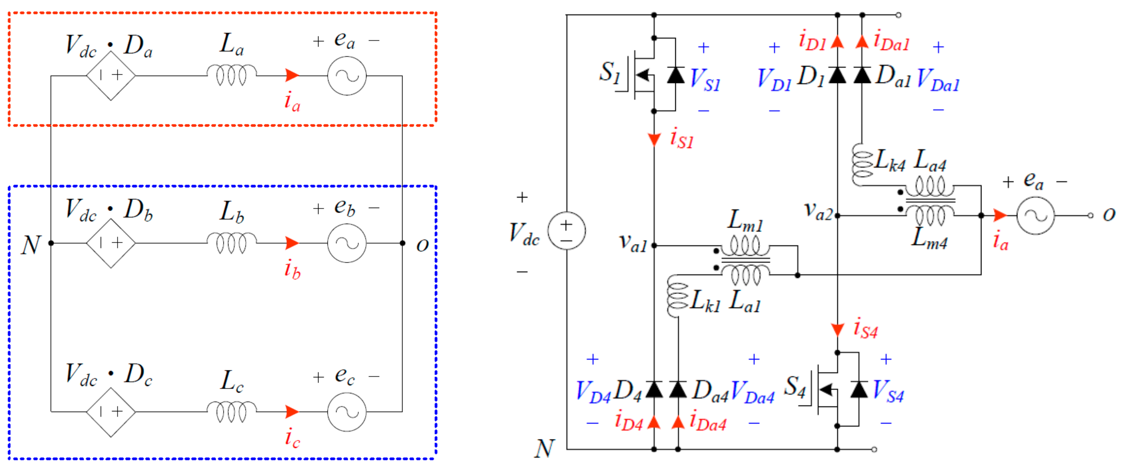


Figure 2. Circuit diagram of the proposed inverter.

2. Proposed Inverter

2.1. Inverter Configuration

Figure 2 shows the circuit diagram of the proposed inverter. The proposed inverter consists of SiC MOSFETs (S_1~S_6), SiC schottky diodes (D_1~D_6), auxiliary SiC schottky diodes (D_{a1}~D_{a6}), and coupled inductors (L_1~L_6). The main and auxiliary windings of each coupled inductor are connected together. They are also connected to the mid-junction of each switching leg. V_{dc} is the dc-link voltage. N is the negative dc-link voltage. e_a, e_b, and e_c are the phase voltage. o is the neutral point of the three-phase voltage. Dead-time is not necessary because when S_1 operates, S_4 is always turned off and vice versa. The output waveforms are more sinusoidal, and the energy is transferred more perfectly without the dead-time compensation. Assumed that the switching frequency is much higher than the grid frequency, the three-phase switching legs can be considered as three-phase voltage-controlled voltage-sources. Its equivalent switching-cycle average model can be derived, as shown in Figure 3a. In Figure 3a, D_a, D_b, and D_c are the duty ratio for switches S_1, S_3, and S_5, respectively. i_a, i_b, and i_c are the phase current, respectively. Figure 3b shows the circuit diagram for A-phase, which shows the reference directions of currents and voltages. The circuit diagram in Figure 3b can be applies to the B-phase and C-phase equivalently. The coupled inductors are modeled as a combination of the magnetizing inductors (L_{m1}~L_{m6}), auxiliary winding inductors (L_{a1}~L_{a6}), and leakage inductors (L_{k1}~L_{k6}). The auxiliary winding has a slightly larger number of turns than does the main winding. The leakage inductors are considered to be at the auxiliary winding of the coupled inductor.

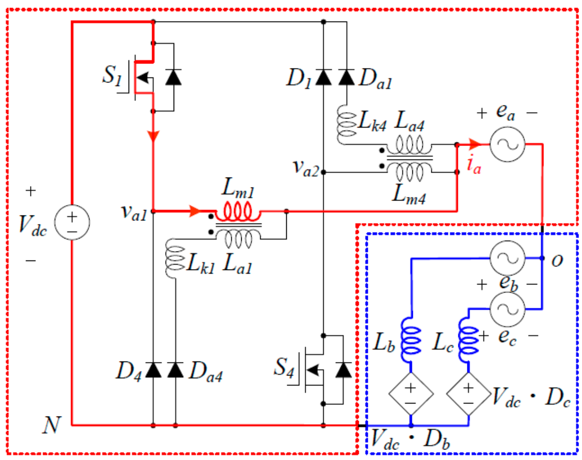


(**a**) (**b**)

Figure 3. Switching-cycle average model and circuit diagram of the proposed inverter with reference directions of currents and voltages for *A*-phase: (**a**) switching-cycle average model; (**b**) circuit diagram for *A*-phase.

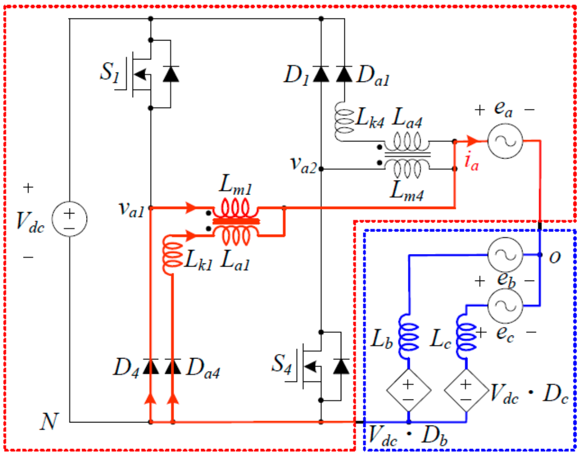
2.2. Steady-State Operation

Figure 4 shows switching-circuit diagrams of the proposed inverter during one switching period T_s for the positive cycle of the phase voltage e_a. The operations of switching devices are determined by the phase current. Take *A*-phase, for example; when i_a is positive, S_1, D_4, and D_{a4} are the operating devices, and when i_a is negative, S_4, D_1, and D_{a1} are the operating devices. Figure 5 shows the steady-state operation waveforms during T_s for the positive cycle of the phase voltage e_a. *Stage I*, *Stage II*, and *Stage III* in Figure 4 represent the current paths when i_a is positive. Figure 5 shows the corresponding steady-state operation waveforms when i_a is positive.



(**a**)

Figure 4. *Cont.*



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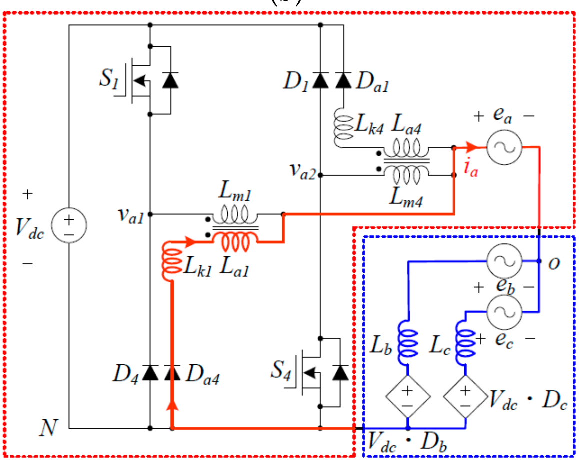


(**c**)

Figure 4. Switching-circuit diagrams of the proposed inverter during T_s for the positive cycle of the phase voltage e_a: (**a**) *Stage I*, (**b**) *Stage II*; (**c**) *Stage III*.

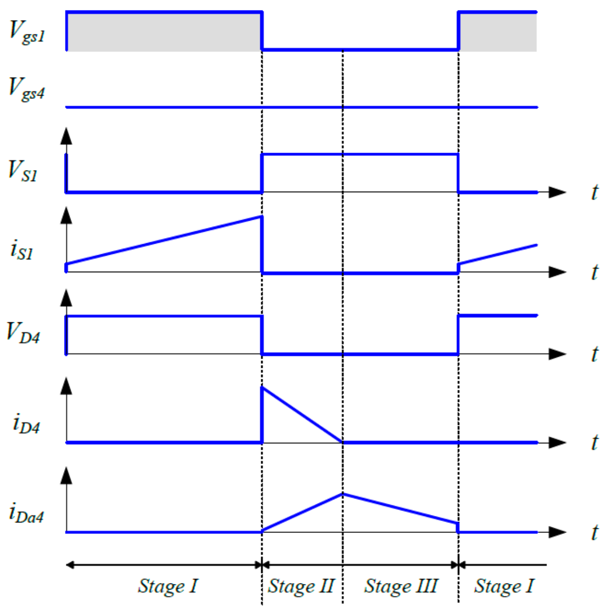


Figure 5. Steady-state operation waveforms corresponding to the switching circuit diagrams of the proposed inverter during T_s for positive cycle of the phase voltage e_a.

In *Stage I*, the switch S_1 is turned on and the diodes D_4 and D_{a4} are turned off. When S_1 is turned on, the energy of the magnetizing inductor L_{m1} is linearly charged by the dc-link voltage V_{dc}. Since diodes D_4 and D_{a4} are reverse-biased, L_1 operates like a simple inductor even though it is a coupled inductor. The phase current i_a flows through V_{dc}, S_1, L_{m1}, and e_a. In this *Stage I*, the auxiliary winding of the coupled inductor L_1 does not work.

In *Stage II*, the switch S_1 is turned off and the diodes D_4 and D_{a4} are turned on. Because S_1 is turned off, the energy stored in the magnetizing inductor L_{m1} is released to the output side through the main diode D_4 and auxiliary diode D_{a4}. In this *Stage II*, both main and auxiliary windings of the coupled inductor L_1 work. When S_1 is turned off, the main diode D_4 is immediately turned on by the inductor current freewheeling. By the auxiliary winding of the coupled inductor L_1, the voltage across the auxiliary winding is produced in an ideal turns ratio relationship. Then, auxiliary diode D_{a4} is turned on. The phase current i_a flows through L_{m1}, e_a, and D_4. Simultaneously, i_a flows through L_{a1}, e_a, D_{a4}, and L_{k1}. Because the auxiliary winding of the coupled inductor L_1 has a slightly larger number of turns than does the main winding, a positive voltage is applied to the leakage inductor L_{k1}. The current of the main diode D_4 keeps decreasing to zero current and the current through L_{k1} increases linearly. The current-shifting process from the main diode D_4 to the auxiliary diode D_{a4} begins.

In *Stage III*, the main diode D_4 is turned off and auxiliary diode D_{a4} is still turned on. If the leakage inductor L_{k1} is provided with sufficient charge voltage and time, the phase current i_a is completely shifted to the new branch through diode D_{a4}. Since switch S_1 is still turned off and current of the main diode D_4 is zero, L_1 operates like a simple inductor even though it is a coupled inductor, and no current flows through L_{m1}. By the operation of coupled inductor, the main diode current is shifted to the auxiliary diode without the reverse-recovery process. The auxiliary diode current i_{Da4} decreases linearly. This switching state ends when S_1 is turned on again.

The steady-state operation for the negative cycle of the phase voltage e_a is not descried here, because it can be explained similarly to the steady-state operation of the positive cycle of the phase voltage e_a.

Since the phase currents flow simultaneously, the steady-state operation principle applies to the *B*-phase and *C*-phase. For the *B*-phase, when i_b is positive, S_3, D_6, and D_{a6} are the operating devices, and when i_b is negative, S_6, D_3, and D_{a3} are the operating devices. For the *C*-phase, when i_c is positive, S_5, D_2, and D_{a2} are the operating devices, and when i_c is negative, S_2, D_5, and D_{a5} are the operating devices. For each switching leg, by using only one auxiliary diode and adding one coupled winding to the inductor, the current through the original diode can be steered to an auxiliary diode and can be reduced to zero before the switch turns on. The leakage inductor of the coupled inductor is used to control the di/dt.

In a practical design, the SiC schottky diodes suffer from significant current overshoots and voltage oscillations due to the resonance of *RLC* circuit formed by the diode parasitic resistance, stray inductance, and diode capacitance. Figure 6 shows the switching characteristic of the SiC schottky diode for one switching-leg. L_{stray} is the parasitic stray inductance. Figure 6a,b show the switching characteristic of the conventional inverter when the diode D_4 is turned on and turned off, respectively. Figure 6c,d show the switching characteristic of the proposed inverter when the diode D_{a4} is turned on and turned off, respectively. The steady-state operation of the proposed inverter is changed from *Stage III* to *Stage I*. In the conventional inverter, when the switch has started operating again as shown Figure 6b, the parasitic capacitances of the switch and the parasitic *RLC* circuit of the diode D_4 including L_{stray} resonate within the switching leg. Thus, the switch peak current and diode reverse-recovery peak current are quite high. These high currents cause switching-power losses, which reduce the power efficiency. On the other hand, in the proposed inverter, before the switch is turns on, the current through the original diode is already zero and the switch current flows through the magnetizing inductor. Thus, the reverse-recovery peak current and reverse-recovery time of the main diode are reduced. The current rising rate of the switch will be lowered, which can reduce the turn-on switching-power loss of the switch. Also, the current through the auxiliary diode at the end of *Stage III* can be limited by the leakage inductor of the auxiliary winding. Therefore, the reverse-recovery peak current and reverse-recovery time of the auxiliary diode are also reduced.

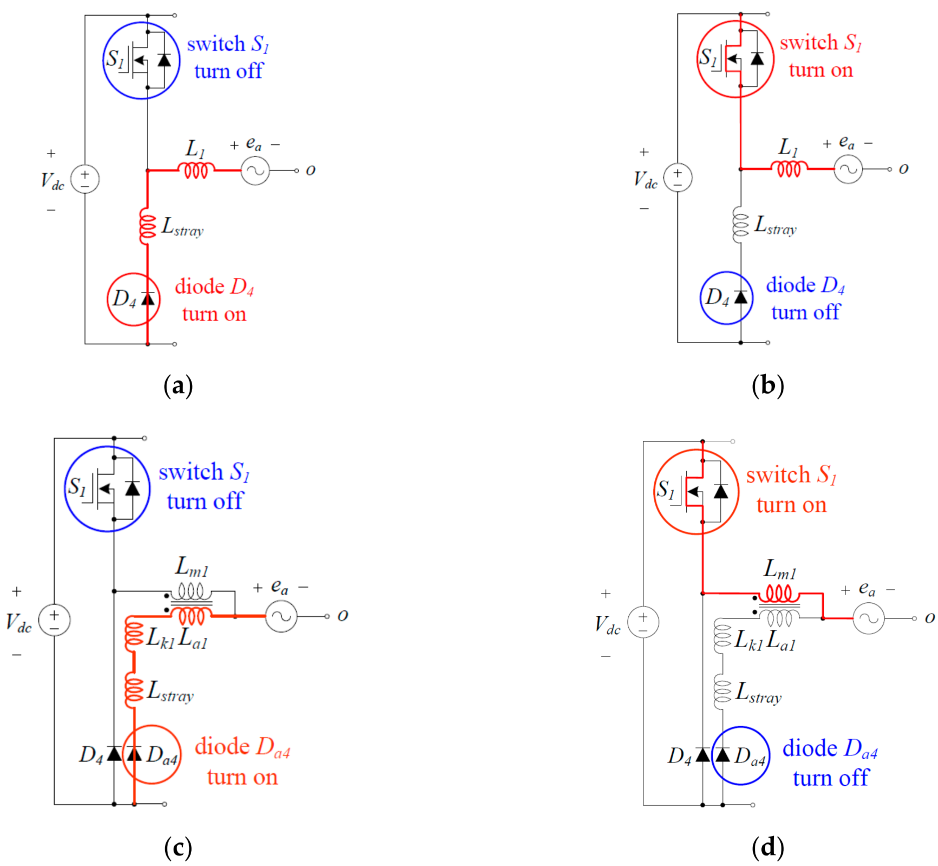


Figure 6. Switching characteristic of the SiC schottky diode for one switching leg: (**a**) D_4 turn on of the conventional inverter; (**b**) D_4 turn off of the conventional inverter (**c**); D_{a4} turn on of the proposed inverter; (**d**) D_{a4} turn off of the proposed inverter.

2.3. Contol and Modulation

The proposed inverter provides smooth powering and controls the phase currents i_a, i_b, and i_c for the unity power factor. The phase voltages e_a, e_b, and e_c are expressed as

$$e_a = E\cos(\omega t), \tag{1}$$

$$e_b = E\cos\left(\omega t - \frac{2}{3}\pi\right), \tag{2}$$

$$e_c = E\cos\left(\omega t - \frac{4}{3}\pi\right) \tag{3}$$

where E is the maximum phase voltage and ω is angular frequency. The phase-leg voltages v_{ao}, v_{bo}, and v_{co} are expressed as

$$v_{io} = \begin{cases} v_{i1} & \text{when } v_{io} > 0 \\ v_{i2} & \text{when } v_{io} \leq 0 \end{cases} \tag{4}$$

where $i = a, b, c$. The voltage equations in the stationary a-b-c frame are

$$e_a = -L\frac{di_a}{dt} + v_{ao}, \tag{5}$$

$$e_b = -L\frac{di_b}{dt} + v_{bo}, \tag{6}$$

$$e_c = -L\frac{di_c}{dt} + v_{co} \tag{7}$$

where coupled inductor L (=L_1~L_6) has the same value. The voltage equations in the synchronous d-q frame are

$$\begin{aligned}
\begin{bmatrix} e_d \\ e_q \end{bmatrix} &= \begin{bmatrix} \cos(\omega t) & \sin(\omega t) \\ -\sin(\omega t) & \cos(\omega t) \end{bmatrix} \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} \\
&= \begin{bmatrix} \cos(\omega t) & \sin(\omega t) \\ -\sin(\omega t) & \cos(\omega t) \end{bmatrix} \left(-L\frac{d}{dt}\right) \begin{bmatrix} \cos(\omega t) & \sin(\omega t) \\ -\sin(\omega t) & \cos(\omega t) \end{bmatrix}^{-1} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} v_d \\ v_q \end{bmatrix} \\
&= -L\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} - \omega L \begin{bmatrix} -i_q \\ i_d \end{bmatrix} + \begin{bmatrix} v_d \\ v_q \end{bmatrix}.
\end{aligned} \tag{8}$$

The grid voltages of the synchronous d-q frame are $e_d = E$ and $e_q = 0$. For the unity power factor, it is desirable that the i_q be zero. Then i_q is controlled with the zero reference current $i_q^* = 0$. The voltage equations from (5) to (7) are transformed from the stationary a-b-c frame to the synchronous d-q frame as follows

$$E = -L\frac{di_d}{dt} + \omega L i_q + v_d, \tag{9}$$

$$0 = -L\frac{di_q}{dt} - \omega L i_d + v_q. \tag{10}$$

The proportional and integral-type controllers do not work well as rapid tracking controllers in (9) and (10). To solve this problem, the following decoupling control is used as

$$v_d = E - \omega L i_q + \Delta v_d, \tag{11}$$

$$v_q = \omega L i_d + \Delta v_q \tag{12}$$

with the addition of the current controller (11) and (12) to the inverter (9) and (10), respectively, the input-output relations of the inverter become first-order decoupled linear systems as

$$0 = -L\frac{di_d}{dt} + \Delta v_d, \tag{13}$$

$$0 = -L\frac{di_q}{dt} + \Delta v_q \tag{14}$$

where the output signals Δv_d and Δv_q of the current controllers

$$\Delta v_d = k_{pd}\left(i_d^* - i_d\right) + k_{id}\int\left(i_d^* - i_d\right)dt, \tag{15}$$

$$\Delta v_q = k_{pq}\left(i_q^* - i_q\right) + k_{iq}\int\left(i_q^* - i_q\right)dt \tag{16}$$

where k_{pd} and k_{pq} are proportional control gains and k_{id} and k_{iq} are integral control gains, respectively. In terms of the conduction times T_a, T_b, and T_c of switches S_1, S_3, and S_5, the voltages v_{aN}, v_{bN}, and v_{cN} are expressed as

$$v_{aN} = \frac{V_{dc}}{T_s}T_a, \tag{17}$$

$$v_{bN} = \frac{V_{dc}}{T_s}T_b, \tag{18}$$

$$v_{cN} = \frac{V_{dc}}{T_s} T_c. \tag{19}$$

The neutral-point voltage v_{oN} of the balanced three-phase system is obtained by the superposition theorem as

$$v_{oN} = \frac{1}{3}\frac{V_{dc}}{T_s}\left(T_a + T_b + T_c\right). \tag{20}$$

The relation of the stationary *a*-*b*-*c* voltage components and the conduction times of switches are derived as

$$\begin{bmatrix} v_{ao} \\ v_{bo} \\ v_{co} \end{bmatrix} = \begin{bmatrix} v_{aN} - v_{oN} \\ v_{bN} - v_{oN} \\ v_{cN} - v_{oN} \end{bmatrix} = \frac{1}{3}\frac{V_{dc}}{T_s}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} T_a \\ T_b \\ T_c \end{bmatrix}. \tag{21}$$

In *Region* 1, substituting $T_c = 0$ into equation (21) when using V_0 (0 0 0) as the zero vector, the conduction times of switches are obtained as

$$\begin{bmatrix} T_a \\ T_b \\ T_c \end{bmatrix} = \frac{T_s}{V_{dc}}\begin{bmatrix} v_{ao} - v_{co} \\ v_{bo} - v_{co} \\ 0 \end{bmatrix} \tag{22}$$

where the stationary *a*-*b*-*c* voltage components are given by

$$\begin{bmatrix} v_{ao} \\ v_{bo} \\ v_{co} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} \cos\omega t & -\sin\omega t \\ \sin\omega t & \cos\omega t \end{bmatrix}\begin{bmatrix} v_d \\ v_q \end{bmatrix}. \tag{23}$$

Applying a similar procedure to all regions, the conduction times of switches for modulating the required space vector are simplified as

$$\begin{bmatrix} T_a \\ T_b \\ T_c \end{bmatrix} = \frac{T_s}{V_{dc}}\begin{bmatrix} v_{ao} - v_{\min} \\ v_{bo} - v_{\min} \\ v_{co} - v_{\min} \end{bmatrix} = \begin{bmatrix} T_s \\ T_s \\ T_s \end{bmatrix} - \begin{bmatrix} v_{\max} - v_{ao} \\ v_{\max} - v_{bo} \\ v_{\max} - v_{co} \end{bmatrix} \tag{24}$$

where $v_{min} = min\ (v_{ao}, v_{bo}, v_{co})$ and $v_{max} = max\ (v_{ao}, v_{bo}, v_{co})$. Figure 7 shows the control block diagram of the proposed inverter. The conduction times T_a, T_b, and T_c of switches S_1, S_3, and S_5 for three-phase PWM pulses are generated by the space-vector modulation technique without a computational burden such as square root and arctangent.

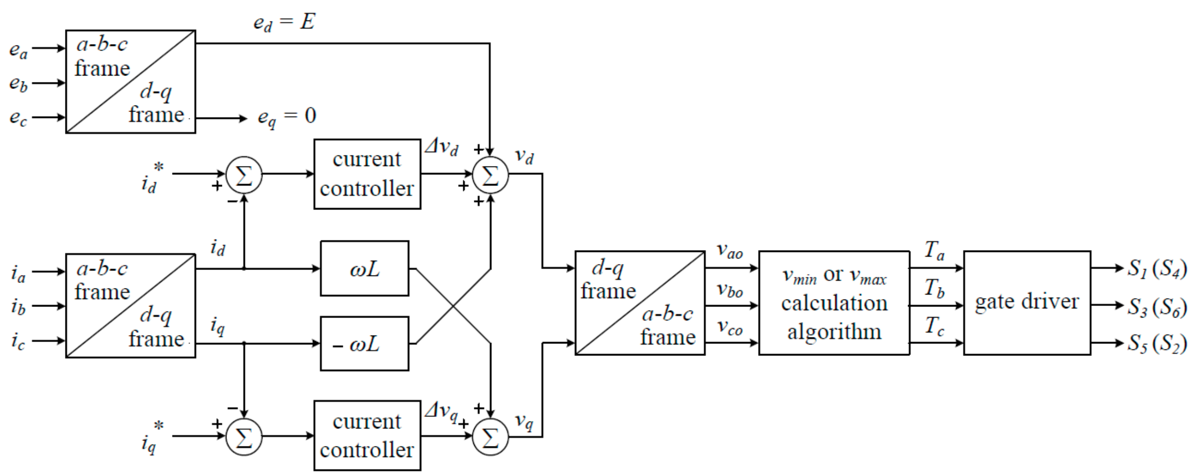


Figure 7. Control block diagram of the proposed inverter.

3. Simulation and Experimental Results

3.1. Simulation Results

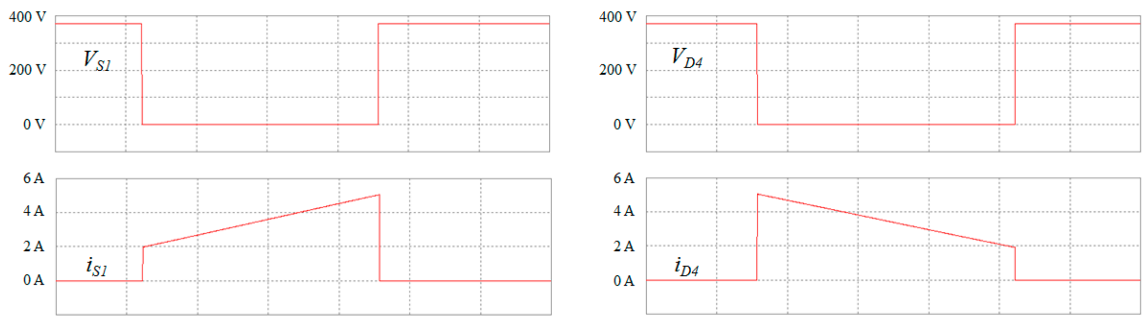
We executed a computer simulation for steady-state operation of the conventional inverter and the proposed inverter by using Physical Security Information Management (PSIM) software [21]. Table 1 shows the electrical specifications of the inverters. The dc-link voltage V_{dc} should be higher than the peak line-to-line voltage of the inverter. Then, the inverters will require minimum dc-link voltage of 311 V. In addition, the voltage margin, modulation index, and device voltage rating must be taken into account. Thus, we selected the dc-link voltage of 370 V.

Table 1. Electrical specifications of the inverters.

Symbol	Quantity	Value
V_{dc}	dc-link voltage	370 V
e_a, e_b, e_c	phase voltages	60 Hz/127 V_{rms}
e_{ab}, e_{bc}, e_{ca}	line-to-line voltages	60 Hz/220 V_{rms}
f_s	switching frequency	50 kHz
P_o	output power	1.0 kW

Figure 8 shows the simulation results of the conventional inverter in Figure 1 when V_{dc} is 370 V, e_a, e_b, and e_c are 127 V_{rms}. Figure 8a shows V_{S1} and i_{S1}. Figure 8b shows V_{D4} and i_{D4}. As shown in Figure 8a,b, V_{S1} and V_{D4} are clamped to V_{dc}, and the slope of i_{S1} and i_{D4} is opposite.

Figures 9 and 10 show the simulation results of the proposed inverter when V_{dc} is 370 V, e_a, e_b, and e_c are 127 V_{rms}. Figure 9a shows V_{S1} and i_{S1}. Figure 9b shows V_{D4}, i_{D4}, and i_{Da4}. As shown in Figure 9a,b, the V_{S1} and V_{D4} are clamped to V_{dc} and the current through the original diode can be steered to an auxiliary diode and can be reduced to zero before the switch turns on. Figure 10 shows e_{ab}, e_{bc}, e_{ca}, and V_{dc}. Balanced line-to-line voltages are equal in magnitude and frequency and out of phase with each other by 120°.



(**a**) (**b**)

Figure 8. Simulation results of the conventional inverter: (**a**) V_{S1} and i_{S1}; (**b**) V_{D4} and i_{D4}.

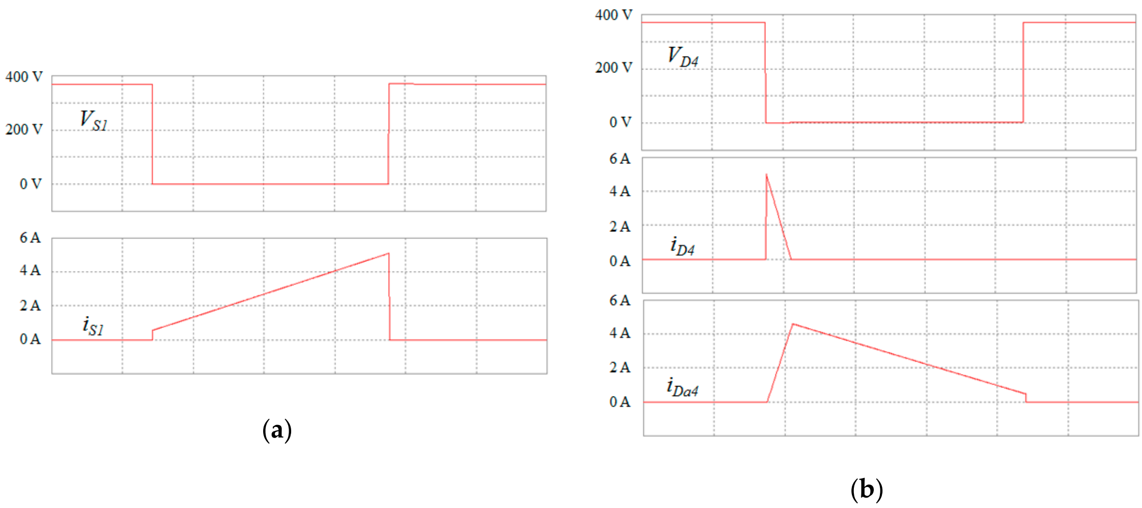


Figure 9. Simulation results of the proposed inverter: (**a**) V_{S1} and i_{S1}; (**b**) V_{D4}, i_{D4}, and i_{Da4}.

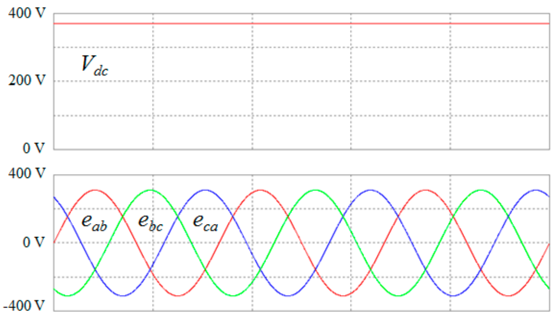


Figure 10. Simulation results of the proposed inverter: e_{ab}, e_{bc}, e_{ca}, and V_{dc}.

3.2. Experimental Results

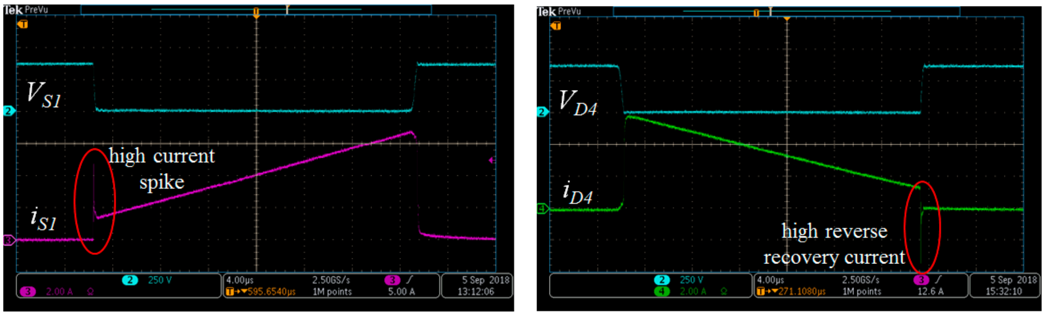
To evaluate the performance of the proposed inverter, we built and tested a 1.0 kW prototype inverter. The conventional inverter was also designed for the performance comparison with the proposed inverter. The electrical specifications of the prototype inverter are shown in Table 1. Table 2 shows the component parameters of the prototype inverter. The hardware prototype is divided into two parts: the microprocessor-based control circuit and the power circuit. We have implemented the control block diagram of the proposed inverter, as shown in Figure 7, by using a dsPIC30F6015 (Microchip Technology, Chandler, AZ, USA) 16-bit fixed point digital signal controller. We have measured the signals using an analog to digital converter in the microprocessor. The controllers have been executed for every sample period of 100 µs.

Table 2. Component parameters of the prototype inverter.

Symbol	Quantity	Value
S_1~S_6	power switches	UJC06505K
D_1~D_6	power diodes	C3D20060D
D_{a1}~D_{a6}	auxiliary power diodes	C3D20060D
L_1~L_6 (= L)	coupled inductors	CM508125
L_{m1}~L_{m6} (= L_m)	magnetizing inductances	1.0 mH
L_{a1}~L_{a6} (= L_a)	auxiliary winding inductances	1.1 mH
L_{k1}~L_{k6} (= L_k)	leakage inductances	5~20 µH

Figure 11 shows the experimental waveforms of the conventional inverter in Figure 1 when V_{dc} is 370 V, and e_a, e_b, and e_c are 127 V_{rms}. Figure 11a shows V_{S1} and i_{S1}. Figure 11b shows V_{D4} and

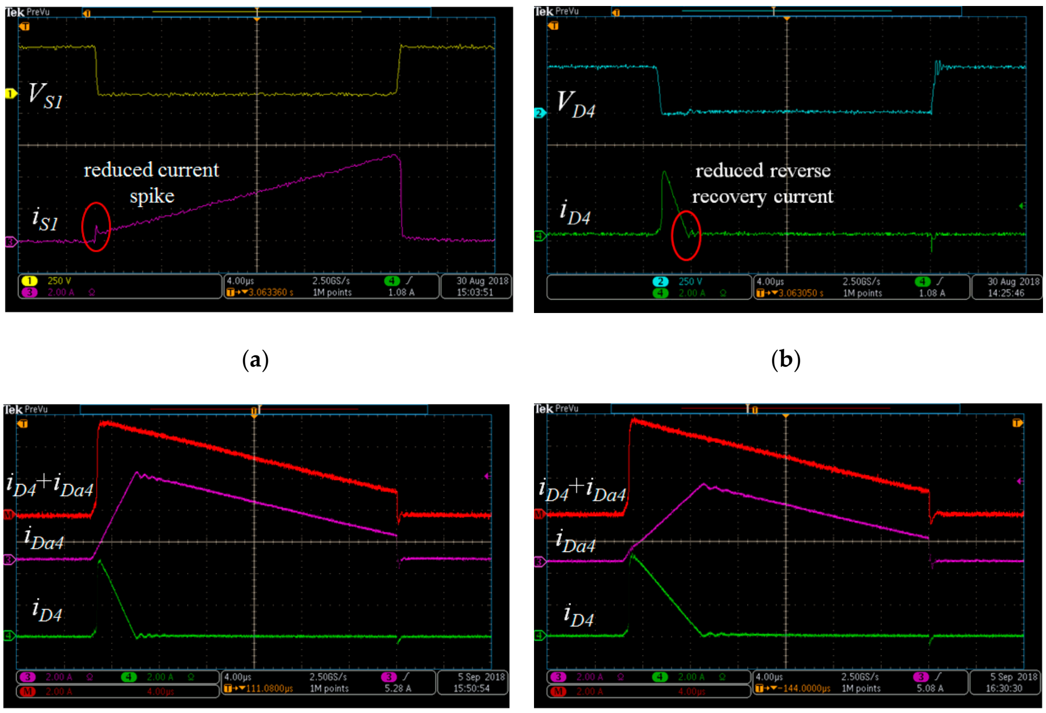
i_{D4}. The switch peak current and diode reverse-recovery peak current are quite high. As shown in Figure 11a,b, switching-power losses related to switch current and diode reverse-recovery current are increased, reducing the power efficiency of the inverter.



(**a**) (**b**)

Figure 11. Experimental waveforms of the conventional inverter: (**a**) V_{S1} and i_{S1}; (**b**) V_{D4} and i_{D4}.

Figure 12 shows the experimental waveforms of the proposed inverter in Figure 2 when V_{dc} is 370 V, and e_a, e_b, and e_c are 127 V_{rms}. Figure 12a shows V_{S1} and i_{S1}. Figure 12b shows V_{D4} and i_{D4}. As shown in Figure 12a,b, the switch peak current and diode reverse-recovery peak current are reduced, as is the reverse-recovery time. Therefore, switching-power loss related to the switch current and diode reverse-recovery current are dramatically reduced. Figure 12c shows i_{D4} + i_{Da4}, i_{D4} and i_{Da4} with L_k = 5 µH. Figure 12d shows i_{D4} + i_{Da4}, i_{D4} and i_{Da4} with L_k = 15 µH. As shown in Figure 12c,d, the experimental waveforms show the significant performance improvement attained by controlling the diode *di*/*dt*.

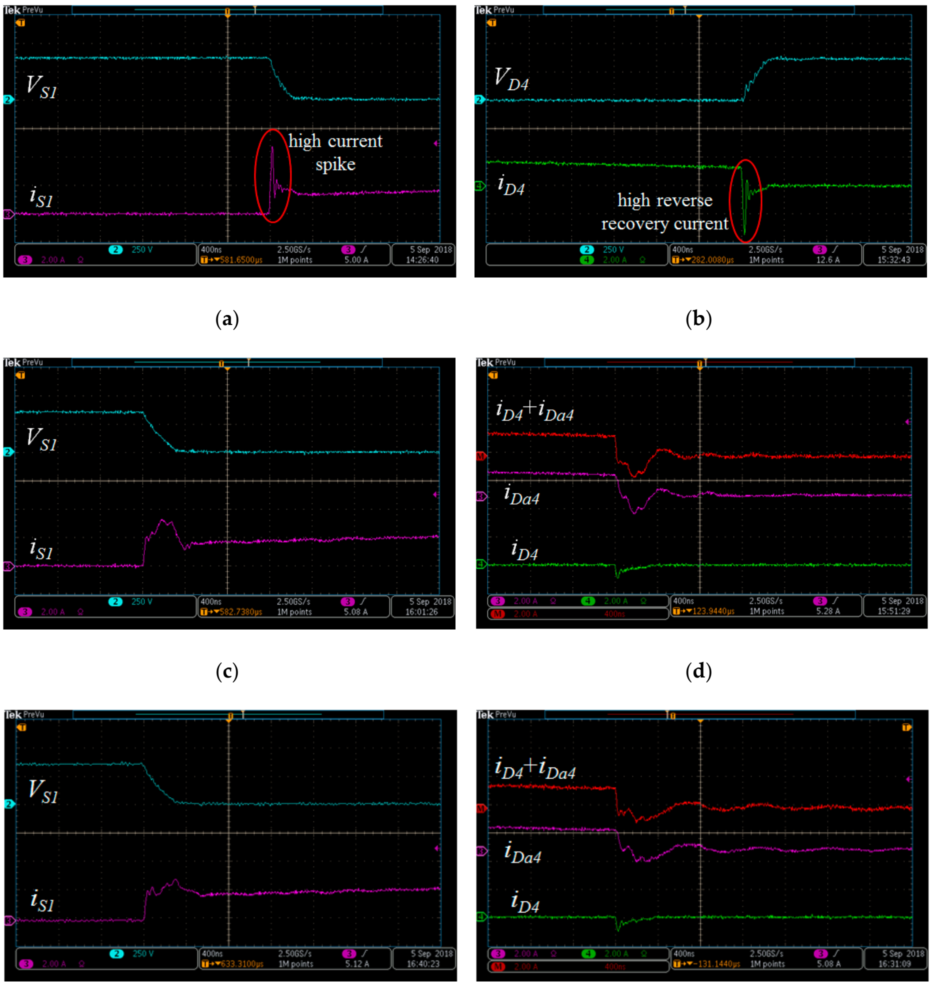


(**a**) (**b**)

(**c**) (**d**)

Figure 12. Experimental waveforms of the proposed inverter: (**a**) V_{S1} and i_{S1}; (**b**) V_{D4} and i_{D4}; (**c**) i_{D4} + i_{Da4}, i_{Da4} and i_{D4} with L_k = 5 µH; (**d**) i_{D4} + i_{Da4}, i_{Da4} and i_{D4} with L_k = 15 µH.

Figure 13 shows the experimental waveforms of the conventional inverter in Figure 1 and the proposed inverter in Figure 2 when V_{dc} is 370 V, and e_a, e_b, and e_c are 127 V_{rms}. Figure 13a shows V_{S1} and i_{S1} in the conventional inverter of the enlarged Figure 11a. Figuere 13b shows V_{D4} and i_{D4} in the conventional inverter of the enlarged Figure 11b. We observed in Figure 13a,b that there is a high switch current spike and the diode reverse-recovery current is increased, as shown in Figure 11a,b, which reduces the power efficiency of the inverter. Especially, Figure 13b shows significant output oscillations of the SiC schottky diode, which result from the ringing formed between the diode parasitic capacitance, parasitic stray inductance, and diode resistance. Figure 13c shows V_{S1} and i_{S1} with L_k = 5 µH in the proposed inverter of the enlarged Figure 12a. Figure 13d shows i_{D4} + i_{Da4}, i_{D4} and i_{Da4} with L_k = 5 µH in the proposed inverter of the enlarged Figure 12c. Figure 13e shows V_{S1} and i_{S1} with L_k = 15 µH in the proposed inverter. Figure 13f shows i_{D4} + i_{Da4}, i_{D4} and i_{Da4} with L_k = 15 µH in the proposed inverter of the enlarged Figure 12d. We observed from Figure 13c to 13f that the switch peak current and diode reverse-recovery peak current are reduced, as is the reverse-recovery time, as shown in Figure 12a,b. Also, the current oscillation has been much alleviated because the current through the original diode can be steered to an auxiliary diode by using magnetically coupled inductors.



(**a**) (**b**)

(**c**) (**d**)

(**e**) (**f**)

Figure 13. Experimental waveforms of the conventional inverter and the proposed inverter: (**a**) V_{S1} and i_{S1} in the conventional inverter; (**b**) V_{D4} and i_{D4} in the conventional inverter; (**c**) V_{S1} and i_{S1} with L_k = 5 µH in the proposed inverter; (**d**) i_{D4} + i_{Da4}, i_{Da4} and i_{D4} with L_k = 5 µH in the proposed inverter; (**e**) V_{S1} and i_{S1} with L_k = 15 µH in the proposed inverter; (**f**) i_{D4} + i_{Da4}, i_{Da4} and i_{D4} with L_k = 15 µH in the proposed inverter.

Figure 14 shows the experimental waveforms of the proposed inverter when V_{dc} is 370 V, e_a, e_b, and e_c are 127 V_{rms}. Figure 14a shows e_{ab}, e_{bc}, e_{ca}, and V_{dc}. Balanced line-to-line voltages are equal in magnitude and frequency and out of phase with each other by 120°. Figure 14b shows i_a, e_{bc}, and V_{dc} for a 1.0 kW output power.

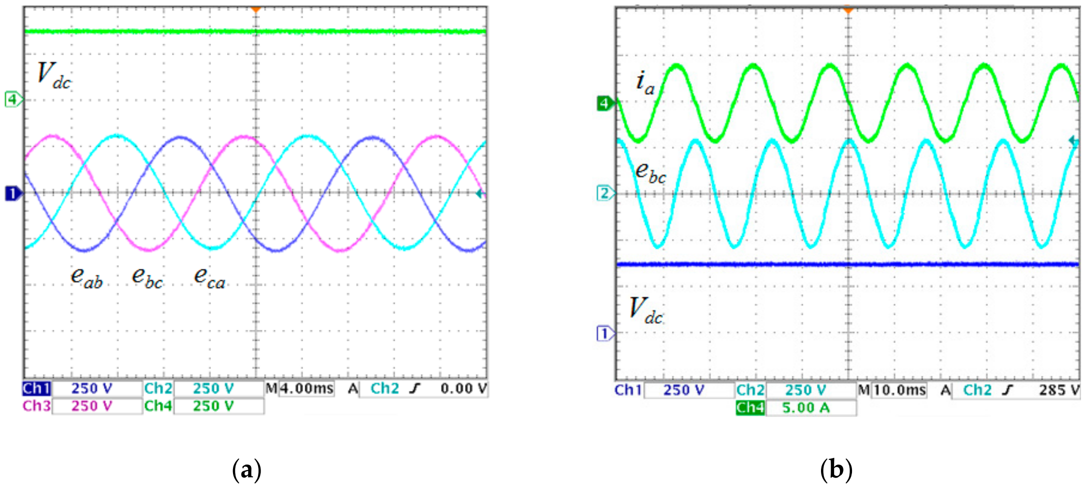


Figure 14. Experimental waveforms of the proposed inverter: (**a**) e_{ab}, e_{bc}, e_{ca} and V_{dc}; (**b**) i_a, e_{bc}, and V_{dc}.

Figure 15 shows the measured power efficiencies for the conventional inverter in Figure 1, the proposed inverter with L_k = 5 µH, and the proposed inverter with L_k = 15 µH, respectively. Figure 15a shows the power efficiencies of the inverters for different output power levels when V_{dc} is 370 V, and e_a, e_b, and e_c are 127 V_{rms}. The conventional inverter has the power efficiency of 97.6% at the rated power. On the other hand, the proposed inverter with L_k = 5 µH has improved power efficiency, achieving a power efficiency of 98.0% at the rated power. The proposed inverter improves the power efficiency by 0.4% compared to the conventional inverter by using magnetically coupled inductor switching technique. The proposed inverter with L_k = 15 µH has achieved a power efficiency of 98.2% for a 1.0 kW output power. Figure 15b shows the power efficiencies of the proposed inverter for different leakage inductances when V_{dc} is 370 V, and e_a, e_b, and e_c are 127 V_{rms}. The leakage inductances of the proposed inverter have major impact on the results. As shown in Figure 15b, the proposed inverter with L_k = 15 µH has achieved the highest efficiency compared to the extra leakage inductance. Both the proposed inverter with L_k = 10 µH and L_k = 20 µH have achieved a power efficiency of 98.1% at the rated power. If the leakage inductance is lower than 5 µH, the proposed inverter does not operate normally. On the other hand, if the leakage inductance is higher than 15 µH, the conduction loss of the coupled inductor increases, decreasing the power efficiency. The minimum value of the leakage inductance that the proposed inverter can operate normally is 5 µH, and the maximum value of the leakage inductance that the proposed inverter can achieve high efficiency is 15 µH. Figure 15c shows the power efficiencies of the inverters for different dc-link voltage levels at the rated power. As shown in Figure 15c, the maximum power efficiency of the inverters is dc-link voltage of 370 V at the rated power. If the dc-link voltage is lower than 370 V, the modulation index is very high. High modulation index causes switching-power loss, decreasing the power efficiency. On the other hand, if the dc-link voltage is higher than 370 V, the voltage stress of switching devices is very high. The use of high-rating switching devices causes the high cost as well as low efficiency.

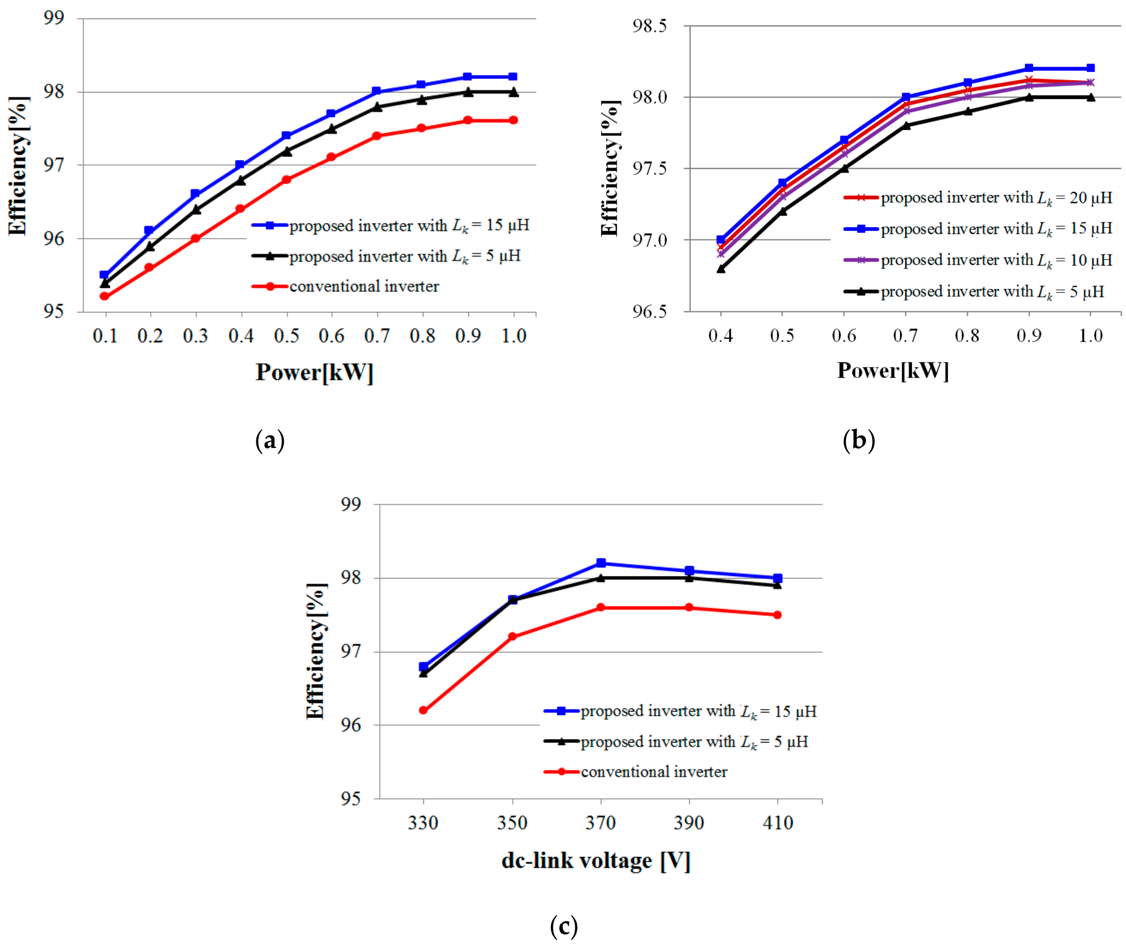


Figure 15. Measured power efficiencies of the inverters: (**a**) for different output power levels when V_{dc} is 370 V, and e_a, e_b, and e_c are 127 V_{rms}; (**b**) for different leakage inductances when V_{dc} is 370 V, and e_a, e_b, and e_c are 127 V_{rms}; (**c**) for different dc-link voltage levels at the rated power.

3.3. Power Loss Analysis

In order to analysis the power loss for a switching device, switching characteristics are presented, as shown in Figure 16. Figure 16a shows the switching waveforms and instantaneous switching-power loss. During the turn-on transition of the switching device, the current build-up consists of a short delay time $t_{d(\mathrm{on})}$ followed by the current rise time t_{ri}. The voltage falls to a small on-state value of V_{on} with a voltage fall time of t_{fv}. Then, the energy dissipated in the device during this turn-on transition can be approximated as

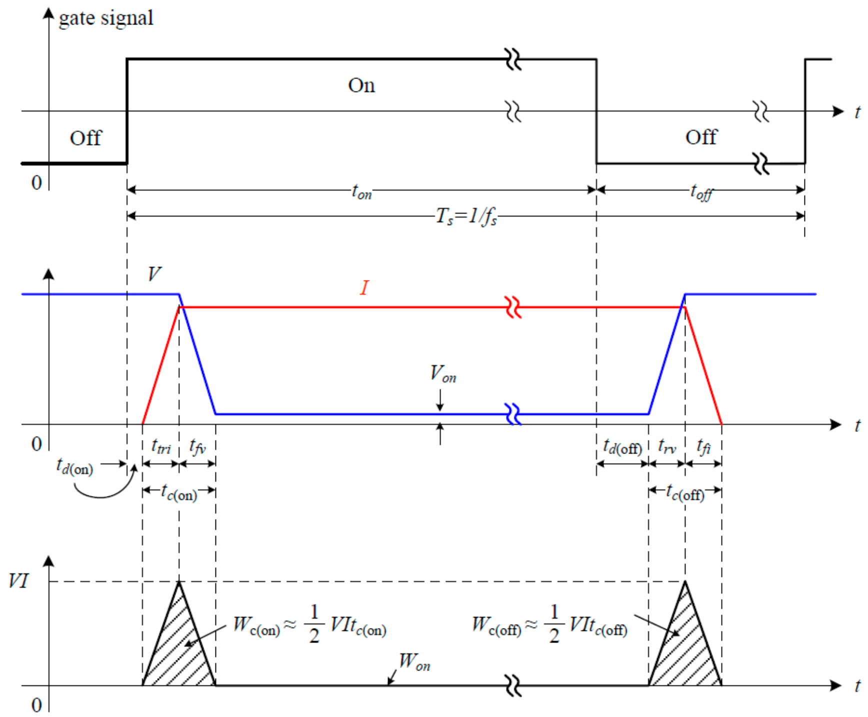
$$W_{c(on)} \approx \frac{1}{2} VIt_{c(on)} \tag{25}$$

where it is recognized that no energy dissipation occurs during the turn-on delay interval $t_{d(\mathrm{on})}$. During the turn-off transition period of the switching device, the voltage build-up consists of a turn-off delay time $t_{d(\mathrm{off})}$ and a voltage rise time t_{rv}. The current falls to zero with a current fall time t_{fi}. Then, the energy dissipated in the device during this turn-off transition can be written as

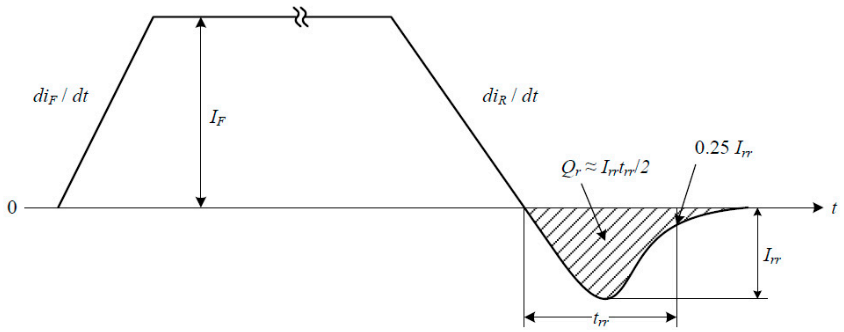
$$W_{c(off)} \approx \frac{1}{2} VIt_{c(off)} \tag{26}$$

where any energy dissipation during the turn-off delay interval $t_{d(\mathrm{off})}$ is ignored since it is small compared to $W_{c(\mathrm{off})}$. Therefore, the average switching-power loss P_s because of these transitions can be approximated from (25) and (26) as

$$P_s = \frac{1}{2} VIf_s \left(t_{c(on)} + t_{c(off)} \right). \tag{27}$$



(**a**)



(**b**)

Figure 16. Switching characteristics: (**a**) switching waveforms and instantaneous switching-power loss; (**b**) current waveform for a power diode.

Figure 16b shows the current waveform for a power diode. The time interval t_{rr} is the reverse-recovery time, the current I_{rr} is the reverse-recovery current, i_F is forward current, and i_R is the reverse current. Therefore, reverse-recovery charge Q_r can be approximated as

$$Q_r \approx \frac{1}{2} I_{rr} t_{rr}. \tag{28}$$

Figure 17 compares the loss breakdown plots of the inverters for a 1.0 kW output power. The proposed inverter with L_k = 15 μH achieves the power efficiency of 98.2% at 1.0 kW, resulting in power losses of 18 W. The proposed inverter with L_k = 5 μH achieves the power efficiency of 98.0%, resulting in power losses of 20 W. On the other hand, the conventional inverter achieves the power efficiency of 97.6%, resulting in power losses of 24 W. P_{Loss_Cond} is the conduction losses of switching devices including SiC MOSFETs and SiC schottky diodes. P_{Loss_Switch} is the switching losses of the SiC MOSFETs. P_{Loss_Diode} is the reverse-recovery loss of the SiC schottky diodes. P_{Loss_Ind} is the core losses of the coupled inductors. P_{Loss_Total} is the total power losses. The core losses of the proposed inverter because of the coupled inductors are high compared with those of the conventional inverter. However, the switching losses and the reverse-recovery losses of the proposed inverter are reduced remarkably.

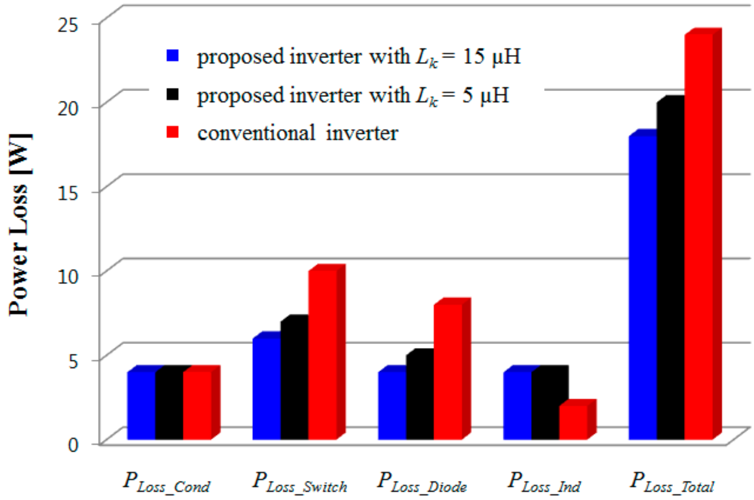


Figure 17. Loss breakdown plots of the inverters for a 1.0 kW output power.

Table 3 shows the comparison results of different approaches for reducing switching-power losses. It shows that the required components in each switching leg, advantages, and drawbacks. Compared with the proposed inverter, the *RC* snubber in [13] has a simple structure and low cost, but its efficiency very low because it dissipates the switching-power loss in the resistor. Passive lossless snubber in [14] can achieve zero-current turn on and zero-voltage turn off, but it requires many components and increases system complexity. Moreover, additional feedback circuit is required. Undeland snubber in [15] has a relatively simple structure, but it requires additional circuits of regenerative and dissipative. Active-clamping circuit in [16] provides zero-voltage switching conditions for all switches, but voltage stress of power devices is increased higher than the dc-link voltage. The use of high-rating switching devices causes the high cost as well as low efficiency. The proposed inverter is compared with the recently presented approaches as well as the conventional approaches. Compared with the proposed inverter, the bus-side *RCD* snubber presented in [17] has the advantages of simple topology, high reliability, and low cost. However, the series resistor in the snubber circuit makes contributes to energy loss, similar to the reference [13]. The qZSI presented in [18] effectively reduced number of switch commutations, resulting in reduced switching-power losses. However, modulation methods of the qZSI are more complicated than the proposed inverter. The ZVS three-phase four-wire inverter presented in [19,20] can achieve the zero-voltage switching operation of all switches, including the main switches and the auxiliary switch. However, the voltage stress of power devices is higher than the input dc voltage, similar to the reference [16]. For such a reason, the proposed inverter is superior to other different approaches in the state of art.

Table 3. Comparison results of different approaches for reducing switching-power losses.

	Components	Advantages	Drawbacks
RC snubber in [13]	resistor × 1 capacitor × 1	simple structure, high reliability, and low cost	low efficiency
Passive lossless snubber in [14]	diode × 4 inductor × 2 capacitor × 2 coupled inductor × 2	zero-current turn on and zero-voltage turn off	additional circuit, complex structure, and high cost
Undeland snubber in [15]	diode × 2 inductor × 1 capacitor × 1	simple structure of snubber	additional circuit, voltage and current oscillations
Active-clamping circuit in [16]	switch × 1 inductor × 1 capacitor × 1	zero-voltage switching	high voltage stress of power device
Bus-side *RCD* snubber in [17]	diode × 1 resistor × 1 capacitor × 1	simple structure, high reliability, and low cost	low efficiency
qZSI in [18]	diode × 1 inductor × 2 capacitor × 2	reduced number of switch commutations	complex modulation method
ZVS four-wire inverter in [19,20]	switch × 1 inductor × 1 capacitor × 1	zero-voltage switching	high voltage stress of power device
Proposed inverter	diode × 1 coupled inductor × 1	reducing switching-power losses	-

4. Conclusions

We have proposed a three-phase SOI with SiC devices using magnetically coupled inductor switching. The proposed inverter improves the power efficiency by using a magnetically coupled inductor switching technique. The current through the original diode can be steered to a new branch to reduce the significant output oscillations of the conventional inverter. We have discussed the configuration, steady-state operation, control, and modeling of the proposed inverter. In addition, the proposed solution is compared not only with conventional solutions [13–16] but also with recent solutions [17–20]. The proposed solution reduces switching-power losses simply and effectively, compared to the previous solutions, which require additional circuits, complex modulation methods, and high voltage stresses of power device. We have designed and tested a 1.0 kW prototype inverter to verify the performance of the proposed inverter. The proposed inverter improves the power efficiency more than does the conventional inverter by alleviating the voltage oscillations of SiC schottky diodes.

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