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A Low-Dropout Regulator with PSRR Enhancement through Feed-Forward Ripple Cancellation Technique in 65 nm CMOS Process

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Abstract: In this paper, a low-dropout (LDO) regulator with an enhanced power supply rejection ratio (PSRR) is proposed with a feed-forward ripple cancellation technique (FFRC) in 65 nm CMOS technology. This technique significantly improves the PSRR over a wide range of frequencies, compared to a conventional LDO regulator. The LDO regulator provides 35–76.8 dB of PSRR in the range of 1 MHz–1 GHz, which shows up to 30 dB of PSRR improvement, compared with that of the conventional LDO regulator. The implemented LDO regulator has a dropout voltage of 0.22 V and a maximum load current of 20 mA. It can also provide an output voltage of 0.98 V at a range of 1–1.3 V of the input voltage. The load regulation is 2.3 mV/mA while the line regulation is 0.05 V/V. The circuit consumes 385 µA with an input voltage of 1.2 V. The total area without pads is 0.092 mm^2.

Keywords: CMOS; LDO; low dropout; power supply rejection ratio; regulation

1. Introduction

In the power management system, the demand for integrating the whole power management integrated circuit (PMIC) into a single chip has significantly increased [1]. By integrating the power management system into a chip, the system cost is reduced significantly, since the external power management blocks can be dramatically simplified. The main reason for using a low-dropout (LDO) regulator is to reject the ripples from the voltage source, which means power supply rejection (PSR) is vital. For a conventional LDO regulator, it is necessary to have a high DC gain and bandwidth of the error amplifier [2]. For the voltage regulators, the bandwidth of the circuit should be improved and must provide a higher power supply rejection (PSR) according to the surrounding blocks. Conventional LDO regulators provide poor PSR at relatively high frequencies even around 300 kHz.

Various techniques have been introduced to improve PSR. Using an RC filter at the output of the LDO regulator or using two regulators helps to improve the PSR [3]. This technique can improve the PSR, but it also increases the dropout voltage because of the series resistor or the second regulator. Another technique is using a charge pump and an NMOS pass transistor [4]. This method utilizes an NMOS pass transistor which requires that the bias of the NMOS should be higher than the supply voltage. [4] implemented a charge pump in order to provide a higher bias which is an independent bias for the regulator. However, this technique dissipates more DC power and increases the complexity of the circuit.

In this paper, we introduce an LDO regulator which achieves a significantly improved PSR by utilizing the feed-forward ripple cancellation technique. The purpose of this technique is to duplicate the input ripples to the gate of the pass transistor so that it will cancel out the input ripples to increase

the power supply rejection significantly. The proposed LDO regulator consists of a three-stage error amplifier (EA), a summing amplifier (SA), and a feed-forward amplifier (FFA), which helps to increase the PSR and provide a robust output voltage. To precisely control the gain of the summing amplifier, we employ a variable resistor consisting of MOS switches and a binary resistive bank which can change the total resistance linearly with the control bits. This paper is structured as follows. Section 2 describes the operation of a conventional LDO regulator and describes various techniques used to improve the PSR of an LDO regulator. Section 3 explains the circuit design of the proposed LDO regulator, and the measurements for the proposed LDO regulator are presented in Section 4, followed by the conclusion in Section 5.

2. Techniques Used in Low-Dropout Regulator for the Enhanced Power Supply Rejection Ratio (PSRR)

A conventional LDO regulator, shown in Figure 1, includes a pass transistor M_{pass} and an error amplifier for comparing the voltage of the feedback circuit and V_{ref}. The conventional LDO regulator has three paths by which the noise can couple with the output of the LDO regulator. The first path is through the pass transistor, the second path is from the error amplifier which is connected with the supply voltage, VDD, and the third path is from the V_{ref}. The first path is mainly dependent on the feedback network produced by R_1 and R_2 at low frequencies. As the frequency starts to increase, the load capacitance, C_L, takes the role of getting rid of the input ripples. However, the equivalent self-inductance and resistance of the capacitor C_L will reduce the effect [1]. The PSR of the second path is limited by the DC gain and bandwidth of the error amplifier. Therefore, the challenge of the error amplifier is that both DC gain and bandwidth have to be large. At high frequencies, the effect of the second path is weak due to the capacitance seen at the gate of the pass transistor. The PSR of the third path is limited by the bandgap reference or the bias voltage source.

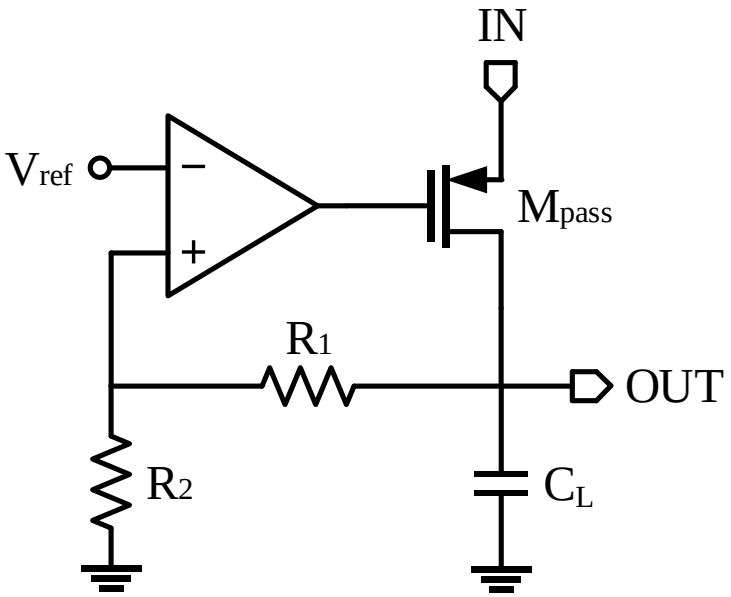

Figure 1. The schematic diagram of the conventional low-dropout regulator.

3. Proposed LDO Regulator Circuit Design

The schematic diagram of the proposed low-dropout regulator is shown in Figure 2. To have a clean output voltage, a zero-transfer gain from the input to the output is required. To achieve the zero-transfer gain in an ideal case, a feed-forward ripple cancellation technique is used in the proposed LDO regulator. A feed-forward path carries the same input ripples through the feed-forward amplifier and the summing amplifier to the gate of the M_{pass}. Then, the ripples at the gate cancel out the ripples at the source of the M_{pass}. However, in the practical case, some of the ripples at the source leak through

the drain-source resistance ($r_{ds,pass}$) of the M_{pass}. Thus, to cancel out the additional ripples from $r_{ds,pass}$, the produced ripples at the gate of the M_{pass} should be higher in ripple amplitude [1]. The pass transistor (M_{pass}) is implemented using a PMOS transistor considering that the DC voltage level required at the gate is lower than the supply voltage VDD, while the NMOS pass transistor needs a higher DC voltage level at the gate. The length of the pass transistor is 0.1 um and the width is 1.5 mm.

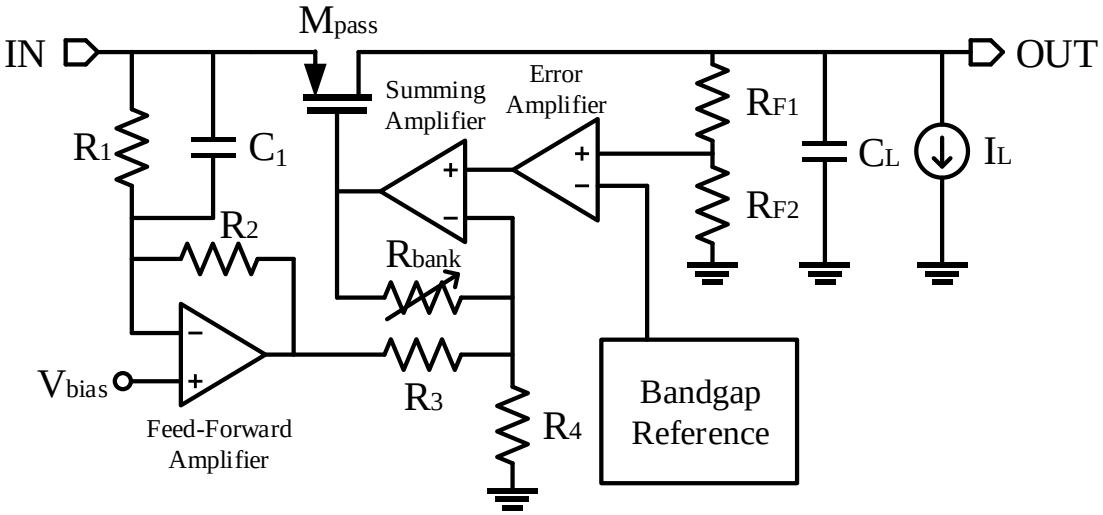

Figure 2. The schematic diagram of the proposed low-dropout regulator.

The error amplifier is implemented to have a feedback circuit and controls the output voltage with R_{F1} and R_{F2}. The summing amplifier's objective is to combine the signal from the feed-forward path with the feedback regulating loop. The summing feedback resistances (R_3, R_4, R_{bank}) push the output pole higher so that it is higher than the gain bandwidth (GBW) of the LDO regulator [1].

Figure 3 shows the transistor-level schematic diagram of the feed-forward, summing, and error amplifier implemented in the proposed LDO regulator. Specific size and parameters are given in Table 1. The operational transconductance amplifier (OTA) consists of a differential amplifier with active load, common source amplifier, compensating capacitor, and a series resistor next to the compensating capacitor. The differential amplifier with active load performs differential to single-ended conversion while maintaining the gain [5]. The capacitor C_C for compensation achieves pole-splitting in the circuit, which will affect the stability. The series resistor, R_{gd}, provides a left half-plane zero to compensate for the right half-plane zero that was produced by C_C.

Table 1. Parameters of the feed-forward, summing amplifier, and error amplifier.

	Feed-Forward Amp.	**Summing Amp.**	**Error Amp.**
M_1 [μm/μm]	10/1	10/1	5/1
M_2 [μm/μm]	10/1	10/1	5/1
M_3 [μm/μm]	25/1	25/1	15/1
M_4 [μm/μm]	25/1	25/1	15/1
M_5 [μm/μm]	27/1	50/1	95/1
M_6 [μm/μm]	12/1	8/1	6/1
M_7 [μm/μm]	12/1	-	6/1
M_8 [μm/μm]	12/1	12/1	26/1
M_9 [μm/μm]	12/1	12/1	26/1
C_C [pF]	4	4	1
R_{gd} [kΩ]	4	5	-

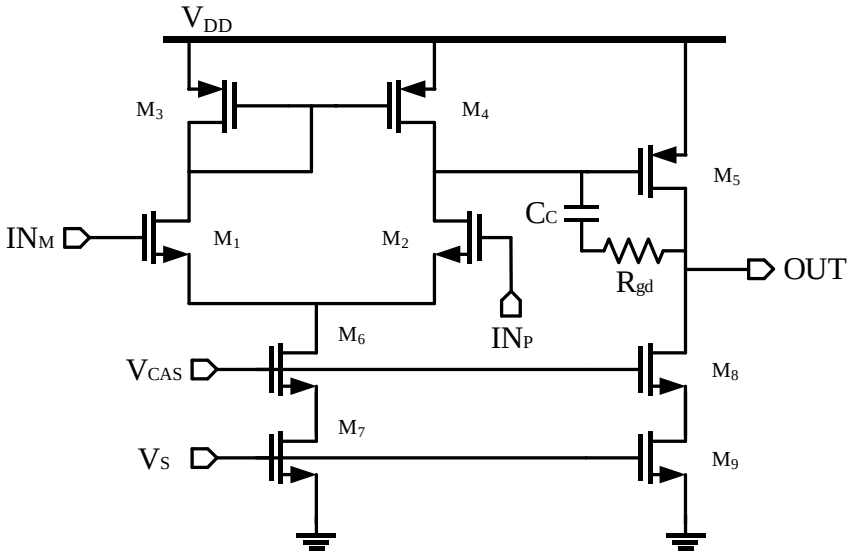

Figure 3. Schematic of the feed-forward, the summing amplifier, and the error amplifier.

For the resistive bank (R_{bank}) presented in Figure 2, it is implemented to cover the range of resistance from 750 Ω to 1125 Ω in the typical process condition. Considering the process variation of the polyresistor and the active device, the designed resistive bank was designed to provide the correct summing gain over the possible process variation. Figure 4 presents the schematic diagram of the proposed resistive bank. The aimed resistance of the resistor bank is 950 Ω. The parallel switch and the series switches use the bits 0, 1, 2, and 3. The 15 resistors, R_B, are added to provide a 25 Ω step from 750 Ω to 1125 Ω. The parallel switches make the entire resistance fixed so that only the number of R_B determines the total resistance. The equation for the resistor bank is given by

$$R_{bank}[\Omega] = 600 + \frac{R_{MOSFET}R_P}{R_P + (b_0 + b_1 + b_2 + b_3)R_{MOSFET}} + R_B b_0 + 2R_B b_1 + 4R_B b_2 + 8R_B b_3\ [\Omega] \quad (1)$$

where R_P is the parallel switch and b_{number} is the bit number. The resistance bit table is shown in Table 2.

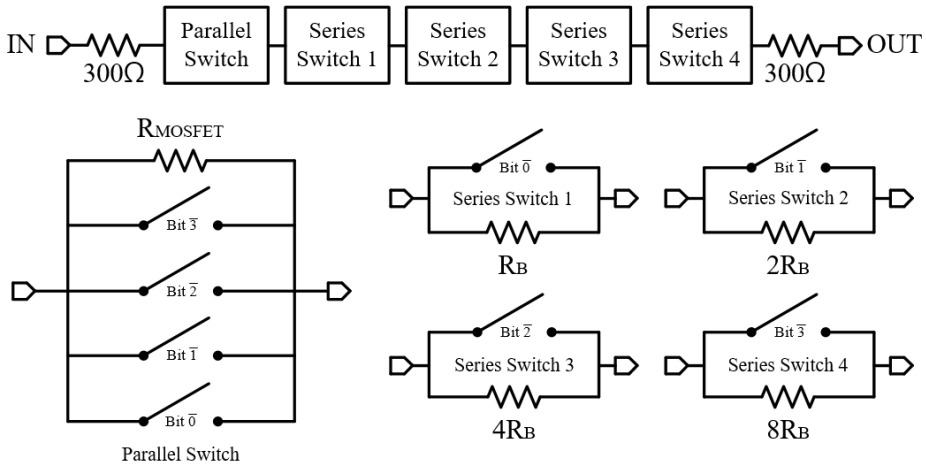

Figure 4. Schematic diagram of the proposed resistive bank.

To supply a fixed reference voltage to the error amplifier in any conditions like temperature changes or power supply variations, the circuit needs a bandgap voltage reference shown in Figure 5. An OTA is implemented to provide feedback for M_{B1} and M_{B2}. The feedback on the M_{B1} side is implemented as positive feedback and the other side as negative feedback. To stabilize the output

voltage of the bandgap reference is to have more negative feedback than the positive one. Three resistors, R_{B1}, R_{B2}, and R_{B3}, make the loop gain of the negative feedback stronger than that of the positive feedback.

Table 2. Bit table of the resistive bank.

Bit 3	Bit 2	Bit 1	Bit 0	Resistance [Ω]
0	0	0	0	744
0	0	0	1	772
0	0	1	0	796
0	0	1	1	827
0	1	0	0	845
0	1	0	1	876
0	1	1	0	900
0	1	1	1	935
1	0	0	0	951
1	0	0	1	981
1	0	1	0	1006
1	0	1	1	1041
1	1	0	0	1056
1	1	0	1	1091
1	1	1	0	1115
1	1	1	1	1157

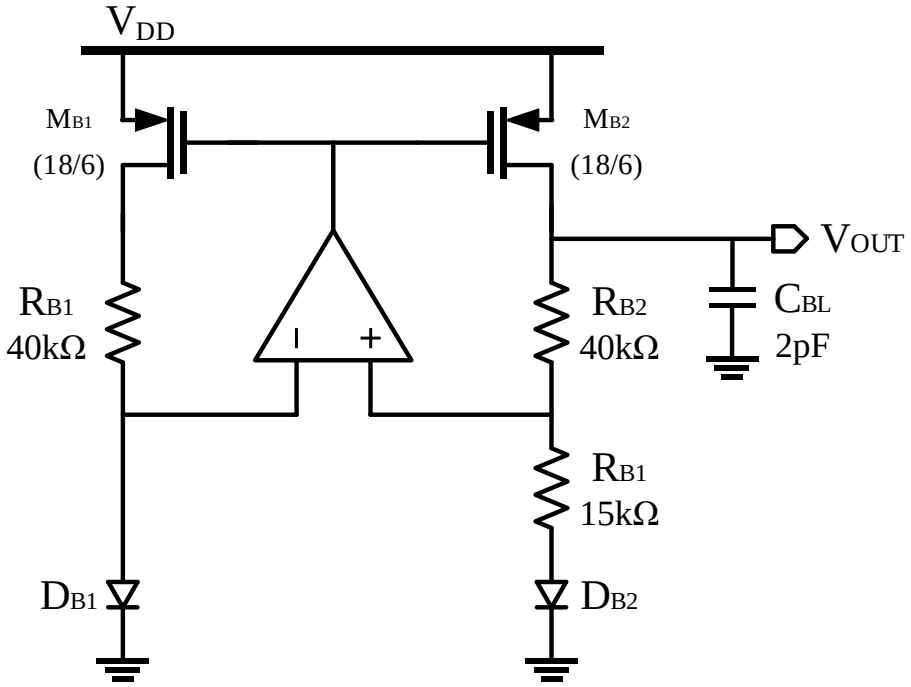

Figure 5. Schematic diagram of the bandgap voltage reference.

The OTA in the bandgap voltage reference is presented in Figure 6. The reference voltage (V_{REF}) of 880 mV was selected to have 1 V as the output voltage. The resistors R_{F1} and R_{F2} determine the output voltage, 1 V, based on the ratio of those resistors and the reference voltage from the bandgap reference. The equation for the output voltage (V_{output}) can be expressed as

$$V_{OUTPUT}[V] = V_{REF} \times \frac{R_{F1} + R_{F2}}{R_{F2}}[V]. \quad (2)$$

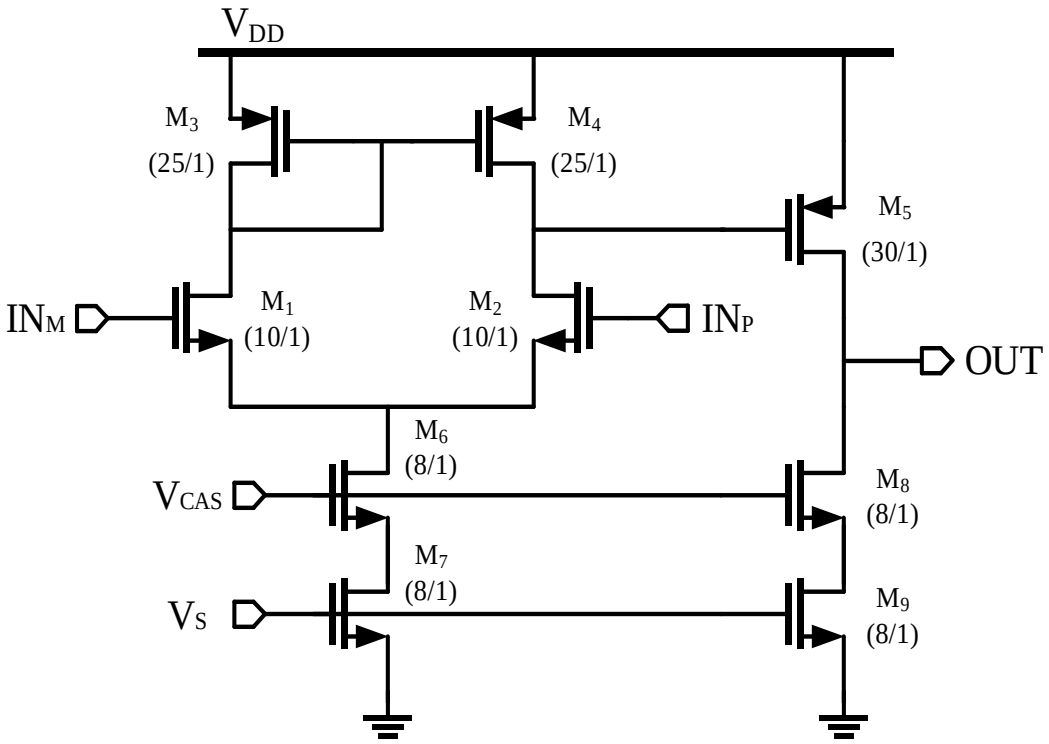

Figure 6. Schematic diagram of the operational transconductance amplifier (OTA) used in the bandgap voltage reference.

4. Measurement Results

Figure 7 shows a microphotograph of the implemented LDO regulator with a chip size of 0.092 mm^2 without pads, while Figure 8 is the power supply rejection ratio (PSRR) and regulation measurement setup. R_{par} is the parasitic resistance in the measurement setup. An SPI (Serial Peripheral Interface) module is used to control the resistor bank and the biasing points of each OTA. The quiescent current consumption of the circuit is 0.385 mA under a 1.2 V supply voltage.

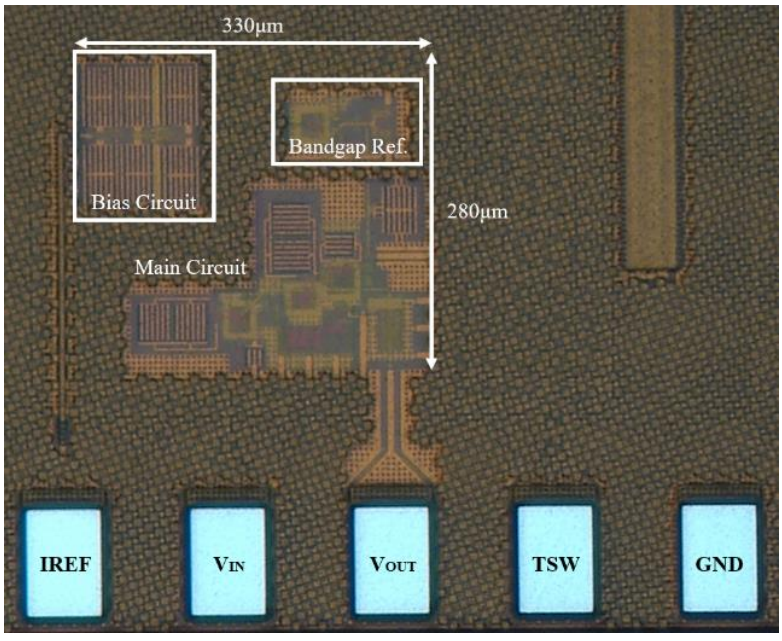

Figure 7. A microphotograph of the proposed low-dropout (LDO) regulator.

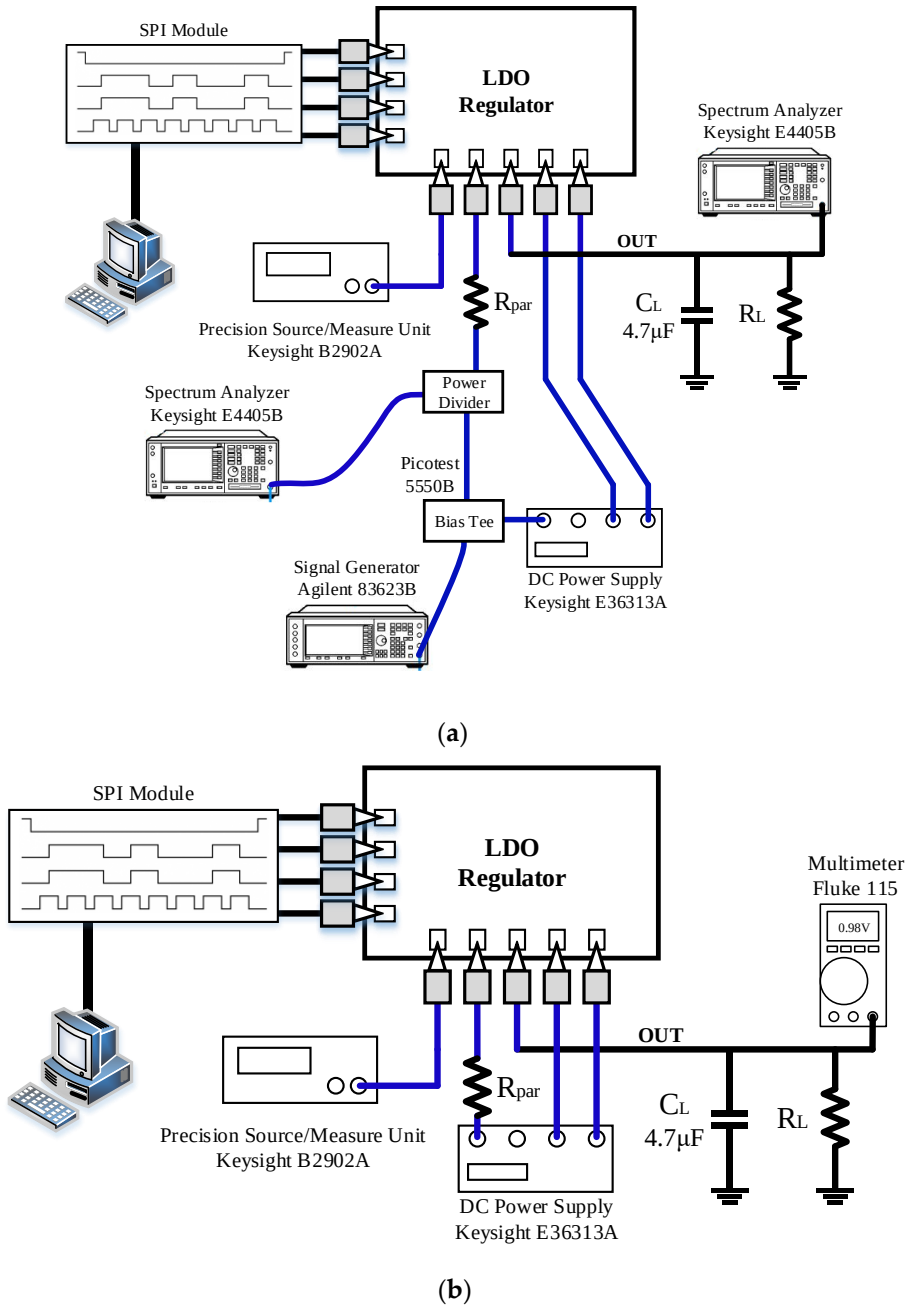

Figure 8. (**a**) Power supply rejection ratio (PSRR) and (**b**) regulation measurement setup of the proposed LDO regulator.

In Figure 9, the PSRR comparison graph between the simulation and measurement of the proposed LDO regulator and a conventional LDO regulator is shown. Measurements and simulation correspond well when we include the parasitic series resistance R_{par} in the VDD input port as presented in Figure 8. Compared with a conventional LDO regulator, 30–40 dB of extra PSRR were observed from 10 kHz–10 MHz. Figure 10 shows the output voltage when the load changes. Load regulation can be calculated by Equation (3).

$$\text{Load Regulation} = \frac{\Delta V_{OUT}}{\Delta I_L}[mV/mA]. \quad (3)$$

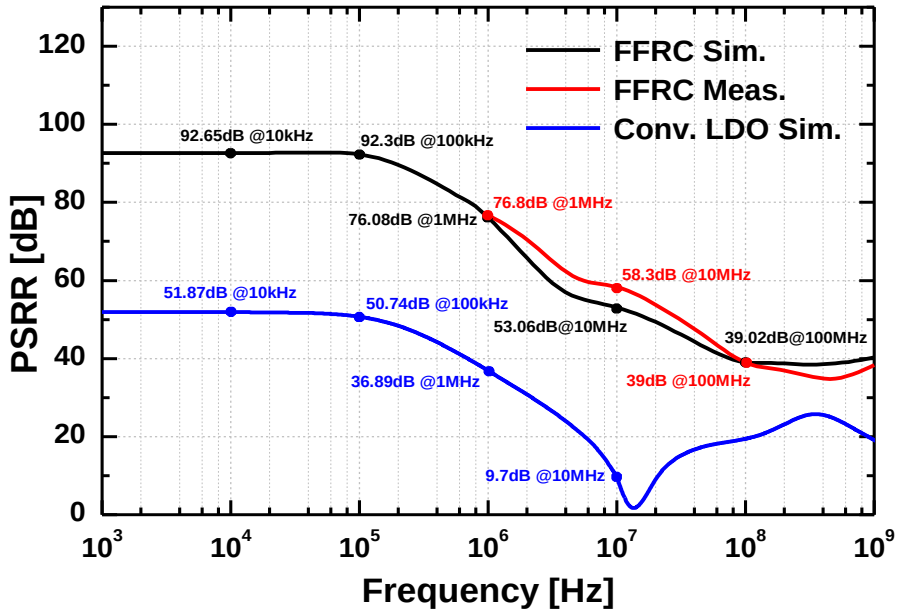

Figure 9. PSRR comparison graph between the simulation and measurement.

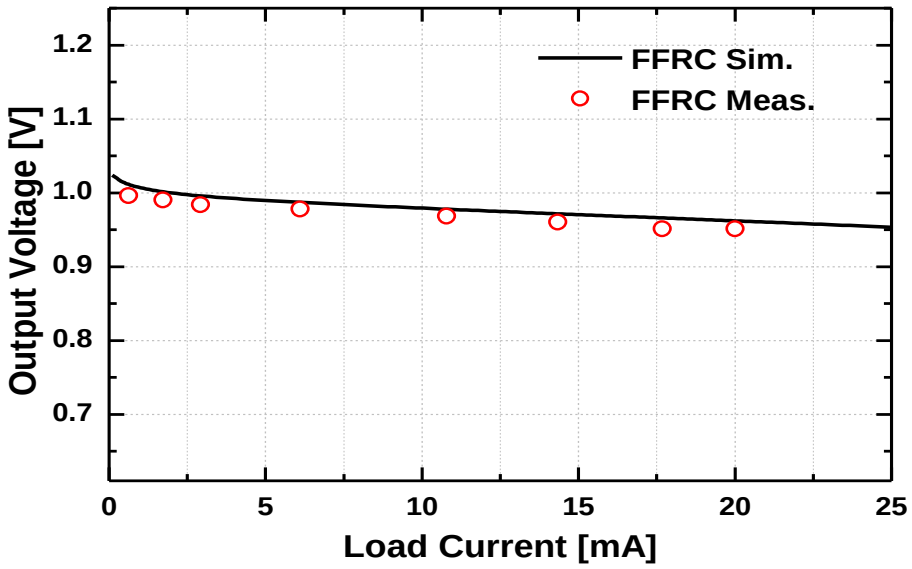

Figure 10. Load regulation comparison graph between the simulation and measurement.

ΔV_{OUT} is 45 mV when ΔI_L is 19.38 mA in this work. Thus, the load regulation is calculated to be 2.3 (mV/mA).

Figure 11 shows the change in V_{OUT} when changing the V_{IN} with a 100 Ω load. With Figure 11, the line regulation can be calculated by Equation (4).

$$\text{Line Regulation} = \frac{\Delta V_{OUT}}{\Delta V_{IN}}[V/V] \tag{4}$$

ΔV_{OUT} is 5 mV when ΔV_{IN} is 300 mV in this work. Thus, the line regulation is calculated to be 0.08 (V/V).

The performances of the proposed LDO regulator are summarized and compared with the recently reported LDO regulators in Table 3.

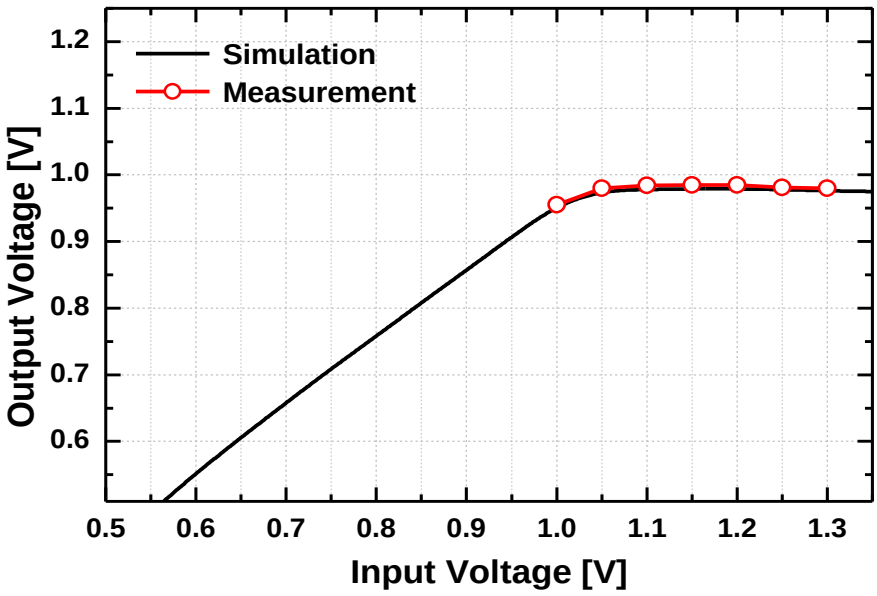

Figure 11. Line regulation comparison graph between the simulation and measurement with a 100 Ω load.

Table 3. Summary of the proposed LDO regulator compared with recently reported LDO regulators.

LDO Regulator	This Work	[1]	[2]	[6]	[7]
Technology [nm]	65	130	130	180	65
V_{IN} [V]	1.2	1.15	1.2	1.8	1.2
V_{OUT} [V]	0.98	1	1	1.6	1
Dropout Voltage [V]	0.22	0.15	0.2	0.2	0.2
Maximum Load [mA]	20	25	50	50	25
Quiescent Current [μA]	385	50	65	55	8–297.5
PSRR [dB]	76.8@1 MHz 58.3@10 MHz	67@1 MHz 56@10 MHz	49@2 MHz 38@10 MHz	70@1 MHz 37@10 MHz	52@1 MHz 36@10 MHz
Load Regulation [mV/mA]	2.3	0.048	0.13	0.14	0.042
Line Regulation [mV/mV]	0.08	0.026	4.25	0.075	0.0038
Area [mm^2]	0.092	0.049	0.4	0.14	0.087

5. Conclusions

A power supply rejection ratio (PSRR)-enhanced LDO regulator is proposed by utilizing the feed-forward ripple cancellation technique (FFRC) in 65 nm CMOS technology. In the summing amplifier, we introduced a resistive bank which is linearly controlled by binary signals to achieve an optimal ripple cancellation. The regulator provides 35–76.8 dB of PSRR at 1 MHz–1 GHz. The LDO regulator has a dropout voltage of 0.22 V and a maximum load current of 20 mA. It can also provide an output voltage of 0.98 V at a range of 1–1.3 V of the input voltage. The load regulation is 2.3 (mV/mA), while the line regulation is 0.05 (V/V). The circuit consumes 385 μA with an input voltage of 1.2 V. The area without the pads is 0.092 mm^2.

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