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# A Survey of Analog-to-Digital Converters for Operation under Radiation Environments

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**Abstract:** In this work, we analyze in depth multiple characteristic data of a representative population of radenv-ADCs (analog-to-digital converters able to operate under radiation). Selected ADCs behave without latch-up below 50 MeV·cm$^2$/mg and are able to bear doses of ionizing radiation above 50 krad(Si). An exhaustive search of ADCs with radiation characterization data has been carried out throughout the literature. The obtained collection is analyzed and compared against the state of the art of scientific ADCs, which reached years ago the electrical performance that radenv-ADCs provide nowadays. In fact, for a given Nyquist sampling rate, radenv-ADCs require significantly more power to achieve lower effective resolution. The extracted performance patterns and conclusions from our study aim to serve as reference for new developments towards more efficient implementations. As tools for this purpose, we have conceived FOM$_{TID}$ and FOM$_{SET}$, two new figures of merit to compare radenv-ADCs that consider electrical and radiation performance.

**Keywords:** ADC performance patterns; ADC state of the art; ADC survey; analog-to-digital converters; applications under radiation environments; figure of merit under radiation; radenv-ADC design guidelines; radiation effects; radiation hardening; radiation test methods

## 1. Introduction

Several high reliability applications such as HEP (high energy physics), avionics, defense and space demand ADCs operating in harsh radiation and extreme temperature environments [1,2]. The design, manufacture and test of these ADCs require additional considerations and steps that, added to their low volume market, increase their price compared to COTS (commercial off-the-shelf ADCs). Different fields of knowledge—solid-state and nuclear physics, manufacturing technologies, radiation hardening and mixed-signal design techniques, test methodologies, industry standards, etc.—have to be combined to achieve a successful design.

The lack of ADCs meeting at the same time demanding electrical performance and radiation hardness specifications allows the use of COTS for high reliability applications. Furthermore, COTS could also be convenient in low radiation environments or in applications allowing replacement of damaged parts. Therefore, many COTS have been characterized to predict their behavior under radiation [3–5]. In fact, using COTS could economize development time and cost; however, radiation characterization cannot be skipped and additional countermeasures at system level—shielding, redundancy, watch-dogs, etc.—could be required to avoid unacceptable system malfunctioning. In addition, different manufacturing lots could perform differently during TID (total ionizing dose) screening, making hard to predict the final cost of the qualification campaign of COTS. In any case, inserting advanced commercial electronics operating in radiation environments has become an industrial trend that aims to benefit from cutting-edge IC (integrated circuit) solutions together

with ad-hoc radiation hardening techniques at system level. Our revision work takes COTS into consideration and analyses this subset also separately.

Technology scaling has allowed faster applications integrating more functionalities in a single chip; collaterally, sensitivity to radiation has also varied [6,7]. In fact, atmospheric radiation can affect deep-submicron CMOS (complementary metal-oxide semiconductor) ICs not only in-flight but also on land [8,9]. Fortunately, some modern 'More Moore' [10] process options—SOI-FinFET (silicon on insulator fin-shaped field effect transistor), UTBB-FDSOI (ultra-thin body and buried oxide combined with fully-depleted silicon on insulator), etc.—and materials—high-$\kappa$ dielectrics, germanium or silicon-germanium p-channels, etc.—show enhanced resilience to radiation [11–13]. Recurrent ADCs in space applications are usually implemented with mature technologies due to their in-flight heritage and the wide voltage ranges handled by the integrated analog front-end. Nevertheless, recent space market trends like fleets of compact-size satellites based on SoC (system on-chip) ICs require new radenv-ADC IP-cores (intellectual property) with reduced area and power consumption that can only be achieved with modern technologies. New radenv-ADC developments can benefit from the analyses presented in our work, since it collects the key references to overcome.

Several FOMs (figures of merit) are defined in the literature to evaluate the efficiency of an ADC; many of them are collected in [14]. Unfortunately, parameters used to evaluate radiation performance of radenv-ADCs are not considered in these FOMs. Moreover, radiation-hardened ADCs require additional power to accomplish their radiation requirements, making unfair their comparison with unhardened devices. In Section 2.3, we propose new figures of merit to evaluate the efficiency of radenv-ADCs that consider not only their electrical performance but also their radiation characterization.

In this work, we extract patterns on conversion resolution, characteristic frequencies, radiation performance, power efficiency, architectures and manufacturing processes of radenv-ADCs. After an exhaustive search in the literature, we have gathered a collection of ADCs without degradation of electrical performance below 50 krad(Si) of TID and with a latch-up $\mathrm{LET}_{th}$ (linear energy transfer threshold) above 50 MeV$\cdot$ cm$^2$/mg. We have collected for each ADC several performance data from data-sheets, scientific publications and radiation reports (specially data considered in [15], to allow the comparison with scientific ADCs). The main contributions of this study with regard to previous analyses [16–20] are the inclusion of transients and upsets, the comparison of electrical performance patterns with scientific ADCs, the analysis of the COTS subset and the definition of new FOMs considering radiation performance. The methodology of our work described in this paragraph is graphically schematized in Figure 1.

This article has been organized such that: Section 2 summarizes how ADCs are evaluated electrically under radiation and proposes new figures of merit; Section 3 presents the selected ADCs for analysis; Section 4 analyses the selection of radenv-ADCs and compares it with the state of the art of scientific ADCs; Section 5 explains how to take advantage of the previous analysis while designing radenv-ADCs; overall conclusions are drawn in Section 6.

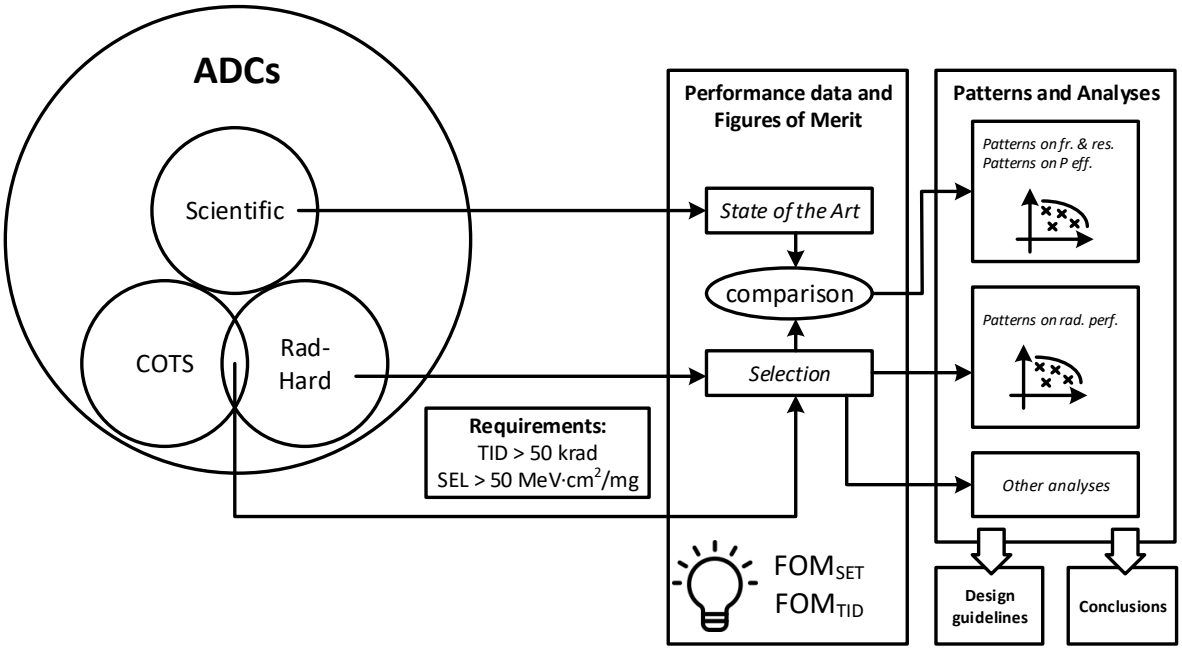


**Figure 1.** Applied methodology in the survey of radenv-ADCs.

## 2. Performance Evaluation

We have classified the parameters used for performance evaluation of radenv-ADCs into three categories. Firstly, we recall the standard parameters used to measure electrical performance. Secondly, we collect conventional parameters used to evaluate radiation performance. Unfortunately, the power efficiency is not considered within the parameters of this second category, which is the reason why we propose new figures of merit in the third category to evaluate the efficiency of radenv-ADCs.

### *2.1. Parameters Shared with COTS*

ADC data-sheets usually include standard parameters—input signal bandwidth, digital output rate, resolution and power dissipation—accompanied with FOMs in quasi-static—DNL (differential non-linearity), INL (integral non-linearity), gain and offset errors—and dynamic—DR (dynamic range), ENOB (effective number of bits), SFDR (spurious-free dynamic range), SINAD (signal-to-noise and distortion), SNDR (signal-to-noise and distortion ratio), SNR (signal-to-noise ratio) and THD (total harmonic distortion)—operations. Other parameters of interest provided are the operational temperature range, the input full-scale and the required clock frequency and jitter. Physical implementation details (such as manufacturing process or silicon area) are usually hard to find due to their commercial sensitive nature.

Parameters presented in the data-sheet of a radenv-ADC could depend on the target application. For example, linearity is evaluated with ENOB in telecommunications while INL and DNL are preferred in video acquisition. In Section 3.2 we explain how we have overcome this inconvenience to established a common playground to compare radenv-ADCs.

### *2.2. Parameters to Evaluate Radiation Performance*

Radiation effects are a vast topic [21,22] even particularized for ADCs; this section provides a condensed summary that should be sufficient to understand radiation data presented afterwards.

Radiation effects on electronic devices can be classified in two main categories: CE and SEE (cumulative and single event effects, respectively). CE, in turn, are classified as TID effects if they are caused by ionizing radiation, or as DD (displacement damage) if radiation is non-ionizing. On the other hand, SEE are discerned into destructive or non-destructive, and can also be referred as hard or soft errors, respectively.

The radiation characterization of an ADC is performed by measuring the threshold of the physical magnitude provoking each effect. However, it is not necessary to reach the threshold if it is below the environmental specifications of the target application; in that case, the maximum tested value is reported. Bearable non-destructive effects are characterized such that the degradation (in case of CE) and the statistical error rate SER (in case of non-destructive SEE) during operation can be extrapolated; for those effects, the threshold and the behavior above it are reported.

The performance under radiation of an ADC is bound to the technology and libraries of devices used to implement it; this information is critical to plan effectively the radiation test campaign of an ADC, where accelerated tests (with harsher radiation conditions than during operation) are required to predict its behavior throughout its lifetime in a reasonable time. Below in this section, we bind some radiation effects with recurrent devices used in ADCs' implementations.

#### 2.2.1. Cumulative Effects

Tests performed for measuring CE are characterized by the total dose reached before unacceptable performance degradation. In mature technologies, ionizing radiation (usually measured in krad(Si) by exposure to a $^{60}$Co source) mainly affects MOS (metal oxide semiconductor) devices, while non-ionizing radiation (measured with the fluence in particles/cm$^2$) specially involves bipolar ones. Additionally, bipolar devices (even parasitic structures [23]) can be affected by ionizing radiation at low dose rate ($\leq$10 mrad(Si)/s) [24–26], making also the dose rate an important parameter for TID tests. For some 'More Moore' processes with thinner gate oxide but using thick BOX (buried oxide), ionizing radiation can provoke a back-gate effect [27].

#### 2.2.2. Single Event Effects

The characterization of an ADC for a particular non-destructive SEE—SEFI, SET or SEU (single event functional interrupt, transient or upset, respectively)—can be summarized with the limits of the resultant Weibull fit—the LET$_{th}$ (measured in MeV·cm$^2$/mg) and the saturation cross section $\sigma_{sat}$ (given in cm$^2$/device) —. On the other hand, destructive SEE—SEB, SEDR, SEL or SESB (single event burnout, dielectric rupture, latch-up or snap-back, respectively)—are characterized only with the LET$_{th}$.

Sensibility to non-destructive SEE has varied with technology scaling, making the characterization of SEFI, SET and SEU already necessary in SEE tests fifteen years ago. In addition, upsets could be difficult to be discerned from registered transients; tests reports shall clearly define these events to avoid confusions. Furthermore, in ADCs with high conversion rates, a SET could spread out through several samples; if this occurs, only one event is counted but the length of the burst of samples is also reported.

In some cases, SEL and SESB can be mitigated to non-destructive SEE if over-current watchdogs are implemented in the power supply at system level. In other words, SEL and SESB could be turned from hard to soft errors with an opportune power cycling.

### *2.3. Proposed Figures of Merit*

A popular FOM to evaluate the efficiency of an ADC was proposed in [16]; it combines its power dissipation $P$ together with its Nyquist sampling rate $f_s$ and its effective number of quantization levels $2^{ENOB}$ in the formula:

$$\mathrm{FOM}_W = \frac{\mathrm{P}}{f_s \cdot 2^{ENOB}} \tag{1}$$

where:

$$\mathrm{ENOB} = \frac{\mathrm{SNDR}_{max} - 10 \cdot log_{10}(3/2)}{20 \cdot log_{10}(2)} \tag{2}$$

From Equation (1) it is deduced that the more efficient an ADC, the smaller its FOM$_W$. However, increasing wisely by design the power consumption of an ADC enhances its radiation tolerance.

This assertion is based on the fact that higher biasing makes leakage currents due to TID and charge generated during transients less representative with regards to the affected internal analog signals; in addition, higher currents imply faster transient response and hence shorter recovery time from a SET. In fact, from a performance under radiation point of view:

- The higher irradiated dose an ADC can stand without performance degradation, the robuster against radiation the ADC is.
- The more energized a particle shall be to cause an event in an ADC, the robuster against radiation the ADC is.
- The smaller the area an ADC has where a particle impact can affect its performance, the less sensitive to radiation the ADC is.

These trade-offs flow into the FOMs that we propose in Equations (3) and (4), which aim to evaluate the efficiency of an ADC operating under radiation:

$$\text{FOM}_{TID} = \frac{\text{TID}_{max}}{\text{FOM}_W} \tag{3}$$

$$\text{FOM}_{SET} = \frac{\text{LET}_{th}}{\text{FOM}_W \cdot \sigma_{sat}} \tag{4}$$

where $\text{FOM}_W$ is given by Equation (1), $\text{TID}_{max}$ is the maximum ionizing dose without performance degradation and the other two parameters, $\text{LET}_{th}$ and $\sigma_{sat}$, are the characteristic limits of the Weibull fit for a particular SET definition.

Regarding units, $\text{FOM}_W$ is given in joules per quantization level, $\text{TID}_{max}$ in rads or Grays, $\text{LET}_{th}$ in MeV·cm$^2$/mg, $\sigma_{sat}$ in cm$^2$/device and both $\text{FOM}_{TID}$ and $\text{FOM}_{SET}$ in quantization levels per milligram (levels/mg). Note that some minor unit conversions are required to obtain the proper values of $\text{FOM}_{TID}$ and $\text{FOM}_{SET}$. It is deduced from Equation (3) that the more efficient an ADC is against TID, the bigger its $\text{FOM}_{TID}$; comparably, a similar conclusion can be extracted from Equation (4): the more efficient an ADC is against SET, the bigger its $\text{FOM}_{SET}$.

Fine tuning of the proposed figures may be accomplished by the exponentiation of the parameters on the right side of Equations (3) and (4), depending on the importance that the analyst wants to give to each parameter. Following the general formula for ADCs' figures of merit presented in [14], the exponents of the bases $\text{FOM}_W$, $\text{TID}_{max}$, $\text{LET}_{th}$ and $\sigma_{sat}$ are respectively $-1$, 1, 1 and $-1$ in Equations (3) and (4). For example, $\text{FOM}_{TID}$ can be customized having $\text{TID}_{max}$ to the power of 2, if more emphasis to radiation performance is targeted evaluating the efficiency of the ADCs under analysis.

Furthermore, as will be shown in Section 4.3, the proposed figures of merit can be used to estimate which design solutions are more efficient considering their performance under radiation.

## 3. Inventory

### *3.1. Selection Criteria*

We have surveyed and assessed the ADCs among the catalog of the leading suppliers to the space market—Analog Devices, Atmel, Cobham Gaisler, ST Microelectronics, Teledyne e2V, Texas Instruments, etc.—and among the more relevant publications about radiation effects on components—2010–2019 NSREC/REDW's (and previous publications considered relevant) and all AMICSA's and RADECS' proceedings —. Candidates with degradation of electrical performance below 50 krad(Si) of TID or with a $\text{LET}_{th}$ for latch-up below 50 MeV· cm$^2$/mg were discarded. It is important to remark that neither all qualified ADCs are compliant with these two requirements nor, just because an ADC is not qualified, it is non-compliant. In fact, several EMs (engineering models) and COTS were included in the assessment.

### *3.2. Collected Data*

Selected ADCs target different applications with different key parameters: high linearity and resolution are mandatory in video acquisition, while larger bandwidths are prioritized in telecommunications. However, while comparing two radenv-ADCs for a particular application, secondary parameters could become critical when the key ones are similar. It is hence important to establish a common playground to compare selected ADCs, as we explain below.

We have collected performance data and additional information from data-sheets [28–33] (both commercial and SMD formats), radiation reports [1,3,4,34–39] and scientific publications [20,40–62]. We have considered a total of 22 fields for each ADC: power consumption P, differential and integral non-linearities DNL/INL, effective number of bits ENOB, Nyquist sampling rate $f_s$, input Nyquist bandwidth $f_{in}$, $\text{FOM}_W$, $\text{FOM}_{TID}$ for low and high dose rates, $\text{FOM}_{SET}$ for transients and upsets, operational temperature range (T range), TID for low and high dose rates LDR/HDR, $\text{LET}_{th}$ for latch-up events, Weibull curve limits for transients and upsets, SEE test method, technology and architecture.

Electrical performance data (P, INL, DNL and ENOB) were collected at nominal operation (nominal bias and sampling rate at 25 °C). Power consumption data from data-sheets were limited to single core information (excluding IO cells, other ADC cores inside the same chip, additional functionalities, etc.) to enable comparison with scientific publications that usually refer to single core data. ENOB was considered for the best case frequency inside the first Nyquist band. For few cases (AD7712S, RHD5940, RHD5950, RHD5958, ADS1258 and VASP), neither the $\text{SNDR}_{max}$ nor the ENOB could be found. Therefore, the ENOB (needed for $\text{FOM}_W$ calculation) had to be inferred from their declared number of bits NB and DNL or INL (expressed in LSBs) with the formula:

$$\text{ENOB}_{infer} = \text{NB} - log_2(1 + max(|\text{DNL}|, |\text{INL}|)) \quad (5)$$

Since the actual ENOB comes from a dynamic measure, it would always be close but below the inferred ENOB (that comes from a quasi-static measure).

Since it is hard to discern SETs from SEUs during SEE tests of an ADC, radiation data were collected and classified as originally reported. In case that multiple data are available, the worst case is considered.

### *3.3. Selected ADCs for Analysis*

To increase the number of samples under analysis, few exceptions were made for both requirements described in Section 3.1:

- TID requirement was relaxed for a few ADCs with characterization data for transients and upsets (AD7712, MAX145, ADS1258, LTC1419, AD7984, ADS5483 and ADS5444-SP).
- Three TID compliant ADCs for which no SEE data could be found in the literature were exempt from the latch-up requirement (AD570S, AD9254S and TS8388B).

Finally, fifty four ADCs were selected for the analysis; their collected data are presented in Table 1. For a better understanding of the table, the following explanations shall be considered:

- The table's header is divided into four lines: 'Group' (uppermost line), 'Sub-group' (second uppermost line), 'Field' (second lowermost line) and 'Units' (lowermost line).
- Each of the 22 fields described in Section 3.2 is represented in one column of the table.
- The 22 fields are classified in tree different groups: 'Performance', 'Hi-Rel', and 'Additional Information'.
- Fields conceptually related and/or sharing the same units in the 'Performance' and 'Hi-Rel' groups are gathered in the same sub-group.
- Collected data are presented in the table's body, below the table's header. Empty boxes therein (fulfilled with symbol "-") are non-available data due to lack of information in the literature.

- The leftmost column of the table's body collects the names of the selected radenv-ADCs. Particularly, COTS are marked with a double asterisk (**) after their name.
- The 'FOM' sub-group within the 'Performance' group is composed by the FOMs described in Section 2.3. Columns 'W', 'TID(L)', 'TID(H)', 'SET' and 'SEU' of this sub-group collect respectively for the selected radenv-ADCs their $FOM_W$, their $FOM_{TID}$ for TID measured at low and/or high dose rates, and their $FOM_{SET}$ for transients and/or upsets characterization.
- In the 'ENOB' column, inferred data using Equation (5) are marked with a single asterisk (*). Additionally, in the 'FOM' sub-group columns, data calculated using an inferred ENOB are also marked with a single asterisk (*).
- In the 'Hi-Rel' group, TID, $LET_{th}$ and $\sigma_{sat}$ measurements are gathered respectively in the 'TID', '$LET_{th}$' and '$\sigma_{sat}$' sub-groups. TID measurements are discerned in two columns ('LDR' or 'HDR') depending on the dose rate as defined in Section 2.2.1. On the other hand, $LET_{th}$ and $\sigma_{sat}$ measurements are segregated in different columns depending on the nature of the SEE ('SEL', 'SET', or 'SEU' columns for latch-up, transients or upsets respectively). As explained in the first paragraph of Section 2.2.2, SEL measurements only consider the $LET_{th}$.
- Acronyms used in the 'SEE test' column are listed in Table 2.
- The 'Tech.' column collects manufacturing process details extracted from the literature. This information could be: the process type (bipolar, complementary-bipolar, CMOS, linear compatible CMOS, bipolar-CMOS, etc.), the process name (B7HF200, BiCom3, BiCom3X, BiCMOS9, C021.A, CMOS9, CMOS9X, XFCB, XH035, etc.), or the CMOS node (350 nm, 250 nm, 180 nm, 130 nm, 32 nm, etc.). Additional technological explanations are provided in Section 4.4.
- Acronyms used for the different ADC architectures in the 'Arc.' column are listed in the first sentence of Section 4.5.

**Table 1.** Selection of radenv-ADCs.

| Group | Performance | | | | | | | | | | | | Hi-Rel | | | | | | | | Additional Information | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Sub-group | | Linearity | | | Frequencies | | FOM | | | | | | TID | | LET$_{th}$ | | | $\sigma_{sat}$ | | | | | |
| Field | P | DNL | INL | ENOB | $f_s$ | $f_{in}$ | W | TID(L) | TID(H) | SET | SEU | T range | LDR | HDR | SEL | SET | SEU | SET | SEU | SEE test | Tech. | Arc. |
| Units | mW | LSB | | bits | MHz | | pJ/lev. | levels/mg | | | | °C | krad | | MeV-cm$^2$/mg | | | cm$^2$/device | | - | - | - |
| ADS1281** | 12 | - | 0,1 | 20,3 | 0,001 | 5E-4 | 9,3 | - | 2,2E8 | - | - | -40; 125 | - | 200 | 87 | - | - | - | - | DIS | - | ΔΣ |
| ADS1282-SP | 25,5 | - | 1074 | 20,3 | 0,001 | 5E-4 | 19,7 | 2,5E7 | 2,5E7 | 59,3 | 876 | -55; 125 | 50 | 50 | 52,3 | 2,7 | 1,4 | 3,7E-4 | 1,3E-5 | S | 50HPA07 | ΔΣ |
| RHD5940 | 100 | 0,5 | 0,5 | 13,4* | 0,025 | 0,0125 | 366* | - | 2,7E6* | - | - | -55; 125 | - | 100 | 100 | - | - | - | - | - | - | SAR |
| AD7712** | 45 | - | 252 | 16,0* | 0,039 | 0,0195 | 17,3* | - | 5,8E6* | 246* | - | -55; 125 | - | 10 | 87 | 8,0 | - | 3E-4 | - | DIS | LC$^2$MOS | ΔΣ |
| AD570S | 800 | 0,5 | 0,5 | 8,0 | 0,04 | 0,02 | 78125 | 6,4E3 | - | - | - | -55; 125 | 50 | - | - | - | - | - | - | - | Bipolar | SAR |
| RHD5950 | 60 | 8,2 | 48 | 8,4* | 0,05 | 0,025 | 3589* | - | 2,8E5* | - | - | -55; 125 | - | 100 | 100 | - | - | - | - | - | - | SAR |
| RHD5958 | 60 | 8,2 | 41 | 8,6* | 0,05 | 0,025 | 3073* | - | 3,3E6* | - | - | -55; 125 | - | 1E3 | 100 | - | - | - | - | - | - | SAR |
| ADS1278-SP | 515 | - | 50 | 17.98 | 0.053 | 0.0265 | 37,8 | - | 1,3 | 27,3 | - | -55; 125 | - | 50 | 75 | 5,5 | - | 8,5E-4 | - | S | 350nm | ΔΣ |
| AD7872T** | 50 | - | 1 | 12,5 | 0,083 | 0,0415 | 104 | - | 9,6E6 | 2,2 | 27 | -55; 125 | - | 100 | 104 | 1,4 | 8,8 | 1E-3 | 5E-4 | - | LC$^2$MOS | SAR |
| 7809LP | 132 | 3 | 3 | 14,32 | 0,1 | 0,05 | 64,4 | - | 1,6E7 | - | - | -40; 85 | - | 100 | Inf | - | - | - | - | - | - | SAR |
| MAX145** | 2,7 | 0,75 | 0,5 | 11,3 | 0,108 | 0,0504 | 9,6 | - | - | 1E4 | - | -55; 125 | - | - | 53,9 | 17,0 | - | 2,8E-5 | - | DAC | - | SAR |
| ADS1258** | 42 | - | 50 | 18,3* | 0,125 | 0,0625 | 1* | - | 9,7E7* | 1E4* | - | -40; 105 | - | 10 | 67 | 8,0 | - | 1,2E-4 | - | DIS | - | ΔΣ |
| LTC1604** | 220 | 0,6 | 0,6 | 14,5 | 0,333 | 0,1615 | 28,7 | - | 3,5E7 | - | - | -40; 85 | - | 100 | 55 | - | - | - | - | DIS | - | SAR |
| LTC1409** | 80 | 0,25 | 0,25 | 11,7 | 0,8 | 0,4 | 29 | - | 3,4E7 | - | - | -40; 85 | - | 100 | 75 | - | - | - | - | - | - | SAR |
| LTC1419** | 150 | 0,4 | 0,6 | 13,0 | 0,8 | 0,4 | 23 | - | 1,7E7 | 19,5 | - | -55; 125 | - | 40 | 50 | 2,8 | - | 1E-3 | - | S | - | SAR |
| RAD1419 | 150 | 0,7 | 0,8 | 13,0 | 0,8 | 0,4 | 23 | - | 4,4E7 | - | - | -55; 125 | - | 100 | 60 | - | - | - | - | - | - | SAR |
| ADC128S102QML-SP | 2,7 | 0,5 | 0,6 | 11,7 | 1 | 0,5 | 0,831 | 1,2E9 | 1,2E9 | - | 2,7E4 | -55; 125 | 100 | 100 | 122 | - | 5,8 | - | 4,1E-5 | S(x2) | 350nm | SAR |
| ADC124S101** | 4,3 | 0,9 | 0,64 | 11,7 | 1 | 0,5 | 1,3 | - | 7,7E8 | - | - | -40; 85 | - | 100 | 120 | - | - | - | - | - | - | SAR |
| RHFAD128 | 5,94 | 0,9 | 1,1 | 11,7 | 1 | 0,5 | 1,8 | - | 164,2 | 9,4E5 | - | -55; 125 | - | 300 | 125 | 32 | - | 3E-6 | - | S | 130nm | SAR |
| AD7984** | 10,5 | 1 | 0,6 | 16,0 | 1,33 | 0,665 | 0,1 | - | - | 9,6E4 | - | -40; 85 | - | - | 106 | 23,4 | - | 3,2E-4 | - | - | - | SAR |
| UT14AD03 | 100 | 0,5 | 2 | 12,9 | 3 | 1,5 | 4,4 | - | 6,9E8 | - | - | -55; 125 | - | 300 | 111 | - | - | - | - | - | CMOS | PIP? |
| 9240LP | 230 | 0,7 | 2,5 | 12,2 | 10 | 5 | 4,7 | - | 2,1E8 | - | - | -55; 125 | - | 100 | Inf | - | - | - | - | - | CMOS | PIP? |
| VASP | 275 | 0,5 | 2 | 10,4* | 12 | 6 | 16,8* | 6E7* | - | - | - | -55; 125 | 100 | - | 67,7 | - | - | - | - | - | XH035 | PIP |
| LM98640QML-SP | 232 | 0,78 | 6 | 9,5 | 20 | 10 | 15,9 | - | 6,3E7 | - | 0 | -55; 125 | - | 500 | Inf | - | - | - | - | - | CMOS9 | PIP |
| RH9225 | 335 | 0,4 | 1,2 | 10,7 | 20 | 10 | 10,3 | - | 4,9E8 | - | - | room | - | 50 | 63 | - | 3 | - | 9,6E-6 | S | - | PIP |
| RHF1401 | 67,5 | 0,4 | 3 | 11,3 | 20 | 10 | 1,3 | - | 2,3E9 | - | - | -55; 125 | - | 300 | 120 | - | - | - | - | QS | 250nm | PIP |
| IMCAS-1 | 240 | 0,4 | 0,5 | 9,7 | 25 | 12,5 | 11,5 | - | 4,3E7 | - | 4338 | -55; 125 | - | 100 | 120 | - | 0 | - | 5,9E-4 | - | 350nm | PIP? |
| UT16AD40P | 5120 | 0,4 | 2,5 | 12,3 | 40 | 20 | 24,8 | - | 8E8 | 1,3E4 | - | -55; 125 | - | 2E3 | 121 | 30,0 | - | 1,5E-5 | - | 1P | 180nm | PIP |
| AD9042S | 595 | 1 | 0,75 | 10,8 | 41 | 20,5 | 7,9 | 3,2E8 | 2E9 | 52,9 | 37 | -55; 125 | 250 | 1600 | 67,7 | 1,1 | 1,1 | 4,2E-4 | 6E-4 | S | XFCB | PIP |
| RHF1201 | 100 | 0,5 | 1,7 | 10,2 | 50 | 25 | 1,7 | - | 1,7E9 | 0,0 | - | -55; 125 | - | 300 | 120 | 0 | - | 3,5E-4 | - | DIS | 250nm | PIP |
| AD6640** | 708 | 1,5 | 1,25 | 10,8 | 65 | 32,5 | 6,0 | - | 1,7E8 | 15,6 | - | -40; 85 | - | 100 | 60 | 1,44 | - | 2,5E-3 | - | S | - | PIP |
| AD6645S | 1749 | 1,5 | 1,5 | 11,5 | 80 | 40 | 7,5 | 2E8 | 1,3E8 | - | - | -55; 125 | 150 | 100 | 83 | - | - | - | - | - | XFCB | PIP |
| ADS5424-SP | 1930 | 0,5 | 3 | 11,3 | 105 | 52,5 | 7,4 | - | 2E8 | 271,8 | 271,8 | -55; 125 | - | 150 | 60 | 2,5 | 2,5 | 2E-4 | 2E-4 | 4P | BiCom3 | SAR |
| AD9246S | 396 | 1,5 | 0,4 | 11,3 | 125 | 62,5 | 1,3 | - | 8E8 | 5,1E5 | - | -55; 125 | - | 100 | 80 | 10,0 | 80 | 2,5E-6 | - | S | - | PIP |
| ADS5483** | 2200 | 0,5 | 3 | 12,9 | 135 | 67,5 | 2,2 | - | - | 462,9 | - | -40; 85 | - | - | 83,4 | 2,5 | - | 4E-4 | - | 1P, 4P | BiCom3 | PIP |
| AD9254S | 468 | 1,4 | 6 | 11,2 | 150 | 75 | 1,4 | - | 7,4E8 | - | - | -55; 110 | - | 100 | - | - | - | - | - | - | - | PIP |
| ADC14155QML-SP | 967 | 0,5 | 2,3 | 11,3 | 155 | 77,5 | 2,5 | 6E8 | 6E8 | 91,5 | 91,5 | -55; 125 | 150 | 150 | 122 | 1,0 | 1 | 7E-4 | 7E-4 | 1P,BF,4P | CMOS9 | PIP |
| Boeing-1 | 39 | 1 | 2,5 | 7,4 | 200 | 100 | 1,1 | - | 8,8E9 | 3.4E7 | - | 25,0 | - | 1E3 | 170 | 30,9 | - | 1,3E-7 | - | CS | 32nm | PIP |
| ADS5444-SP | 1700 | 0,4 | 2,8 | 11,1 | 250 | 125 | 3,2 | - | - | - | 343 | -55; 125 | - | - | 86 | - | 1,83 | - | 2,7E-4 | QS | BiCom3X | SAR |
| SPT7725** | 2200 | 0,95 | 0,95 | 5,9 | 300 | 150 | 126,9 | - | 7,9E6 | - | - | -25; 85 | - | 100 | Inf | - | - | - | - | - | - | F |
| ADS5474-SP | 2548 | 0,7 | 1,5 | 11,2 | 400 | 200 | 2,8 | 3,6E8 | 3,6E8 | 6687 | 6687 | -55; 125 | 100 | 100 | 87 | 18,7 | 18,7 | 1,6E-4 | 1,6E-4 | CS | BiCom3 | SAR |
| ADS5463-SP | 2504 | 1 | 1,5 | 10,0 | 500 | 250 | 4,9 | - | 2E8 | 162,6 | - | -55; 125 | - | 100 | 86 | 0,90 | - | 1,8E-4 | - | QS | BiCom3X | SAR |
| TS8388B | 3025 | 0,4 | 0,7 | 6,8 | 1000 | 500 | 26,5 | - | 5,7E7 | - | - | -55; 125 | - | 150 | - | - | - | - | - | - | BiCMOS | FIF |
| ADC08D1000WG-QV | 817 | 0,15 | 0,3 | 7,4 | 1000 | 500 | 4,8 | 4,1E8 | 6,2E8 | 196,5 | 196,5 | -55; 125 | 200 | 300 | 122 | 3,0 | 3 | 5E-4 | 5E-4 | BF | CMOS9X | FIF |
| ADC10D1000QML-SP | 959 | 0,2 | 0,7 | 8,9 | 1000 | 500 | 2 | - | 5E8 | 793,6 | 595,2 | -55; 125 | - | 100 | 120 | 3,0 | 3 | 3E-4 | 4E-4 | BF | CMOS9 | PIP |
| ADS5400-SP | 983 | 0,4 | 1,5 | 9,1 | 1000 | 500 | 1,8 | - | 2,8E8 | - | - | -55; 125 | - | 50 | Inf | - | - | - | - | - | BiCom3X | PIP |
| ADC08D1520QML-SP | 1074 | 0,15 | 0,3 | 7,2 | 1500 | 750 | 4,7 | 4,3E8 | 6,4E8 | 583,5 | 756,4 | -55; 125 | 200 | 300 | 122 | 6,0 | 6 | 3,5E-4 | 2,7E-4 | BF | CMOS9 | FIF |
| EV12AD500A/550A | 1961 | 3 | 6,5 | 9,4 | 1500 | 750 | 1,9 | | 7,8E8 | 118,3 | - | -55; 125 | - | 150 | 84,5 | 1,0 | - | 7E-4 | - | - | BiCMOS9 | FIF? |
| EV10AS180A | 1442 | 0,5 | 1 | 8,4 | 1500 | 750 | 2,8 | 3,9E8 | - | 197,1 | - | -55; 125 | 110 | - | 80 | 0,7 | - | 2E-4 | - | S, BF | B7HF200 | FIF? |
| ADC12D1600QML-SP | 1208 | 0,5 | 2,5 | 9,1 | 1600 | 800 | 1,4 | - | 2,2E9 | 145,8 | - | -55; 125 | - | 300 | 120 | 0,9 | - | 7,1E-4 | - | S, BF | CMOS9X | FIF |
| ADC12D1620QML-SP | 1208 | 0,5 | 2,5 | 9,1 | 1600 | 800 | 1,4 | - | 2,2E9 | - | - | -55; 125 | - | 300 | 120 | - | - | - | - | - | CMOS9X | FIF |
| AT84AS008 | 3500 | 0,8 | 2,5 | 7,6 | 2200 | 1100 | 8,2 | 1,8E8 | - | 225,7 | - | -55; 125 | 150 | - | 56 | 1,49 | - | 1,3E-4 | - | - | B7HF200 | FIF? |
| AD9689** | 1550 | 0,4 | 5 | 9,5 | 2600 | 1300 | 0,8 | - | 123,5 | 362,3 | - | -40;125 | - | 100 | 80,5 | 0,5 | - | 2,7E-4 | - | DT | - | PIP |
| ADC12DJ3200QML-SP | 1800 | 0,4 | 3 | 8,7 | 3200 | 1600 | 1,3 | - | 228,5 | 14,4 | - | -55;125 | - | 300 | 120 | 1,4 | - | 1,2E-2 | - | CER | C021.A | PIP |

* Inferred ENOB
** COTS

## 4. Data Analysis

As advanced in Figure 1, the selection described in Section 3 is analyzed and compared with designs presented at the IEEE ISSCC (International Solid-State Circuits Conference) and the VLSI (Symposia on Very Large Scale Integration Technology and Circuits) from 1997 to 2019. These designs are considered the state of the art of scientific ADCs in this analysis. From now on in this section, the former population of ADCs is referred as the *selection* and the latter as the *state of the art*.

The presented analysis aims to extract patterns of the power efficiency of radenv-ADCs. Unfortunately, it cannot be warrantied that all collected data were measured with the same criteria; consequently data presented in Table 1 could be slightly shifted. This is specially critical for radiation data, as will be explained in Section 4.3. However, this fact will have little impact on the final conclusions about patterns and performance envelopes of radenv-ADCs.

Data from Table 1 are represented in several ways in Figures 2–8 to extract different patterns of the *selection*; the envelope defined by the best performing specimens is depicted with a dashed line in each figure. Additionally, the envelope defined by the best performing specimens of the *state of the art* is represented with a solid line in Figures 2–5. Detailed data about each specimen and envelope of the *state of the art* can be found in [15]. Furthermore, we have discerned data by ADC architecture using different symbols (cf. legends).

Figures 2, 3 and 5 present envelopes shaped alike for both the *selection* and the *state of the art*; the same behavior is observed in Figure 4 up to 100 MHz. These facts endorse the assumptions that patterns between both populations can be compared and that conclusions from this comparison can be extracted considering that the main difference between both populations is the radiation hardening feature.

Inferred data in Figures 2–5, 7 and 8 are marked with a black round circle around their symbolic representation. Since inferences could be slightly improved with regard to measures, the former are not considered to establish the envelopes in those figures. In any case, only one case with inferred data (ADS1258) is close to the envelopes.

### 4.1. Frequency and Resolution

Nyquist sampling rate and input bandwidth were selected as reference frequencies to establish a common playground for the whole *selection*. The choice of the latter is in detriment of some ADCs with a passband wider than their Nyquist input bandwidth; however, the best SNDR is usually obtained within the Nyquist input bandwidth, which justifies its choice.

Figure 2 depicts the ENOB of each *selection*'s member versus its Nyquist sampling rate $f_s$. Their ceiling is 20.5 bits up to 1 kHz, decaying 1.5 bits per decade from this point (dashed line with interleaved crosses in Figure 2). Unfortunately, no TID data could be found in the literature for specimens supporting that ceiling (AD7984 and ADS5483). We have hence considered a more accurate envelope; it has the same slope from 10 kHz, but shifted 1 bit down (dashed line in Figure 2). The ceiling of the *the state of the art* is 20 bits up to 10 kHz and decays from this point 1.5 bits per decade. Comparing both envelopes, it can be said that radiation hardening does not affect the maximum achievable ENOB up to 1 kHz; nevertheless, ENOB is punished with 2 bits above 10 kHz. For both the *selection* and the *state of the art*, ENOB decays 1.5 bits per decade above 10 kHz. Furthermore, if data of the *state of the art* after 2008 were not considered, both envelopes would be overlapped. In other words, for a given $f_s$, the best scientific ADCs back in 2008 already achieved the ENOB that the best available radenv-ADCs do nowadays.

In addition to the intrinsic limitations of ADCs—quantization noise, input-referred circuit noise, aperture uncertainty and comparators ambiguity —, radenv-ADCs are also limited in speed by the qualified packaging technologies [63]. This explains the sparsely populated area in Figure 2 for radenv-ADCs above 1 GHz and 10 bits compared to the *the state of the art*. Furthermore, our study has limited the collected data to single core solutions, while ADCs operating above 1 GHz are usually implemented with time-interleaved multi-core architectures.

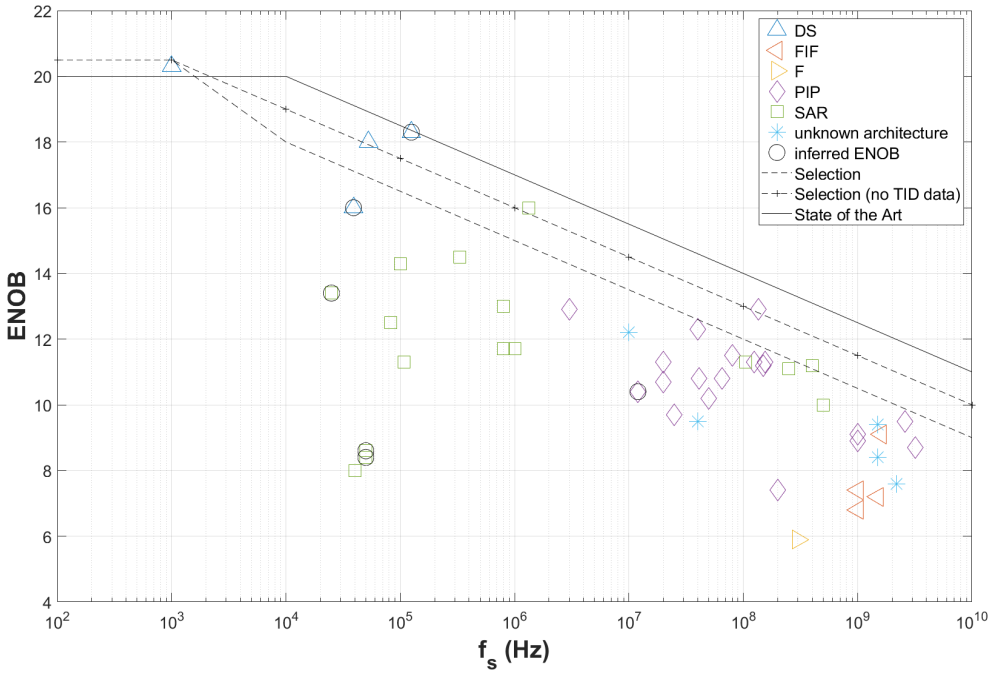


**Figure 2.** Effective Number of Bits against Nyquist sampling rate.

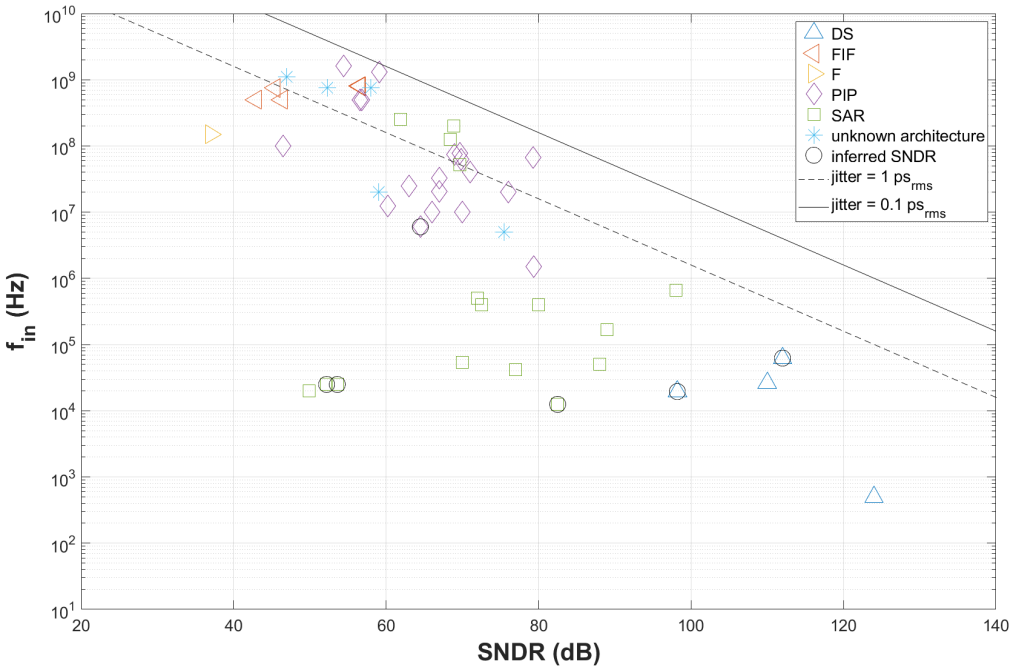


**Figure 3.** Nyquist input bandwidth against signal-to-noise and distortion ratio.

Figure 3 plots the Nyquist input bandwidth against maximum SNDR for the *selection*'s members. It also includes the performance of an ideal sampler with sinusoidal input for two jitter cases of its sampling clock: solid and dashed lines represent 0.1 and 1 $ps_{rms}$ cases respectively. For a given ENOB, *selection*'s members with the highest bandwidth perform as ideal samplers with a sampling aperture uncertainty close to 1 $ps_{rms}$. Jitter becomes more critical for bandwidths close to 100 MHz and above, for which the most performing *selection*'s members exceed the 1 $ps_{rms}$ line but without surpassing the

0.1 $ps_{rms}$ one. A practical conclusion at system level is that hi-rel TID tolerant oscillators shall provide a sampling clock better than 0.1 $ps_{rms}$ to avoid jitter limiting the performance of new radenv-ADC designs; this requirement can also be extended to PLLs in SoC implementations. Note indeed that this is a best case figure based on the comparison with a simplified mathematical model; jitter can be more harmful in the actual performance of an ADC depending on implementation particularities of each design. Jitter requirements for the *state of the art* are just above the 0.1 $ps_{rms}$ line (less than one order of magnitude above the *selection*'s). In fact, for the *state of the art*, jitter becomes more critical for bandwidths close to 1 GHz and above, for which the most performing members exceed the 0.1 $ps_{rms}$ line. In addition, if data after 2012 of the *state of the art* were not considered, its envelope in Figure 3 would be similar to the one of the *selection*. In other words, for a given SNDR, best scientific ADCs back in 2012 already achieved the input bandwidth that the best available radenv-ADCs do nowadays.

### 4.2. Power Efficiency

Differences between the *selection* and the *state of the art* are even more evident when power consumption is considered. Figure 4 represents $FOM_W$ of each *selection*'s member against their Nyquist sampling rate $f_s$; on the other hand, Figure 5 portrays their power consumption over $f_s$ against their peak SNDR. In both figures, the slashed line stands for the *selection*'s bottom line (831 fJ/level) while the solid line does for the *state of the art*'s (0.89 fJ/level up to 100 MHz). Almost three orders of magnitude separate both lines in favor of the *state of the art*. Again, one specimen without TID data (AD7984) is excluded to determine the *selection*'s envelope. In both Figures 4 and 5, *selection*'s and *state of the art*'s envelopes would match if data after 2002 of the *state of the art* were not considered. Put another way, best scientific ADCs back in 2002 already achieved the $FOM_W$ that the best available radenv-ADCs achieve nowadays.

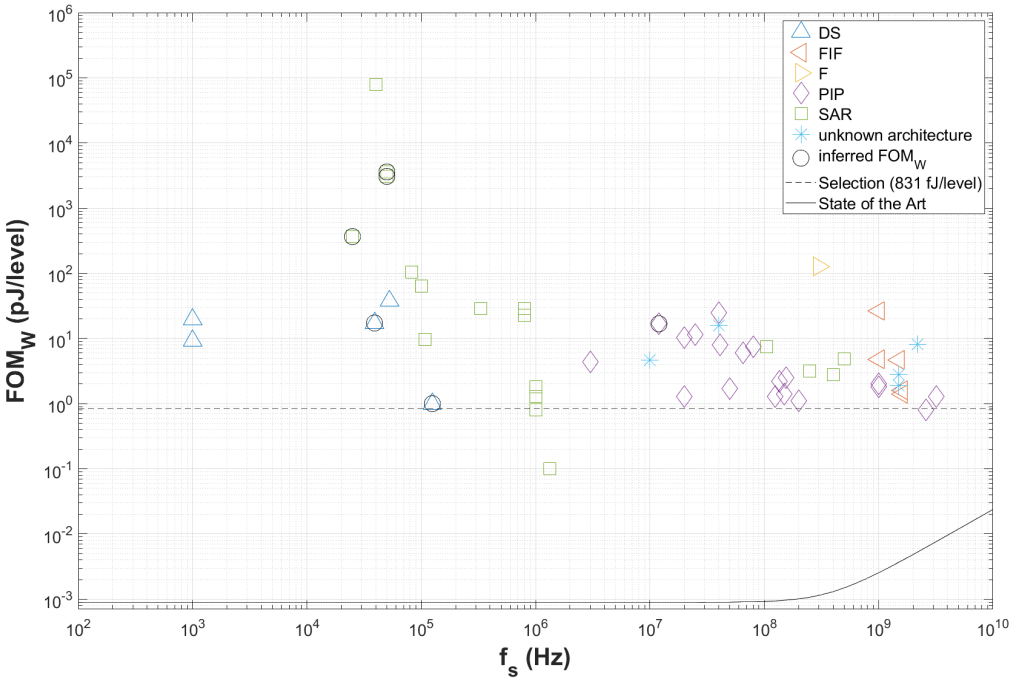


**Figure 4.** Walden's figure of merit against Nyquist sampling rate.

From Section 4.1 it was concluded that, for a given $f_s$ above 10 kHz, the best ENOB achievable for the *selection* is 2 bits below the *state of the art*'s. Additionally, Figure 4 shows that, for a given $f_s$ below 100 MHz, the best $FOM_W$ achievable for the *selection* is more than 933 times (831/0.89) the *state of the art*'s. Using this information in Equation (1), we can extract that, for a given $f_s$ between 10 kHz and

100 MHz, the *selection* requires at least 233 times more power to achieve an ENOB at least 2 bits lower, in regard to the best members of the *state of the art*.

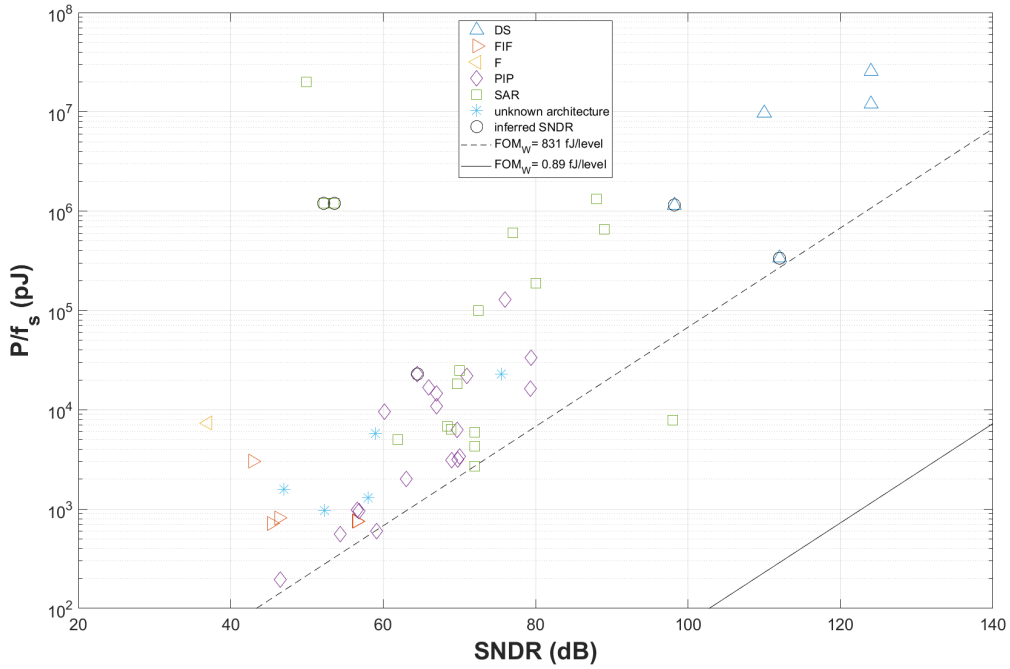


**Figure 5.** Conversion energy against signal-to-noise and distortion ratio.

Radiation hardening entails additional power consumption. Bias currents are not optimized to enhance radiation tolerance. In addition, a design can be hardened including specific ad hoc blocks, which entail additional area and power. Furthermore, performance under radiation can be enhanced increasing the separation between devices and reducing the impedance to ground of critical nodes; both techniques increase circuit parasites and hence power consumption.

In mature CMOS technologies (180 nm nodes and above), the minimum width of ELT devices (enclosed layout transistors, used to mitigate TID effects), is several times the width of regular transistors, which also scale the design into a more power hungry one. From the digital circuitry point of view, hardened cells can consume twice power and be two to four times bigger than cells with the same functionality and speed from a commercial library [64].

### *4.3. Radiation Performance*

TID is usually measured up to a predefined dose that can be lower than the maximum bearable before performance degradation. Something similar occurs with SEL characterization, where the maximum LET tested does not necessarily provoke latch-up events. SET and SEU tests have several degrees of freedom—test method, event detection criteria, sampling frequency, bias conditions, etc.—that make each ADC characterization very specific. In Table 2, we have listed the nine test methods used in the literature to evaluate the soft-error sensibility of radenv-ADCs; methods known by two different names are presented in the same line. Identified test methods for the *selection* are collected in column 'SEE Test' of Table 1. Unfortunately, different test methods used for the same ADC give similar SET $LET_{th}$ but different SET cross-sections (even if within the same order of magnitude) [3,34,35,37,65]. In addition, SET/SEU cross-sections can depend on the sampling frequency of the ADC under test [34] and on the ionizing dose [5,66]. Therefore, comparing radiation performance across devices shall be accomplished carefully. This variability in test complicates the extraction of patterns on radiation performance. $FOM_{TID}$ and $FOM_{SET}$ can be used as a first filter to compare performance, but a closer look is required when figures are close.

**Table 2.** Detection methods of soft errors in radenv-ADCs testing.

| # | Test Method | Abbreviation | Reference(s) |
|---|---|---|---|
| 1 | Beat Frequency/Two-Point | BF/2P | [34,37,65,67] |
| 2 | Code Error Rate/Coherent Sampling | CER/CS | [4,51,54,68] |
| 3 | Comparison with DAC input | DAC | [1] |
| 4 | Comparison with 'golden chip' | GOLD | [69] |
| 5 | Dynamic Input Signal | DIS | [70] |
| 6 | Four-Point | 4P | [3,34,71,72] |
| 7 | Quasi-Static | QS | [36] |
| 8 | Single-Point | 1P | [3,34,45] |
| 9 | Static | S | [35,37,73,74] |

Figure 6 plots the reported TID against nominal power consumption for each *selection*'s member. As expected, the best performing ADCs (slashed line), present greater TIDs for higher nominal power consumptions. However, power consumption is also related with other ADC parameters; the most important ones are included in $\text{FOM}_W$ ($f_s$ and ENOB). Since $\text{FOM}_{TID}$ combines TID with $\text{FOM}_W$, it can be used to evaluate the efficiency of an ADC including its TID performance. Figure 7 represents the calculated $\text{FOM}_{TID}$ against nominal power consumption for each *selection*'s member. Just Boeing-1 ADC [50,51] with $8.85 \times 10^9$ levels/mg surpasses the *selection*'s envelope (slashed line), established in $2 \times 10^9$ levels/mg by the rest of the best performing ADCs. This ADC is analyzed with other particular cases in Section 4.7.

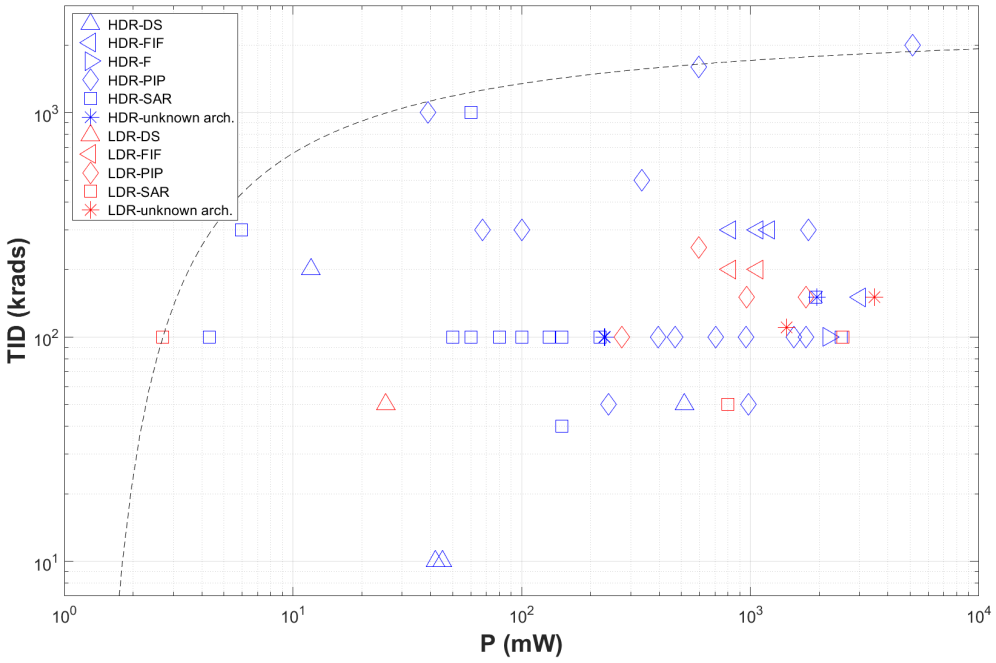


**Figure 6.** Total ionizing dose against power consumption.

The fact that $\text{FOM}_W$'s envelope is constant across $f_s$ for the *selection* (see Figure 4) could help to extract patterns about $\sigma_{sat}$, and hence $\text{FOM}_{SET}$, across $f_s$. SET and SEU data were both used to calculate $\text{FOM}_{SET}$ due to the common physical phenomenon producing both effects. It is expected for both transients and upsets that $\text{LET}_{th}$ and $\sigma_{sat}$ envelopes increase with $P$ and $f_s$ respectively. Even if the *selection* seems to behave so, the limited number of *selection*'s members characterized in transients and/or upsets does not allow to extract clear patterns about these effects.

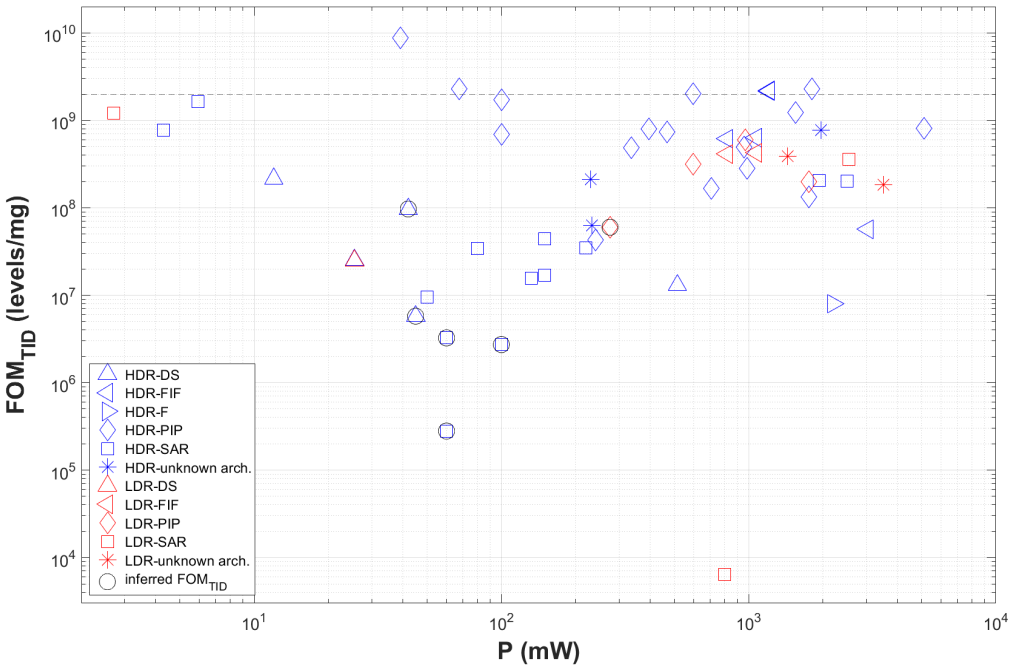


**Figure 7.** FOM$_{TID}$ against power consumption.

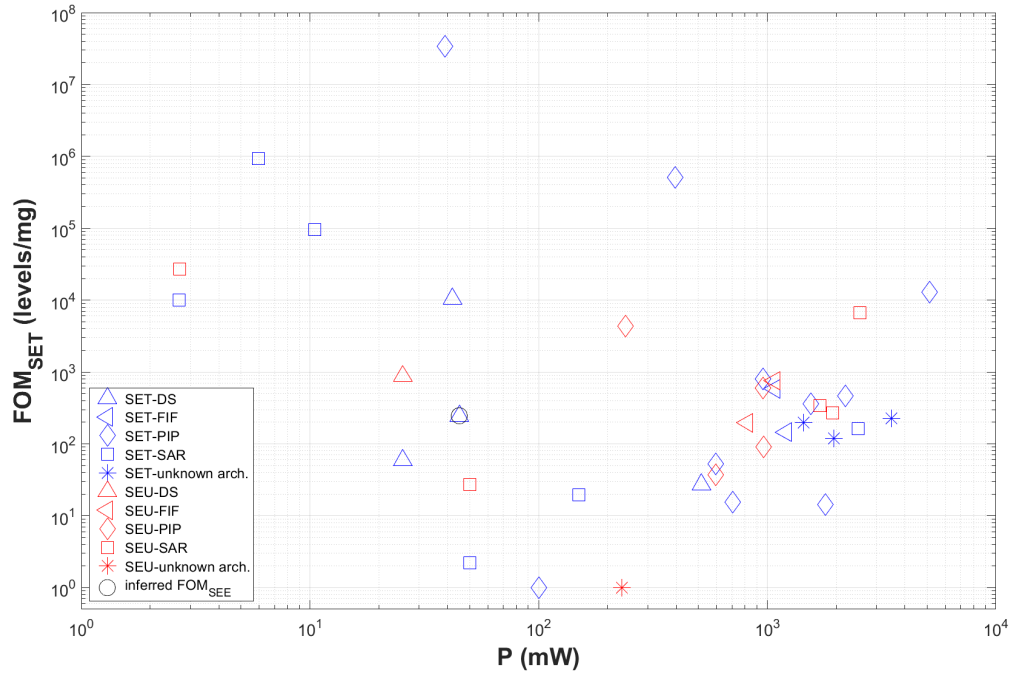


**Figure 8.** FOM$_{SET}$ against power consumption.

Figure 8 plots the calculated FOM$_{SET}$ for both SET and SEU against the nominal power consumption for each *selection*'s member. Also in this scenario, Boeing-1 ADC clearly outperforms the rest of the *selection*: its FOM$_{SET}$ ($3.37 \times 10^7$ levels/mg) is around two orders of magnitude above the second best value: $5 \times 10^5$ levels/mg obtained by AD9246S. In a closer look to these two best values, both have similar FOM$_W$ but the radiation performance of Boeing-1 ADC is clearly better than those of AD9246S (LET$_{th}$: 30.9 $>$ 10 MeV·cm$^2$/mg, $\sigma_{sat}$: $1.3 \times 10^{-7} < 2.5 \times 10^{-6}$ cm$^2$/device). Considering

only upsets, the best $FOM_{SEU}$ is obtained by ADC128S102QML-SP with $2.7 \times 10^4$ levels/mg; its good performance is not only due to a good $FOM_W$ (second best with 831 fJ/level), but also to a reduced $\sigma_{sat}$ ($4.14 \times 10^{-5}$ cm$^2$/device).

Since Boeing-1 has both the best $FOM_{TID}$ and the best $FOM_{SET}$ (both several times better than the second classified), we can conclude that it is the most power efficient randenv-ADC of the *selection*.

### *4.4. Technologies*

Bipolar, CB (complementary-bipolar), LC$^2$MOS (linear compatible CMOS), BiCMOS (bipolar-CMOS) and pure CMOS processes [75–77] are found among the *selection* (cf. column 'Tech.' in Table 1). Particularly, MOS processes have characteristic lengths of 0.35 µm, 250 nm, 180 nm, 130 nm, 90 nm, 65 nm and 32 nm, being 0.35 µm and 180 nm the two more recurrent (with at least ten and eleven specimens, respectively). Both 0.35 µm and 180 nm MOS nodes are usually accompanied with other process options—BJTs (bipolar juntion transistors), additional thicker gate oxide, etc.—that allow to integrate in a monolithic solution a wide voltage range analog front-end together with the ADC.

The organization contributing the most to the *selection* is Texas Instruments (with 22 specimens). BiCom3 and CMOS9 are its most recurrent technologies within the *selection* (with at least six and seven specimens, respectively); both are briefly described below.

BiCom3 is a CB SiGe BiCMOS triple-metal technology on SOI [78]. It includes 5V NPN and PNP SiGe BJTs and isolated 3.3 V 0.35 µm CMOS devices. It offers several process options for faster BJTs (3X and 3Y options for 25 and 33 GHz, respectively), for high voltage applications (3XHV option, up to 36 V) and without SOI (3XL bulk option); however, only BiCom3 (basic) and BiCom3X options can be found within the *selection*. The technology can be considered latch-up free and ELDRS immune (enhanced low dose rate sensitivity), and has been tested up to 150 krad(Si) of TID (ADS5424-SP) and up to $6.08 \times 10^{11}$ neutrons/cm$^2$ of DDD (DD dose) (ADS5400-SP).

CMOS9 is a DGO (dual gate oxide) CMOS process using STI (shallow trench isolation) for inter-device isolation [23]. It provides 1.8 V and 3.3 V CMOS devices with, respectively, 180 nm and <400 nm minimum gate lengths, and 5 nm and <10 nm gate oxide thicknesses. The process is originally from National Semiconductor, derived from the TSMC's 180 nm process (Taiwan Semiconductor Manufacturing Company). The technology can be considered ELDRS immune and has been tested up to 300 krad(Si) at LDR and HDR of TID (ADC08D1000).

Special mention is deserved by the 32 nm CMOS SOI technology by IBM used to implement the best $FOM_{TID}$ and $FOM_{SET}$ specimen: the Boeing-1 pipelined ADC [50]. Combined with on-chip calibration, the technology has shown practically no variation up to 1 Mrad(Si) of TID for this application. In addition to analog-to-digital conversion, the technology was also proven suitable for other high-speed applications (such as SerDes, PLL and DRAM) in heavy-ions environments.

Radiation hardening in ADC applications can be achieved with multiple technologies; several options are combined to achieve a versatile and power efficient design. RHBD (radiation hardening by design) techniques at physical level (additional contact rings, smart device distribution, etc.) and certain technology options (buried layers, trenches, etc.) are used to enhance radiation performance. The smallest MOS node (32 nm) used up to now for radenv-ADCs seems, not only the most suitable for a SoC solution, but also the most power + radiation efficient when combined with calibration; however, greater nodes (0.35 µm and 180 nm, including other technology options) offer the possibility to integrate a wide voltage range analog front-end without neglecting the power + radiation efficiency. In any case, we shall remark that the SOI feature is always present in the best performing specimens of the *selection*.

### *4.5. Architectures and Applications*

Five architectures can be found among the *selection*: ΔΣ, SAR (successive approximation register), PIP (pipelined), F (flash), and FIF (folded interpolated flash). We have illustrated this diversity by discerning data by architecture in Figures 2–8 (cf. legends). Additionally, we have denoted surmised

architectures with a question mark in column 'Arc.' of Table 1. As a briefing, we have collected in Table 3 the number of specimens, the ranges of ENOB, $f_s$ and $\text{FOM}_W$, and the average $\text{FOM}_{TID}$ and $\text{FOM}_{SET}$ for each architecture. Flash was dismissed from Table 3, since only one specimen uses this architecture among the *selection*.

**Table 3.** Operation ranges within the *selection* segregated by architecture.

| Architecture | Count | ENOB | $f_s$ [MHz] | $\text{FOM}_W$ [pJ/Level] | $\overline{FOM}_{TID}$ [Levels/mg] | $\overline{FOM}_{SET}$ |
|---|---|---|---|---|---|---|
| ΔΣ | 5 | [16; 20.3] | [0.001; 0.125] | [1; 37.8] | 6 | 2320 |
| SAR | 19 | [8; 16] | [0.025; 500] | [0.1; 78125] | 34 | 83,313 |
| PIP | 21 | [7.4; 12.9] | [3; 3200] | [0.8; 24.8] | 109 | 2,139,462 |
| FIF | 8 | [6.8; 9.4] | [1000; 2200] | [1.4; 26.5] | 79 | 303 |

ADC architectures are similarly distributed along frequency and resolution either the target application operates under radiation or not: ΔΣ ADCs target low-frequencies high-resolution applications, SAR do low/medium-frequencies medium/high-resolution, PIP do medium/high-frequencies moderate-resolution, and FIF do high-frequencies low-resolution. Radiation hardening can be enhanced at the expense of area and power consumption by including additional blocks (triple redundancy, anti-glitches, anti-bubbles, SEL and/or SEFI watch-dogs, digital error correction, etc.). On the other hand, selecting specific circuit structures for the composing blocks of the randenv-ADC can also enhance its radiation performance without significant impact in area or power consumption (i.e., using auto zeroing comparators against SET). The PIP architecture presents the best $\overline{FOM}_{TID}$ and $\overline{FOM}_{SET}$ within the *selection* (cf. Table 3). In fact, PIP is the preferred architecture for hardened ADCs, with 21 specimens among the *selection*. SAR is also well represented, but it has more COTS among its population (7/19 versus 3/21 for PIP), and worst $\overline{FOM}_{TID}$ and $\overline{FOM}_{SET}$.

Latency is a major concern for some ADC applications. As a rule of thumb, we can arrange architectures in the following order, from shorter to longer latency: flash < FIF < PIP < SAR < ΔΣ. Additionally, some ADC applications recur to down-sampling to extend the analogue bandwidth to be digitized; this technique has being lately the tendency in satellite communications where digital down-conversion of L- and S-bands signals relaxes the requirements of the RF front end. On the other hand, the inherent loop filter of ΔΣ architectures provides an intrinsic anti-aliasing feature that can save additional filtering stages at system level. In addition, the intrinsic oversampling feature of ΔΣ ADCs can be seen as a redundancy spread in time [79].

Considering the virtues and drawbacks of each architecture briefly discussed in this section, in Table 4 we have linked the more recurrent applications in radiation environments with their most suitable ADC architectures; a higher suitability is emphasized with a double check mark instead of a single one. We can consider SAR the most versatile architecture since it fits in almost all the considered applications.

Depending on the target application, some soft error test methods (cf. Table 2) could be more adequate than others. In Table 5, we present our recommendations according to the following criteria: test methods 1P or S are dismissed due to their reduced monitoring of output codes; QS is perfect for slow high-resolution applications; DAC method is discarded for long latency and/or very high resolution applications; the other test methods are similar, and can all fit for medium/high-speed applications.

**Table 4.** Suitability of ADC architectures for applications in radiation environments.

| Application | | ΔΣ | SAR | PIP | FIF | Flash |
|---|---|---|---|---|---|---|
| collider experiments | | | ✓✓ | ✓ | | |
| discrete-time control | | | ✓ | ✓✓ | ✓ | |
| earth observation | | ✓✓ | ✓ | | | |
| house-keeping | | ✓ | ✓ | | | |
| satellite communications | base-band | ✓✓ | ✓ | | | |
| | DDC | | | ✓✓ | ✓✓ | ✓ |
| sensor acquisition | thermistor | ✓✓ | ✓ | | | |
| | gauge | ✓✓ | ✓ | | | |
| | magnetometer | ✓✓ | ✓ | | | |
| star tracker | | | ✓ | ✓✓ | | |
| sun sensor | | | ✓ | ✓✓ | | |
| telemetry | fast dynamics | | ✓ | | | |
| | slow dynamics | ✓✓ | ✓ | | | |
| video | | | ✓ | ✓✓ | | |

**Table 5.** Suitability of ADC soft error test methods for applications in radiation environments.

| Application | | BF | CS | DAC | GOLD | DIS | 4P | QS | 1P | S |
|---|---|---|---|---|---|---|---|---|---|---|
| collider experiments | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| discrete-time control | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| earth observation | | | | | ✓ | | | ✓ | | |
| house-keeping | | | | ✓ | ✓ | | | ✓ | | |
| satellite communications | base-band | ✓ | ✓ | | ✓ | ✓ | ✓ | | | |
| | DDC | ✓ | ✓ | | | ✓ | ✓ | | | |
| sensor acquisition | thermistor | | | | ✓ | | | ✓ | | |
| | gauge | | | | ✓ | | | ✓ | | |
| | magnetometer | | | | ✓ | | | ✓ | | |
| star-tracker | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| sun sensor | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| telemetry | fast dynamics | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| | slow dynamics | | | | ✓ | | | ✓ | | |
| video | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |

### *4.6. COTS within the Selection*

COTS are marked with a double asterisk (**) after their name in Table 1 (ADS1281, AD7712, AD7872T, MAX145, ADS1258, LTC1604, LTC1409, ADC124S101, AD7984, AD6640, ADS5483 and SPT7725); they are also easily recognizable therein since their temperature range is smaller than $[-55; 125]$ °C. Two main reasons explain the presence of COTS in the *selection*: either they cover a range of sampling frequencies that hardened ADCs do not, or they offer a better $\mathrm{FOM}_W$ compared to their surrounding hardened counterparts.

If we consider the efficiency including TID performance, COTS are far from the envelopes in Figures 6 and 7. On the other hand, even if the best performing COTS are far from the most efficient specimen in Figure 8 (Boeing-1 pipelined ADC), they present good $\mathrm{FOM}_{SET}$ compared to other hardened ADCs. In other words, COTS could have shorter lifetime due to TID compared to hardened ADCs; however, since soft errors are almost impossible to be totally mitigated (even in hardened ADCs), COTS usage could be worthy in short lifetime applications, where the power consumption and/or the cost are prioritized. HEP (where data acquisition systems can be replaced) and fleets of small satellites (where the viability depends on the price per satellite) are de facto target applications for COTS.

### *4.7. Particular Cases*

ADCs of the *selection* with outstanding efficiency under radiation are deeply analyzed below.

AD7984: This COTS is a SAR ADC with the best $FOM_W$ of the *selection* (122 fJ/level). It offers 16 ENOB sampling at 1.33 MS/s. No TID data were found in the literature, but its good electrical performance gives to this ADC a high $FOM_{SET}$ ($9.6 \times 10^4$ levels/mg). It also has a high SEL $LET_{th}$ (106.2 MeV·cm$^2$/mg).
ADC128S102QML-SP: This qualified SAR ADC is implemented with a 0.35 µm CMOS process. Its 2.7 mW reduced power consumption together with its 11.7 ENOB at 1 MS/s give it a $FOM_W$ of 0.8 pJ/level. Its good $FOM_W$ combined with its performance under radiation give it the best $FOM_{SET}$ for SEU ($2.7 \times 10^4$ levels/mg). It also has a high $FOM_{TID}$ ($1.2 \times 10^9$ levels/mg for both LDR and HDR) and SEL $LET_{th}$ (121.8 MeV·cm$^2$/mg).
Boeing-1: This pipelined ADC is implemented with a 32 nm CMOS SOI process. Its high 200 MS/s sampling rate together with its 7.4 ENOB and 39 mW power consumption give it a $FOM_W$ of 1.1 pJ/level. It performs exceptionally good under radiation (mainly due to its calibration features and the technology used for its implementation) which, combined with a good $FOM_W$, results in the best $FOM_{TID}$ and $FOM_{SET}$ within the *selection* ($8.8 \times 10^9$ and $3.37 \times 10^7$ levels/mg, respectively). It also offers the best SEL $LET_{th}$ (170 MeV·cm$^2$/mg).

## 5. Design Guidelines

From the analysis presented in Section 4, we have extracted several recommendations for the circuit design of radenv-ADCs. We have distributed these advises along the following simplified 5-step design flow:

Step 1—Analysis of the target application and the available solutions
Step 2—Selection of the manufacturing technology
Step 3—Selection of the ADC architecture
Step 4—Circuit design
Step 5—Design validation

For a better understanding, before describing each step in Sections 5.2–5.6, we have summarized in Section 5.1 the overall radiation hardening strategy across the design flow.

### *5.1. Radiation Hardening Strategy*

The hardening strategy against radiation effects mainly depends on the target application (Step 1) and the selected manufacturing technology (Step 2). Nevertheless, an optimum outcome is only possible when the strategy is tailored for the whole design flow. Below, we have broken down our proposal into a sequence of activities linked with the design steps (specified in parentheses):

1. For mature applications, reference data are extracted from previous radenv-ADC solutions. (Step 1)
2. Electrical and radiation requirements are specified based on the high-level requirements of the target application. (Step 1)
3. Technologies and architectures in line with the specified requirements are noted down. (Step 1)
4. Hardening-by-process options and hardening-by-design techniques are identified and analyzed for each considered technology. (Step 2)
5. Technologies offering libraries of hardened cells and/or basic IP-cores are prioritized. (Step 2)
6. As a result of the two previous activities, the manufacturing technology is selected from the preliminary options. (Step 2)
7. Devices to be used in the design are chosen from the technology libraries. (Step 2)
8. Needed rad-hard cells (but unavailable in the selected technology) are identified. (Step 2)

9. Relying on the previous technological choices, the basic ADC architecture is selected from the preliminary options. Hardening blocks against SEFI (current alarms, watch-dogs, etc.), and test structures (test buses, built-in self tests, etc.) are included as part of the radenv-ADC architecture. (Step 3)
10. Unhardened ADC designs with compatible requirements, implemented in the same technology, and with the same architecture, are compiled and analyzed. If plausible, one of them could be used as the starting point of the circuit design. (Step 4)
11. Unavailable rad-hard cells are designed with a full-custom approach. (Step 4)
12. Hardening-by-design techniques are applied at block-level. (Step 4)
13. Electrical and radiation requirements are verified by simulation for the whole design. (Step 4)
14. Electrical and radiation requirements are validated with test measurements. (Step 5)

Note that this hardening strategy can be adapted with minor changes to the design flow of other mixed-signal devices.

### *5.2. Step 1—Analysis of the Target Application and the Available Solutions*

A good understanding of the target application is critical to effectively extract the functional (interfaces, communication protocols, operating modes, etc.), electrical (voltage levels, expected power consumption, etc.), mechanical (die and package dimensions, bond-pads dimension and position, bonding method, etc.), environmental (temperature range, performance under radiation, etc.), and reliability (lifetime, SER, etc.), requirements of the new radenv-ADC. Particularly, radiation and reliability requirements can be estimated using space environments software, models, and tools, such as CRÈME [80,81], FASTRAD [82], GEANT4 [83,84], OMERE [85], etc. Furthermore, previous solutions (i.e., data collected in Table 1) and/or cutting-edge technologies can inspire particular requirements and other design features (such as the manufacturing technology and the ADC architecture).

For novel applications, new radenv-ADCs are developed to fulfill key requirements that available radenv-ADCs cannot fulfill. On the other hand, for mature applications, new developments usually enhance important parameters that were considered secondary in early stages of the application's life cycle. A good example illustrating both cases is the power consumption of radenv-ADCs targeting digital down-conversion of L-band signals; this requirement has become more demanding over time to offer more competitive solutions. It is hence critical to identify in Step 1 which parameters should be prioritized above others, considering that the preferences could have changed over time for mature applications. This approach helps solving possible trade-off conflicts in later steps.

The recent industrial trend of compact-size satellite-fleets in LEO with reduced lifetime (5 to 7 years) relaxes the radiation requirements of radenv-ADCs targeting related applications. In fact, TID is smaller for shorter missions, and the exposure to solar particle events in LEO is reduced compared to higher orbits. Collaterally, this approach reduces power consumption and shielding requirements, and is hence consistent with the size and weight reduction of the overall satellite.

The most important outcomes of Step 1 are the requirements specification, and the preliminary options of manufacturing technologies and ADC architectures that are suitable for the new design.

### *5.3. Step 2—Selection of the Manufacturing Technology*

In this step, the best technology for the implementation of the new radenv-ADC is identified. The options were limited in Step 1 to those in line with the application requirements. For example, a low-voltage technology could be incompatible with the monolithic implementation of a radenv-ADC requiring a wide voltage front-end. In fact, technologies without radiation characterization data are usually discarded, but those with latch-up immunity and minimum TID degradation are marked as preferential. Particularly, deep sub-micron CMOS nodes offering SOI-FinFET, UTBB-FDSOI [13], high-$\kappa$ dielectrics, or devices with Ge or SiGe p-channel should be preferred [11,12]. For all the considered technologies, the following features should be analyzed:

- Inter-device isolation options—LOCOS (LOCal Oxidation of Silicon), STI, DTI (Shallow or Deep Trench Isolation), buried layers, SOI, etc.—to evaluate the SEL sensibility.
- TID degradation and possible countermeasures: ELT availability, transistors minimum aspect ratio to mitigate performance degradation, etc.
- Effective volume of the technology devices to calculate the collected charge at an ion strike for different energies (for SET simulations).
- Availability of rad-hard libraries and IP-cores.

The selected technology is the one offering the best trade-off between electrical performance, hardening capability, and manufacturing price (usually following this prioritized order for radenv-applications). After the technology's choice, the process options (top-metal thickness, use of buried layers, etc.) and the technology devices to be used in the design are selected. Additionally, missing rad-hard cells considered important for the design are identified for their later implementation in Step 4.

### *5.4. Step 3—Selection of the ADC Architecture*

Usually, after analyzing the radenv-ADC requirements in Step 1, no more than two possible architectures are considered. Traditionally, the preferred choice has been a PIP architecture, since it offers a good trade-off between electrical performance and radiation robustness (cf. Section 4.5). In fact, PIP achieves higher resolutions than F or FIF, and is easier to harden against SET than ΔΣ or SAR. However, PIP cannot reach the ENOB that ΔΣ does, or be as power efficient as modern SAR. In short, the architecture choice is highly dependent on the particular radenv-ADC requirements. As a rule of thumb, it is advisable to use ΔΣ architecture for low-frequencies high-resolution applications, SAR for low/medium-frequencies medium/high-resolution, PIP for medium/high-frequencies moderate-resolution, and FIF for high-frequencies low-resolution.

Once the basic ADC architecture is chosen, the need of additional hardening blocks against SEFI (current alarms, watch-dogs, etc.) is evaluated with system-level simulation. Additionally, test structures (test buses, built-in self tests, etc.) to be included are also assessed.

### *5.5. Step 4—Circuit Design*

Intuitively, it makes sense to start a new radenv-ADC from a previous unhardened design with good electrical performance. However, the hardening task may be impractical if important radiation hardening considerations were overlooked in the original design. For example, for technologies requiring the replacement of the planar transistors by ELTs [86,87] (to avoid excessive performance degradation caused by TID), it must be checked that the original design does not have planar transistors narrower than the minimum width required by ELTs ($W_{min,ELT} \approx 3 \cdot W_{min,planar}$). Something similar occurs for the node splitting technique [88] against SET (transistor width should allow being divided at least by two or four in the dual- and quad-paths hardening, respectively). The comparison between radenv-ADCs and scientific ADCs (cf. Sections 4.1 and 4.2) gives an order of magnitude of what is reasonable to increase the power consumption to mitigate radiation effects (for a given $f_s$ between 10 kHz and 100 MHz, collected radenv-ADCs require at least 200 times more power to achieve an ENOB at least 2 bits lower than scientific ADCs). In any case, a new radenv-ADC can be designed from scratch, considering all the applicable hardening-by-design techniques from the beginning. To avoid unnecessary design effort, the unavailable rad-hard cells identified in Step 4 are designed with advanced TCAD (Technology Computer-Aided Design) tools once it is required to integrate them in the circuit. Furthermore, to avoid unnecessary power consumption, it is strongly recommendable to tailor the hardening effort for each particular design case: not all nodes are critical, and some of them can be SET hardened with a capacitance to ground (DC biased nodes, for example). A good approach to detect SET sensitive nodes is by analyzing the effects of injecting calibrated current pulses [89] throughout the circuit in different moments of a transient simulation [90,91].

### *5.6. Step 5—Design Validation*

The test conditions for the soft error characterization of the developed radenv-ADC shall emulate the target application as much as possible. Considering the features of each soft error test method, QS better fits with low-speed high-resolution applications, and CS with the rest.

## 6. Conclusions

After an exhaustive search in the literature, we have analyzed a collection of radenv-ADCs able to bear TID above 50 krad(Si) and without latch-up below 50 MeV·cm$^2$/mg regarding resolution, characteristic frequencies, power efficiency, radiation performance, manufacturing technologies, circuit architectures, and possible applications. Furthermore, we have also exposed remarks about its COTS sub-population and other particular cases. For the analyses only relying on electrical parameters, we have compared the extracted patterns with those of scientific ADCs. In this comparison, we have extracted that, for a given $f_s$ between 10 kHz and 100 MHz, collected radenv-ADCs require at least 200 times more power to achieve an ENOB at least 2 bits lower than scientific ADCs.

In this survey, we have discerned up to nine different test methods to characterize the soft errors of an ADC under heavy ions; two of them can be considered obsolete because of the scarce output codes monitored. Unfortunately, radiation performance is not consistent among different test methods for the same ADC, which complicates the comparison between ADCs characterized with different test methods. In any case, RHBD was proven to be effective in almost all CMOS technology nodes from 350 nm down to 32 nm; particularly, the SOI feature can be considered a mandatory technology option to achieve an optimum radiation performance. Regarding ADC architectures, we have confirmed that pipeline is the most recurrent among hardened ADCs; however, we have considered SAR the most versatile, since it is suitable for the vast majority of applications in radiation environments. We have pointed out that systems engineers recur to COTS looking for specific sampling frequencies or higher electrical performance uncovered by hardened ADCs. However, radiation characterization of COTS cannot be skipped and additional countermeasures could be required to avoid unacceptable system malfunctioning. Furthermore, we have defined FOM$_{TID}$ and FOM$_{SET}$, two new figures of merit that evaluate the efficiency of radenv-ADCs considering electrical and radiation performance. These FOMs were used as a first approximation to orient many of our analyses; however, a closer look to the appropriate specific data is required afterwards to extract accurate conclusions about radenv-ADCs.

Finally, based on the analyses that we have presented before, we have recommended some guidelines for circuit designers interested in the development of radenv-ADCs.

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## Abbreviations

The following abbreviations are used in this manuscript:

| | |
|---|---|
| 1P | Single-Point (SEE test method) |
| 4P | Four-Points (SEE test method) |
| ADC | Analog-to-Digital Converter |
| AMICSA | (International Workshop on) Analogue and Mixed-Signal Integrated Circuit for Space Applications |

| | |
|---|---|
| BF | Beat Frequency (SEE test method) |
| BiCMOS | Bipolar CMOS |
| BJT | Bipolar Junction Transistor |
| BOX | Buried Oxide |
| CER | Code Error Rate (SEE test method) |
| COTS | Commercial Off-The-Shelf (ADCs) |
| CMG | Control Moment Gyroscope |
| CMOS | Complementary Metal-Oxide Semiconductor |
| CS | Coherent Sampling (SEE test method) |
| DAC | Digital-to-Analog Converter |
| DC | Direct Current |
| DD | Displacement Damage |
| DDC | Digital Down-Converter |
| DDD | DD Dose |
| DGO | Dual Gate Oxide |
| DIS | Dynamic Input Signal (SEE test method) |
| DNL | Differential Non-Linearity |
| DOI | Digital Object Identifier |
| DR | Dynamic Range |
| DS or $\Delta\Sigma$ | Delta-Sigma (ADC architecture) |
| DT | Dynamic Threshold (SEE test method) |
| DTI | Deep Trench Isolation |
| ELDRS | Enhanced Low Dose Rate Sensitivity |
| ELT | Enclosed Layout Transistor |
| EM | Engineering Model |
| ENOB | Effective Number Of Bits |
| ESA | European Space Agency |
| F | Flash (ADC architecture) |
| FDSOI | Fully Depleted Silicon On Insulator |
| FIF | Folded-Interpolated Flash (ADC architecture) |
| FinFET | Fin-shaped Field Effect Transistor |
| FOM | Figure Of Merit |
| GNSS | Global Navigation Satellite Systems |
| HDR | High Dose Rate |
| HEP | High Energy Physics |
| IC | Integrated Circuit |
| IEEE | Institute of Electrical and Electronics Engineers |
| INL | Integral Non-Linearity |
| IP-core | Intellectual Property core |
| ISSCC | International Solid-State Circuit Conference |
| $LC^2MOS$ | Linear Compatible CMOS |
| LDR | Low Dose Rate |
| LEO | Low Earth Orbit |
| $LET_{th}$ | Linear Energy Transfer Threshold |
| LOCOS | LOCal Oxidation of Silicon |
| LSB | Least Significant Bit |
| MDPI | Multidisciplinary Digital Publishing Institute |
| MOS | Metal-Oxide Semiconductor |
| NASA | National Aeronautics and Space Administration (USA) |
| NB | Number of Bits |
| NSREC | Nuclear and Space Radiation Effects Conference |
| P | Power (consumption) |
| PIP | Pipelined (ADC architecture) |
| PLL | Phase-Locked Loop |

| | |
|---|---|
| QS | Quasi-Static (SEE test method) |
| RADECS | (European Conference on) Radiation and its Effects on Components and Systems |
| radenv | (ADCs/applications operating in) Radiation Environments |
| rad-hard | Radiation Hardened |
| R&D | Research and Development |
| REDW | Radiation Effects Data Workshop |
| RF | Radio Frequency |
| S | Static (SEE test method) |
| SAR | Successive Approximation Register (ADC architecture) |
| SEB | Single Event Burnout |
| SEDR | Single Event Dielectric Rupture |
| SEE | Single Event Effect(s) |
| SEFI | Single Event Functional Interrupt |
| SEHE | Single Event Hard Error |
| SEL | Single Event Latch-up |
| SER | statistical error rate |
| SESB | Single Event Snap-Back |
| SET | Single Event Transient |
| SEU | Single Event Upset |
| SFDR | Spurious Free Dynamic Range |
| SINAD | Signal-to-Noise And Distortion (ratio) |
| SNDR | Signal-to-Noise and Distortion Ratio |
| SNR | Signal-to-Noise Ratio |
| SoC | System on-Chip |
| SOI | Silicon On Insulator |
| STI | Shallow Trench Isolation |
| TCAD | Technology Computer-Aided Design |
| THD | Total Harmonic Distortion |
| TID | Total Ionizing Dose |
| TSMC | Taiwan Semiconductor Manufacturing Company |
| USA | United States of America |
| UTBB | Ultra-Thin Body and BOX |
| VLSI | Very Large Scale Integration |
| VLSICS | VLSI Circuits Symposium |

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