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A Negative Charge Pump Using Enhanced Pumping Clock for Low-Voltage DRAM

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Abstract: As the supply voltage decreases, there is a need for a high-speed negative charge pump circuit, for example, to produce the back-bias voltage (V_{BB}) with high pumping efficiency at a low supply voltage (V_{DD}). Beyond the basic negative charge pump circuit with the small area overhead, advanced schemes such as hybrid pump circuit (HCP) and cross-coupled hybrid pump circuits (CHPC) were introduced to improve the pumping efficiency and pump down speed. However, they still suffer from pumping efficiency degradation, low level $|V_{BB}|$, and small pumping currents at very low V_{DD}. A novel negative charge pump using an enhanced pumping clock is proposed. The proposed cross-coupled charge pump consists of the enhanced pumping clock generator (ECG) having a pair of inverters and PMOS latch circuit to produce an enhanced control signal with a greater amplitude, thereby working efficiently especially at low supply voltages. The proposed scheme is validated with a HSPICE simulation using the TSMC 180 nm process. The proposed scheme can be operated down to V_{DD} = 0.4 V, and $|V_{BB}|/V_{DD}$ is obtained to be 86.1% at V_{DD} = 0.5 V and C_{load} = 20 nF. Compared to the state-of-the-art CHPC scheme, the pumping efficiency is larger by 35% at V_{DD} = 0.6 V and R_L = 10 KΩ, and the pumping current is 2.17 times greater at V_{DD} = 1.2 V and V_{BB} = 0 V, making the circuit suitable for very low supply voltage applications in DRAMs.

Keywords: charge pump; negative voltage generator; back-bias voltage generator; low-voltage charge pump; high-speed charge pump

1. Introduction

The need for low-power circuits has drastically increased with the wide spread of mobile applications and wearable devices. The supply voltage is lowered for low power operation, but the threshold voltage is seldom scaled proportionally due to a sharp leakage current increase [1]. With the high threshold voltage, the leakage current in sub-threshold voltage region is diminished, but the circuit must be content with a degraded operation speed. Therefore, a multi-threshold system [1] employs the low threshold voltage transistors in selective parts where the fast operating speed is required and the high threshold voltage transistors elsewhere. On the other hand, for the variable threshold voltage schemes [2,3], the threshold voltage of MOS transistors is changed with the controlled voltage between the bulk and source nodes. Using the substrate bias circuit, the threshold voltage can be decreased to increase the operation speed during on-states, while the threshold voltage can be increased to reduce the steady power consumption during off-states. In DRAM, the leakage current [4–6] in the cell access transistor, aggravated by the scaling in the supply voltage and the storage cell dimensions, reduces the data retention time. As a result, the refresh time must be shortened, and the power consumption is increased. To reduce the leakage current, the method of increasing the threshold voltage with an internal negative voltage generator is truly vital for DRAMs [4,7,8].

The Dickson charge pump [4,9] consisting of diode connected transistor and pumping capacitor is simple but has a low pumping efficiency because the threshold voltage drop in the diode connected transistor hinders charge transfer from the load to ground. To improve the pumping efficiency, a hybrid pumping circuit (HPC) [10] using NMOS and PMOS transistors is introduced. An auxiliary circuit consisting of diode connected PMOS and small capacitor provides the appropriate pumping control signal under the condition that V_{DD} is higher than 2 times the threshold voltage. A cross-coupled hybrid charge pump circuit (CHPC1) [11] is introduced to improve the pump down speed and pumping efficiency at low V_{DD}. This circuit has two pumping branches whose controls are provided by non-overlapping clock signals. CHPC1 increases the pump down speed using sequential pump down operations and mitigates V_{DD} constraints using non-overlapping pumping clocks. In another cross-coupled hybrid charge pump circuit (CHPC2) [7], the pumping nodes are disconnected from the gate nodes in the opposite pumping branch transistors, but the auxiliary circuit is needed to serve as the gate control signal. Both CHCP1 and CHPC2 show better pumping efficiencies and pump down speeds but still have considerable performance degradation at very low V_{DD}. We present a negative charge pump circuit using enhanced pumping clock to serve as a negative voltage generator with a high efficiency and fast pump down speed at very low supply voltage.

In Section 2, conventional negative charge pumps are reviewed. In Section 3, the proposed scheme is presented with performance benefits explained at low supply voltage. Various performance aspects are evaluated for the proposed and conventional schemes in Section 4. Conclusions are drawn in Section 5.

2. Conventional Negative Charge Pump Circuits

Figure 1 shows the schematic diagram of the hybrid pumping circuit (HPC). The HPC scheme consists of transfer transistor (Mn1), discharge transistor (Mp1), and auxiliary transistor (Mp2). The gate nodes of Mn1 and Mp1 are connected together from which Mp2 links to the ground rail in a diode connected configuration [6,10]. The pumping clocks, CLK1 and CLK2, are two non-overlapping clocks. Through diode connected Mp2, nB remains at a positive voltage when CLK2 goes 'high'. As a result, the charge transfer is facilitated because Mn1 maintains a relatively high gate voltage during the charge transfer operation from nOUT to nA. However, V_{DD} has to be 2 times higher than $|V_{thp}|$ for proper operation for Mp2. Therefore, HPC is not suitable for very low supply voltage conditions.

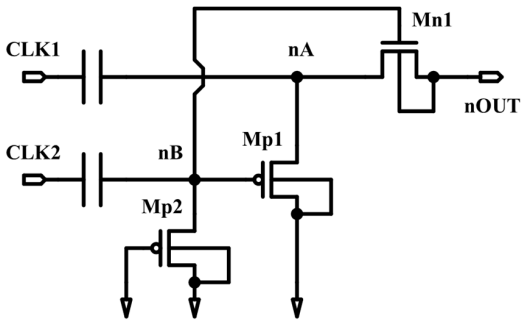

Figure 1. The schematic diagram of hybrid pumping circuit (HPC).

Figure 2 shows the schematic diagram of the cross-coupled hybrid pump circuit 1 (CHPC1). A pair of inverters is connected in a cross-coupled configuration [12–14]. The pumping capacitors are controlled by non-overlapping clocks. The voltage difference between nA and nB is V_{DD}. If V_{DD} is higher than $|V_{thp}|$, PMOS transistors are turned on and off alternately. Because the V_{DD} constraint of CHPC1 is reduced over HPC, CHPC1 is better than HPC in a low voltage condition. There exists a phenomenon of pumping speed degradation at the initial pump down operation.

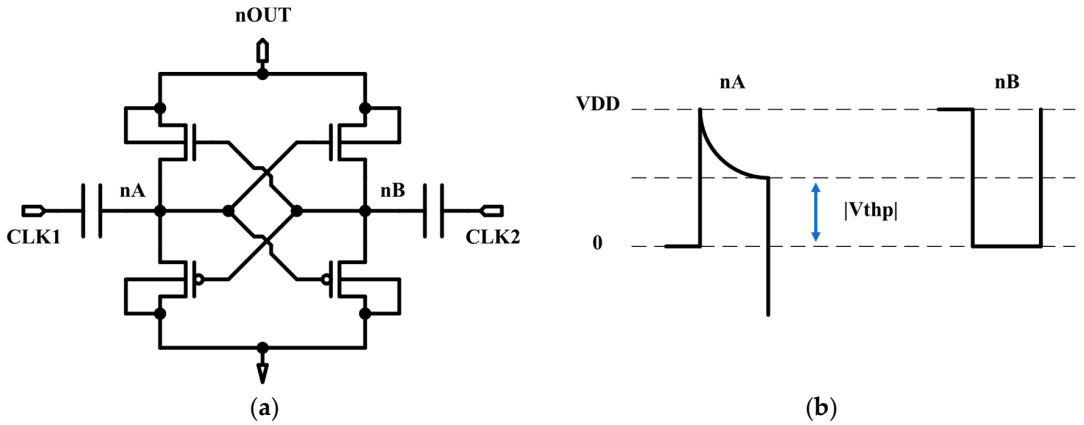

Figure 2. (**a**) Cross-coupled hybrid pump circuit 1 (CHPC1) and (**b**) its voltage waveforms at pumping nodes during the initial pump down operation.

In CHPC1, the two pumping nodes (nA, nB) are connected to the output node (nOUT) through NMOS latch circuit. During the initial pumping operations, nA and nB do not have sufficiently low voltage values. Therefore, the voltage at the node nA (V_{nA}) remains still positive when CLK1 is 'high'. When CLK1 goes to 'low' and CLK2 goes to 'high', charge sharing takes place between nOUT and nA. Because the load capacitance is generally larger than the pumping capacitance, V_{nA} reflects the charge shared voltage from V_{nOUT}. In the next pumping clock, V_{nB} is lowered by CLK2, but Mp1 turns on weakly because V_{nB} is not fully discharged by relatively high V_{nA}. Hence, the pump down speed slows during the initial pumping operation period.

The cross-coupled hybrid pump circuit 2 (CHPC2) is shown in Figure 3. It consists of a pair of HPC and cross-coupled PMOS latch [7,15]. The HPC circuit in the CHPC2 is controlled by the non-overlapping pump clocks, CLK1 and CLK2, respectively, and the gate node of HPC circuit is connected to the output of cross-coupled PMOS latch. The distinguishing difference is that the pumping nodes (nC, nD) are separated from gate nodes (nA, nB). The output nodes of PMOS latch (nA, nB) are operated with auxiliary pump capacitors which are controlled by CLK1 and CLK2. V_{nA} and V_{nB} easily swing from $-V_{DD}$ to 0 because nA and nB are separated from nC and nD, respectively. When CLK1 is 'high', V_{nC} is increased and V_{nA} is decreased to $-V_{DD}$. V_{nC} discharges to the ground through Mp1.

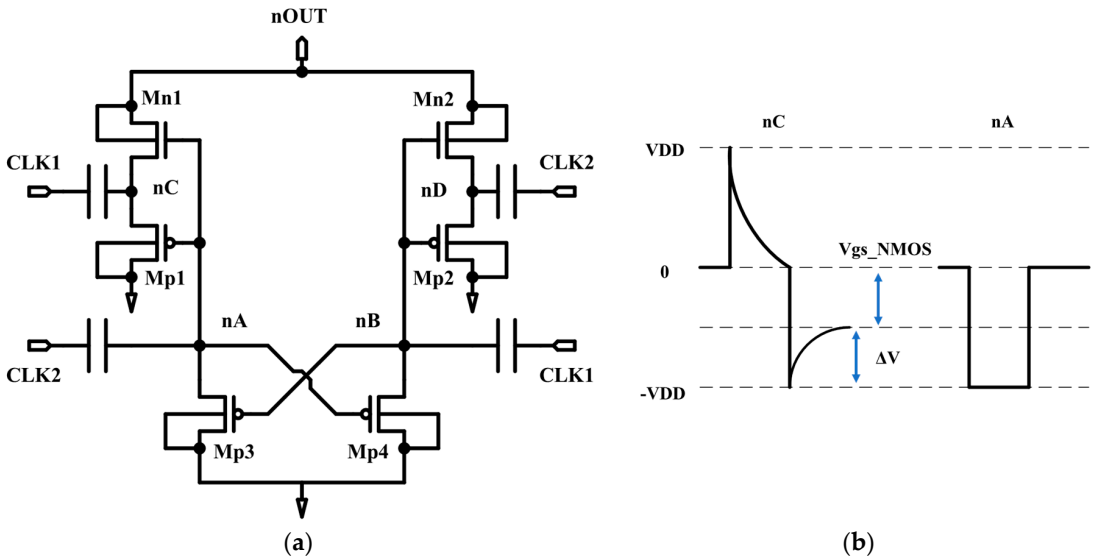

Figure 3. (**a**) Cross-coupled hybrid pump circuit 2 (CHPC2) and (**b**) its voltage waveforms at pumping nodes during the initial pump down operation.

At the next clock phase when CLK1 goes to 'low', V_{nC} is decreased and V_{nA} is increased to 0. With the charge sharing through Mn1, V_{nOUT} decreases and V_{nC} increases. With repeated pumping operations, V_{nOUT} can be lowered to $-V_{DD}$. In the initial pumping operation, CHPC2 can overcome the drawbacks of CHPC1 using independent gate control nodes. Yet, the voltage elevation of nC weakens the charge sharing performance. This weakness is further aggravated with the large load capacitance and small pumping capacitance. To increase the pump down speed and the efficiency at low supply voltage, considerations and measures are required to improve not only the discharge operation but also the transfer operation.

3. Enhanced Clock Pump Circuit (ECPC)

Figure 4 shows the proposed enhanced clock pumping circuit (ECPC). The proposed circuit consists of the enhanced pumping clock generator (ECG) and the cross-coupled pumping circuit (CCP) which are shown in Figure 5a,b, respectively. The ECG circuit consists of a pair of inverters and PMOS latch circuit. The ECG generates the control signal for CCP using non-overlapping clock signals. When CLK1 is 'high' and CLK2 is 'low', the PMOS transistor, Mp1, is turned on, and V_{nA} rises to V_{DD}. On the other hand, the node nC is discharged to the ground because V_{nD} is decreased by CLK2 after the PMOS transistor, Mp3, is turned on. Therefore, the NMOS transistor, Mn1, is turned off, and nA is isolated from nC. On the other side, the transistors, Mp2 and Mp4, are turned off, and V_{nD} is decreased to $-V_{DD}$. Therefore, Mn2 is turned on and V_{nB} turns to $-V_{DD}$. So, the voltages on nA, nB, nC, and nD become V_{DD}, $-V_{DD}$, 0, and $-V_{DD}$, respectively. It can be seen that ECG generates two types of non-overlapping control signals. The voltages of nA and nB swing from $-V_{DD}$ to V_{DD}, and the voltages of nC and nD swing from $-V_{DD}$ to 0. The CCP circuit consists of a pair of NMOS transfer transistors and a pair of PMOS discharge transistors. The gate nodes of transfer transistors, Mn3 and Mn4, are connected to nB and nA, respectively. The gate node discharge transistors, Mp5 and Mp6, are controlled by nodes nC and nD, respectively. When CLK1 is 'high', V_{nA} is V_{DD}, V_{nB} is $-V_{DD}$, V_{nC} is 0, and V_{nD} is $-V_{DD}$. When CLK1 rises, nE is increased, and charges stored in the pumping capacitor are discharged through Mp5. As a result, V_{nE} is lowered to 0. Next, CLK1 goes to 'low' and CLK2 goes to 'high'. V_{nA}, V_{nB}, V_{nC}, and V_{nD} become $-V_{DD}$, V_{DD}, $-V_{DD}$, and 0, respectively. Then, the charge sharing occurs through Mn3. Because V_{nB} is sufficiently high, the charge sharing operation between nE and nOUT takes place without voltage loss incurred by the threshold voltage drop, achieving a high pumping speed. In the next clock phase, the analogous pump down operation is performed in the opposite pumping branch. Using the ECG circuit, transfer transistors of CCP are provided with sufficiently high voltage to serve an effective charge transfer from the load capacitor even during the early pumping period.

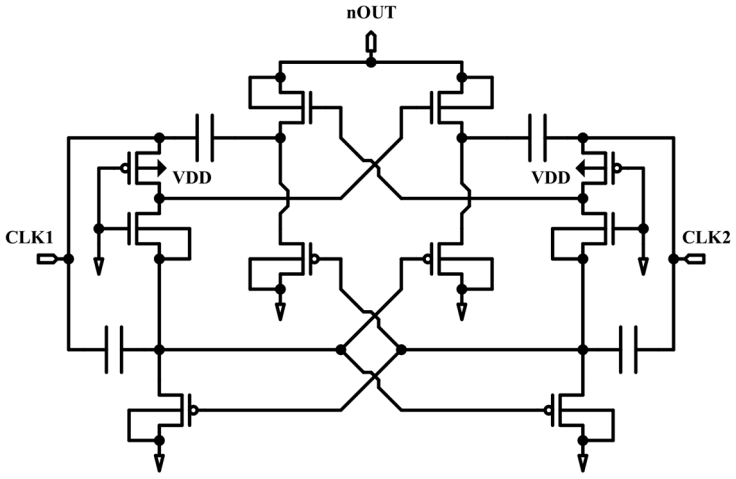

Figure 4. Proposed enhanced clock pump circuit (ECPC).

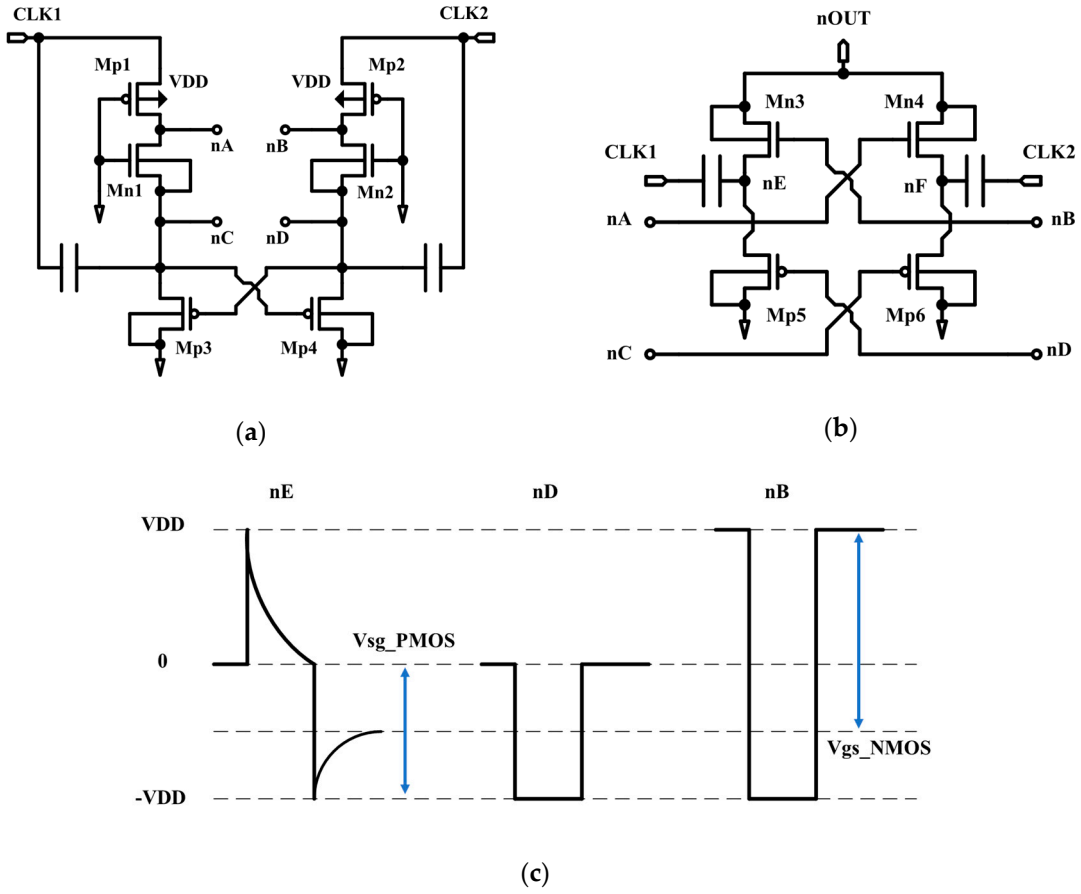

Figure 5. Proposed enhanced clock pump circuit (ECPC) separated into (**a**) enhanced pumping clock generator (ECG) and (**b**) cross-coupled pump circuit (CCP) with (**c**) its voltage waveforms during the initial pump down operation.

Besides, the discharge operation is efficiently performed as well by the ECG circuit for being enabled with the low voltage to discharge transistor of CCP.

4. Simulation Results

To evaluate the performance of the proposed ECPC scheme, a HSPICE simulation with the TSMC 180 nm process is performed. The threshold voltages of NMOS and PMOS with no body bias are 0.445 V and −0.437 V, respectively, with the body bias range being 0.430 V–0.474 V and −0.464 V–−0.437 V. The surface mobilities for the NMOS and PMOS transistors are 0.0459 m^2/V-s and 0.0109 m^2/V-s, respectively. The channel doping concentrations for NMOS and PMOS transistors are 3.90×10^{17} cm^{-3}. The width ratio between the transfer transistor and the discharge transistor is chosen to be 1/2 for all the circuits in the comparison. The auxiliary PMOS transistor in the HPC is sized at 1/10th the width of the discharge transistor. The auxiliary PMOS latch in the CHPC2 is also sized at 1/10th the width of the discharge transistor. In the proposed scheme, the widths of PMOS and NMOS in ECG circuit are sized at 1/10th the widths of its discharge and transfer transistors, respectively. The load capacitance (C_{LOAD}) is 20 nF, the pumping capacitance (C_{PUMP}) is 1 nF, the auxiliary pumping capacitance in HPC, CHPC2, and ECPC are all 0.1 nF, and the pumping clock frequency is 10 MHz. Performance parameters such as the pump down speed, the $|V_{BB}|/V_{DD}$ ratio, the pumping current, and the pumping efficiency are analyzed in comparison with the conventional schemes. For brevity, HPC, CHPC1, and CHPC2 are to be denoted as Conv 1, Conv 2, and Conv 3, respectively.

4.1. Pump down Speed

Figure 6 shows the time-traced pump down speeds. Since the bulk bias of the transfer transistors is connected to the V_{BB} node, the threshold voltage of transfer transistors is relatively high at the early operation phase. The drain current of the transfer transistors is proportional to the carrier mobilities and $V_{gs} - V_{th}$. The negative bulk voltage increases the threshold voltage and reduces the carrier mobilities. As a result, the drain currents of transfer transistor are degraded, then the pump down speed slows down. As $|V_{BB}|$ approaches V_{DD}, the pump down speed slows down because the value of $V_{gs} - V_{th}$ is decreased, resulting in reduced pumping currents. Therefore, a trade-off issue between the pump down speed and the $|V_{BB}|$ level exists. The single-branched structure of Conv 1 inevitably leads to the worst pump down speed. And the charges at pumping nodes cannot be fully discharged because the source-gate voltage difference for the auxiliary PMOS transistor is not sufficient. Therefore, Conv 1's $|V_{BB}|$ achieves 93% of V_{DD} with the slowest pump down speed. In Conv 3, the pumping nodes are separated with gate nodes. Using the auxiliary PMOS latch and an additional pumping capacitor, appropriate gate control signals are provided to each pumping branch. As such, the pump down speed of Conv 3 is faster than that of Conv 2. Our proposed scheme shows the fastest pump down speed among all. The ECG circuit of the proposed scheme generates sufficiently high voltage to control the transfer NMOS transistors. This is helpful to overcome the lowered pumping current with increased threshold voltage due to the body bias effect.

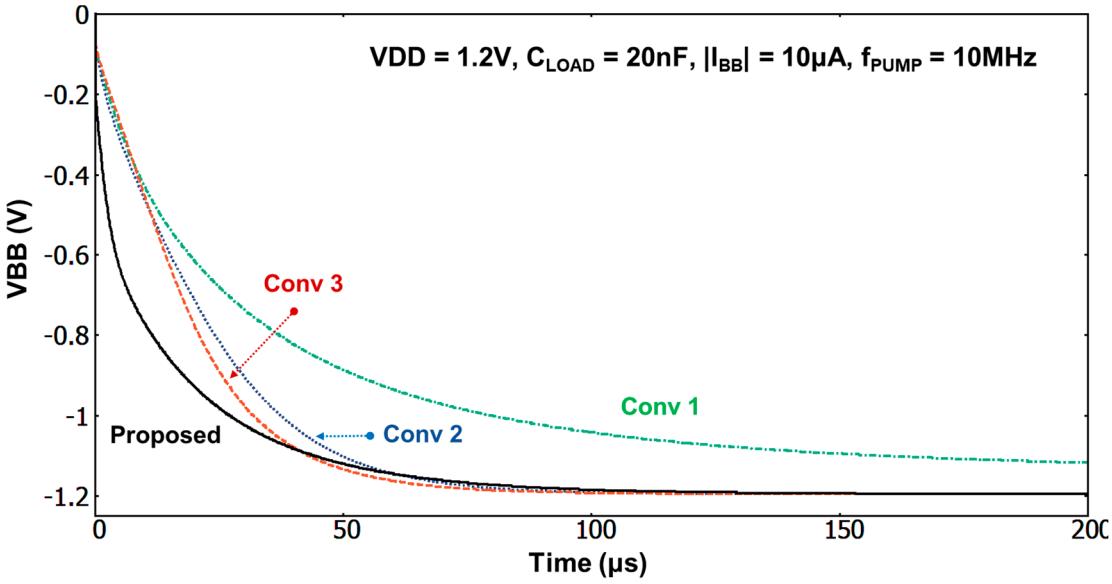

Figure 6. Comparison of the pump down speeds.

4.2. $|V_{BB}|/V_{DD}$ Ratio

Figure 7 shows the comparison of the $|V_{BB}|/V_{DD}$ ratios with various supply voltages. The Conv 1 shows the most drastic degradation in the $|V_{BB}|/V_{DD}$ ratio as the supply voltage is lowered. This is due to the fact that the supply voltage which is greater than 2 times the threshold voltage is required to control the discharge PMOS transistors. Conv 2 and Conv 3 both show similarly degraded trend in the $|V_{BB}|/V_{DD}$ ratio. For the supply voltage over 1.0 V, $|V_{BB}|/V_{DD}$ ratio is close to 99%. However, under 0.8 V, they both start to decrease and do not operate properly below 0.5 V. In the low supply voltage condition, the NMOS transfer transistor's operation is important to effectuate the charge sharing voltage between pumping node and output node down to pump-down voltage of V_{BB}. Yet, Conv 2 and Conv 3 do not have any means to facilitate NMOS transfer transistor's operation. Conv 3 has the auxiliary circuit to help discharge PMOS transistor but the NMOS transfer transistor is deficient in very low supply voltage.

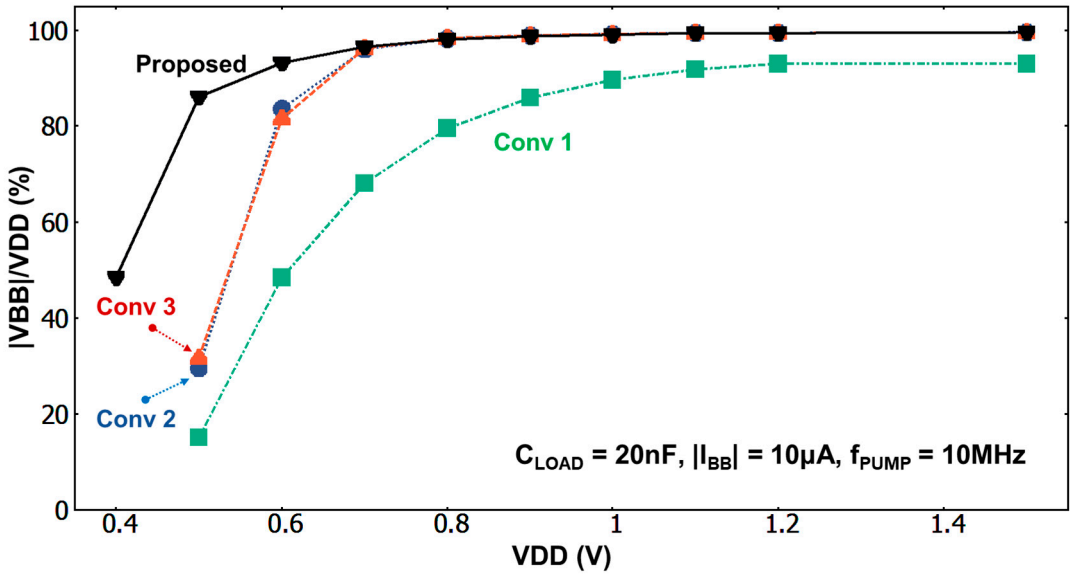

Figure 7. $|V_{BB}|/V_{DD}$ with various supply voltages.

4.3. Pumping Current Comparison with Various V_{BB}

Figure 8 shows the pumping current as a function of V_{BB} at V_{DD} = 1.2 V. As the output voltage approaches the steady value in V_{BB}, the pumping current is decreased because V_{ds} for the NMOS transfer transistor is decreased. Over the entire V_{BB} range, the pumping current of the proposed scheme is larger than all other conventional schemes. This is due to the fact that the ECG circuit generates the large control signal for NMOS transfer transistors. Therefore, the proposed scheme retains relatively high pumping current with high V_{gs} for the NMOS transfer transistors. For V_{BB} = 0 V, the pumping current of Conv 3 is larger than Conv 2, also in account of its larger pump down speed. The difference in pumping currents between the proposed scheme and other conventional schemes becomes apparent for the low supply voltage. For V_{BB} = 0, the pumping current of Conv 3 is 46% of the proposed scheme at V_{DD} = 1.2 V.

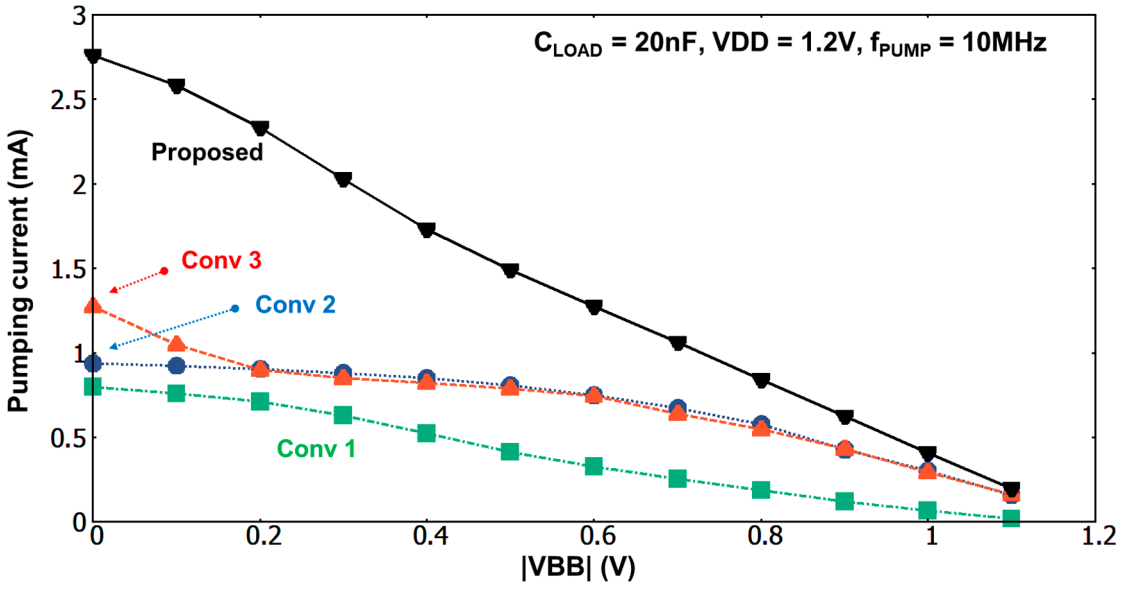

Figure 8. Pumping current with various V_{BB}.

The proposed scheme has the ECG circuit to complement the low voltage operation. As a result, the proposed scheme shows the $|V_{BB}|/V_{DD}$ ratios of 86% and 48% for V_{DD} = 0.5 V and V_{DD} = 0.4 V, respectively. Furthermore, the pumping current of Conv 3 is 19% of the proposed scheme at V_{DD} = 0.6 V. This shows that the proposed scheme will be very suitable for the low supply voltage applications.

4.4. Pumping Efficiency with Various R_{LOAD}

Figure 9 displays the pumping efficiency with the various load resistance. The pumping efficiency (η) is defined as follows [16]:

$$\eta = \frac{\frac{V_{BB}{}^2}{R_{LOAD}}}{V_{DD} \cdot I_{supply}}. \quad (1)$$

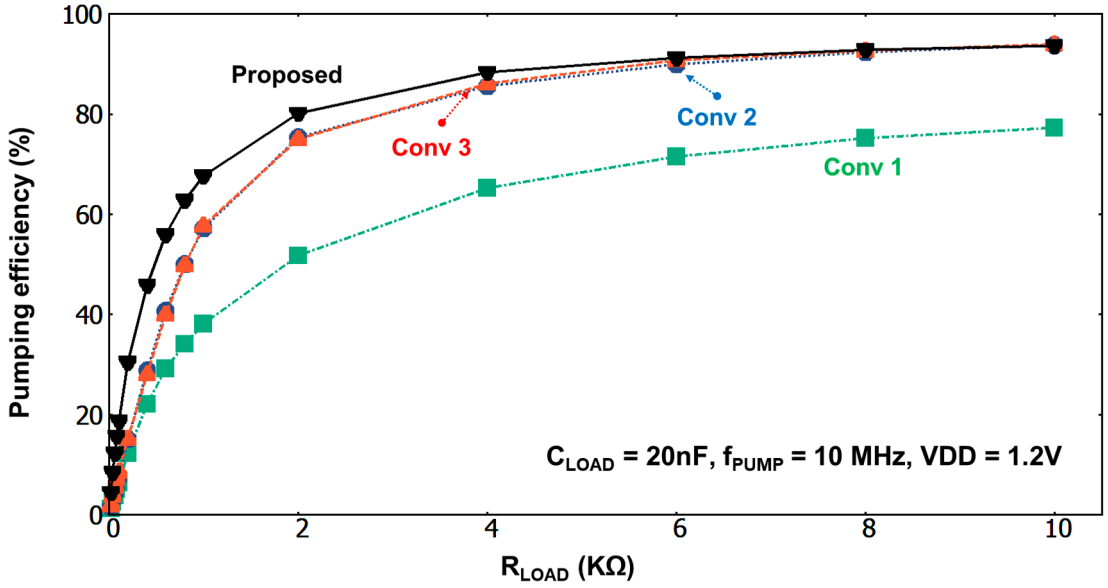

Figure 9. Pumping efficiency with various load resistance at V_{DD} = 1.2 V.

As the load resistance decreases, $|V_{BB}|$ is decreased because of the high load current components. The pumping efficiency of Conv 1 is 77.2% with R_{LOAD} = 10 kΩ at V_{DD} = 1.2 V, while all the other schemes achieve pumping efficiencies above 93%. With R_{LOAD} = 1 kΩ, the efficiency of the proposed scheme is 67.6% which is the highest among all. As the supply voltage decreases, the pumping efficiencies drop clearly.

Figure 10 shows the pumping efficiency at V_{DD} = 0.6V. With V_{DD} = 0.6 V and R_{LOAD} = 10 kΩ, the efficiencies of Conv 1, Conv 2, Conv 3, and the proposed scheme are 34.7%, 48.1%, 46.0%, and 81.1%, respectively. The proposed scheme can generate high $|V_{BB}|$ and high pumping current at low supply voltages. The high pumping efficiency shows that the proposed scheme is suitable for low voltage applications.

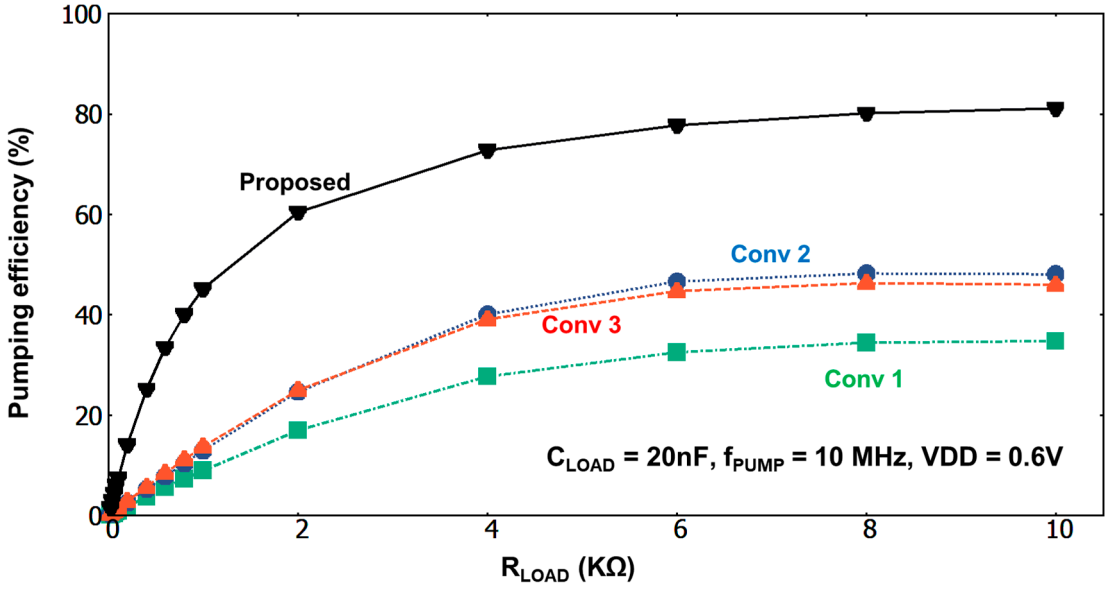

Figure 10. Pumping efficiency with various load resistance at V_{DD} = 0.6 V.

4.5. Power Loss Estimation

In the topological point view of [17] Conv 1 is bootstrapped, Conv 2 is cross-coupled, Conv 3 is cross-coupled with gate biasing, and the proposed scheme is cross-coupled with clock boosting. In the power loss point of view, two types should be considered. One is the conduction power loss influenced by the resistive condition. The other is the dynamic power loss that depends on the pumping clock frequency and transistor's capacitive elements [18]. The conduction and the dynamic power losses can be described as:

$$P_C \propto \frac{L}{W} \cdot \frac{I_L^2}{\mu C_{ox}(V_{GS} - V_T)} \quad (2)$$

$$\text{and } P_D \propto W \cdot I_L \quad (3)$$

where μ is the surface mobility and C_{ox} is the unit area capacitance of the gate oxide. Therefore, the conduction power loss is proportional to the pumping current and inversely proportional to the mobility. The dynamic power loss is proportional to the pumping current and frequency. Conv 1 is assessed with smallest conduction and dynamic power losses due to the smallest transfer transistor size and smallest pumping current. Besides, the auxiliary transistor in Conv 1 for the bootstrap operation is small as well. Conv 2 is next in the order. Conv 2 does not have an auxiliary circuit, but the pumping frequency is greater than Conv 1. As a result, the dynamic power loss for Conv 2 is larger than that for Conv 1. Conv 3 has additional circuit compared with Conv 2. The dynamic power loss in the auxiliary circuit is added. Hence, the power loss of the Conv 3 estimates to be larger than Conv 2. The power loss of the proposed scheme is the largest among all. Because the ECG consumes dynamic power to generate the enhanced clock, the power loss is increased. Together with the largest pumping current, the power loss increases for the proposed scheme.

5. Discussion

For the conventional schemes, the performance of PMOS discharge transistors is improved to increase the pump down speed and pumping efficiency. In this work, the gate voltage of the PMOS discharge transistors can be controlled appropriately in order to increase the initial operating speed and obtain a lower level of V_{BB}. However, as the supply voltage is reduced, the operation of the NMOS transfer transistor is important to maintain the negative charge pump circuit's performance. Failure to apply sufficiently high voltages to the gate of the NMOS transfer transistors will slow down the charge

sharing operation between the pumping node and the load capacitor, leading to pumping current and efficiency reductions. The ECG circuit in the proposed scheme serves both the high positive voltage to activate the NMOS transfer transistors and the low negative voltage to activate the PMOS discharge transistors. In this manner, the proposed negative charge pump scheme can be operated with the high pump down speed and low V_{BB} voltage even with conditions of very low supply voltage and high load current.

The performance of the proposed scheme is now thoroughly evaluated. Table 1 shows the performance of various negative charge pump circuit at V_{DD}=0.6 V and C_L=20 nF. The pump-down speed of the proposed scheme is the fastest because the pump-down operation takes place in half clock cycles by using the cross-coupled topology and the large V_{GS} of the NMOS transfer transistors induces large pumping currents. The $|V_{BB}|/V_{DD}$ ratio of the proposed scheme is the largest, too. The large pumping current and the gate control clock from the ECG circuit provide foreseen benefits for the proposed scheme for the low V_{DD} conditions. The pumping efficiency with various load resistance for the proposed scheme is highest because the pumping efficiency is proportional to $|V_{BB}|$. However, the proposed scheme requires auxiliary transistor and capacitors in forming the ECG circuit. So, the area overhead is largest among them. Besides, the power loss of the proposed scheme is considerable because the ECG circuit continues switching operation that consumes power. Furthermore, the largest pumping current of the proposed scheme increases the dynamic power loss, too, albeit efficiently.

Table 1. Comparison of various negative charge pump circuits at V_{DD} = 0.6 V and C_L = 20 nF.

	Conv 1 (HPC)	**Conv 2 (CHPC1)**	**Conv 3 (CHPC2)**	**Proposed**
Topology	Bootstrap	Cross-coupled	Cross-coupled with gate biasing	Cross-coupled with clock boosting
$\|V_{BB}\|/V_{DD}$ ratio	48.5%	83.6%	81.6%	93.2%
Pump-down speed	177.8 µs	176.4 µs	178.7 µs	120.0 µs
Pumping current at V_{BB} = 0 V	57.7 µA	79.9 µA	89.8 µA	471.6 µA
Pumping efficiency at R_L = 10 kΩ	34.7%	48.1%	46.0%	81.1%

6. Conclusions

A highly efficient and high-speed negative charge pump circuit using enhanced pumping clock generator (ECG) and cross-coupled pumping (CCP) circuit is presented. The ECG supplies the improved control signals to the CCP to enhance its performance. The proposed charge pump circuit shows a comparably fast pump down speed and the $|V_{BB}|/V_{DD}$ ratio which is larger than 93% in the V_{DD} range of 0.6 V–1.5 V. The pumping efficiency of the proposed scheme is higher than 80% with the load resistance in the range of 2 kΩ–10 kΩ at V_{DD} = 1.2 V. Moreover, the pumping current is 2.17 times greater than Conv 3 at V_{DD} = 1.2 V and V_{BB} = 0 V. In very low supply voltage condition of V_{DD} = 0.4 V, the proposed scheme can outperform with the $|V_{BB}|/V_{DD}$ ratio of 48.38%. At V_{DD} = 0.6 V and R_{LOAD} = 10 KΩ, the pumping efficiency of the proposed scheme is 35% larger than Conv 3.

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Conflicts of Interest: The authors declare no conflict of interest.

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